650V, 300/600mA Half Bridge Gate Driver

Description

The ETA85601 is a high voltage and high reliability power MOSFET/IGBT drivers with 300mA source, 600 mA sink current capability. The recommended VDD operating voltage is 10V to 20V for IGBTs and 10V to 17V for power MOSFETS.

ETA85601 features robust drive with excellent noise and transient immunity including input noise filter, high dV/dt tolerance, wide negative transient voltage on switch node (VS).

ETA85601 includes protection features where outputs are held low when the inputs are left open or when the minimum input pulse width specification is not met. Interlock and dead time functions prevent both outputs from being turned on simultaneously. In addition, the logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The device offers UVLO protections for both high side and low side supply.

Features

- Fully Operational up to 650V
- Peak Output Current 0.3A Source, 0.6A Sink
- dV/dt Immunity of 50V/ns
- Logic operational up to -7V on VS pin
- Independent UVLO for Both Channels
- Delay Matching (35ns Typical)
- Dual Inputs with Output Interlock and deadtime
- 3.3V and 5V Logic Compatible
- Schmitt Trigger Input with internal pull down

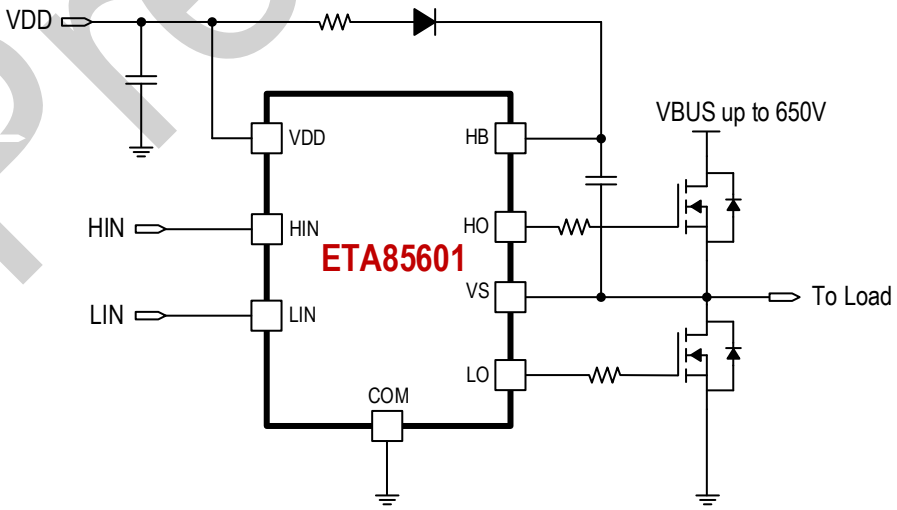
Applications

- Power MOSFET/IGBT Driver
- Motor Drive, Appliances, Refrigerator
- Lighting, LED Power Supply
- DC-to-AC Inverter
- Induction Heating

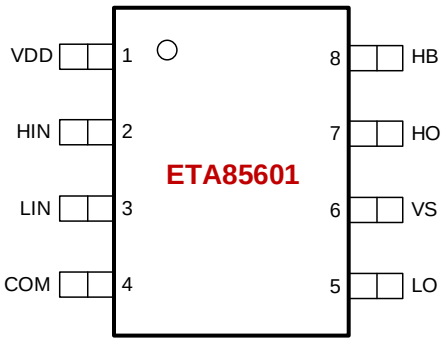
Ordering Information

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA85601FSG	SOP-8	T6YW	5000

Typical Application



Pin Configuration



SOP-8

Absolute Maximum Ratings

Note: 1) All voltages are with respect to COM. Currents are positive into, negative out of the specified terminal. 2) Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

Supply Voltage, VDD.....-0.3 to 20V
Input Voltage, HIN, LIN.....-0.3 to VDD V
Low-Side Output Voltage, LO.....-0.3 to VDD V
High-Side Output Voltage, HO .....-0.3 to HB V
High−Side Floating Supply Voltage, HB ...-0.3 to 670 V
High−Side Floating Offset Voltage, VS .....-5 to 670 V
Allowable VS transient, dVS/dt .....50 V/nS
Operating Junction Temperature .....–40°C to 150°C
Storage Temperature Range .....–60°C to 150°C
Thermal Resistance θ_{JA}
SOP-8.....200..... °C/W
Lead Temperature (Soldering 10sec) .....260°C
ESD HBM (Human Body Mode) 2KV
ESD CDM (Charged Device Mode) 1KV

Recommended Operating Conditions

(Note: Functional operation above the stresses listed in the Recommended Operating Conditions is not implied. Extended exposure to stresses beyond the Recommended Operating Conditions limits may affect device reliability..)

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD	Power supply	10	20	V
HB	High-side floating supply voltage	VS+10	VS+20	V
VS	High-side Floating supply offset voltage	-5	600	V
V_{HIN}, V_{LIN}	Logic input voltage	-0.3	VDD	V
T_A	Ambient Still-Air Operating Temperature	-40	85	°C

Pin Description

PIN #	NAME	TYPE	DESCRIPTION
1	VDD	Power	Positive supply to the low-side driver. Bypass this pin to COM with 1μF or larger value ceremic capacitor
2	HIN	Input	Logic input for high side driver, if HIN is unbiased or floating, HO is held low
3	LIN	Input	Logic input for low side driver, if LIN is unbiased or floating, LO is held low
4	COM	Ground	System ground
5	LO	Output	Low side driver output. Connect to gate of low side power device.
6	VS	HS ground	High side power return. Connect to source of high side power device.
7	HO	Output	High side driver output. Connect to gate of high side power device.
8	HB	HS Power	High side bootstrap supply.

Electrical Characteristics

(VDD=15V, V_{HB}-V_{VS}=15V, unless otherwise specified. Typical values are at T_A = 25°C.)

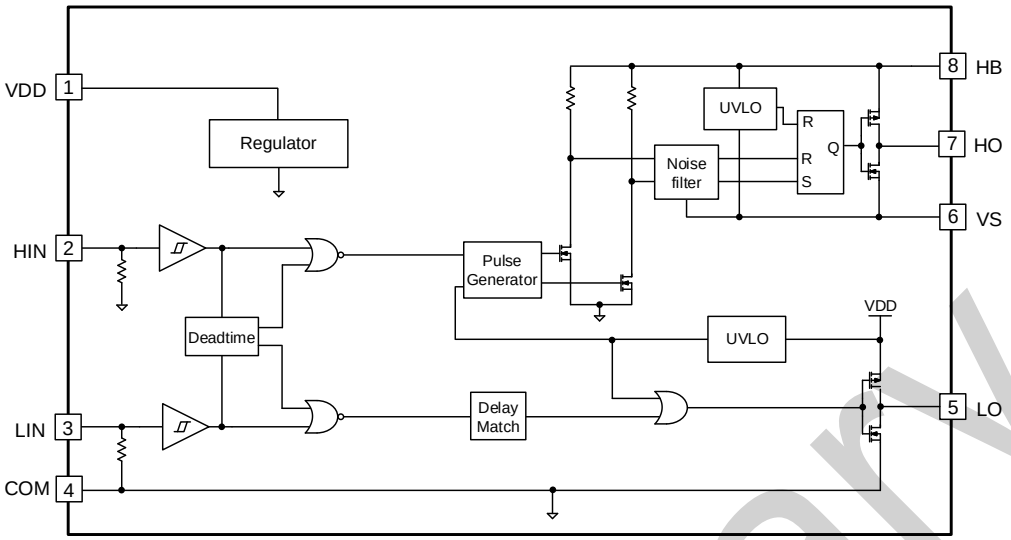
DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
DC Electrical Characteristics						
LOW-SIDE POWER SUPPLY						
V_{DDUV+}	VDD Supply Under-Voltage Positive-Going Threshold	Sweep VDD	8.4	9.0	9.8	V
V_{DDUV-}	VDD Supply Under-Voltage Negative-Going Threshold	Sweep VDD	7.6	8.2	9.2	V
I_{QDD}	Quiescent VDD Supply Current	HIN, LIN = 0 V	–	60	–	uA
I_{PDD}	Operating VDD Supply Current	F= 100 kHz, rms Value	–	2	2.5	mA
HIGH-SIDE POWER SUPPLY						
V_{BSUV+}	VBS Supply Under-Voltage Positive-Going Threshold	V_{BS} = Sweep	7.8	8.7	9.2	V
V_{BSUV-}	VBS Supply Under-Voltage Negative-Going Threshold	V_{BS} = Sweep	6.8	7.7	8.2	V
I_{LK}	Offset Supply Leakage Current	HB = VS = 600 V	–	1	12.5	μA
I_{QBS}	Quiescent VBS Supply Current	HIN, LIN = 0 V	–	25	–	μA
I_{PBS}	Operating VBS Supply Current	F= 100 kHz, rms Value	–	650	–	μA
LOGIC INPUT						
V_{IH}	Logic “1” Input Voltage (HIN, LIN)		2.4			V
V_{IL}	Logic “0” Input Voltage (HIN, LIN)				0.8	V
t_{filter}	Logic input MIN input pulse width			70		ns
I_{IN+}	Logic Input Bias Current (HIN, LIN)	V_{IN} =5 V	–	33	66	μA
I_{IN-}	Logic Input Bias Current (HIN, LIN)	V_{IN} = 0 V	-5	1	5	μA
R_{IN}	Logic Input Pull-Down Resistance		75	150	–	kΩ
HIGH-SIDE AND LOW-SIDE GATE DRIVE						
I_{O+}	Output HIGH Short-Circuit Pulse Current, peak	HIN/LIN from 0V to 5V, CL = 1nF	–	300	–	mA
I_{O-}	Output LOW Short-Circuit Pulsed Current, peak	HIN/LIN from 5V to 0V, CL = 1nF	–	600	–	mA

AC Electrical Characteristics

t_{PDLH}	Turn−On Propagation Delay	V_{LIN} = V_{HIN}= 5 V, V_S = 0 V	–	520	–	ns
t_{PDHL}	Turn−Off Propagation Delay	V_{LIN} = V_{HIN} =0 V, V_S = 0 V	–	170	–	ns
t_R	Turn−On Rise Time	V_{LIN} = V_{HIN} = 5 V, CL=1nF	–	65	–	ns
t_F	Turn−Off Fall Time	V_{LIN} = V_{HIN} = 0 V, CL=1nF	–	25	–	ns
DT	Dead Time		–	350	–	ns
MT	Delay Matching		–	35		ns

Functional Block Diagram



Timing Diagrams

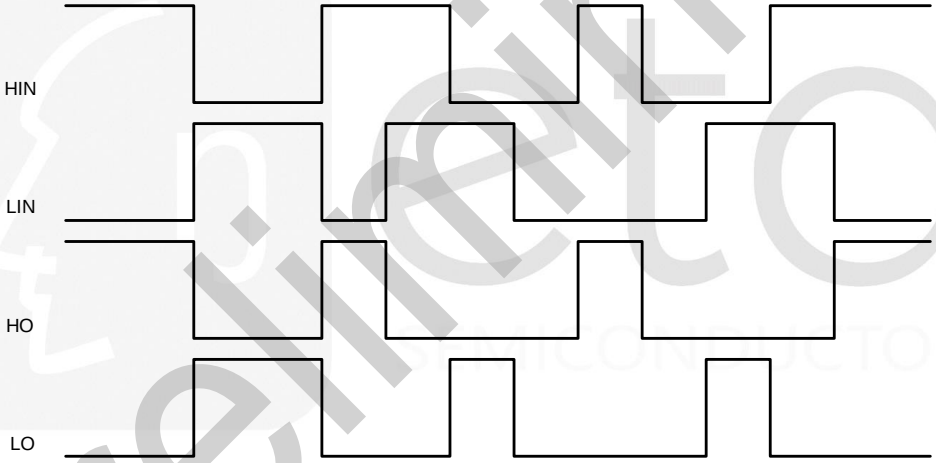


Figure 1. Input and output timing waveform

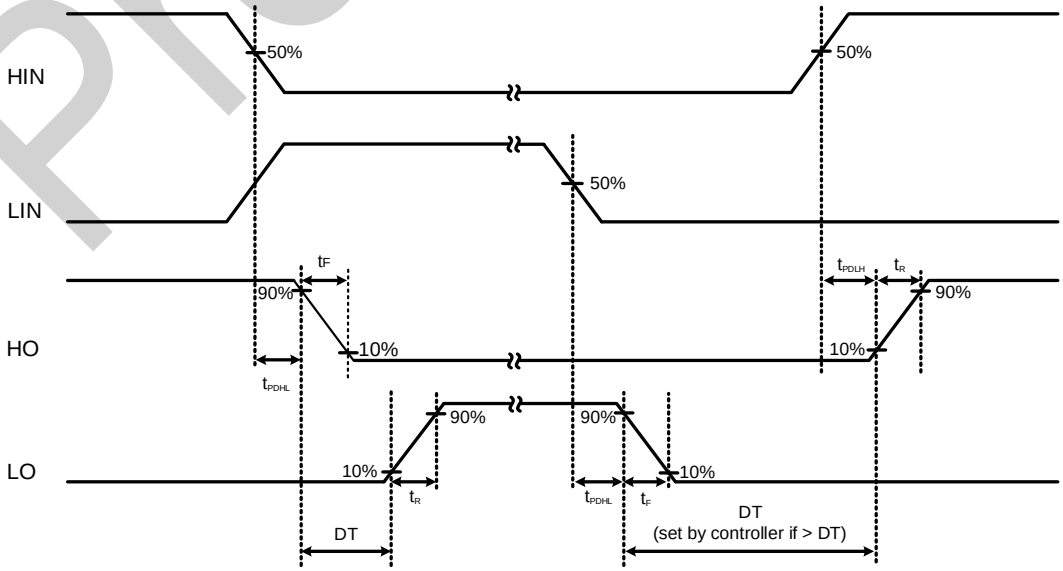


Figure 2. Typical Test Timing Diagram

Functional Description

Input logic compatibility

The input pins are based on a TTL and CMOS compatible input-threshold logic that is independent of the V_{DD} supply voltage. With typical high threshold (V_{IH}) of 2.4 V and typical low threshold (V_{IL}) of 0.8 V, as summarized in Figure 3, the input pins are conveniently driven with logic level PWM control signals derived from 3.3 V and 5 V digital power-controller devices. Wider hysteresis offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. ETA85601 also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The ETA85601 features floating input protection wherein if any of the input pin is left floating, the output of the corresponding stage is held in the low state. This is achieved using pull-down resistors on all the input pins (HIN, LIN) as shown in the block diagram.

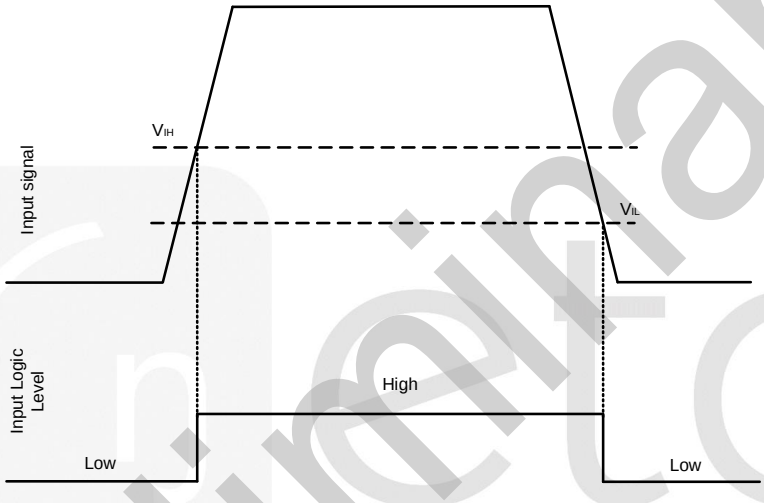


Figure 3. HIN & LIN input thresholds

Undervoltage Lockout

The ETA85601 provides undervoltage lockout protection on both the V_{DD} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 4 is used to illustrate this concept. V_{DD} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{DDUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{DD} voltage fail to reach the V_{DDUV+} threshold, the IC won't turn-on. Additionally, if the V_{DD} voltage decreases below the V_{DDUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high and low-side gate drive outputs.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV+} threshold, the IC won't turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

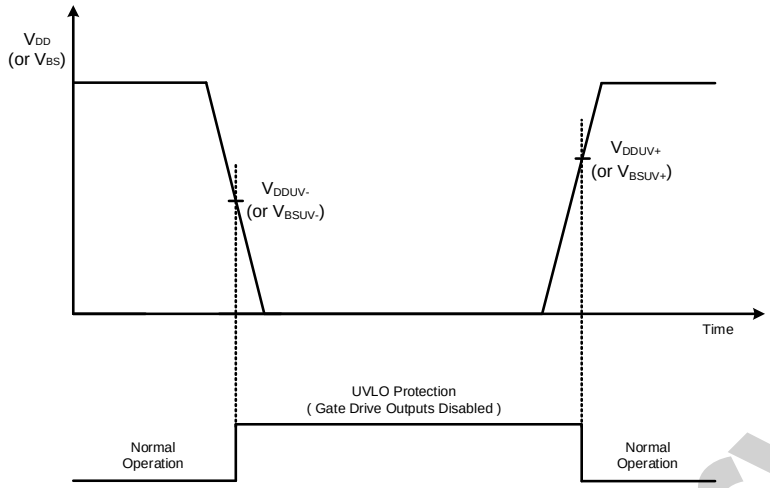


Figure 4. UVLO protection

Shoot-Through Protection

The ETA85601 is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry). The Figure 5 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time.

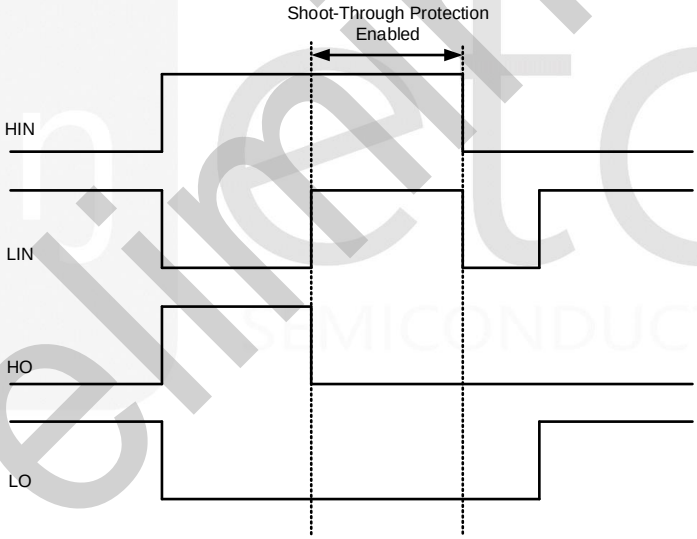


Figure 5. Illustration of shoot-through protection circuitry

Dead time

The ETA85601 features integrated deadtime protection circuitry. The dead time(DT) is automatically inserted whenever the external two input signals (between HIN and LIN signals) toggle high. Figure 6.

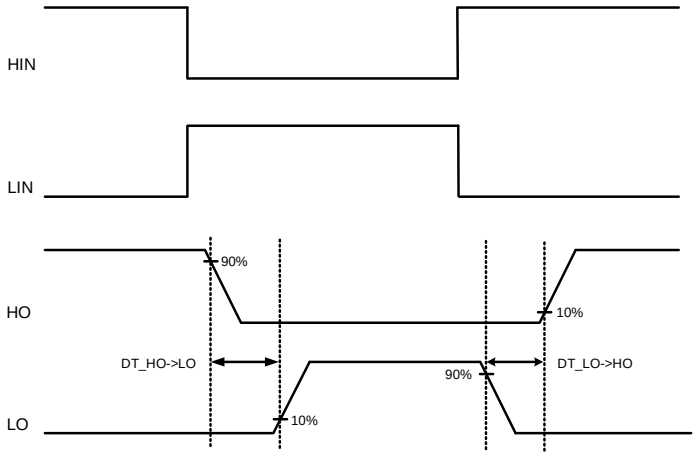


Figure 6. Illustration of deadtime

Matched propagation delays

The ETA85601 is designed with propagation delay matching circuitry. With this feature, the device response at the output to a signal at the input requires approximately the same time duration (turn on or turn off propagation delay) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT).

Application Information

Bootstrap Circuit

Bootstrap Floating Supply

Using a N channel MOSFET as a high side switch requires a voltage supply referenced at the source of the MOSFET. One of the most widely used method in supplying power to the high-side circuitry is the use of the bootstrap floating supply due to its inherent simplicity and inexpensive features. This kind of floating supply is suitable for providing a gate drive circuitry to directly drive high side switches that operate up to rail voltages. The basic circuit of the bootstrap supply, shown in Figure 7, is formed by a diode (D_{BS}) and a capacitor (C_{BS}). But, this type of floating supply has limitations on refreshment of C_{BS} when duty cycle is very high or turn-on time is very long. In the case where the gate voltage is not enough to fully turn-on the MOSFET (Q1), the output of gate drive IC (HO) should be turned-off to prevent the Q1 from operating in high dissipation mode. The optional gate resistor (R_g) is used for the purpose of controlling the turn-on/turn-off time of the Q1, and the bootstrap resistor (R_{BS}) is used to limit the current and prevent the bootstrap capacitor.

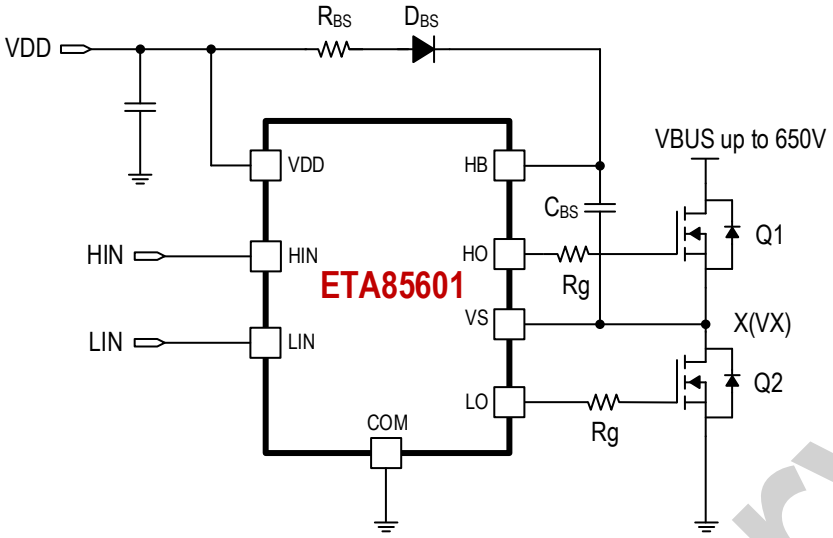


Figure 7. Bootstrap circuit

Operation of Bootstrap Circuit

The charged capacitor (C_{BS}) supplies the voltage to the transistors of the gate drive IC, which is used to turn ON and OFF the external high side switch (Q1). The bootstrap capacitor (C_{BS}) gets charged from the voltage supply (VDD), through the bootstrap diode (D_{BS}), when the voltage at node X (VX) is pulled down to ground or even below ground level. Let us now look at the case that causes the C_{BS} to discharge. C_{BS} discharges when Q1 turns-on or node X is floating. The associated discharging factors are gate drive power, leakage current in each component, and current consumption in the gate drive IC. From an application point of view, specific conditions such as the duty cycle of PWM that causes ripple voltages on C_{BS}, operation frequency, and the type of modulation at which Q1 operates needs to be examined to make sure that C_{BS} can handle.

Selection of Bootstrap Components

Selection of Bootstrap Capacitor

To reduce ripple voltage, ceramic capacitors with low ESR value are recommended for use in the bootstrap circuit. The bootstrap capacitor is determined by the voltage drop level and the total amount of the charge supplied. The maximum voltage drops to be able to turn on the power device of the high-side is determined by following formula.

$$\Delta V_{BS} \leq (V_{DD} - V_F - V_{GSmin} - V_{DSon} - V_{RS})$$

where:

V_{DD} is the gate driver supply voltage.
V_F is the bootstrap diode forward voltage drop.
V_{GSmin} is the minimum gate-source voltage which can turn on the power device.
V_{DSon} is the ON voltage of the low-side power device.
$V_{RS}$is the voltage of the OCP resistance.

The total amount of the charge (Q_{Total}) supplied by the bootstrap capacitor is calculated by the following formula.

$$Q_{Total} = Q_G + Q_{LS} + (I_{QBS} + I_{LKGS} + I_{LK} + I_{LKDIODE} + I_{LKCAP}) * T_{HON}$$

Q_G is MOSFET turn on required Gate charge.
I_{LKGS} is MOSFET gate-source leakage current.
I_{QBS} is Floating section quiescent current.
I_{LK} is Floating section leakage current.

$I_{LKDIODE}$ is Bootstrap diode leakage current.
Q_{LS} is Charge required by the internal level shifters: typical 1nC.
I_{LKCAP} is Bootstrap capacitor leakage current.
T_{HON} is High side on time.
The bootstrap capacitance should satisfy the following formula.

$$C_{BS} \geq \frac{Q_{Total}}{\Delta V_{BS}}$$

However, HB-VS voltage is the voltage that VF of bootstrap diode was dropped. ETA85601 has UVLO function between HB and VS. The value of V_{DD} and C_{BS} should be set so that UVLO does not detect and ΔV_{BS} has margin enough. It is recommended to insert a 1μF ceramic capacitor near HB-VS as a measure against noise.

Selection of Bootstrap Diode

The maximum voltage rating should be higher than power rail (VS) and current rating can be multiplication of total charge and switching frequency. A diode with a fast reverse recovery time is beneficial to minimize the leakage current.

Gate Resistor

The gate resistor $R_{G(on/off)}$ is selected to the switching speed of the power device. The switching time (t_{SW}) is defined as the time spent to reach the end of the plateau voltage, so the turn-on gate resistor $R_{G(on)}$ can be calculated using the following formulas.

$$I_g = \frac{Q_{gs} + Q_{gd}}{t_{sw}}$$

$$R_{total(on)} = R_{pon} + R_{G(on)} = \frac{V_{BS} - V_{gs(th)}}{I_g}$$

$$t_{sw} = \frac{Q_{gs} + Q_{gd}}{I_g} = \frac{(Q_{gs} + Q_{gd})(R_{pon} + R_{g(on)})}{V_{BS} - V_{gs(th)}}$$

Where:

I_g is the gate current of the power device.
Q_{gs} is the charge between gate and source of the power device.
Q_{gd} is the charge between gate and drain of the power device.
$V_{gs(th)}$ is the threshold voltage of the power device.

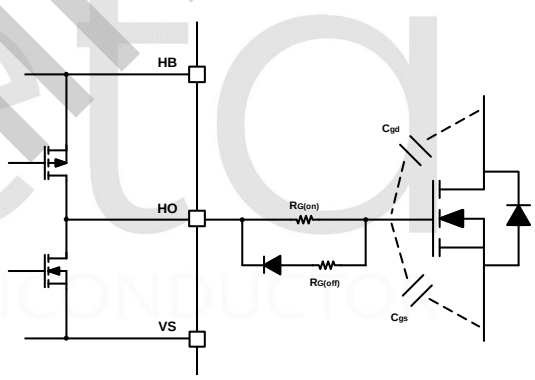


Figure 8. Gate Driver Equivalent Circuit

The turn-on gate resistance can be changed to control output slew rate (dVs/dt). The slew rate of the power device is determined by the following equation.

$$\frac{dVs}{dt} = \frac{I_g}{C_{rss}}$$

where:

C_{rss} is the feedback capacitance.

The gate resistance is determined as following equation.

$$R_{total(on)} = R_{pon} + R_{G(on)} = \frac{V_{BS} - V_{gs(th)}}{C_{rss} \cdot \frac{dVs}{dt}}$$

$$R_{G(on)} = \frac{V_{BS} - V_{gs(th)}}{C_{rss} \cdot \frac{dVs}{dt}} - R_{pon}$$

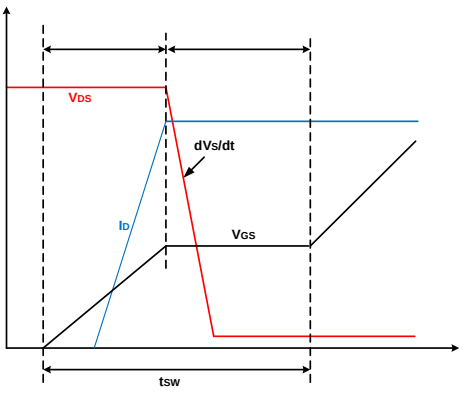


Figure 9. Charge Transfer Characteristics

When other power devices are turned on, current flows in the power device which is off through C_{gd}. At this point, the gate resistance ($R_{G(off)}$) should be set so that the gate voltage does not exceed the threshold of the power device and turn on the power device itself.

$$V_{gs(th)} \geq \left(R_{noff} + R_{G(off)}\right) \cdot I_g = \left(R_{noff} + R_{G(off)}\right) \cdot C_{gd} \frac{dVs}{dt}$$

$$R_{G(off)} \leq \frac{V_{gs(th)}}{C_{gd} \cdot \frac{dVs}{dt}} - R_{noff}$$

Negative voltage transient tolerance of VS pin

In power applications that use half-bridge topologies and typically driving loads with a significant inductive component, the output of the power half-bridge systematically experiences a negative voltage transition, which can be seen in a dynamic contribution as a greater undershoot spike and in a static contribution as a negative static voltage with lower absolute value. This phenomenon happens when the bridge carries out a so-called hard-switching transition towards the low voltage level and the load current is outgoing (from the bridge to the load): when the high-side switch turns off, the output current tends to remain quite constant due to the inductive component of the load, and then has to flow through the low-side freewheeling diode, which turns on going from a high-voltage reverse condition to a forward condition. It is evident that until the output bridge voltage has not reached the “zero” value, the diode is turned off, so the output transition is dominated by the high-side turn-off commutation. After the output voltage reaches a zero voltage level, the diode can turn on and it begins to bring the whole load current in a very brief time, so the high dI_F/dt causes the well-known forward peak voltage, which is the main contribution to the undershoot spikes. Other contributions to dynamic negative voltage are the spikes due to the high dI/dt experienced by the parasitic inductances in series with the freewheeling diode located along the turn-off current path of the half bridge (Figure 10).

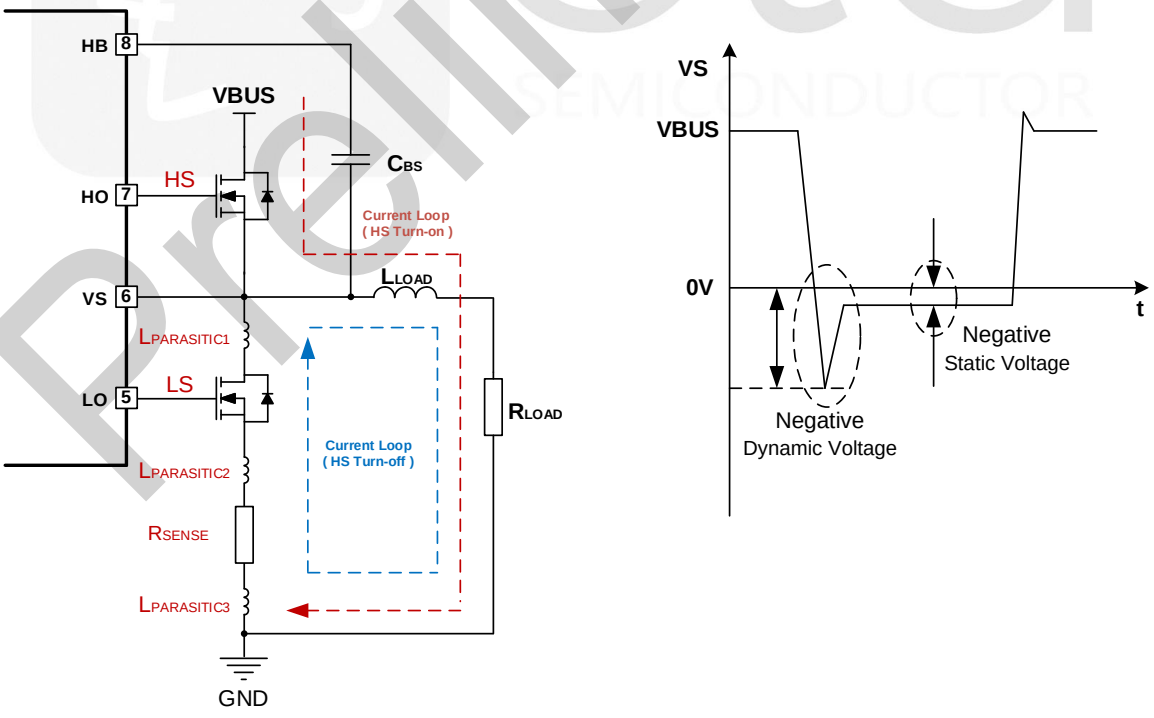


Figure 10. Charge Transfer Characteristics

The negative voltage on the VS pin can be calculated as follows.

$$V_{Smin_{static}} = -(R_{SENSE} \cdot I_{LOAD} + V_F)$$

$$VS_{Spike} = V_{FPK} + L_{PARASITIC} \cdot \frac{dI_F}{dt} + V_{Smin_{static}}$$

Where:

- V_{FPK} is the free-wheeling diode transient peak forward voltage; it depends mainly on the device technology and on the dI_F / dt of the current in the diode. Typical values may range from some volts to more than 10V.
- dI_F / dt is the current slope in the low side IGBT/MOSFET and may have a value from some tens to some hundreds of A/μs. Its value depends mainly on the power switch characteristics and in part on the driving current.
- $L_{PARASITIC}$ is the sum of all parasitic inductances on the current path and mainly depends on the PCB layout. In general, during the design of the power application it is important to pay attention to the layout of the power bridges in order to limit this parameter. Typical values of a good layout are in the order of some tens of nH. Note that it is also useful to use R_{SENSE} resistors with low parasitic inductance for the same reason.
- $R_{SENSE} \cdot I_{LOAD}$ is the value of the V_{SENSE} voltage and is typically less than 1 V, also for thermal dissipation issues on the same resistor.
- V_F is the forward voltage of the free-wheeling diode and is usually less than 2 V.

Reduce the negative voltage spike of VS pin

In order to reduce the negative voltage spike, the following action should be taken:

- Reduce the parasitic inductances.
- Reduce the dI_F/dt by slowing down the turn-off of the high side IGBT/MOSFET.

In most of application the two previous strategies result to be enough to reduce properly the below ground spike voltage, increasing the robustness of power system and then the margin for safe operation of the application. On the other hand in some cases, where the negative voltage spike is significantly higher, the above suggestions may be not sufficient to limit that value and then it could be useful to add some external components to improve further the noise robustness of the power stage section:

- Add a small resistor (2-5 Ω typically) in series to the VS line. The series resistor has the positive effect of limiting the voltage spike on the HB pin, thanks to the filtering effect of such resistor coupled with the bootstrap capacitor. Note that, in order to obtain an effective filtering effect, the resistor must be placed between the minus terminal of bootstrap capacitor and the output of the power stage, as indicated in Figure 11.

In case neither the resistor would not be enough to limit the negative voltage, the following final resolving action could be taken:

- Add a high voltage fast diode between the GND pin and the VS pin (very close to the device pins) in order to clamp directly on the gate driver VS pin the negative voltage spike. Note that, in any case, this diode must be used together with the VS resistance suggested in the previous tip, because it must be avoided that the diode brings the very large load current during low side recirculation, in order to increase the clamping action of the diode itself.

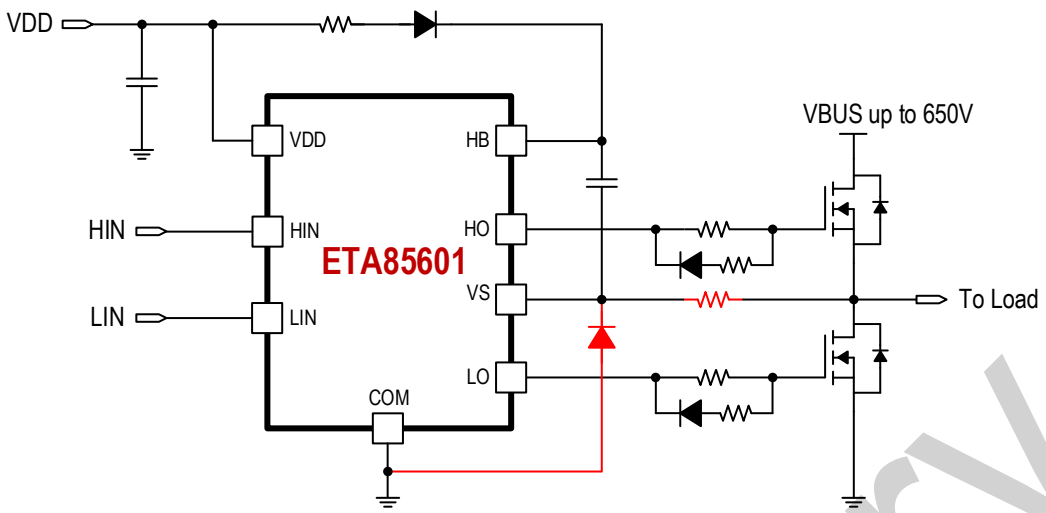


Figure 11. Use of combination of VS resistor and VS diode to limit the negative voltage spike of VS pin

Layout suggestions

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (HB and VS) near the respective high voltage portions of the device.
Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

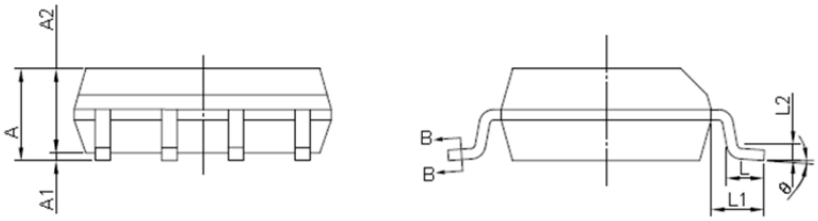
Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise. In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

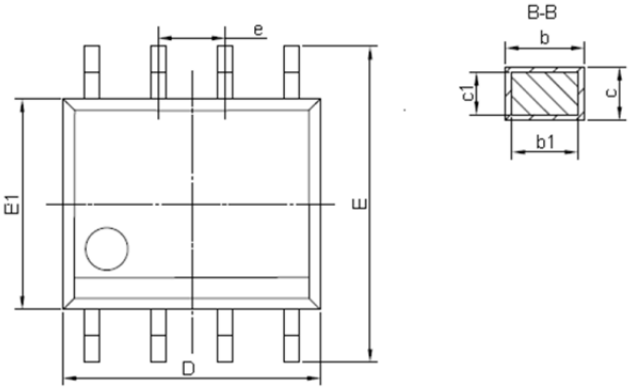
Supply Capacitor: It is recommended to place a bypass capacitor between the VDD and COM pins. A ceramic 1μF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative VS spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the VS pin and the switch node (see Figure 11), and in some cases using a clamping diode between COM and VS.

Package Outline

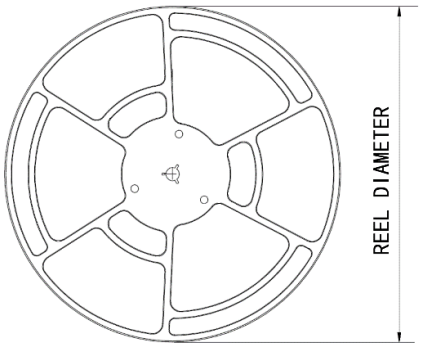
Package: SOP8

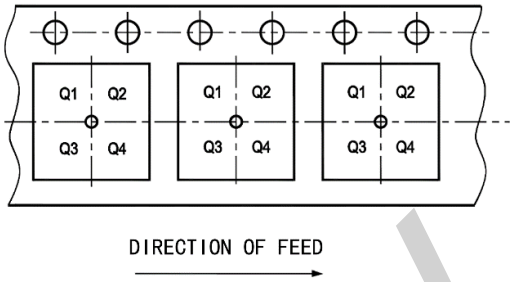


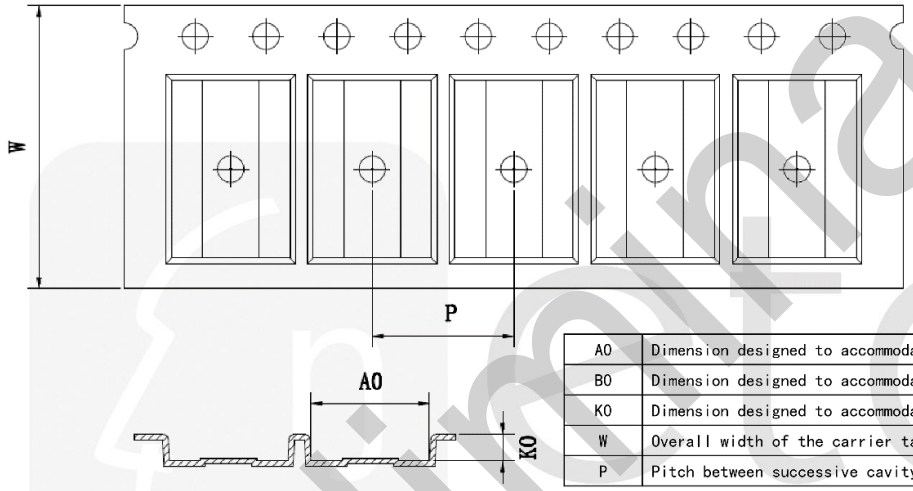


Dimension	MIN	NOM	MAX
A	-	-	1.75
A1	0.1	-	0.25
A2	1.25	-	-
L	0.4	0.835	1.27
L1	-	1.04	-
L2	-	0.25	-
θ	0	-	8
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.1	-	0.25
c1	0.1	-	0.25
D	-	4.9	-
E	-	6	-
E1	-	3.9	-
e	1.27 BSC		
Unit:mm			

Tape and Reel Information







A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P	Pitch between successive cavity centers