LED Controller/Driver

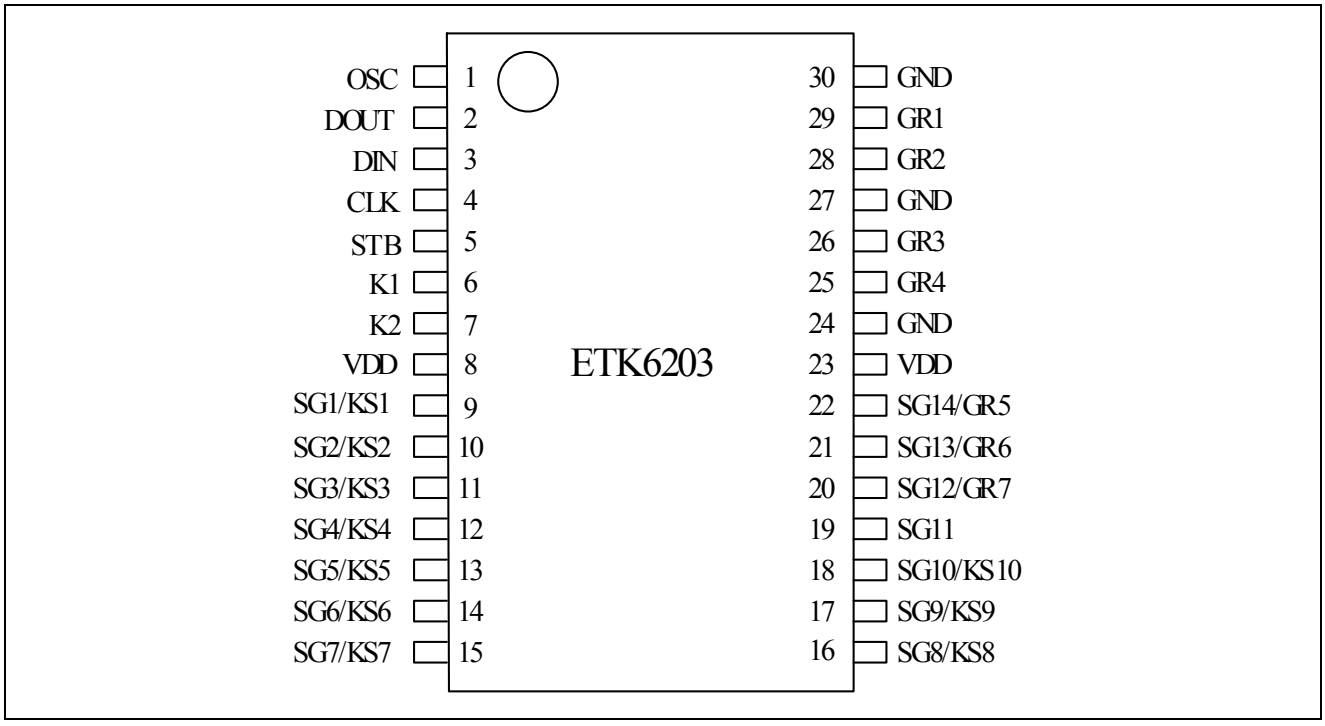
Description

ETK6203 is an LED Controller/driven on a 1/5 to 1/8 duty factor. 11 segment output lines, 4 grid output lines, 3 segment/grid output lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to ETK6203 via a four-line serial interface. Housed in a 30 pins TSSOP, ETK6203 pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

Features

- CMOS Technology
- Low Power Consumption
- Multiple Display Modes (14 segment, 4 Grid to 11 segment, 7 Grid)
- Key Scanning (10×2 Matrix)
- 8-Step Dimming Circuitry
- Serial Interface for Clock, Data Input, Data Output, Strobe Pins and low voltage operation ability when user's MCU power supply is 3.3V.
- Available in 30 pins, TSSOP

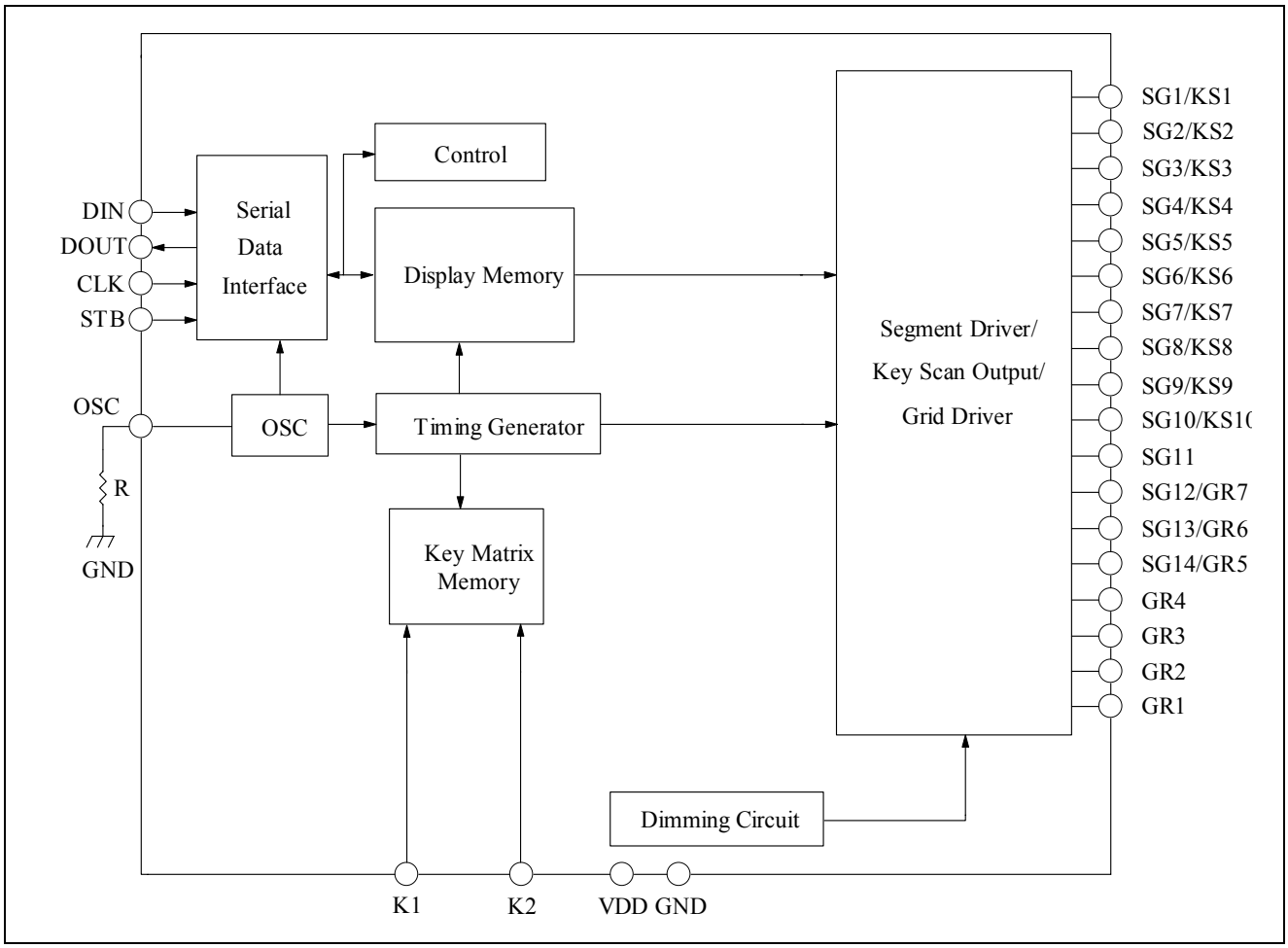
Pin Configuration



Pin Description

Pin No.	Pin Name	I/O	Description
1	OSC	I	Oscillator Input Pin. A resistor is connected to this pin to determine the oscillation frequency.
2	DOUT	O	Data Output Pin (N-channel, Open-Drain). This pin outputs serial data at the falling edge of the shift clock.
3	DIN	I	Data Input Pin. This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit).
4	CLK	I	Clock Input Pin. This pin reads serial data at the rising edge and outputs data at the falling edge.
5	STB	I	Serial Interface Strobe Pin. The data input after the STB has fallen is processed as a command. When this pin is “HIGH”, CLK is ignored.
6，7	K1～K2	I	Key Data Input Pins. The data sent to these pins are latched at the end of the display cycle. (Interface Pull-Low Resistor)
8，23	VDD	—	Power Supply.
9～18	SG1/KS1～SG10/KS10	O	Segment Output Pins (p-channel, open drain). Also acts as the Key Source.
19	SG11	O	Segment Output Pins (p-channel, open drain).
20～22	SG12/GR7～SG14/GR5	O	Segment / Grid Output Pins.
24，27，30	GND	—	Ground Pin.
25，26，28，29	GR4～GR1	O	Grid Output Pins.

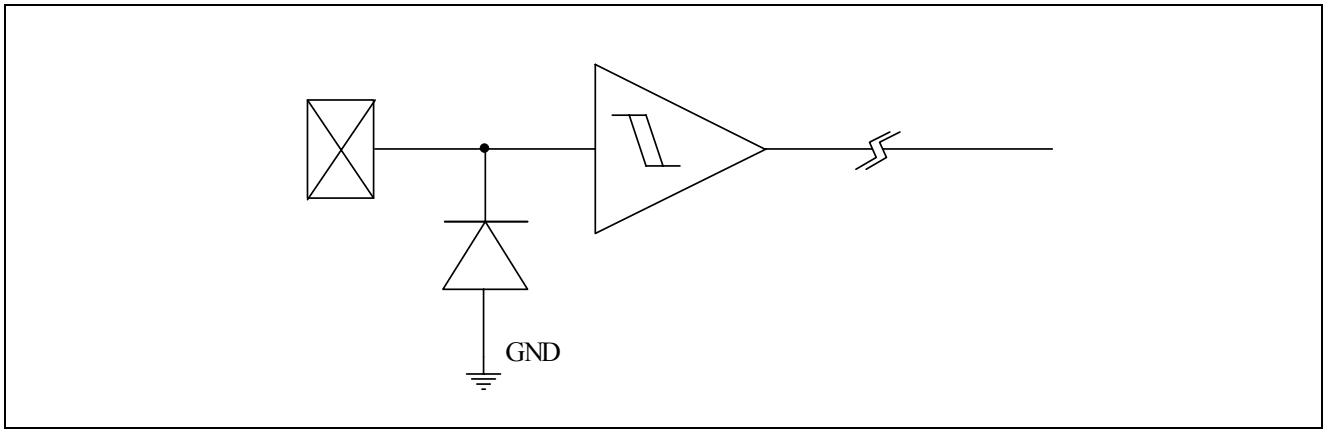
Block Diagram



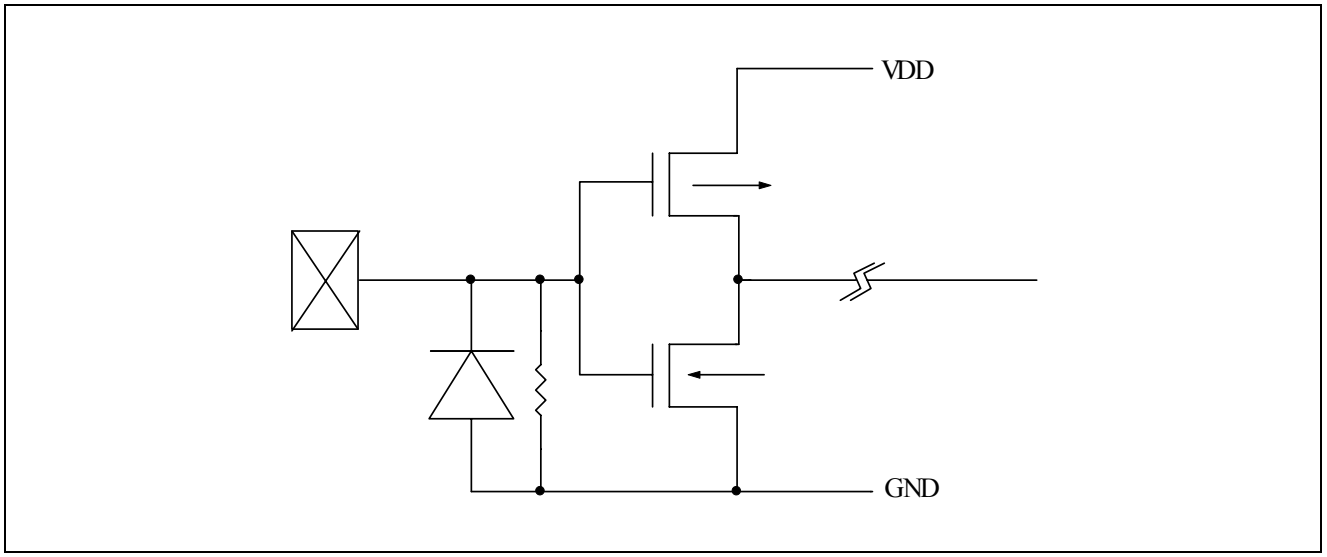
INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below.

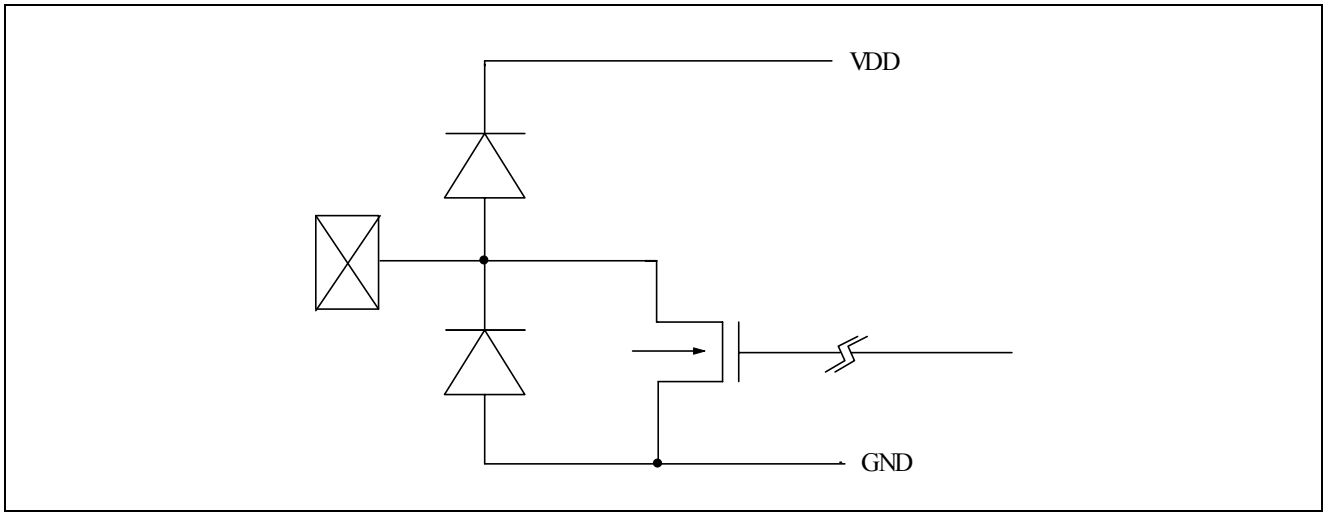
1. Input Pins: CLK, STB & DIN



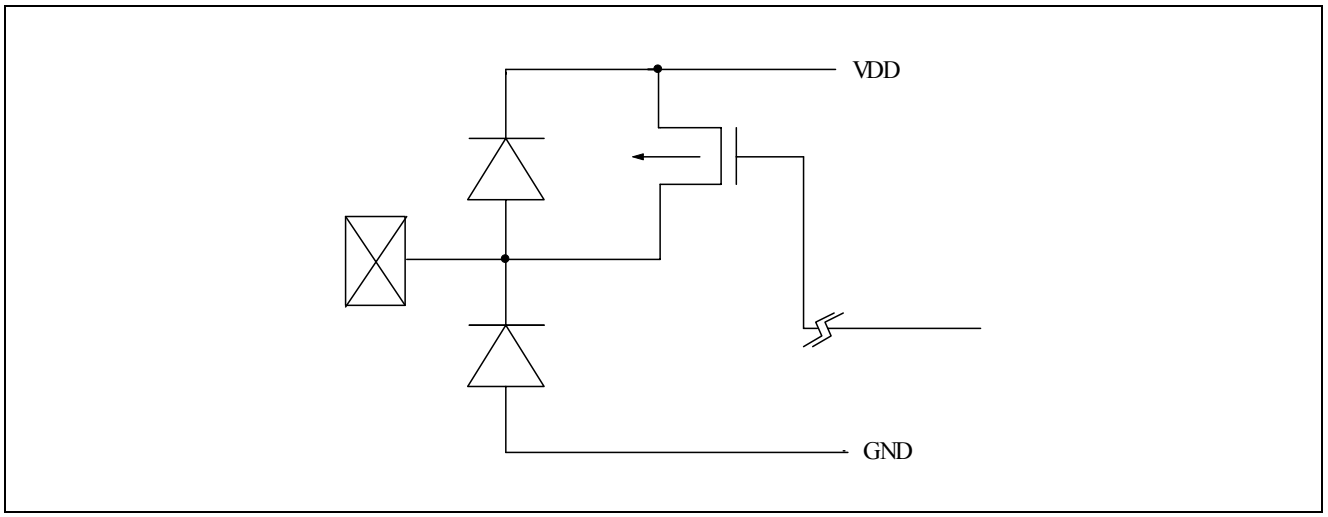
2. Input Pins: K1, K2



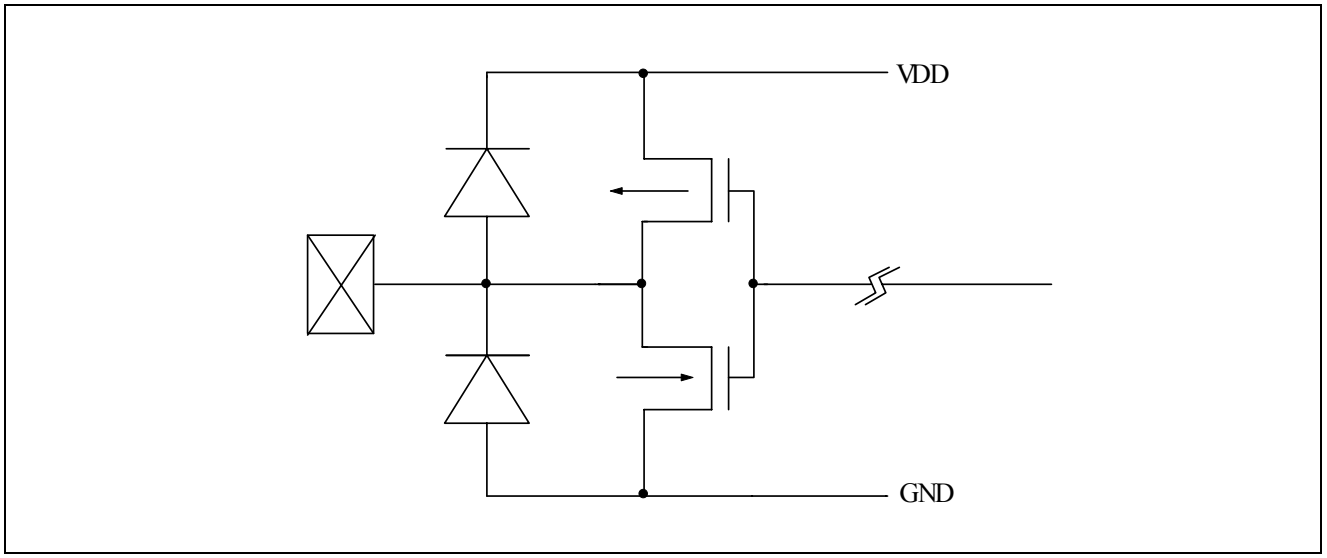
3. Output Pins: DOUT, GR1～GR4



4. Output Pins: SG1～SG11



5. Output Pins: SG14/GR5, SG13/GR6 and SG12/GR7



Functional Description

COMMANDS

A command is the first byte (b0 to b7) inputted to ETK6203 via the DIN Pin after STB Pin has changed from HIGH to LOW State. If for some reason the STB Pin is set to HIGH while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

Command 1：Display Mode Setting Commands

ETK6203 provides 4 display mode settings as shown in the diagram below: As started earlier a command is the first one byte (b0 to b7) transmitted to ETK6203 via the DIN Pin when STB is LOW. However, for these commands, the bit3 & bit8 (b2 to b7) are given a value of 0.

The Display Mode Setting Commands determine the number of segments and grids to be used (14 to 11 segments, 4 to 7 grids). A display command ON must be excited in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned ON, the 7-grid, 11-segment modes is selected.

MSB							LSB
0	0	—	—	—	—	b1	b0

b2～b5: Not Relevant

Display Mode Setting:

b1, b0—0 0: 4 Grids, 14 Segments

b1, b0—0 1: 5 Grids, 13 Segments

b1, b0—1 0: 6 Grids, 12 Segments

b1, b0—1 1: 7 Grids, 11 Segments

Command 2: Data Setting Commands

Data Setting Commands executes the Data Write or Data Read Modes for ETK6203. The data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit7 (b6) is given the value of 1 while bit8 (b7) is given the value of 0. Please refer to the diagram below.

When Power is turned ON, bit4 to bit1 (b3 to b0) are given the value of 0

MSB							LSB
0	1	—	—	b3	b2	b1	b0

b4, b5: Not Relevant

Mode Setting:

b3—0: Normal Operation Mode

b3—1: Test Mode

Address Increment Mode Settings (Display Mode):

b2—0: Increment Address after Data has been written

b2—1: Fixes Address

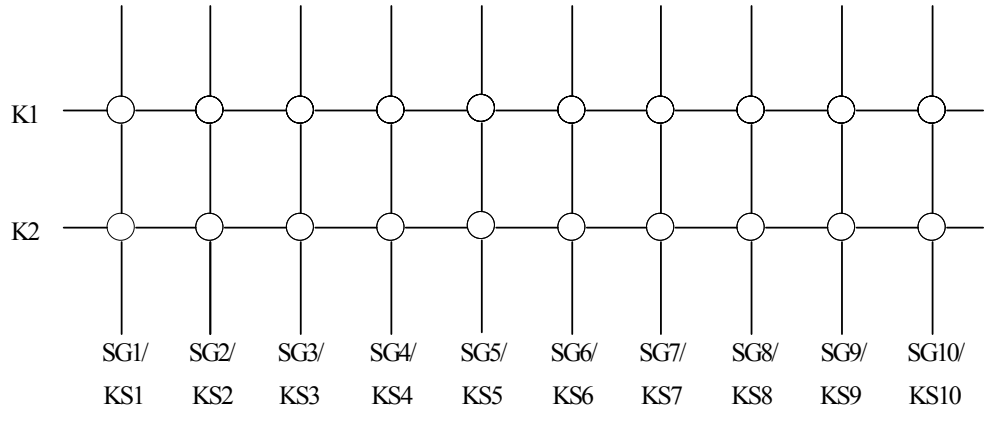
Data Write & Read Mode Setting:

b1, b0—0 0: Write Data to Display Mode

b1, b0—1 0: Read Key Data

ETK6203 KEY MATRIX&KEY INPUT DATA STORAGE RAM

ETK6203 Key Matrix consists of 10×2 array as shown below:



Each data entered by each key is stored as follows and read by a READ Command, starting from the last significant bit of the next data (b7) is read.

K1……**K2**		**K1**……**K2**			READING SEQUENCE
SG1/KS1	x	SG2/KS2	x	x	
SG3/KS3	x	SG4/KS4	x	x	
SG5/KS5	x	SG6/KS6	x	x	
SG7/KS7	x	SG8/KS8	x	x	
SG9/KS9	x	SG10/KS10	x	x	
b0……b1	b2	b3……b4	b5	b6……b7	

Note: b2, b5～b7 do not care.

Command 3: Address Setting Commands

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of 00H to 0DH. If the address is set to 0EH or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at 00H.

MSB							**LSB**
1	1	–	–	b3	b2	b1	b0

b4, b5: Not Relevant

The address of b3～b0: 00H～0DH

DISPLAY MODE AND RAM ADDRESS

Data transmitted from an external device to ETK6203 via the interface are stored in the Display RAM and are assigned address.

The RAM addresses of ETK6203 are given below in 8 bits unit.

SG1……**SG4**	**SG5**……**SG8**	**SG9**……**SG12**	**SG13**……**SG14**	
$00H_L$	$00H_U$	$01H_L$	$01H_U$	DIG1
$02H_L$	$02H_U$	$03H_L$	$03H_U$	DIG2
$04H_L$	$04H_U$	$05H_L$	$05H_U$	DIG3
$06H_L$	$06H_U$	$07H_L$	$07H_U$	DIG4
$08H_L$	$08H_U$	$09H_L$	$09H_U$	DIG5
$0AH_L$	$0AH_U$	$0BH_L$	$0BH_U$	DIG6
$0CH_L$	$0CH_U$	$0DH_L$	$0DH_U$	DIG7

b0……**b3**	**b4**……**b7**
xxH_L	xxH_U
Lower 4 bits	Higher 4 bits

Command 4: Display Control Commands

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF (the key scanning is stopped).

MSB							LSB
1	0	—	—	b3	b2	b1	b0

b4, b5: Not Relevant

Display Setting：

b3—0: Display OFF (Key Scan Continues)

b3—1: Display ON

Dimming Quantity Setting：

000: Pulse width =1/16

001: Pulse width =2/16

010: Pulse width =4/16

011: Pulse width =10/16

100: Pulse width =11/16

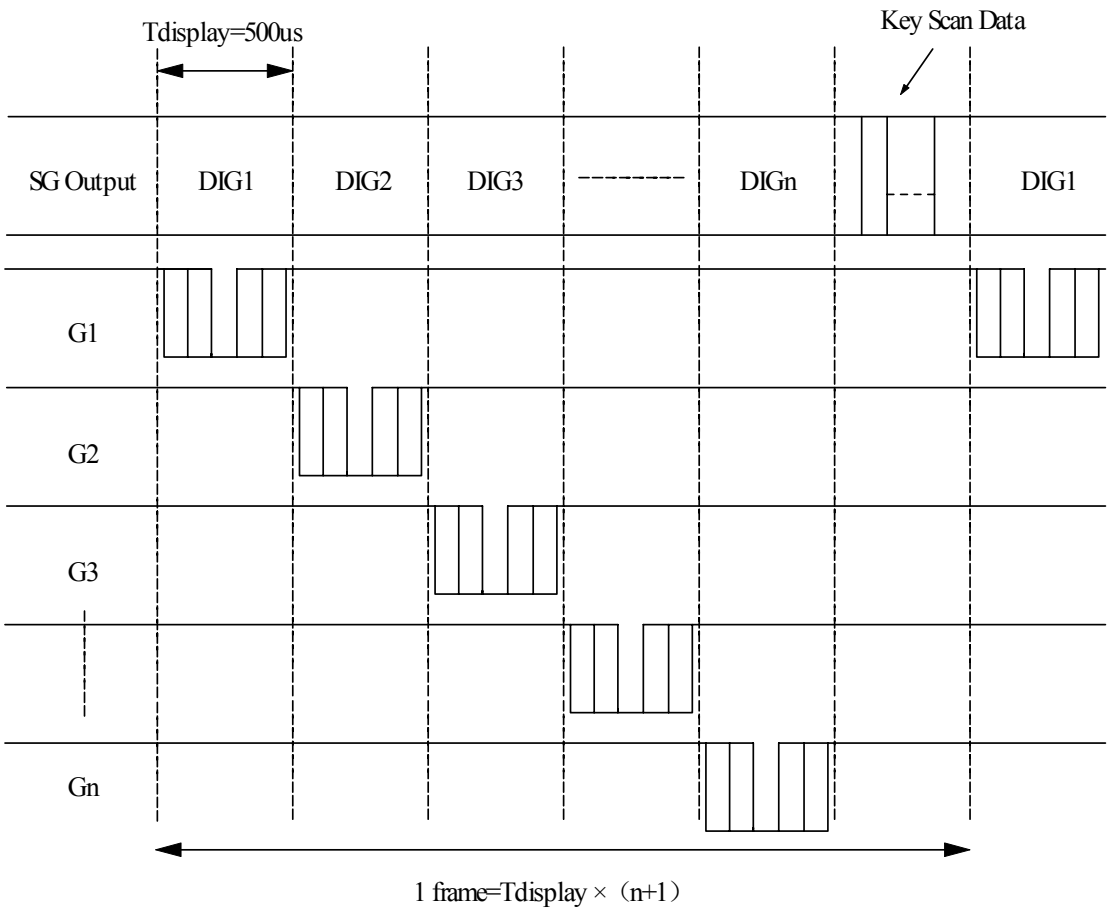
101: Pulse width =12/16

110: Pulse width =13/16

111: Pulse width =14/16

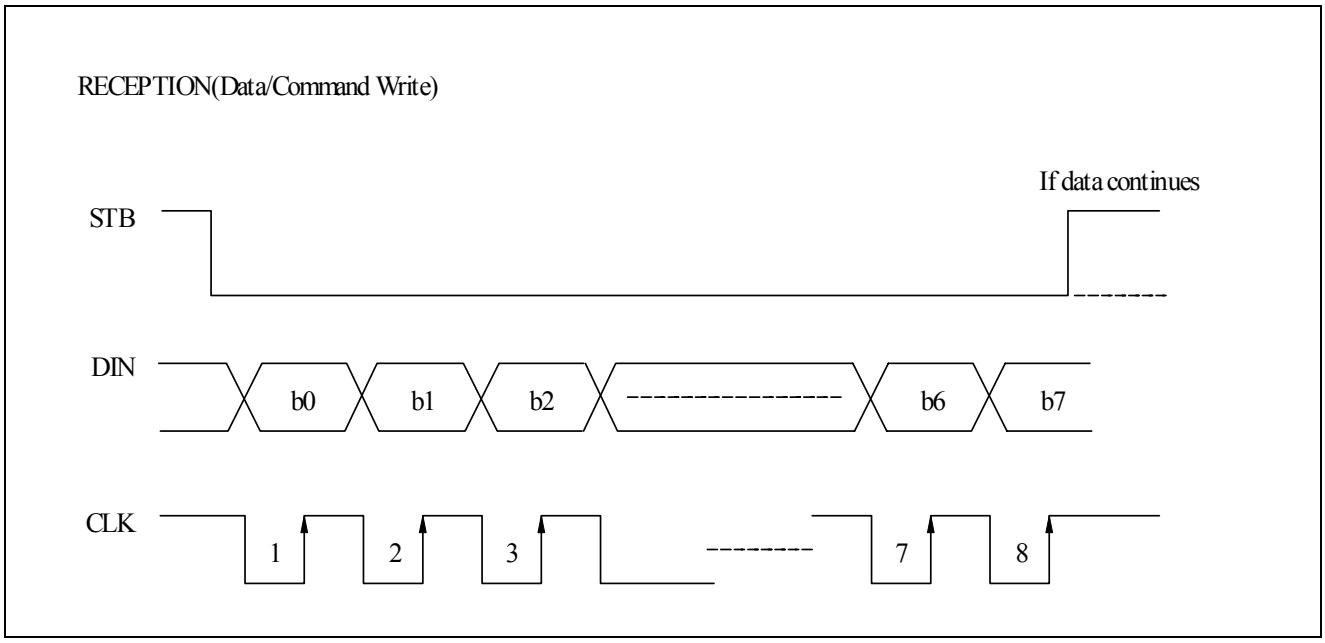
SCANNING AND DISPLAY TIMING

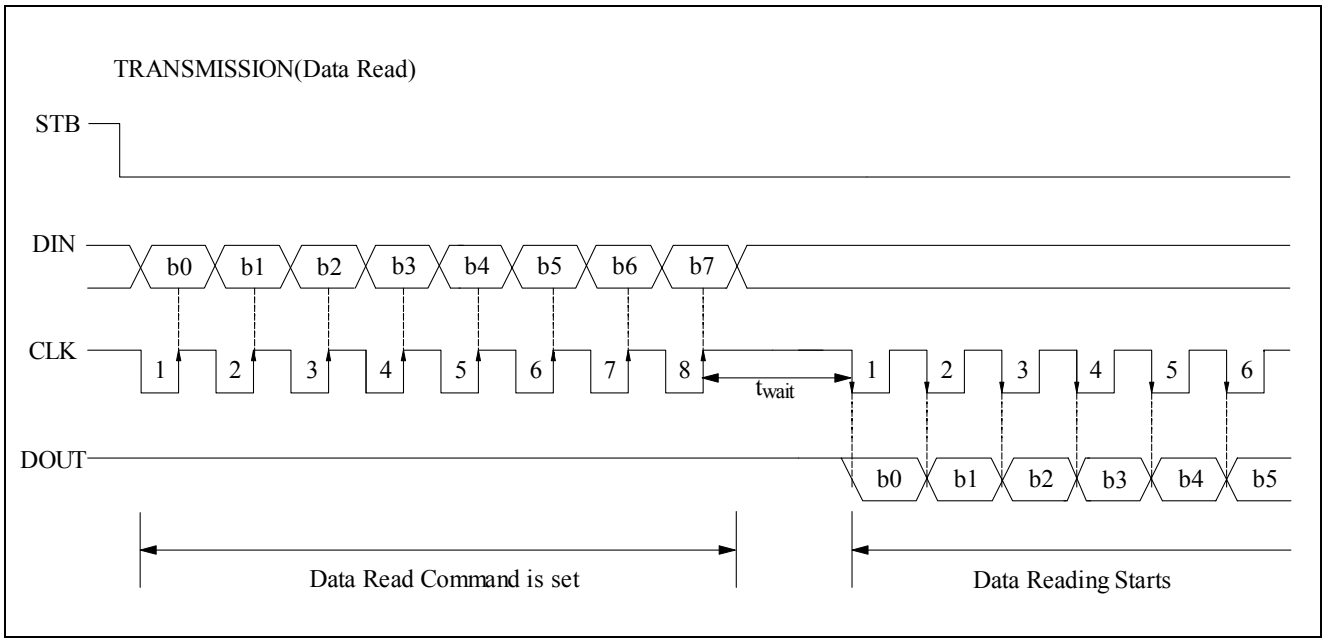
The Key Scanning and Display Timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the 10×2 matrix is stored in the RAM.



SERIAL COMMUNICATION FORMAT

The following diagram shows the ETK6203 serial communication format. The DOUT Pin is an N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor(1K～10K) must be connected to DOUT.



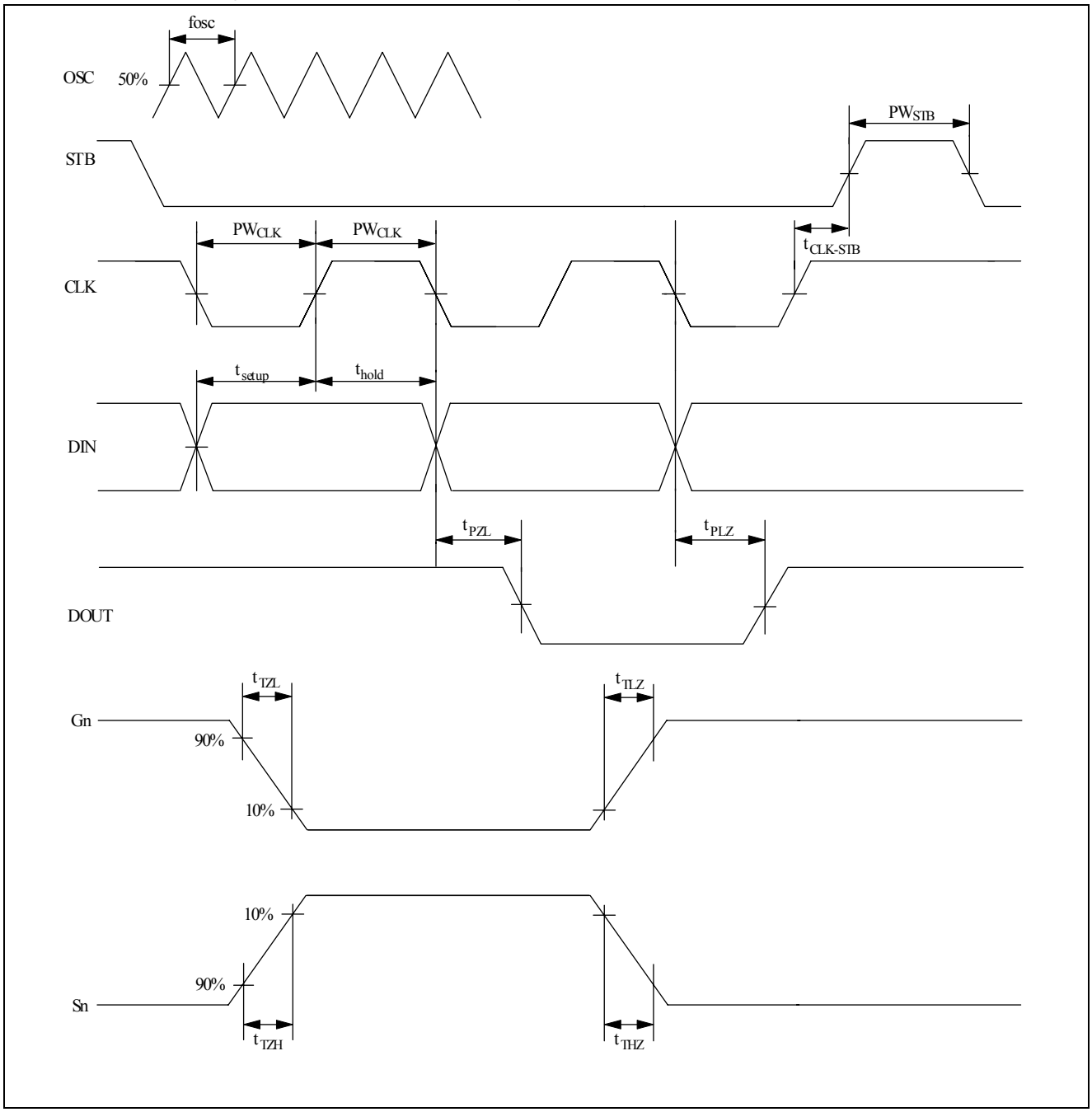


t_{wait} (waiting time) ≥1μs

It must be noted that when the data is read, the waiting time (t_{wait}) between the risings of the eighth clock that has set the command and the galling of the first clock that has read the data is greater or equal to 1μs.

SWITCHING CHARACTERISTIC WAVEFORM

ETK6203 Switching Characteristics Waveform is given below.



PW_{CLK} (Clock Pulse Width) ≥400ns

PW_{STB} (Strobe Pulse Width) ≥1μs

t_{setup} (Data Setup Time) ≥100ns

t_{hold} (Data Hold Time) ≥100ns

$t_{CLK-STB}$ (Clock-Strobe Time) ≥1μs

t_{THZ} (Fall Time) ≤10μs

t_{TZH} (Rise Time) ≤1μs

t_{PZL} (Propagation Delay Time) ≤100ns

fosc=Oscillation Frequency

t_{PLZ} (Propagation Delay Time) ≤300ns

t_{TZL}<1μs

t_{TLZ}<10μs

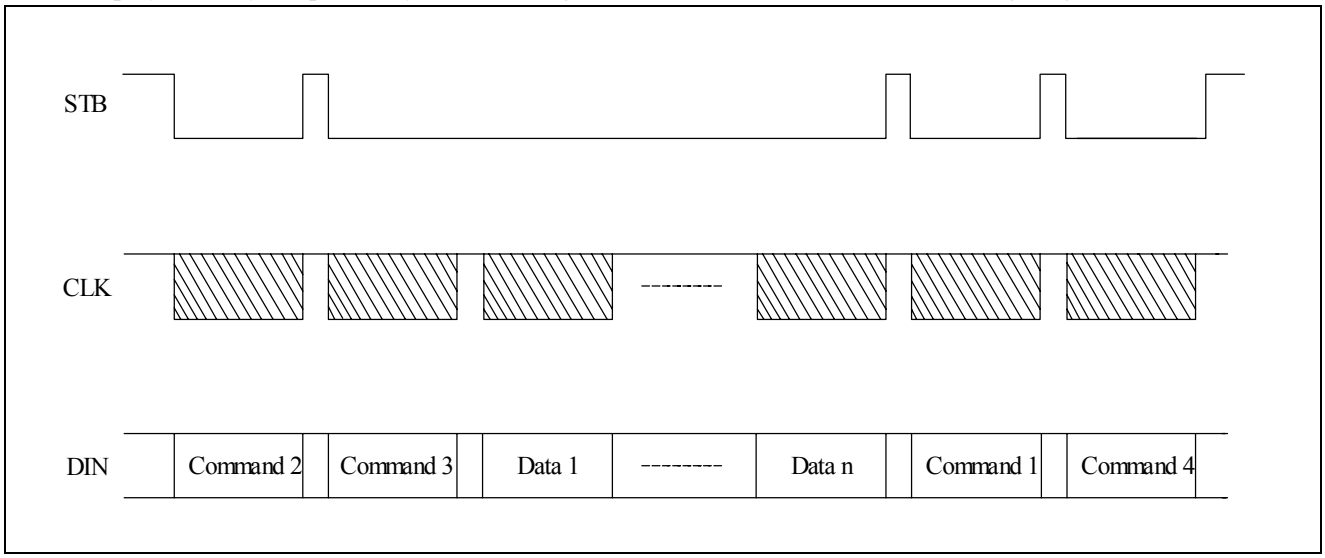
Note: Test condition under

t_{THZ} (Pull low resistor=10kΩ, Loading capacitor=300pF)

t_{TLZ} (Pull low resistor=10kΩ, Loading capacitor =300pF)

APPLICATION

1. Display memory is updated by incrementing addresses. Please refer to the following diagram.



Command 1: Display Mode Setting Command

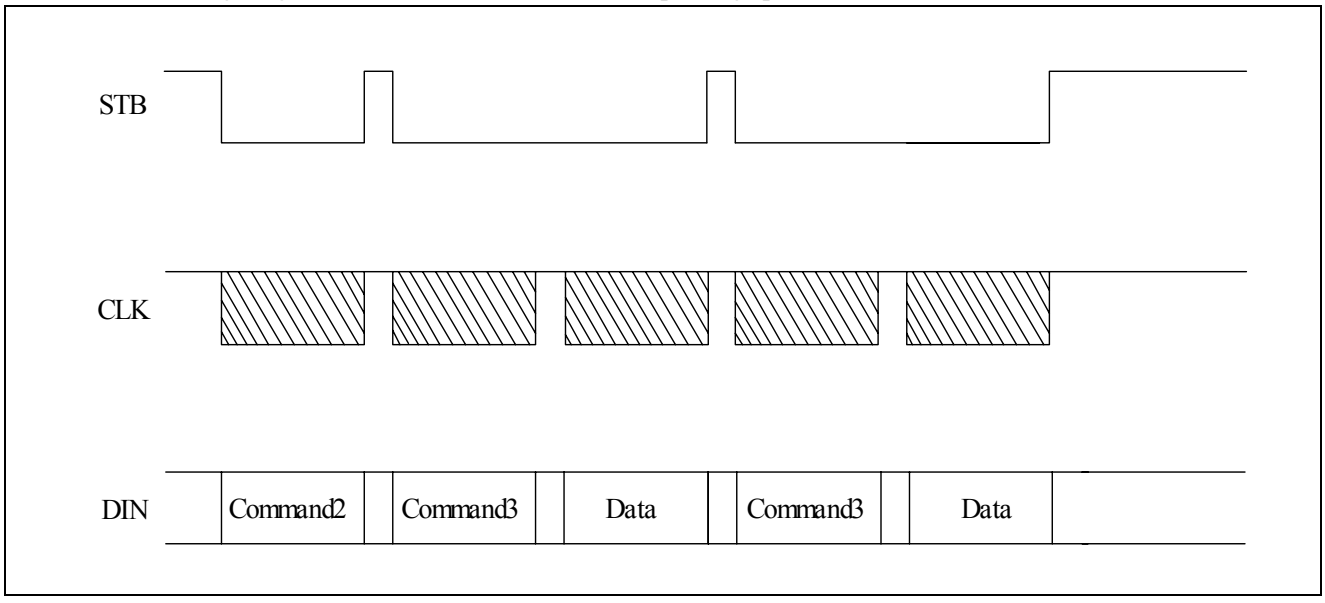
Command 2: Data Setting Command

Command 3: Address Setting Command

Data 1～n: Transfer Display Data (14 Bytes max)

Command 4: Display Control Command

2. The following diagram shows the waveform when updating specific addresses.

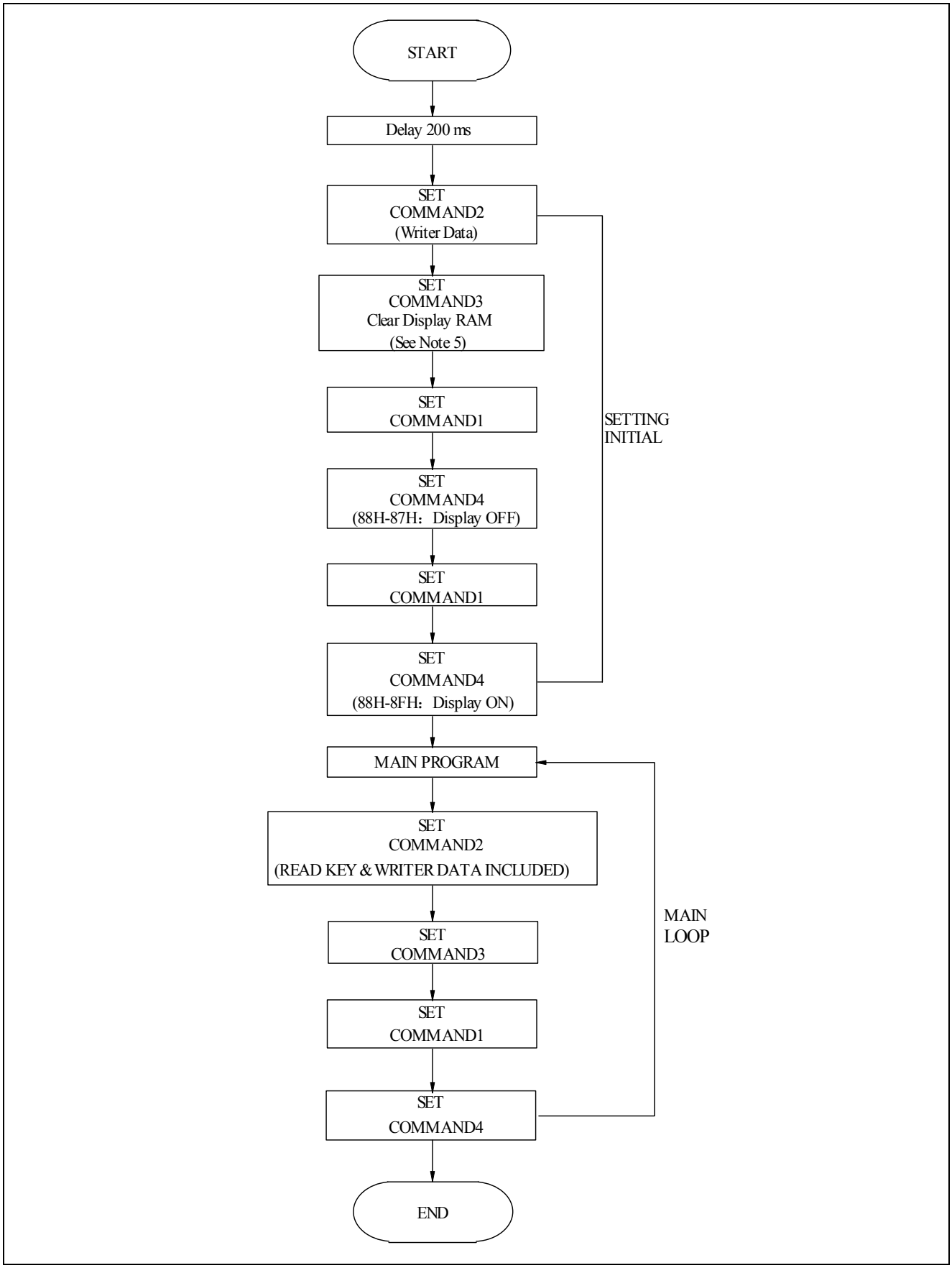


Command 2: Data Setting Command

Command 3: Address Setting Command

Data: Display Data

RECOMMENDED SOFTWARE PROGRAMMING FLOWCHART



Note：

1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands

When IC power is applied for the first time, the content of the Display RAM is not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

Abaolute Maximun Ratings（Ta=25℃, GND=0V）

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	-0.5～+7	V
Logic Input Voltage	V_I	-0.5～V_{DD}+0.5	V
Driver Output Current	I_{OLGR}	+250	mA
	I_{OHSG}	-50	mA
Maximum Driver Output Current/Total	I_{TOTAL}	400	mA
Allowable Power Dissipation	P_D	2	W

Recommended Operating Range（Ta= -20～+70℃, GND=0V）

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic Supply Voltage	V_{DD}	3	5	5.5	V
Dynamic Current(see Note)	I_{DDdyn}	—	—	5	mA
High-Level Input Voltage	V_{IH}	0.8V_{DD}	—	V_{DD}	V
Low- Level Input Voltage	V_{IL}	0	—	0.3V_{DD}	V

Note：Test Condition: Set Display Control Commands=80H (Display Turn OFF State & under no load)

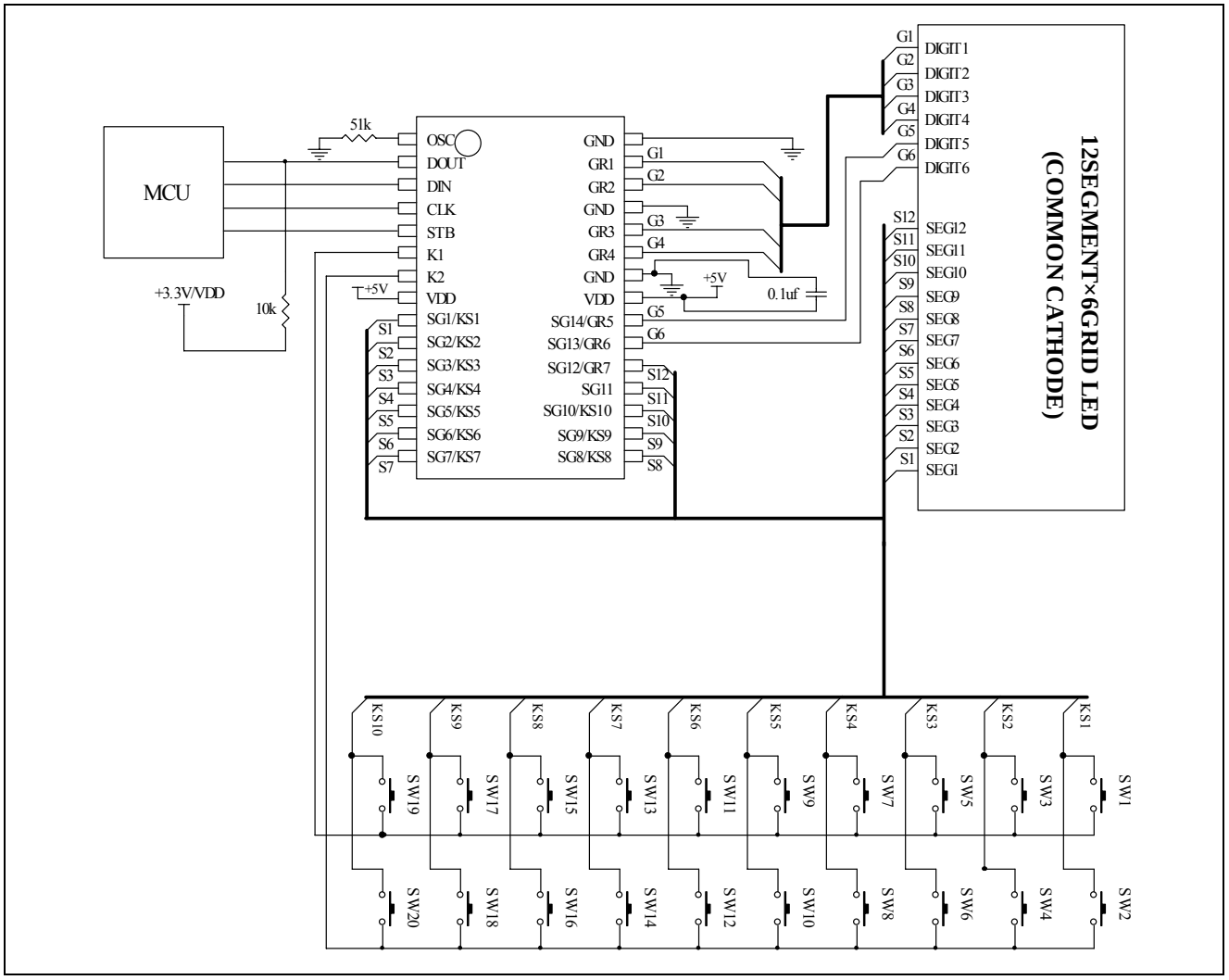
Electrical Characteristics（V_{DD}=5V，GND=0V，Ta=25℃）

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Current	I_{OHSG1}	V_O= V_{DD} -2V SG1～SG11, SG12/GR7~SG14/GR5	-20	-25	-40	mA
	I_{OHSG2}	V_O= V_{DD} -3V SG1～SG11, SG12/GR7~SG14/GR5	-25	-30	-50	mA
Low-Level Output Current	I_{OLGR}	V_O=0.3V GR1～GR4, SG12/GR7~SG14/GR5	100	140	—	mA
Low-Level Output Current	I_{OLDOUT}	V_O=0.4V	4	—	—	mA
Segment High-Level Output Current Tolerance	I_{TOLSG}	V_O= V_{DD} -3V SG1～SG11, SG12/GR7~SG14/GR5	—	—	+5	%
High-Level Input Voltage	V_{IH}	—	0.8V_{DD}	—	5	V
Low-Level Input Voltage	V_{IL}	—	0	—	0.3V_{DD}	V
Oscillation Frequency	fosc	R=51k	560	700	1040	kHz
K1～K2 Pull Down Resistor	R_{KN}	K1～K2 V_{DD} =5V	10	—	50	kΩ

（V_{DD}=3V, GND=0V, Ta=25℃）

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Current	I_{OHSG1}	V_O= V_{DD} -2V SG1～SG6, SG12～SG14	-15	-20	-35	mA
Low-Level Output Current	I_{OLGR}	V_O=0.3V GR1～GR7,	100	140	—	mA
Low-Level Output Current	I_{OLDOUT}	V_O=0.4V	4	—	—	mA
Segment High-Level Output Current Tolerance	I_{TOLSG}	V_O= V_{DD} -3V SG1～SG6, SG12～SG14	—	—	+5	%
High-Level Input Voltage	V_{IH}	—	0.8V_{DD}	—	3.3	V
Low-Level Input Voltage	V_{IL}	—	0	—	0.3V_{DD}	V
Oscillation Frequency	fosc	R=51k	300	420	580	kHz
K1～K2 Pull Down Resistor	R_{KN}	K1～K2 V_{DD} =3V	40	—	100	kΩ

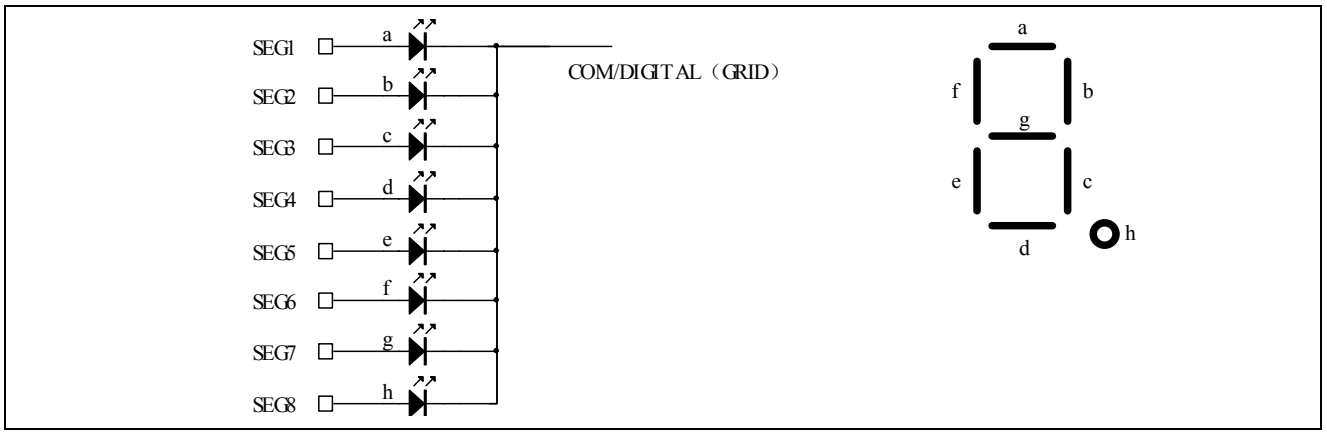
Application Circuit



Notes:

1. The capacitor (0.1μF) connected between the GND and the VDD pins must be located as close as possible to the ETK6203 chip.
2. The ETK6203 power supply is separate from the application system power supply.

COMMON CATHODE TYPE LED PANEL



Package Dimension

TSSOP30