3-W Mono Filterless Class-D Audio Power Amplifier

DESCRIPTION

The EUA2011 is a high efficiency, 3W mono class-D audio power amplifier. A low noise, filterless PWM architecture eliminates the output filter, reducing external component count, system cost, and simplifying design.

Operating in a single 5V supply, EUA2011 is capable of driving 4Ω speaker load at a continuous average output of 3W/10% THD+N or 2W/1% THD+N. The EUA2011 has high efficiency with speaker load compared to a typical class AB amplifier. With a 3.6V supply driving an 8Ω speaker , the efficiency for a 400mW power level is 88%.

In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the EUA2011. The gain of EUA2011 is externally configurable which allows independent gain control from multiple sources by summing signals from separate sources.

The EUA2011 is available in space-saving WCSP and TDFN packages.

FEATURES

- Unique Modulation Scheme Reduces EMI Emissions
- Efficiency at 3.6V With an 8-Ω Speaker:
  - 88% at 400 mW
  - 80% at 100 mW
- Low 2.4-mA Quiescent Current and 0.5-μA Shutdown Current
- 2.5V to 5.5V Wide Supply Voltage
- Shutdown Pin Compatible with 1.8V Logic GPIO
- Optimized PWM Output Stage Eliminates LC Output Filter
- Improved PSRR (−72 dB) Eliminates Need for a Voltage Regulator
- Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor
- Improved CMRR Eliminates Two Input Coupling Capacitors
- Internally Generated 250-kHz Switching Frequency
- Integrated Pop and Click Suppression Circuitry
- 1.5mm × 1.5mm Wafer Chip Scale Package (WCSP) and 3mm × 3mm TDFN-8 package
- RoHS compliant and 100% lead(Pb)-free

APPLICATIONS

- Ideal for Wireless or cellular Handsets and PDAs

Typical Application Circuit

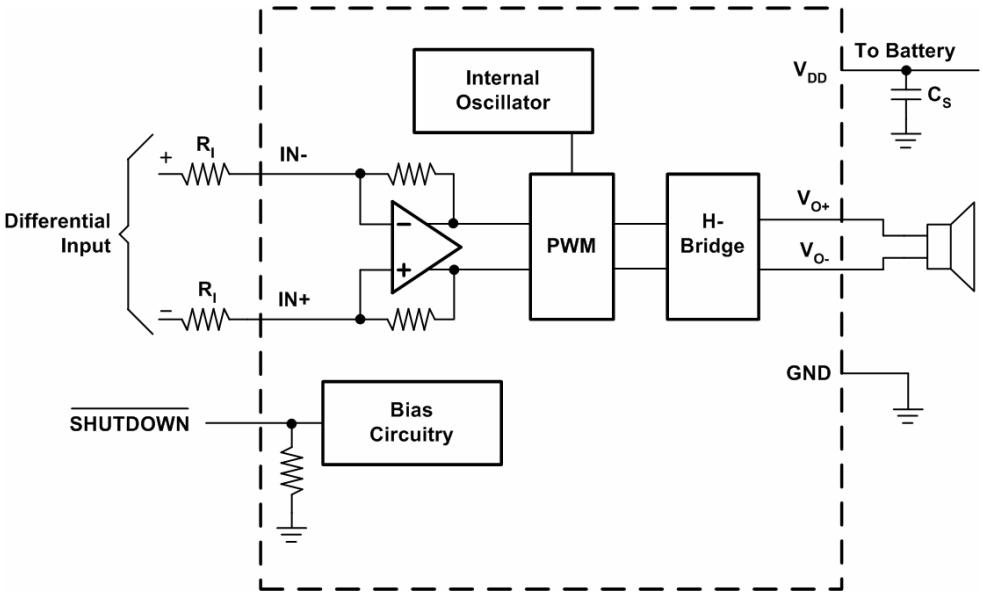
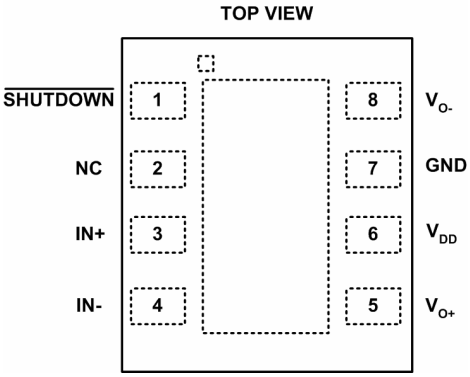
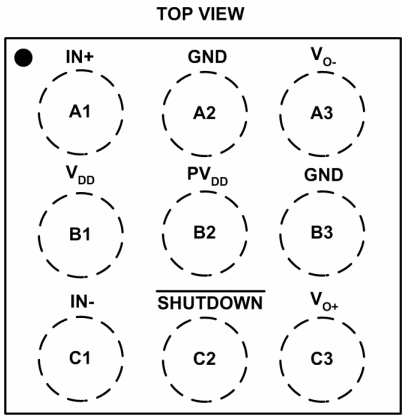


Figure1.

Pin Configurations

Package Type	Pin Configurations	Package Type	Pin Configurations
TDFN-8		WCSP-9	

Pin Description

PIN	TDFN-8	WCSP-9	I/O	DESCRIPTION
$\overline{\text{SHUTDOWN}}$	1	C2	I	Shutdown terminal (active low logic)
PV_{DD}	-	B2	I	Power Supply
+IN	3	A1	I	Positive differential input
-IN	4	C1	I	Negative differential input
V_{O-}	8	A3	O	Negative BTL output
V_{DD}	6	B1	I	Power supply
GND	7	A2/B3	I	High-current ground
V_{O+}	5	C3	O	Positive BTL output
NC	2	-		No internal connection

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUA2011JIR1	TDFN-8	xxxxx A2011	-40 °C to 85°C
EUA2011HIR1	WCSP-9	xxx c0	-40 °C to 85°C

EUA2011 □ □ □ □

- Lead Free Code
  1: Lead Free 0: Lead
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  J: TDFN
  H: WCSP

Absolute Maximum Ratings

- Supply Voltage, V_{DD} ---------- -0.3 V to 6V
- Voltage at Any Input Pin ---------- -0.3 V to V_{DD} +0.3V
- Junction Temperature, T_{JMAX} ---------- 150°C
- Storage Temperature Rang, T_{stg} ---------- -65°C to 150°C
- ESD Susceptibility ---------- 2kV
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ---------- 260°C
- Thermal Resistance
  - θ_{JA} (TDFN) ---------- 47°C/W
  - θ_{JA} (WCSP) ---------- 77.5°C/W

Recommended Operating Conditions

		Min	Max	Unit
Supply voltage, V_{DD}		2.5	5.5	V
High-level input voltage, V_{IH}	$\overline{SHUTDOWN}$	1.3	V_{DD}	V
Low-level input voltage, V_{IL}	$\overline{SHUTDOWN}$	0	0.35	V
Input resistor, R_I	Gain ≤ 20V/V (26dB)	15		kΩ
Common mode input voltage range, V_{IC}	V_{DD}=2.5V,5.5V,CMRR ≤ -49dB	0.5	V_{DD}-0.8	V
Operating free-air temperature, T_A		-40	85	°C

Electrical Characteristics T_A = 25°C (Unless otherwise noted)

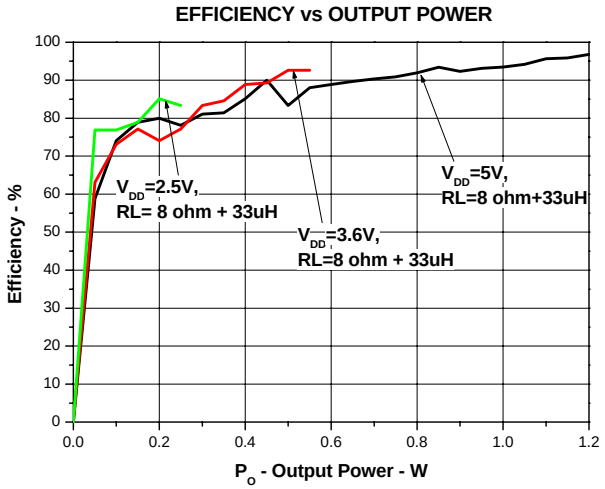
Symbol	Parameter	Conditions	EUA2011			Unit
			Min	Typ	Max.	
$\|V_{OS}\|$	Output offset voltage (measured differentially)	$V_{I=}$ 0V,A_V=2 V/V, V_{DD}=2.5V to 5.5V		1	25	mV
PSRR	Power supply rejection ratio	V_{DD}= 2.5V to 5.5V		-72	-55	dB
CMRR	Common mode rejection ratio	V_{DD}= 2.5V to 5.5V, V_{IC}= V_{DD}/2 to 0.5V, V_{IC}= V_{DD}/2 to V_{DD} -0.8 V		-60	-48	dB
$\|I_{IH}\|$	High-level input current	V_{DD}= 5.5V, V_I= 5.8V			100	µA
$\|I_{IL}\|$	Low-level input current	V_{DD}= 5.5V, V_I= -0.3V			5	µA
$I_{(Q)}$	Quiescent current	V_{DD}= 5.5V, no load		3.5	4.9	mA
		V_{DD}= 3.6V, no load		2.4		
		V_{DD}= 2.5V, no load		2		
$I_{(SD)}$	Shutdown current	V($\overline{SHUTDOWN}$)=0.35V, V_{DD}= 2.5V to 5.5V		0.5		µA
rDS(on)	Static drain-source on-state resistance	V_{DD}= 2.5V		700		mΩ
		V_{DD}= 3.6V		500		
		V_{DD}= 5.5V		400		
	Output impedance in $\overline{SHUTDOWN}$	V($\overline{SHUTDOWN}$)=0.4V		>1		kΩ
$f_{(sw)}$	Switching frequency	V_{DD}= 2.5V to 5.5V	200	250	300	kHz
	Resistance from shutdown toGND			300		kΩ

EUTECH MICROELECTRONICS

Electrical Characteristics T_A = 25°C ,Gain= 2V/V,R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions		EUA2011 Min	EUA2011 Typ	EUA2011 Max.	Unit
P_O	Output power	THD+N=10%, f=1kHz, R_L=4Ω	V_{DD}= 5V		3		W
			V_{DD}= 3.6V		1.4		
			V_{DD}= 2.5V		0.65		
		THD+N=1%, f=1kHz, R_L=4Ω	V_{DD}= 5V		2.15		W
			V_{DD}= 3.6V		1.06		
			V_{DD}= 2.5V		0.49		
		THD+N=10%, f=1kHz, R_L=8Ω	V_{DD}= 5V		1.67		W
			V_{DD}= 3.6V		0.84		
			V_{DD}= 2.5V		0.39		
		THD+N=1%, f=1kHz, R_L=8Ω	V_{DD}= 5V		1.36		W
			V_{DD}= 3.6V		0.66		
			V_{DD}= 2.5V		0.30		
THD+N	Total harmonic distortion plus noise	V_{DD}= 5V,P_O=1W, R_L=8Ω, f=1kHz			0.18		%
		V_{DD}= 3.6V,P_O=0.5W, R_L=8Ω, f=1kHz			0.18		
		V_{DD}= 2.5V,P_O=200mW, R_L=8Ω, f=1kHz			0.17		
kSVR	Supply ripple rejection ratio	V_{DD}= 3.6V, Inputs ac-grounded with C_I= 2μF	f=217 Hz, $V_{(RIPPLE)}$=200mVpp		-60		dB
SNR	Signal-to-noise ratio	V_{DD}= 5V,P_O=1W, R_L=8Ω			93		dB
Vn	Output voltage noise	V_{DD}= 3.6V, f=20Hz to 20kHz,Inputs ac-grounded with C_I= 2μF	No weighting		62		μV_{RMS}
			A weighting		45		
CMRR	Common mode rejection ratio	V_{DD}= 3.6V, V_{IC}=1 V_{PP}	f=217 Hz		-55		dB
Z_I	Start-up time from shutdown	V_{DD}= 3.6V			11.5		ms

Typical Operating Characteristics



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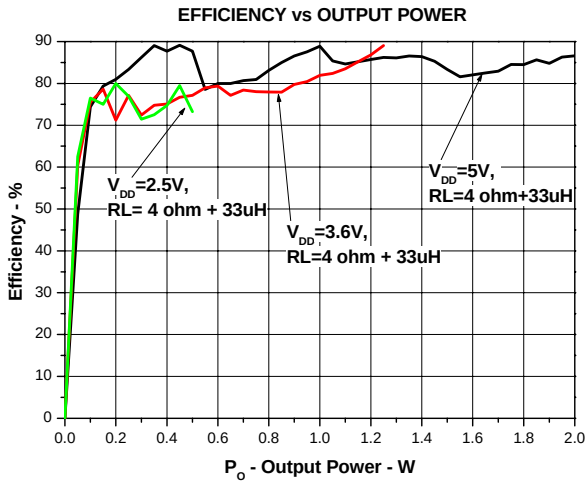

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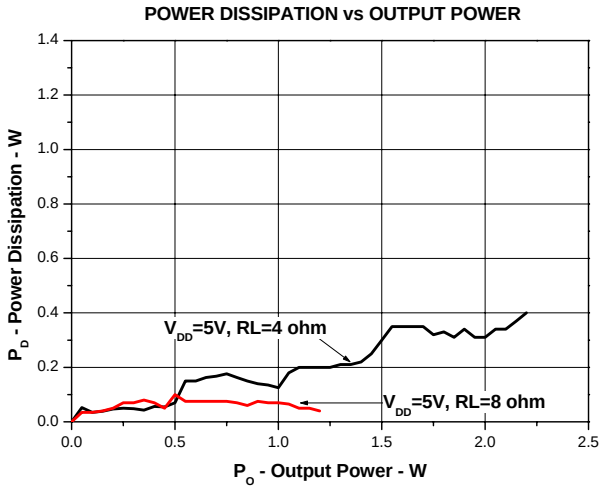

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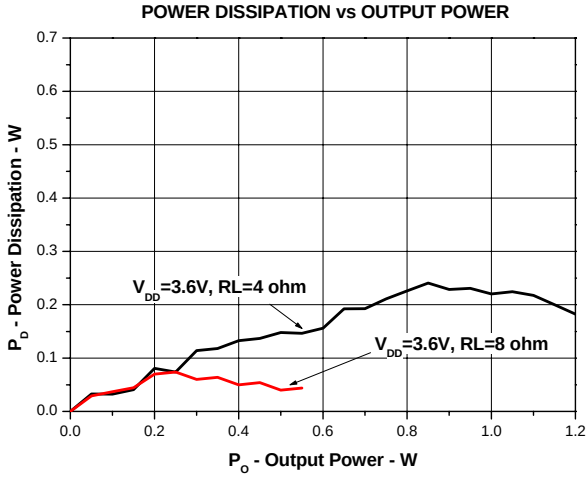

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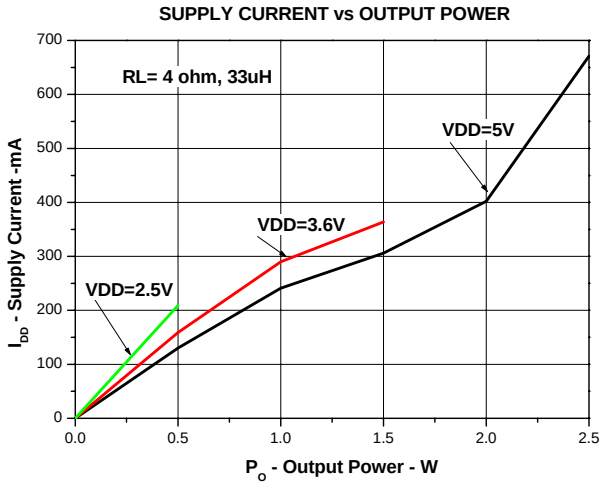

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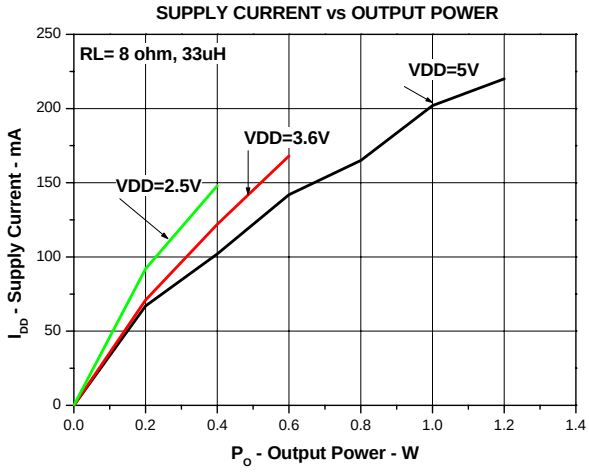

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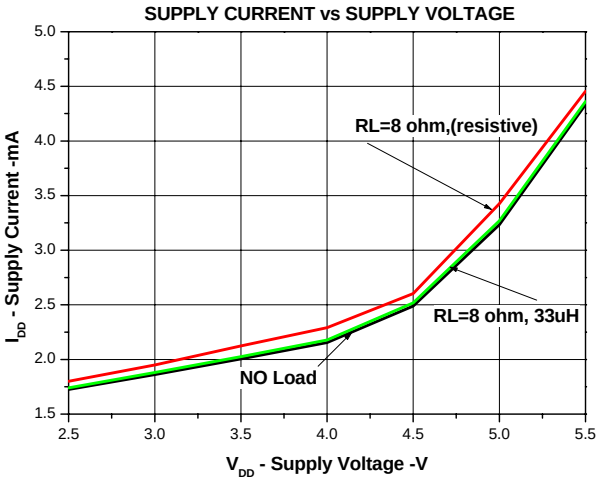

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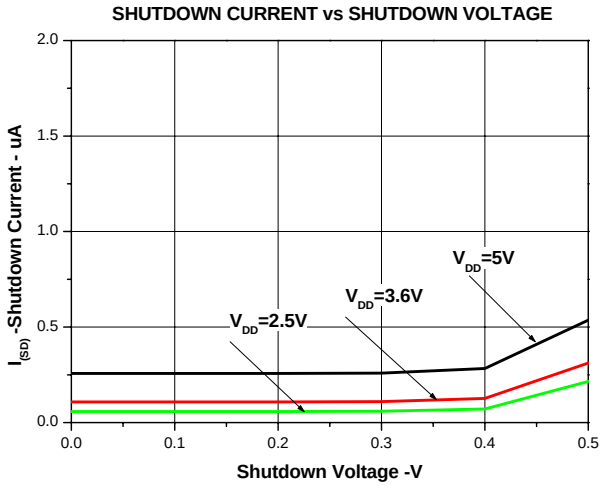

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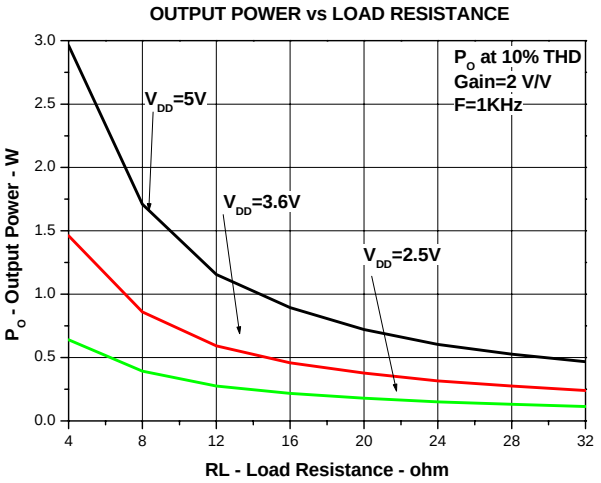

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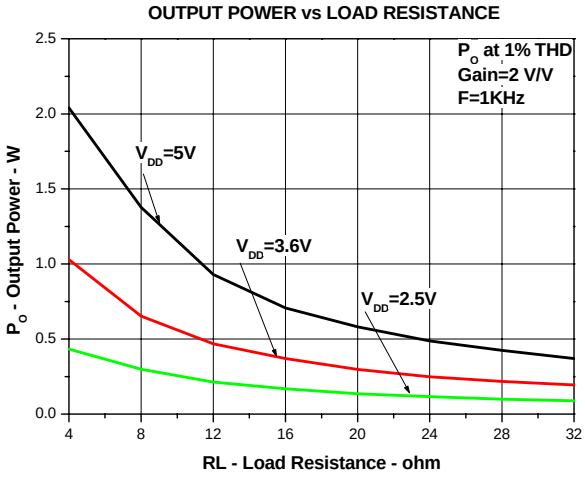

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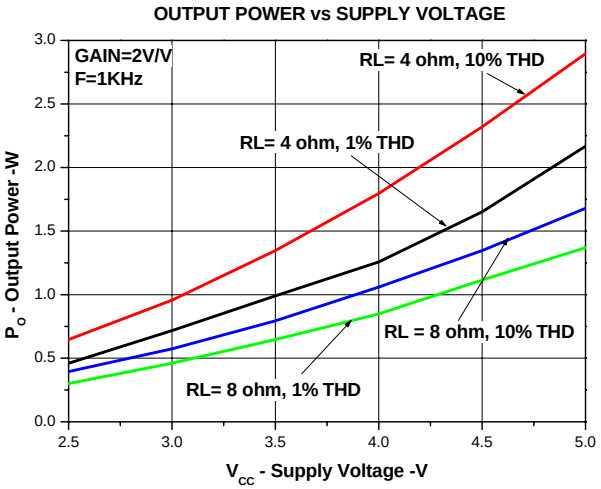

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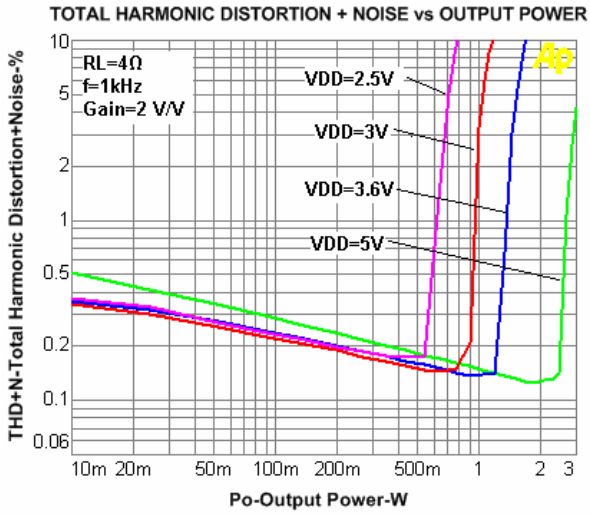

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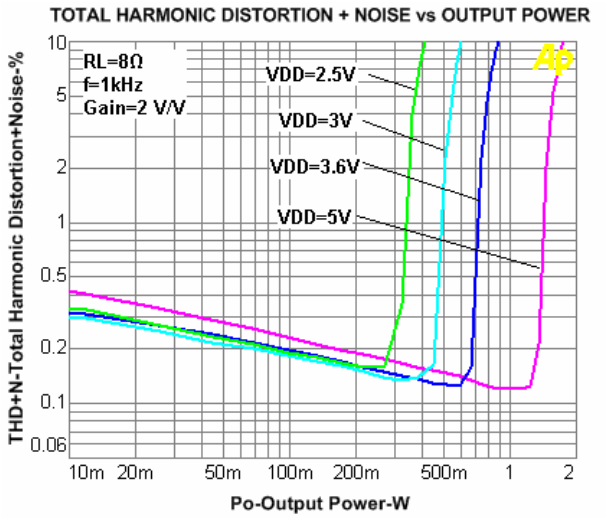

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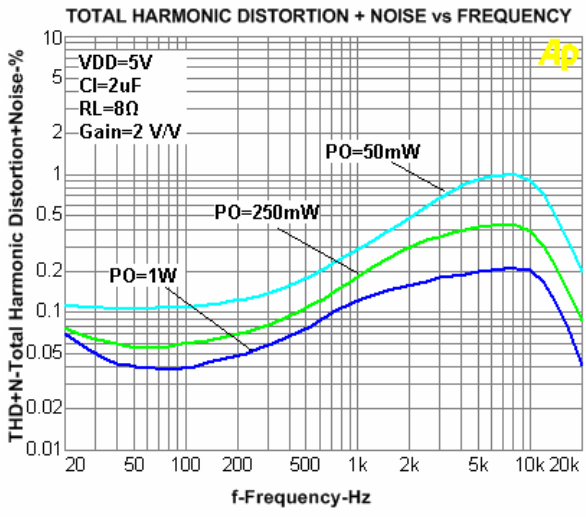

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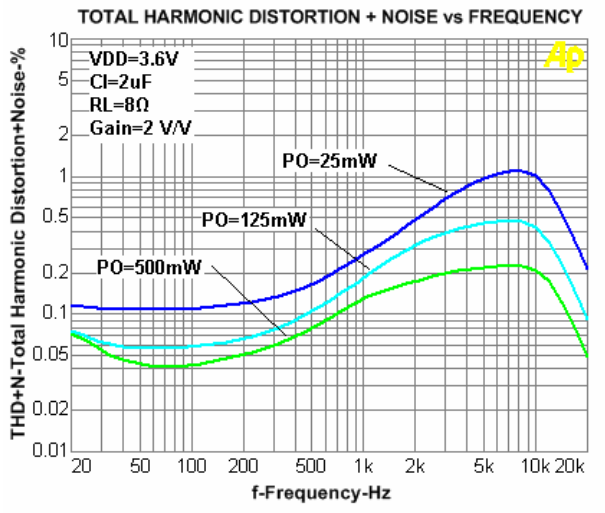

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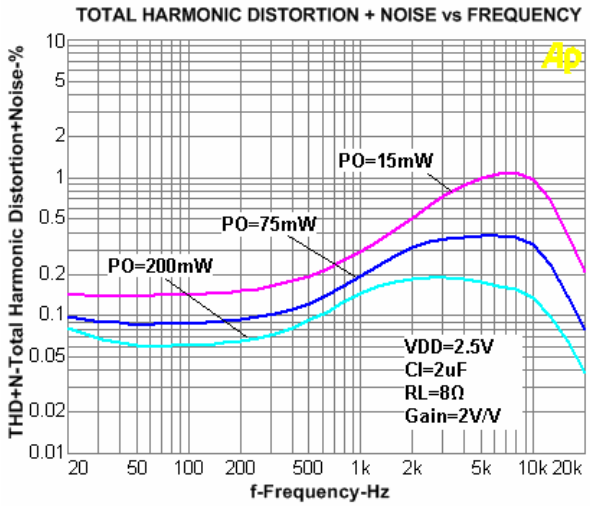

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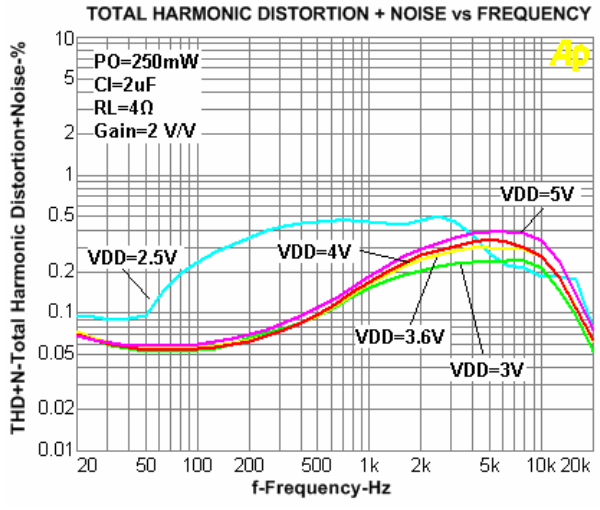

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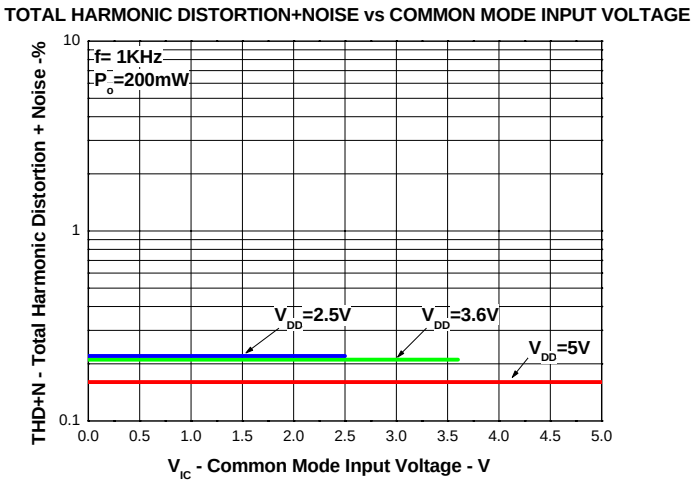

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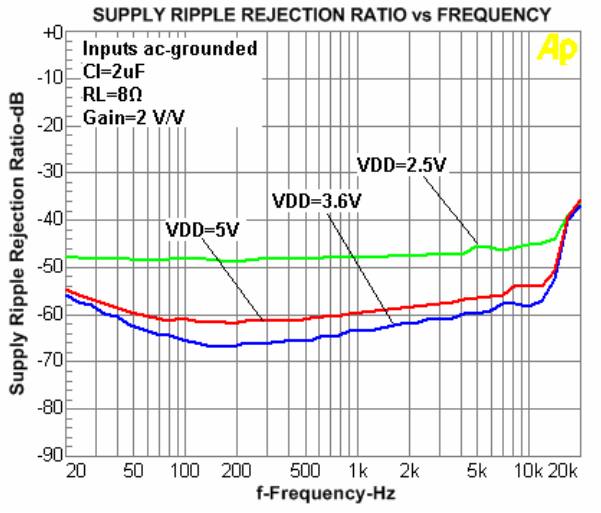

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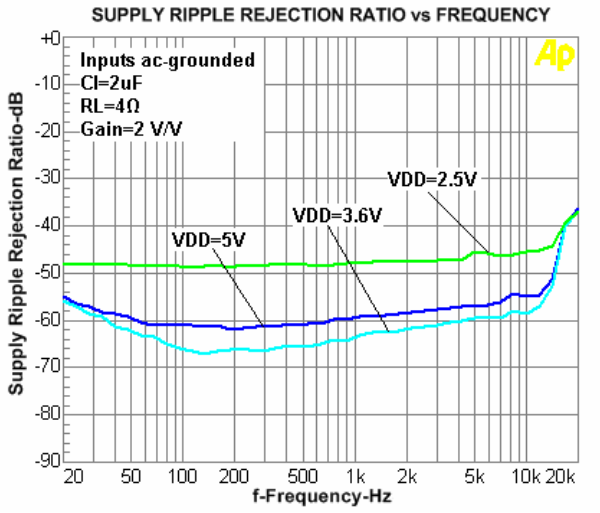

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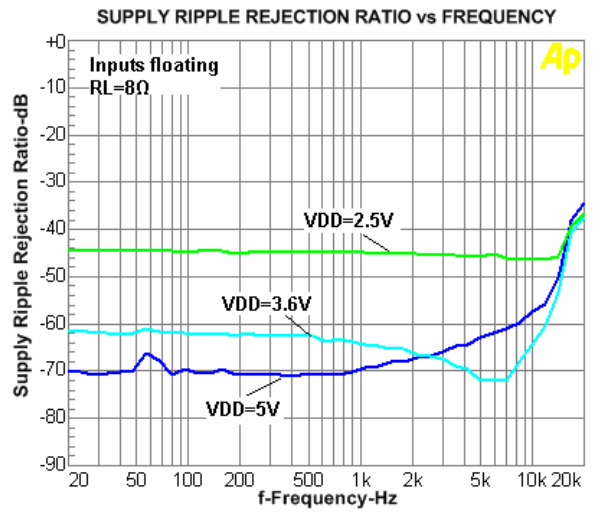

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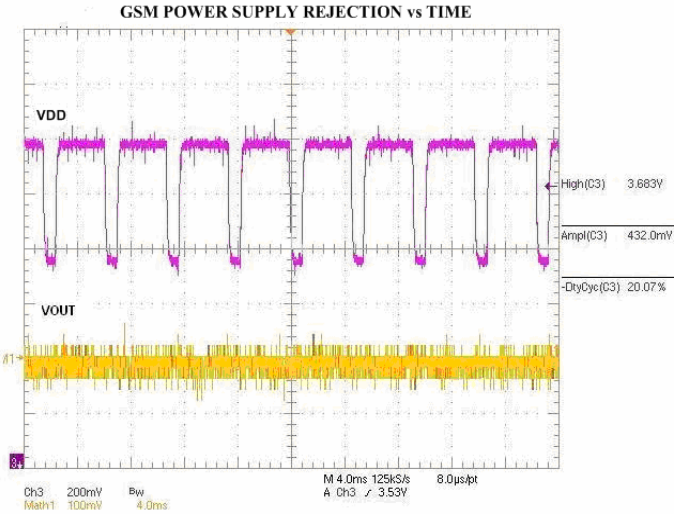

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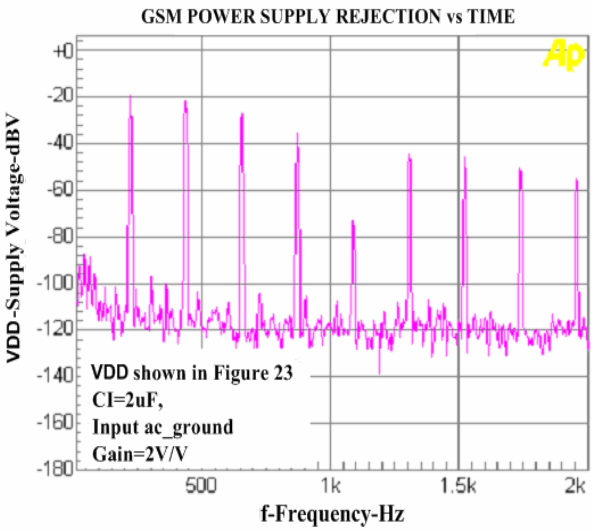

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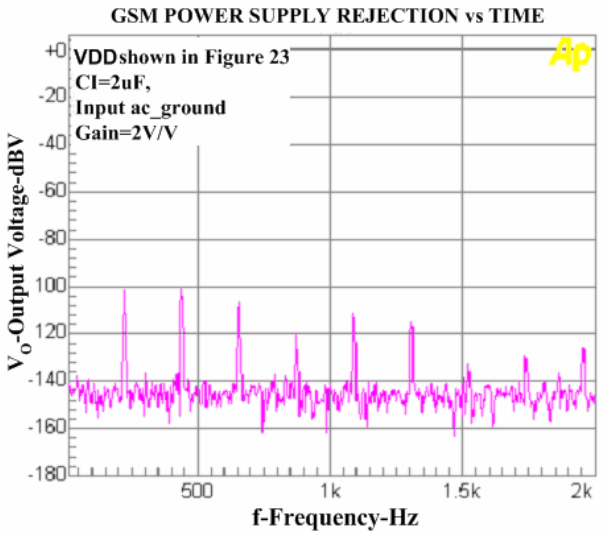

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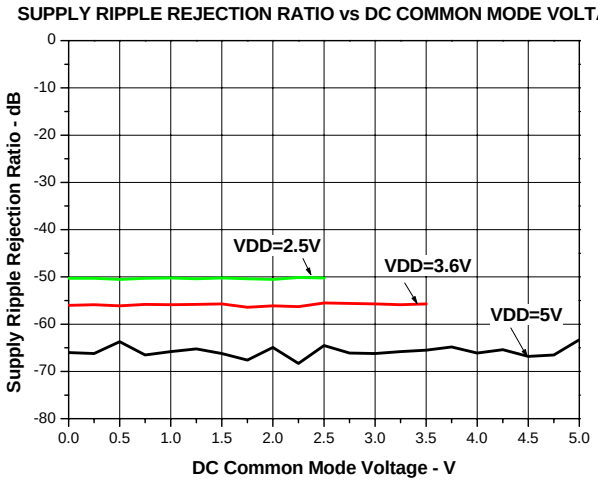

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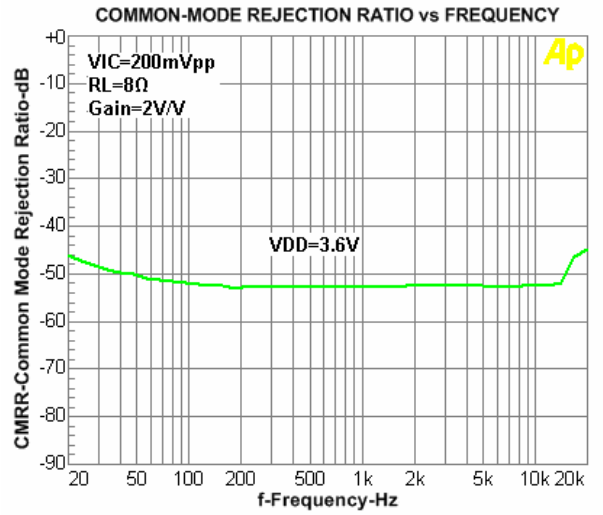

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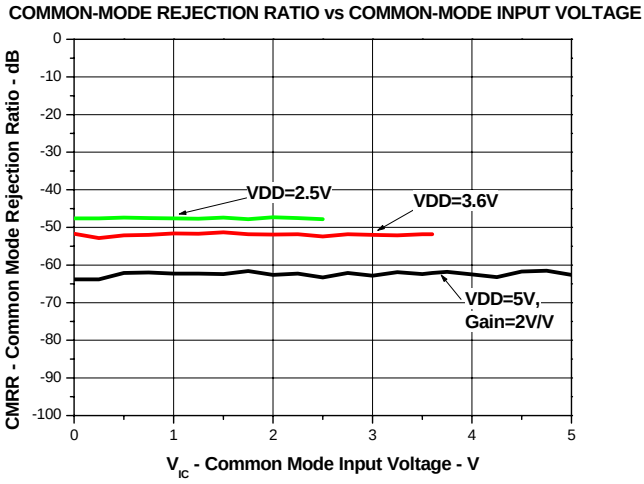

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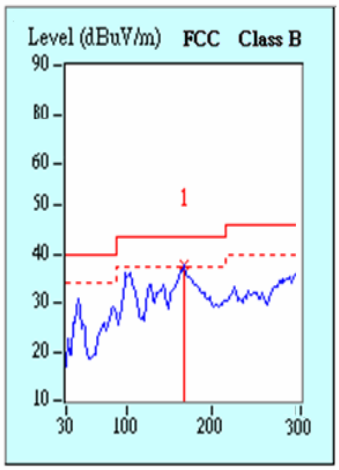


Figure29. EMI Test and FCC Limits

Application Information

Fully Differential Amplifier

The EUA2011 is a fully differential amplifier that features differential inputs and outputs. The EUA2011 also includes a common mode feedback loop that controls the output bias value to average it at $V_{CC}/2$ for any DC common mode input voltage. This allows the device to always have a maximum output voltage swing, and by consequence, maximize the output power. Moreover, as the load is connected differentially, compared to a single-ended topology, the output is four times higher for the same power supply voltage. The fully differential EUA2011 can still be used with a single-ended input; however, the EUA2011 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Advantages of Fully Differential Amplifiers

The advantages of a full-differential amplifier are:

- Very high PSRR (Power Supply Rejection Ratio).
- High common mode noise rejection.
- Virtually zero pop without additional circuitry, giving an faster start-up time compared to conventional single-ended input amplifiers.
- No input coupling capacitors required thanks to common mode feedback loop.
- Midsupply bypass capacitor not required.

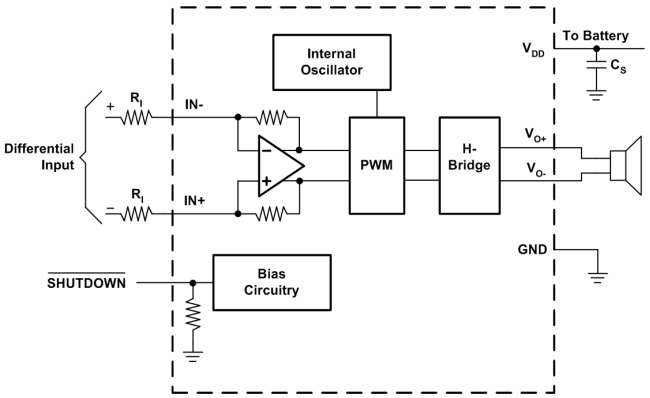


Figure 30. Differential Input Configuration

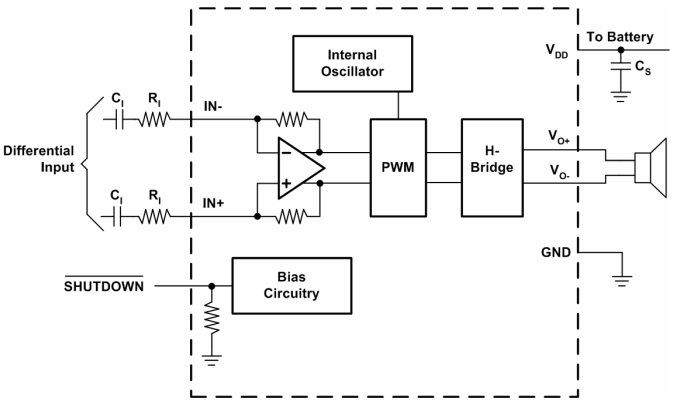


Figure 31. Differential Input Configuration and Input Capacitors

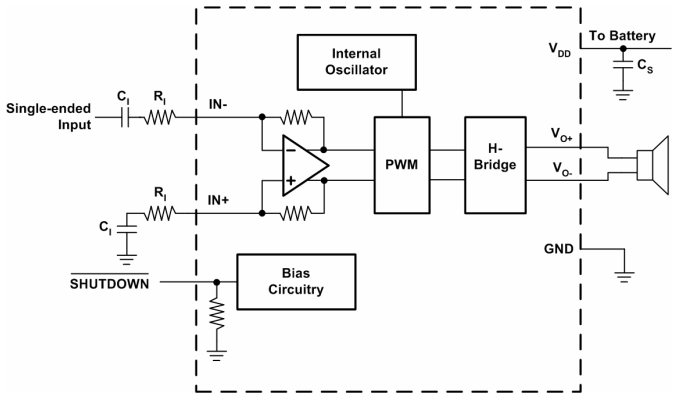


Figure 32. Single-Ended Input Configuration

Gain Selection

The input resistors (R_I) set the gain of the amplifier according to equation (1).

$$\text{Gain} = \frac{2 \times 150\text{k}\Omega}{R_I} \left(\frac{V}{V}\right) \quad \text{----------(1)}$$

Resistor matching is very important for CMRR, PSRR, and harmonic distortion. It is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Keeping the input trace as short as possible to limit noise injection on the high-impedance nodes.

For optimal performance the gain should be set to 2 V/V or lower. Lower gain allows the EUA2011 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

Power Supply Decoupling Capacitor (C_S)

The EUA2011 is a high-performance CMOS class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the EUA2011 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10μF or greater capacitor placed near the audio power amplifier would also help.

Input Capacitors (C_I)

The EUA2011 does not require input coupling capacitors if the input signal is biased from 0.5V to V_{DD} − 0.8V. Input capacitors are required if the input signal is not biased within the recommended common−mode input range, if a high pass filtering is needed (shown in Figure 31), or if using a single-ended source (shown in Figure 32).

The input capacitors and input resistors form a high-pass filter with the corner frequency, fc, determined in equation (2).

$$f_c = \frac{1}{(2\pi R_I C_I)} \quad \text{----------(2)}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.

Equation (3) is reconfigured to solve for the input coupling capacitance.

$$C_I = \frac{1}{(2\pi R_I f_c)} \quad \text{----------(3)}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

Single-Ended Input Depop Function

In single-ended input application, there is an inherently voltage difference in input pairs when shutdown is released. In order to eliminate pop noise, the pop cancellation circuit need to charge the input capacitor C_I until fully-differential inputs are balanced and output power to load gradually.

The RC time constant should within the de-pop delay, if 150kΩ R_I is chosen, the recommended C_I should small than 10nF for a good pop immunity.

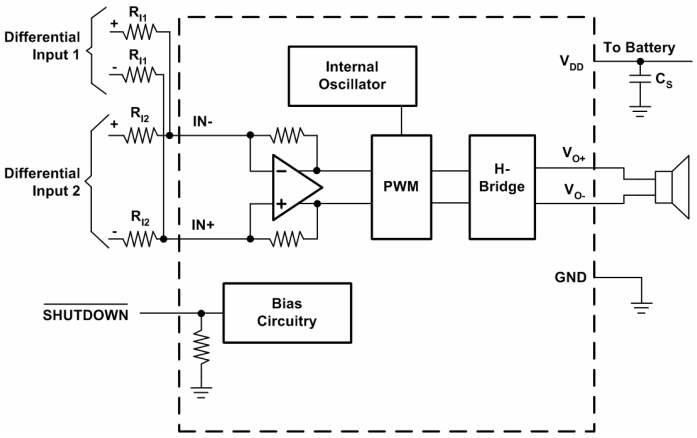


Figure 33. Dual Differential Input Configuration

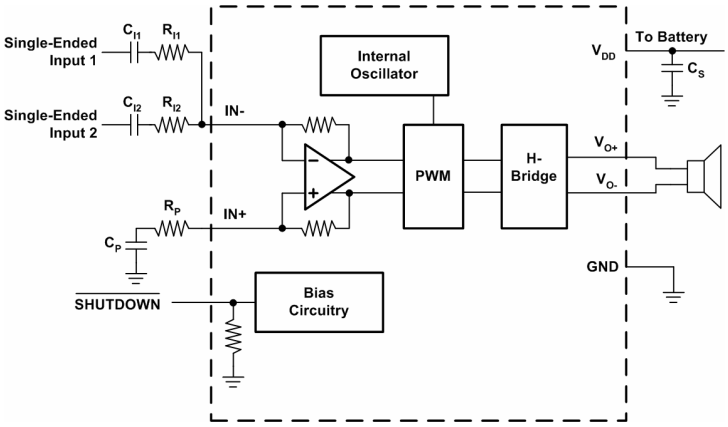


Figure 34. Dual Single-Ended Input Configuration

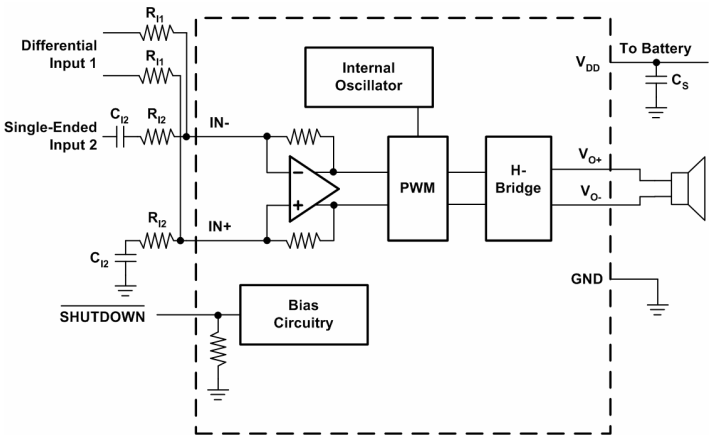


Figure 35. Dual Input with a Differential Input and Single-Ended Input

Summing Input Signals

The EUA2011 can be used to amplify more than one audio source. Figure 33 shows a dual differential input configuration. The gain for each input can be independently set for maximum design flexibility using the R_I resistors for each input and Equation (1).Input capacitors can be used with one or more sources as well to have different frequency responses depending on the source or if a DC voltage needs to be blocked from a source.

When using more than one single-ended source as shown in Figure 34, the impedance seen from each input terminal should be equal. To find the correct values for C_P and R_P connected to the IN+ input pin the equivalent impedance of all the single-ended sources are calculated. Equations (4) and (5) below are for any number of single-ended sources.

$$C_P = C_{i1} + C_{i2} \quad (F) \quad \text{----------(4)}$$

$$R_P = 1/\left(1/R_{i1} + 1/R_{i2}\right) \ (\Omega) \quad \text{----------(5)}$$

The EUA2011 may also use a combination of single-ended and differential sources. A typical application with one single-ended source and one differential source is shown in Figure 35.

PCB Layout

As output power increases, interconnect resistance (PCB traces and wires) between the amplifier, load and power supply create a voltage drop. The voltage loss on the traces between the EUA2011 and the load results is lower output power and decreased efficiency. Higher trace resistance between the supply and the EUA2011 has the same effect as a poorly regulated supply, increase ripple on the supply line also reducing the peak output power. The effects of residual trace resistance increases as output current increases due to higher output power, decreased load impedance or both. To maintain the highest output voltage swing and corresponding peak output power, the PCB traces that connect the output pins to the load and the supply pins to the power supply should be as wide as possible to minimize trace resistance.

The use of power and ground planes will give the best THD+N performance. While reducing trace resistance, the use of power planes also creates parasite capacitors that help to filter the power supply line.

The inductive nature of the transducer load can also result in overshoot on one or both edges, clamped by the parasitic diodes to GND and V_{DD} in each case. From an EMI stand- point, this is an aggressive waveform that can radiate or conduct to other components in the system and cause interference. It is essential to keep the power and output traces short and well shielded if possible. Use of ground planes, beads, and micro-strip layout techniques are all useful in preventing unwanted interference.

As the distance from the EUA2011 and the speaker increase, the amount of EMI radiation will increase since the output wires or traces acting as antenna become more efficient with length. What is acceptable EMI is highly application specific.

Ferrite bead placed close to the EUA2011 may be needed to reduce EMI radiation. Select a ferrite bead with the high impedance around 100MHz and a very low DCR value in the audio frequency range is the best choice. The MPZ1608S221A1 from TDK is a good choice.

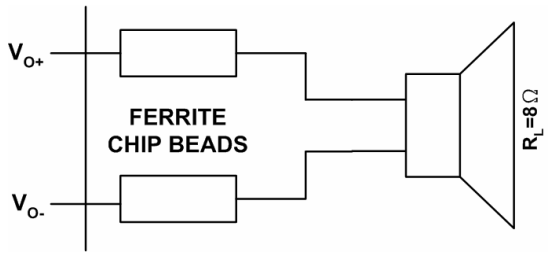
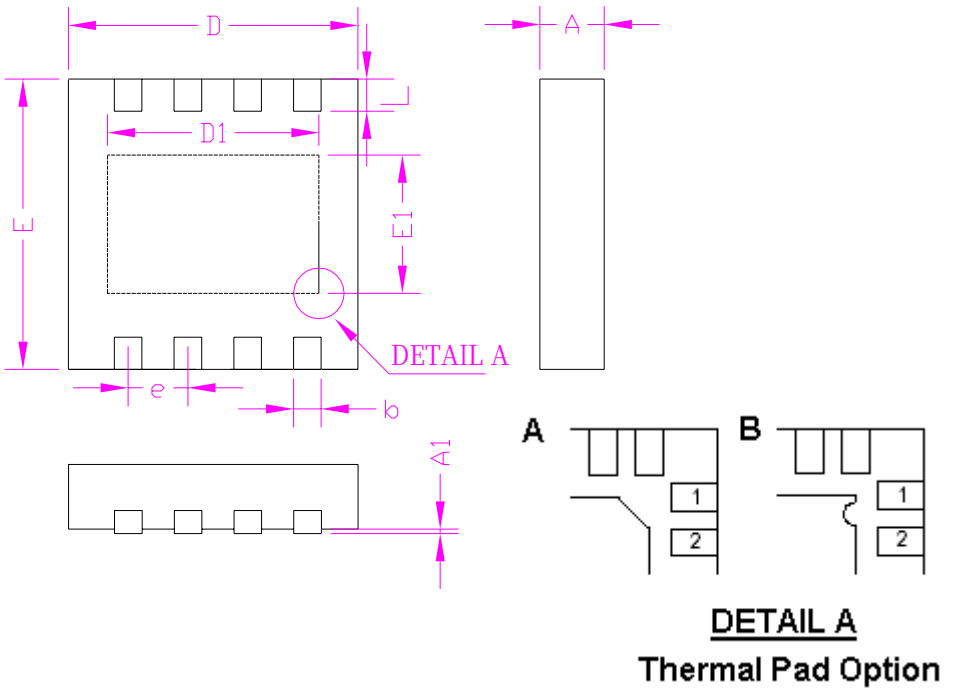


Figure 36. Optional EMI Ferrite Bead Filter

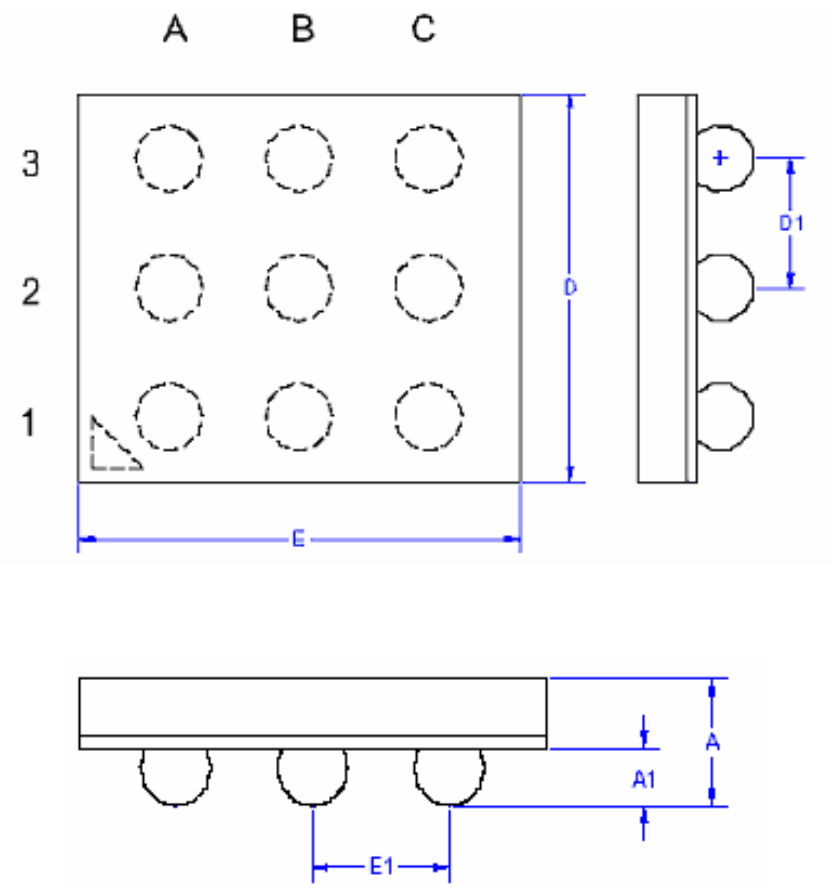
Packaging Information

TDFN-8



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.20	0.40	0.008	0.016
D	2.90	3.10	0.114	0.122
D1	2.30		0.090	
E	2.90	3.10	0.114	0.122
E1	1.50		0.059	
e	0.65		0.026	
L	0.25	0.45	0.010	0.018

WCSP-9



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	0.675	-	0.027
A1	0.15	0.35	0.006	0.014
D	1.45	1.55	0.057	0.061
D1	0.50		0.020	
E	1.45	1.55	0.057	0.061
E1	0.50		0.020	