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EUTECH
MICROELECTRONICS

10-W Stereo Class-D Audio Power Amplifier

DESCRIPTION

The EUA2101A is a high efficiency, 2 channel bridged-tied load (BTL), class-D audio power amplifier. Operating from a 12V power supply, EUA2101A is capable of delivering 10W/ channel of continuous output power to a 8Ω load with 10% THD+N. The EUA2101A features a differential input architecture offering improved noise immunity over a single-ended (SE) input amplifier. Amplifier gain is internally configured and can be selected to 20, 26, 32 or 36dB utilizing the Go and G1 gain select pins.

The EUA2101A also features short-circuit and thermal protection preventing the device from being damaged during a fault condition. The EUA2101A is available in thermally efficient 48-pin TQFP package.

FEATURES

- Wide Supply Voltage: 8V to 15V
- Unique Modulation Scheme Reduces EMI Emission
- 10-W/ch into an 8-Ω Load From a 12-V Supply
- 15-W/ch into an 4-Ω Load From a 12-V Supply
- 90% Efficient Class-D Operation Eliminates Need for Heat Sinks
- Four Selectable, Gain Settings
- Differential Inputs
- Thermal and Short-Circuit Protection
- Clock Output for Synchronization With Multiple Class-D Devices
- 7mm×7mm, 48-pin TQFP Package
- RoHS compliant and 100% lead(Pb)-free

APPLICATIONS

- Televisions

Typical Application Circuit

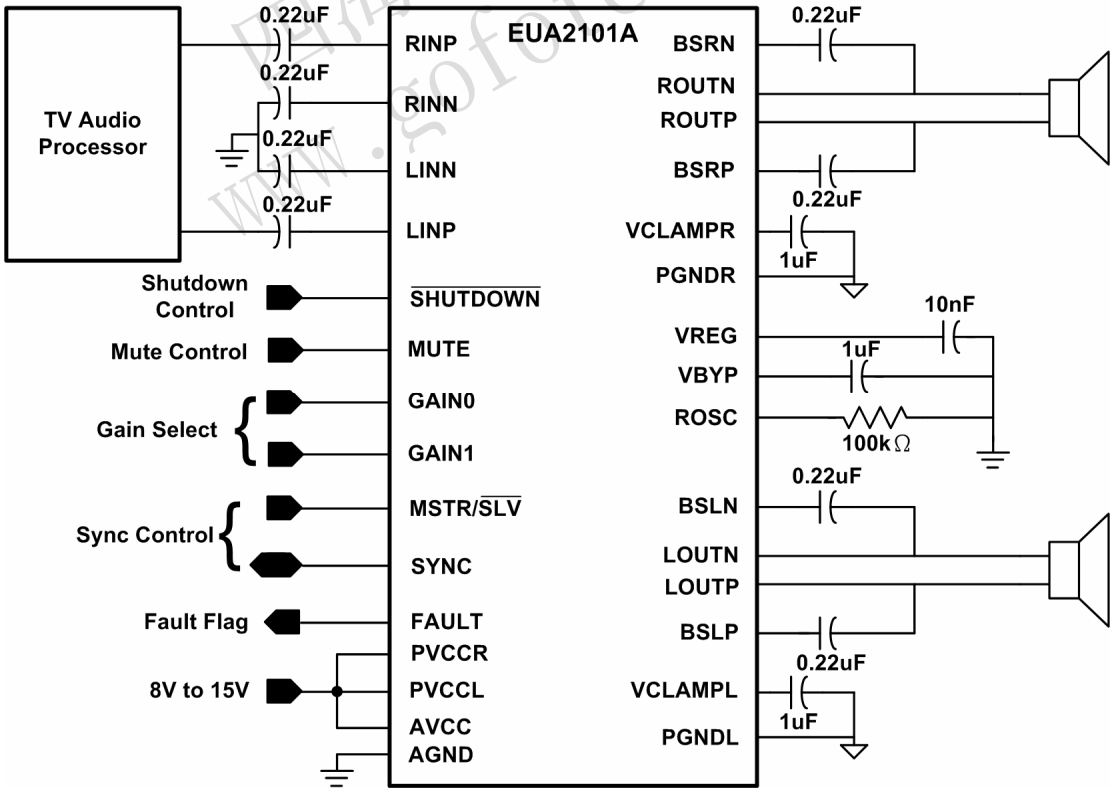

Figure1.

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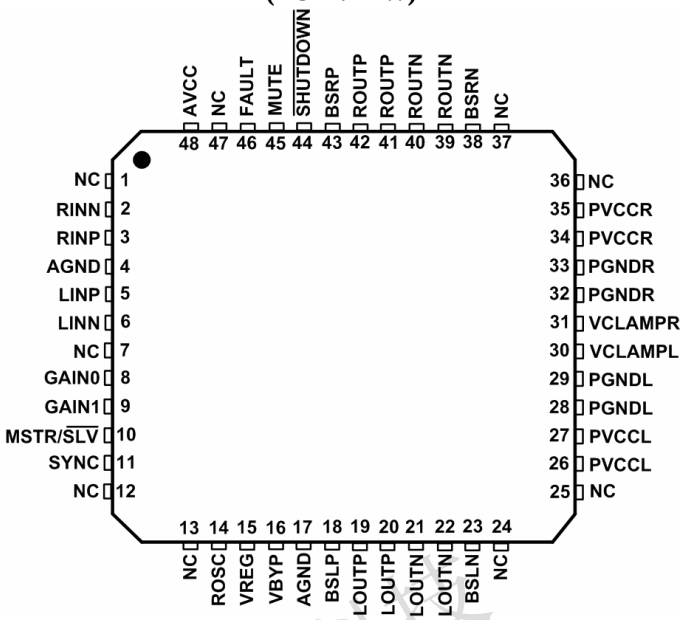
Pin Configurations

Package Type	Pin Configurations
TQFP-48	(TOP VIEW) 

Pin Description

PIN	TQFP-48	I/O	DESCRIPTION
$\overline{\text{SHUTDOWN}}$	44	I	Shutdown signal for IC (LOW = disabled, HIGH = operational). TTL logic levels with compliance to AVCC.
RINN	2	I	Negative audio input for right channel. Biased at VREG/2.
RINP	3	I	Positive audio input for right channel. Biased at VREG/2.
LINN	6	I	Negative audio input for left channel. Biased at VREG/2.
LINP	5	I	Positive audio input for left channel. Biased at VREG/2.
GAIN0	8	I	Gain select least significant bit. TTL logic levels with compliance to VREG.
GAIN1	9	I	Gain select most significant bit. TTL logic levels with compliance to VREG.
MUTE	45	I	Mute signal for quick disable/enable of outputs (HIGH = outputs high-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.
FAULT	46	O	TTL compatible output. HIGH = short-circuit fault. LOW = no fault. Only reports short-circuit faults. Thermal faults are not reported on this terminal.
BSLP	18	I/O	Bootstrap I/O for left channel, positive high-side FET.
PVCCL	26,27		Power supply for left channel H-bridge, not internally connected to PVCCR or AVCC.
LOUTP	19,20	O	Class-D 1/2-H-bridge positive output for left channel.
PGNDL	28,29		Power ground for left channel H-bridge.
LOUTN	21,22	O	Class-D 1/2-H-bridge negative output for left channel.
BSLN	23	I/O	Bootstrap I/O for left channel, negative high-side FET.
VCLAMPL	30		Internally generated voltage supply for left channel bootstrap capacitor.
VCLAMPR	31		Internally generated voltage supply for right channel bootstrap capacitor.

Pin Description (Continued)

PIN	TQFP-48	I/O	DESCRIPTION
BSRN	38	I/O	Bootstrap I/O for right channel, negative high-side FET.
ROUTN	39,40	O	Class-D 1/2-H-bridge negative output for right channel.
PGNDR	32,33		Power ground for right channel H-bridge.
ROUTP	41,42	O	Class-D 1/2-H-bridge positive output for right channel.
PVCCR	34,35		Power supply for right channel H-bridge, not connected to PVCCL or AVCC.
BSRP	43	I/O	Bootstrap I/O for right channel, positive high-side FET.
AGND	4,17		Analog ground for digital/analog cells in core.
ROSC	14	I/O	I/O for current setting resistor of ramp generator.
MSTR/$\overline{\text{SLV}}$	10	I	Master/Slave select for determining direction of SYNC terminal. HIGH=Master mode, SYNC terminal is an output; LOW = slave mode, SYNC terminal accepts a clock input. TTL logic levels with compliance to VREG.
SYNC	11	I/O	Clock input/output for synchronizing multiple class-D devices. Direction determined by MSTR/$\overline{\text{SLV}}$ terminal. Input signal not to exceed VREG.
VBYP	16	O	Reference for preamplifier. Nominally equal to 1.39V. Also controls start-up time via external capacitor sizing.
VREG	15	O	4-V regulated output for use by internal cells, GAINx, MUTE, and MSTR/$\overline{\text{SLV}}$ pins only. Not specified for driving other external circuitry.
AVCC	48		High-voltage analog power supply. Not internally connected to PVCCR or PVCCL.
NC	1,7,12, 13,24,25, 36,37,47		Not internally connected.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUA2101ATIR1	TQFP-48	xxxxx EUA2101A	-40 °C to +85°C

EUA2101A □ □ □ □

- Lead Free Code
  1: Lead Free 0: Lead
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  T:TQFP

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Absolute Maximum Ratings

- Supply Voltage, AVCC,PVCC ---------- -0.3 V to 18V
- Input Voltage, $\overline{\text{SHUTDOWN}}$,MUTE---------- -0.3 V to V_{CC} +0.3V
- Input Voltage,GAIN0,GAIN1,RINN,RINP,LINN,LINP, MSTR/$\overline{\text{SLV}}$,SYNC------- -0.3 V to VREG +0.5V
- Continuous Total Power Dissipation---------- See Dissipation Rating Table
- Free-air Temperature Range, T_A ---------- -40°C to +85°C
- Junction Temperature Range, T_J ---------- -40°C to +150°C
- Storage Temperature Rang, T_{stg} ---------- -65°C to +150°C
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ---------- 260°C
- Load Resistance, R_{LOAD} ---------- 3.2Ω Minimum
- ESD Susceptibility (HBM) ---------- >2kV

Recommended Operating Conditions

		Min	Max	Unit
Supply voltage, V_{CC}	PVCC,AVCC	8	15	V
High-level input voltage, V_{IH}	$\overline{\text{SHUTDOWN}}$,MUTE,GAIN0,GAIN1, MSTR/$\overline{\text{SLV}}$,SYNC	2		V
Low-level input voltage, V_{IL}	$\overline{\text{SHUTDOWN}}$,MUTE,GAIN0,GAIN1, MSTR/$\overline{\text{SLV}}$,SYNC		0.8	V
High-level input current, I_{IH}	$\overline{\text{SHUTDOWN}}$,V_I=V_{CC},V_{CC}=12V		125	μA
	MUTE,V_I=V_{CC}, V_{CC}=12V		75	
	GAIN0,GAIN1, MSTR/$\overline{\text{SLV}}$,SYNC,V_I=VREG, V_{CC}=12V		2	
Low-level input current, I_{IL}	$\overline{\text{SHUTDOWN}}$,V_I=0V,V_{CC}=12V		2	μA
	SYNC,MUTE,GAIN0,GAIN1,MSTR/$\overline{\text{SLV}}$,V_I=0V, V_{CC}=12V		1	
High-level output voltage, V_{OH}	FAULT, I_{OH}=1mA	VREG-0.6		V
Low-level output voltage, V_{OL}	FAULT, I_{OL}= -1mA		AGND+0.4	V
Oscillator frequency, f_{OSC}	R_{OSC} Resistor=100 kΩ	200	300	kHz
Operating free-air temperature, T_A		-40	85	°C

DC Characteristics T_A = +25°C ,V_{CC}=12V, R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2101A			Unit
			Min	Typ	Max.	
$\lvert V_{OS}\rvert$	Class-D output offset voltage (measured differentially)	V_I= 0 V, Gain = 36 dB		5	50	mV
	Bypass reference for input amplifier	VBYP, no load	1.30	1.40	1.50	V
	4-V internal supply voltage	VREG, no load, V_{CC}= 10V to 15V	3.70	4	4.30	V
PSRR	DC Power supply rejection ratio	V_{CC} = 12 V to 15 V, inputs ac coupled to AGND, Gain = 32 dB		-60		dB

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DC Characteristics (Continued)

Symbol	Parameter	Conditions		EUA2101A Min	EUA2101A Typ	EUA2101A Max.	Unit
ICC	Quiescent supply current	$\overline{SHUTDOWN}$ =2V, MUTE=0V, no load, filter or snubber			22	28	mA
$ICC_{(SD)}$	Quiescent supply current in shutdown mode	$\overline{SHUTDOWN}$ =0.8V, no load			500	1000	μA
$ICC_{(MUTE)}$	Quiescent supply current in mute mode	MUTE=2V, no load			1.25	2	mA
r_{DS}(on)	Drain-source on-state resistance	V_{CC}=12V, I_O=500mA, T_J=25°C	High Side		200		mΩ
			Low Side		200		
			Total		400	800	
G	Gain	GAIN1=0.8V	GAIN0=0.8V	19	20	21	dB
			GAIN0=2V	25	26	27	
		GAIN1=2V	GAIN0=0.8V	31	32	33	dB
			GAIN0=2V	35	36	37	
t_{ON}	Turn-on time	$C_{(VBYP)}$=1μF, $\overline{SHUTDOWN}$ =2V			10		ms
t_{OFF}	Turn-off time	$C_{(VBYP)}$=1μF, $\overline{SHUTDOWN}$ =0.8V			20		ms

AC Characteristics T_A = +25°C ,V_{CC}=12V, R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2101A Min	EUA2101A Typ	EUA2101A Max.	Unit
K_{SVR}	Supply ripple rejection	200mV_{PP} ripple from 20 Hz-1 kHz, Gain= 20dB, Inputs ac-coupled to AGND		-58		dB
P_O	Continuous output power	THD+N=7%, f=1kHz		9.20		W
		THD+N=10%, f=1kHz		9.80		
		THD+N=7%, f=1kHz, R_L=4Ω		15.70		
		THD+N=10%, f=1kHz,R_L=4Ω (thermally limited)		16.60		
THD+N	Total harmonic distortion +noise	R_L=8Ω, f=1 kHz, P_O=5W (half-power)		0.07%		
		R_L=4Ω, f=1 kHz, P_O=8W (half-power)		0.096%		
Vn	Output integrated noise	20Hz to 22kHz, A-weighted filter, Gain=20dB		200		μV
				-74		dBV
	Crosstalk	P_O=1 W, Gain=20dB, f=1 kHz		-90		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N< 1%, f=1kHz,Gain=20dB, A-weighted		90		dB
	Thermal trip point			150		℃
	Thermal hysteresis			40		℃

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Block Diagram

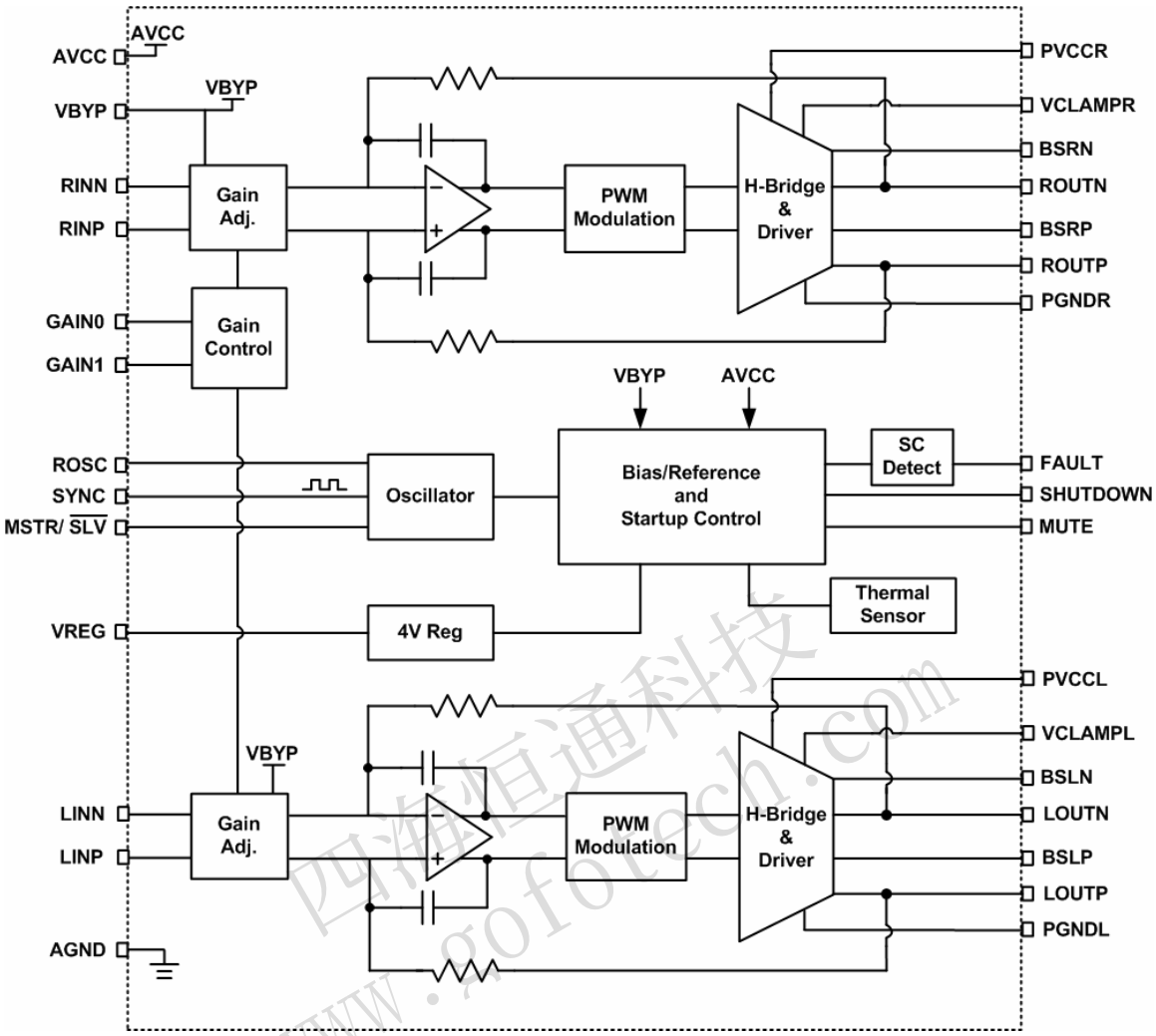
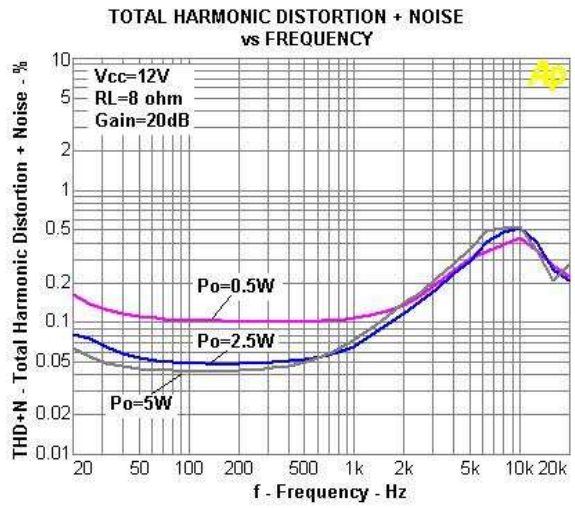


Figure2.

Typical Characteristics



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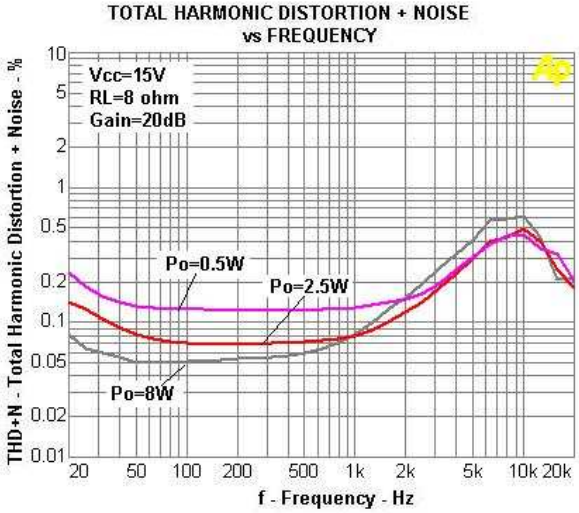

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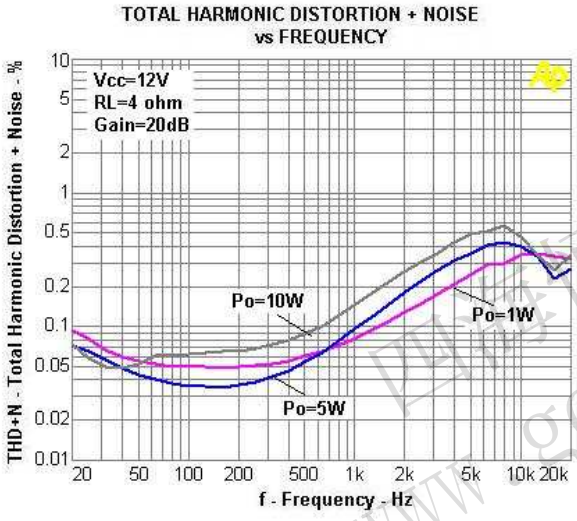

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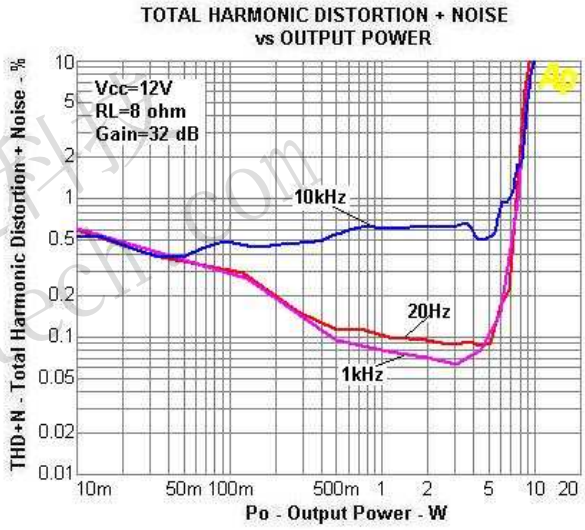

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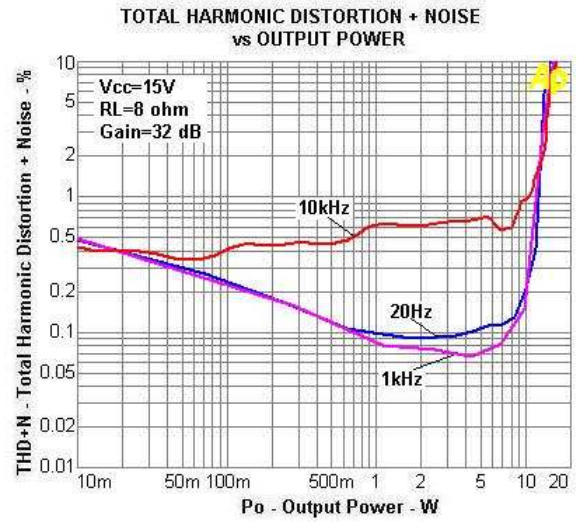

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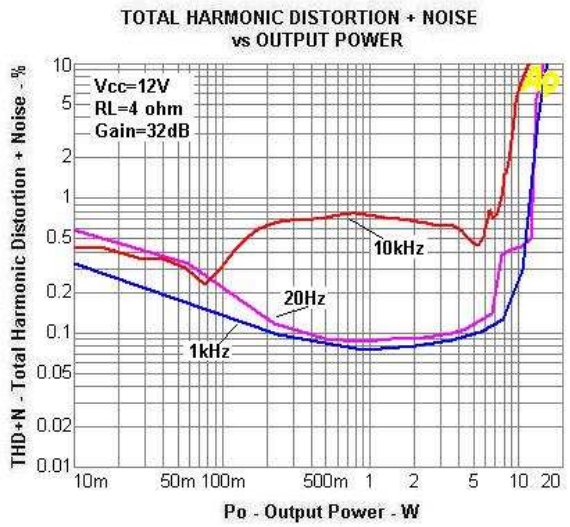

Figure8.

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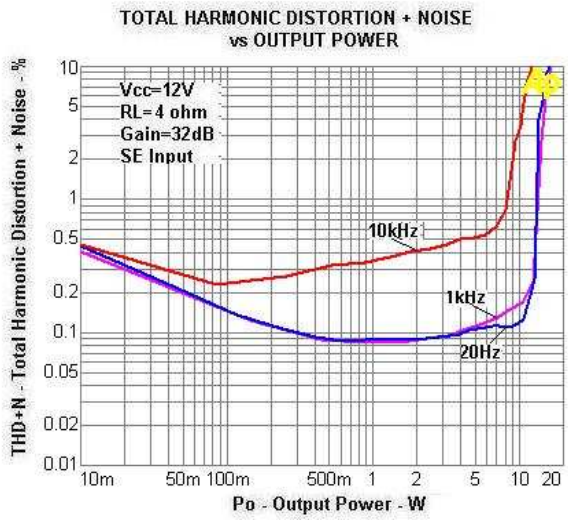

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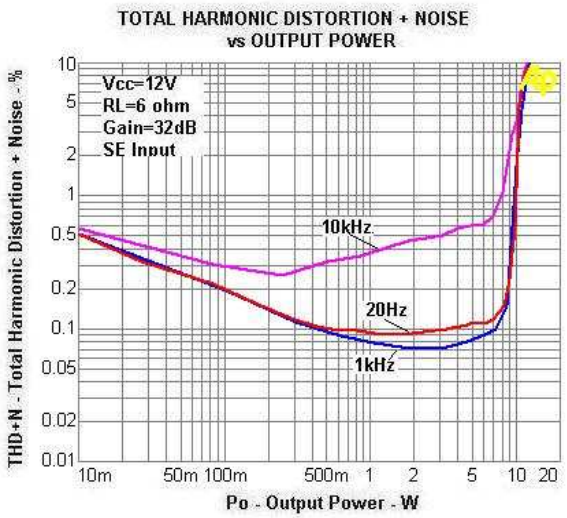

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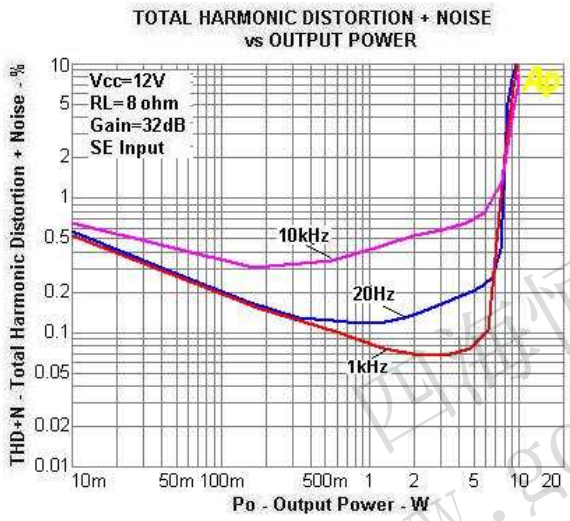

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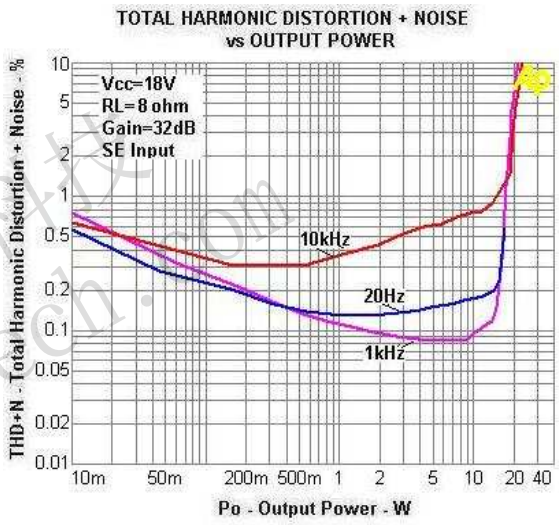

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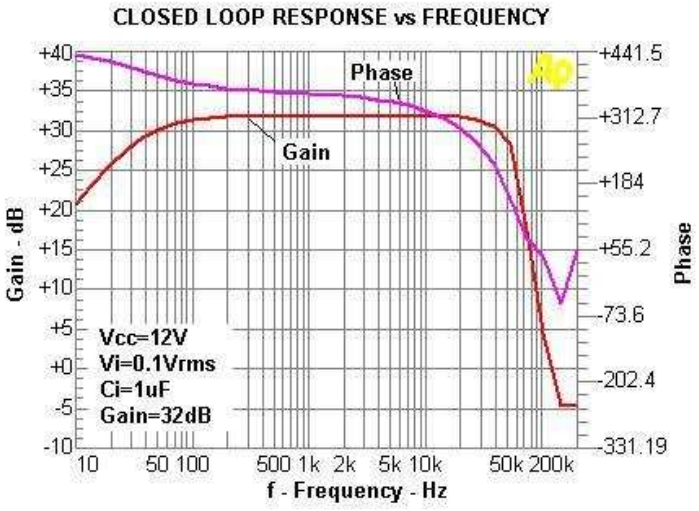

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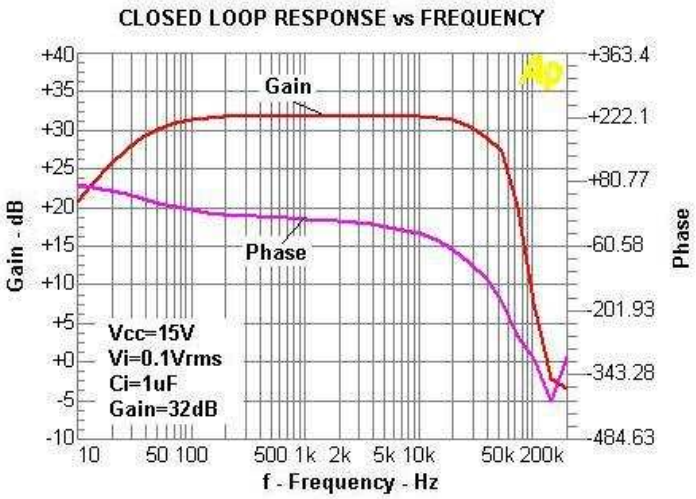

Figure14.

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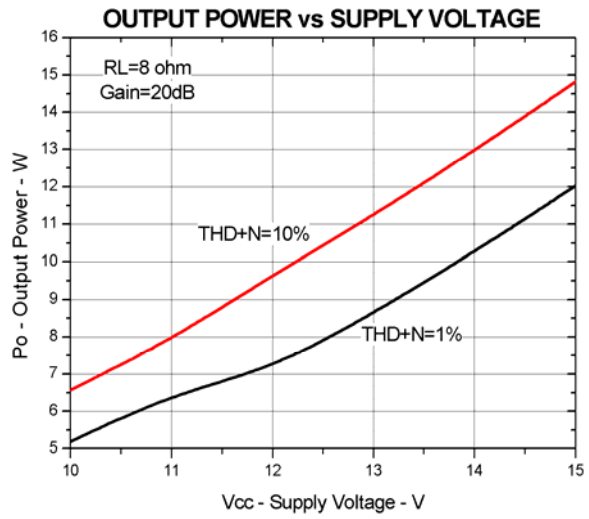

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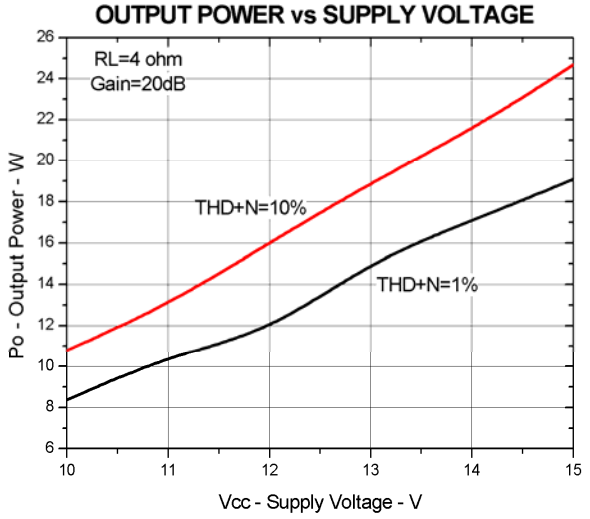

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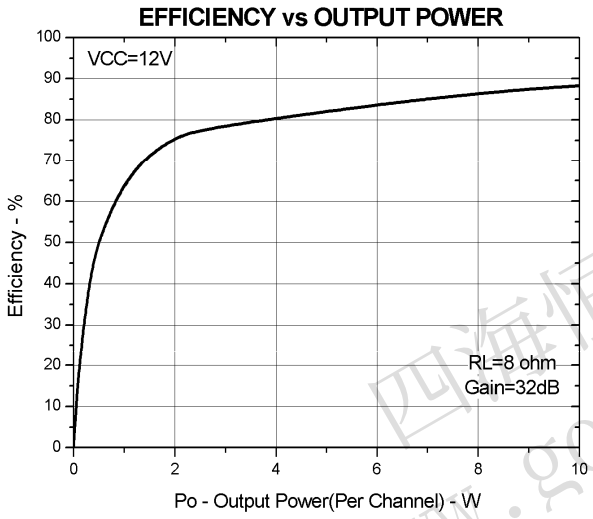

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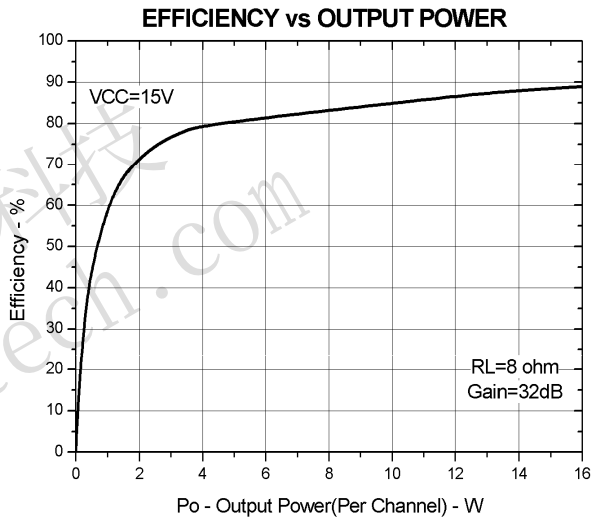

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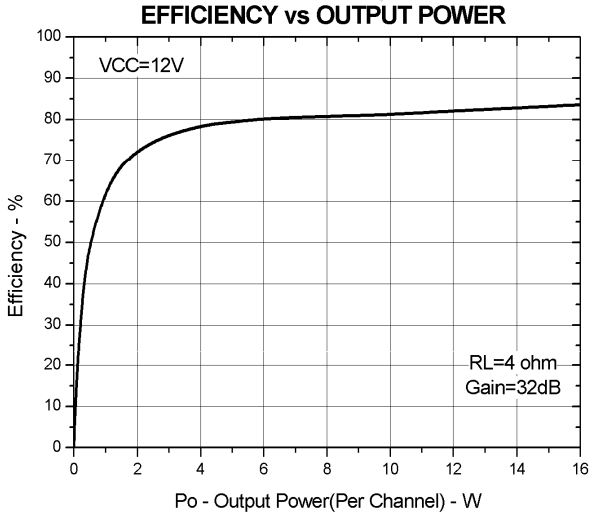

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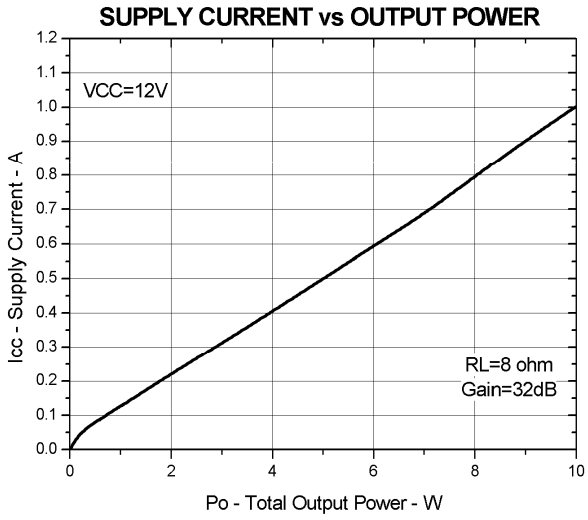

Figure20.

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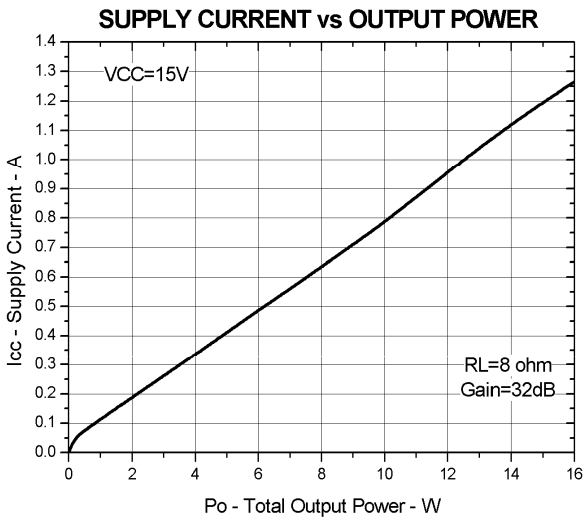

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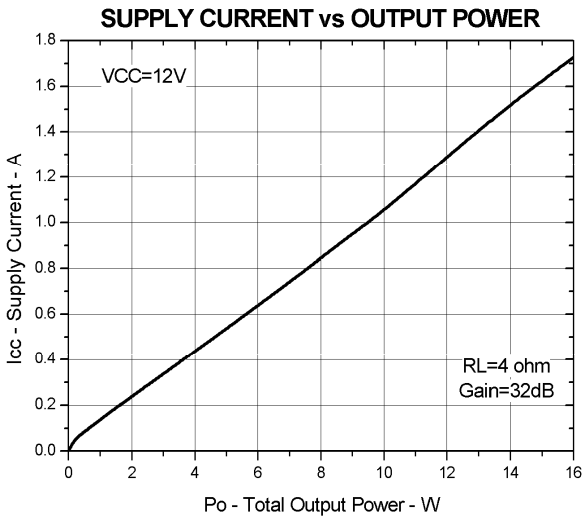

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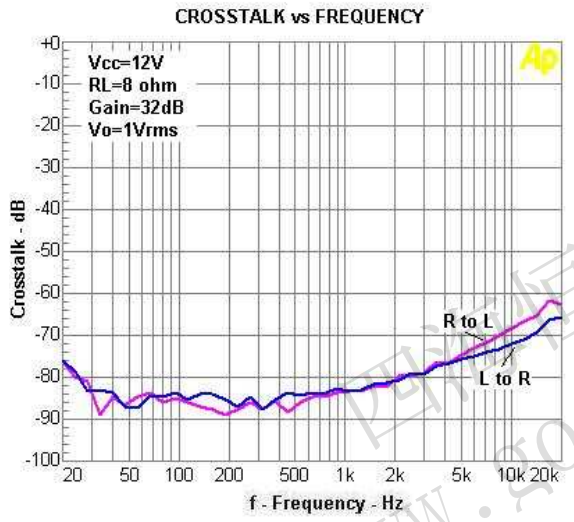

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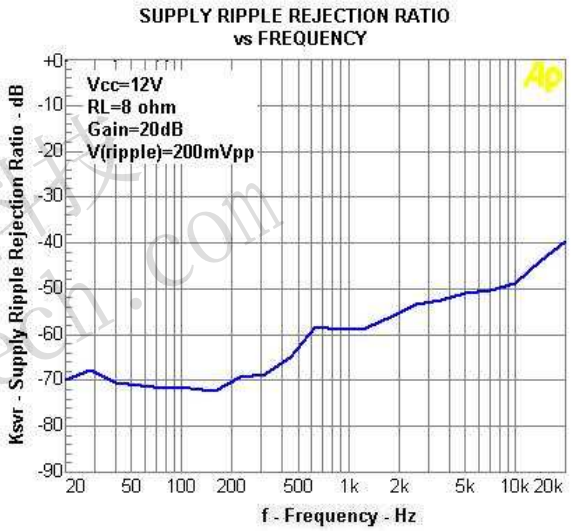

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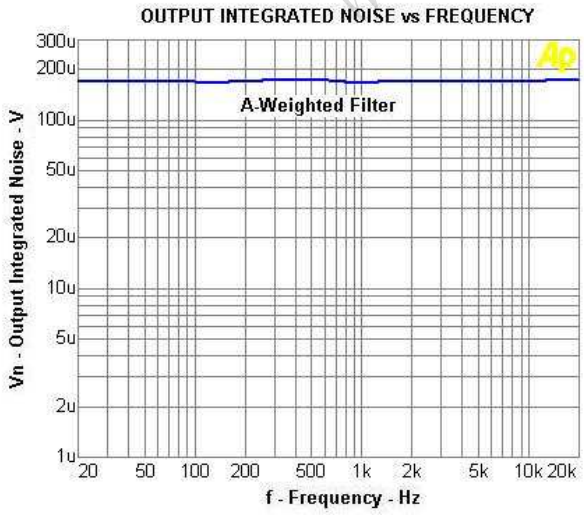

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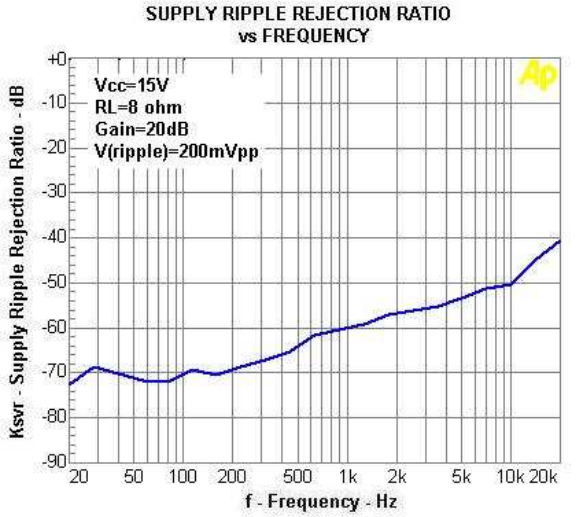

Figure26.

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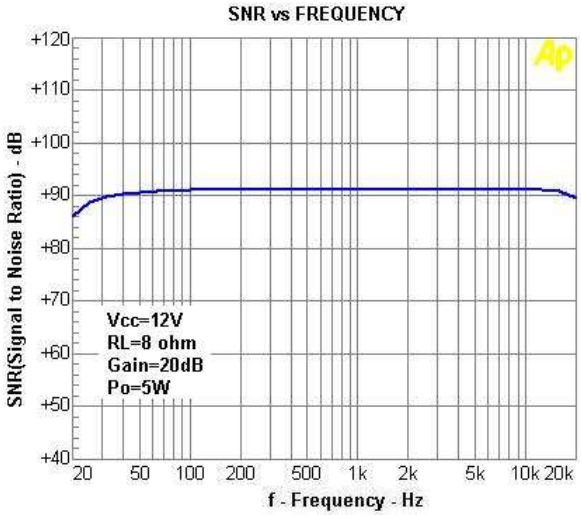
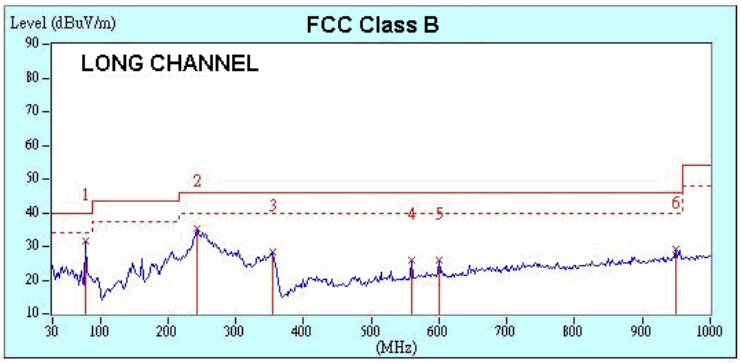


Figure27.



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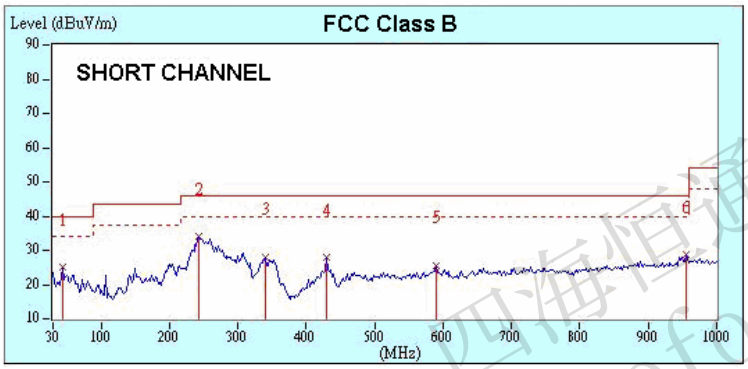

Figure29.

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Application Information

Differential Input

The differential input stage of the amplifier cancels any common-mode noise that appears on both input lines of the audio channel. To use the EUA2101A with a differential source, connect the positive signal of the audio source to the INP pin and the negative signal from the audio source to the INN pin (Figure 30).

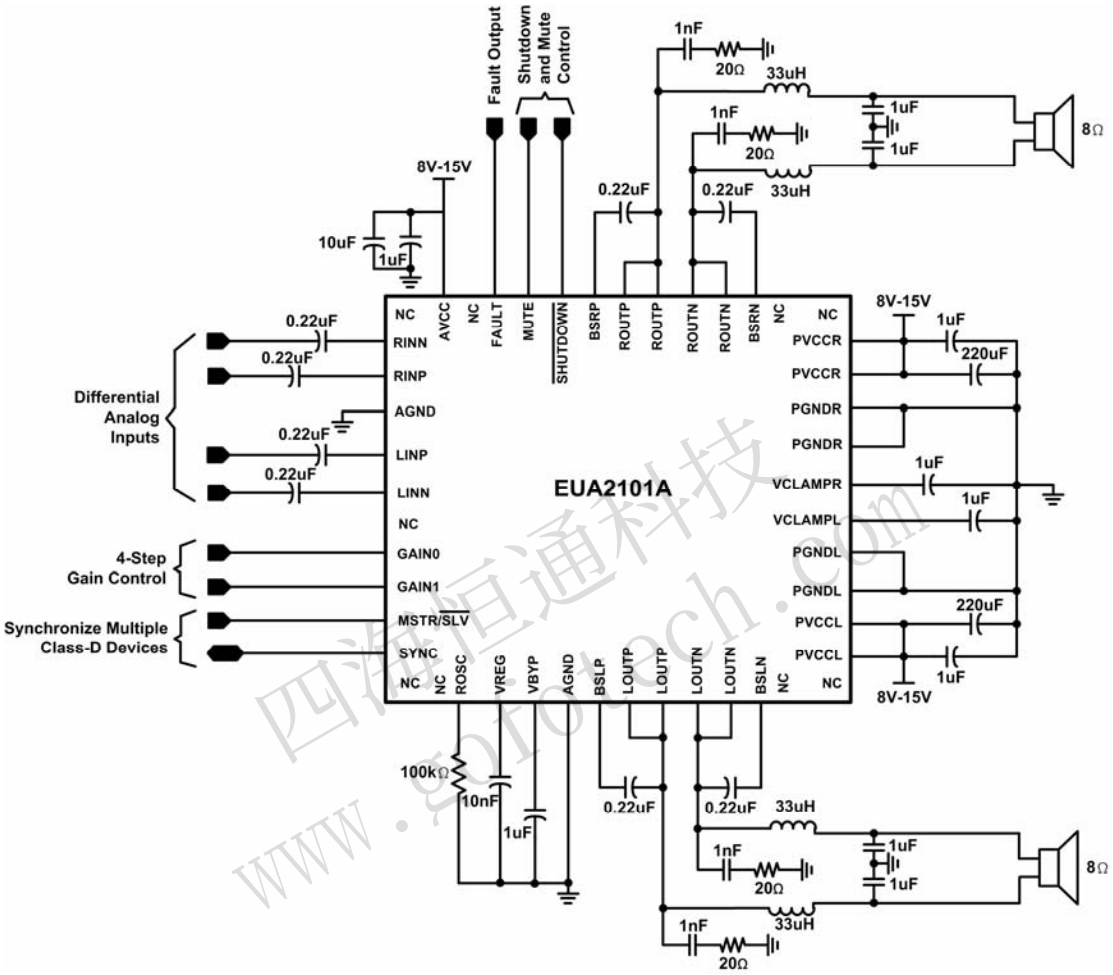

Figure 30. Differential Input

Application Information (continued)

Single-Ended Input

When using an audio source with a single-ended “out”, it is important to connect the RINN and LINN pins to the GND of the audio source with coupling capacitors. (Figure 31).

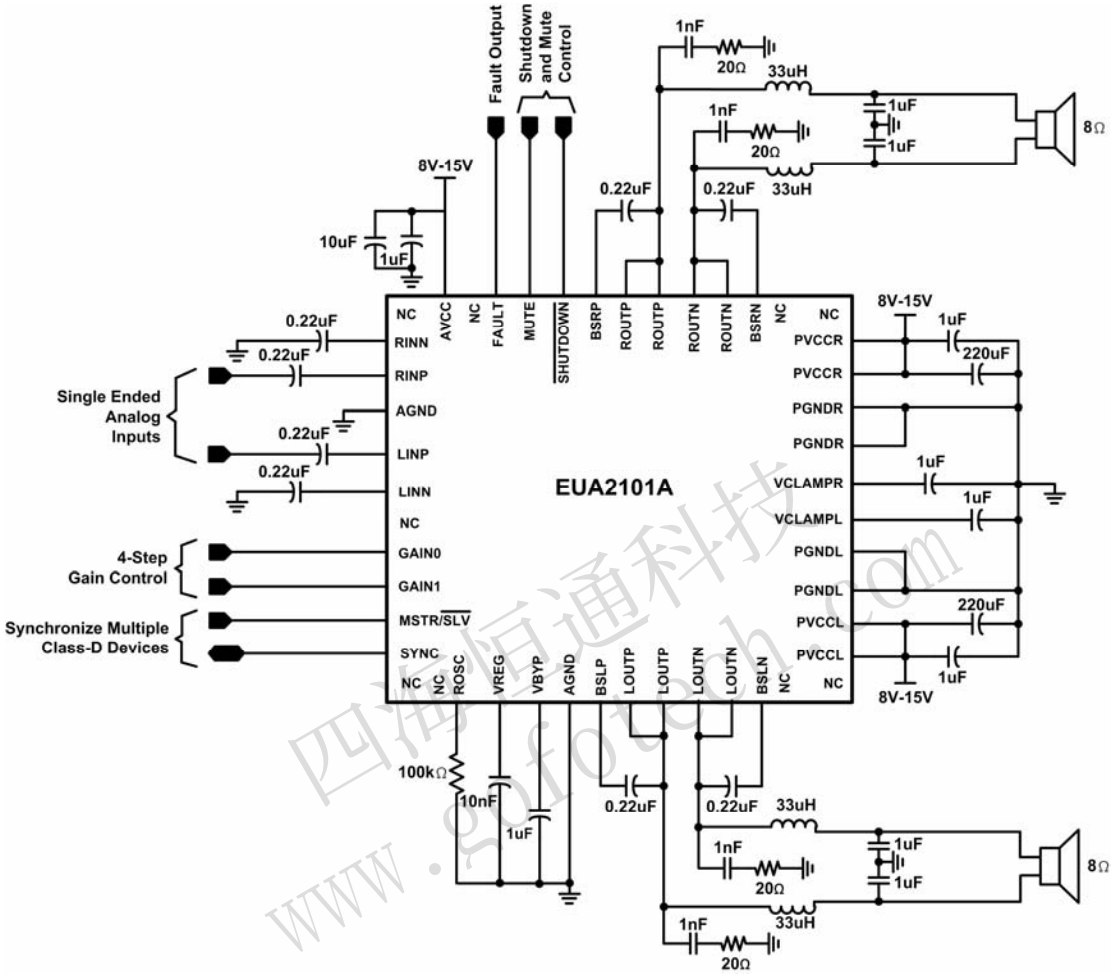

Figure 31. Single Ended Input

Gain Selection

The gain of the EUA2101A is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 1 are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network should be designed assuming an input impedance of 40 kΩ, which is the absolute minimum input impedance of the EUA2101A. At the lower gain settings, the input impedance could increase as high as 120 kΩ.

Table.1 Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	20	100
0	1	26	50
1	0	32	50
1	1	36	50

$\overline{\text{SHUTDOWN}}$ Operation

Connect $\overline{\text{SHUTDOWN}}$ to a logic high for normal operation. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{\text{SHUTDOWN}}$ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown or mute mode prior to removing the power supply voltage.

MUTE Operation

The MUTE pin only control the output state and does not shutdown the EUA2101A. A logic high on this terminal disables the outputs. A logic low on this pin enables the outputs. This terminal may be used as a quick disable/enable of outputs when changing channels on a television or transitioning between different audio sources. Do not leave MUTE terminal floating.

MSTR/$\overline{\text{SLV}}$ and SYNC Operation

The MSTR/$\overline{\text{SLV}}$ and SYNC pins can be used to synchronize the frequency of the class-D output switching. When MSTR/$\overline{\text{SLV}}$ is high, the output switching frequency is determined by the selection of the resistor connected to the ROSC pin. The SYNC becomes an output in this mode, and the frequency of this output is also determined by the selection of the ROSC resistor. This TTL compatible, push-pull output can be connected to another EUA2101A, configured in the slave mode. The output switching is synchronized to avoid any beat frequencies that could occur in the audio band when two class-D amplifiers in the same system are switching at slightly different frequencies.

When MSTR/$\overline{\text{SLV}}$ is low, the output switching frequency is determined by the incoming square wave on the SYNC input. The SYNC becomes an input in this mode and accepts a TTL compatible square wave from another EUA2101A configured in the master mode or from an external GPIO. If connecting to an external GPIO, recommended frequencies are 200kHz to 300kHz for proper device operation, and the maximum amplitude is 4V.

Internal Regulated 4V Supply (VREG)

The EUA2101A features an internal 4V regulator output (VREG), is the output of an internally, used for the oscillator, preamplifier, and gain control circuitry. It requires a 10nF capacitor, placed close to the pin, to keep the regulator stable.

This regulated voltage can also be used to control GAIN0, GAIN1, MSTR/$\overline{\text{SLV}}$, and MUTE, but should not be used to drive external circuitry.

Short-Circuit Protection and Automatic Recovery Feature

The EUA2101A has short-circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-VCC shorts. When a short circuit is detected on the outputs, the part immediately disables the output drive. This is a latched fault and must be reset by cycling the voltage on the $\overline{\text{SHUTDOWN}}$ pin or MUTE pin. This clears the short-circuit flag and allows for normal operation if the short was removed. If the short was not removed, the protection circuitry again activates.

Thermal Protection

Thermal protection on the EUA2101A prevents damage to the device when the internal die temperature exceeds 150°C. There is a 10°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 40°C. The device begins normal operation at this point with no external system interaction.

Input Resistance

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 50 kΩ ±20%, to the largest value, 100 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.

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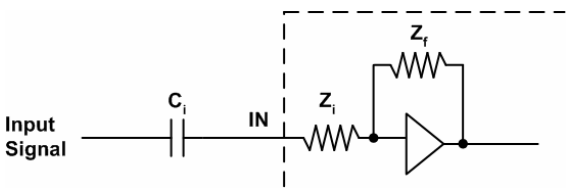
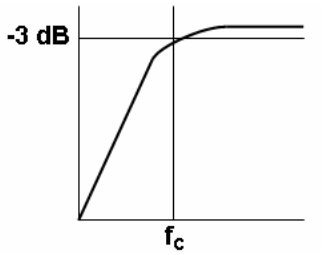


The -3dB frequency can be calculated using Equation 1. Use the Z_I values given in Table 1.

$$f = \frac{1}{2\pi Z_i C_i} \quad \text{---------- (1)}$$

Input Capacitor, C_I

In the typical application, an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 2.



$$f_c = \frac{1}{2\pi Z_i C_i} \quad \text{----------(2)}$$

The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_I is 50 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 2 is reconfigured as Equation 3.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad \text{----------(3)}$$

In this example, C_I is 0.16µF; so, one would likely choose a value of 0.22µF as this value is commonly used. If the gain is known and is constant, use Z_I from Table 1 to calculate C_I.

Power Supply Decoupling, C_S

The EUA2101A is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF to 1µF placed as close as possible to the device VCC lead works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220µF or greater placed near the audio power amplifier is recommended. The 220µF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220µF or larger capacitor should be placed on each PVCC terminal. A 10µF capacitor on the AVCC terminal is adequate.

BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors, that require bootstrap capacitors for the high side of each output to turn on correctly. A 220nF~1uF ceramic capacitor, rated for at least 16V, must be connected from each output to its corresponding bootstrap input. (See application circuit diagram in Figure 26,27.)

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

VCLAMP Capacitors

The EUA2101A also features two regulators used for gate voltage clamping in order to ensure the maximum gate-to-source voltage for the NMOS output transistors is not exceeded. Two 1µF capacitors must be connected from VCLAMPL (pin 30) and VCLAMPR (pin 31) to ground and must be rated for at least 16V. The voltages at the VCLAMP terminals may vary with V_{CC} and may not be used for powering any other circuitry.

Output Pin Snubbers

1nF capacitors in series with 20Ω resistors form the outputs of the EUA2101A IC to ground are switching snubbers. These are illustrated in Figure 32.They linearize switching transitions and reduce overshoot and ringing. By doing so they improve THD+N and EMC. They increase quiescent current by 5 to 15mA depending on power supply voltage.

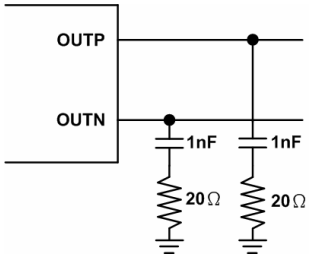


Figure32.

VBYP Capacitor

The internal bias generator (VBYP) nominally provides a 1.4V internal bias for the preamplifier stages. The external input capacitors and this internal reference allow the inputs to be biased within the optimal common-mode range of the input preamplifiers.

The selection of the capacitor value on the VBYP terminal is critical for achieving the best device performance. During power up or recovery from the shutdown state, the VBYP capacitor determines the rate at which the amplifier starts up. The charge rate of the capacitor is calculated using the standard charging formula for a capacitor, I = C x dV/dT. The charge current is nominally equal to 125µA and dV is equal to VBYP. For example, a 1µF capacitor on VBYP would take 10 ms to reach the value of VBYP and turn on outputs. The turn-on time will <30 ms for a 1µF capacitor on the VBYP terminal.

A secondary function of the VBYP capacitor is to filter high-frequency noise on the internal 1.4V bias generator. A value of at least 1µF is recommended for the VBYP capacitor. For the best power-up and shutdown pop performance, the VBYP capacitor should be greater than or equal to the input capacitors.

Using Low-ESR Capacitors

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance. For best performance over the extended temperature range, select X7R capacitors.

Output Filter

Most applications require a ferrite bead filter. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency (<1 MHz) EMI-sensitive circuits and/or there are long wires from the amplifier to the speaker.

When both an LC filter and a ferrite bead filter are used, the LC filter should be placed as close as possible to the IC followed by the ferrite bead filter.

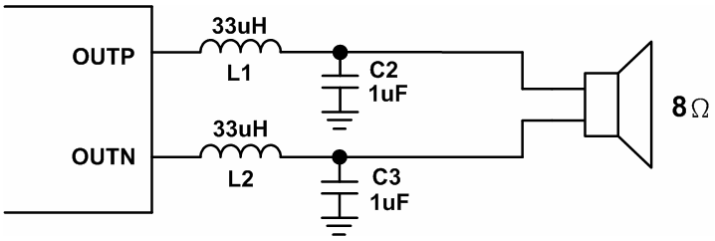


Figure33.

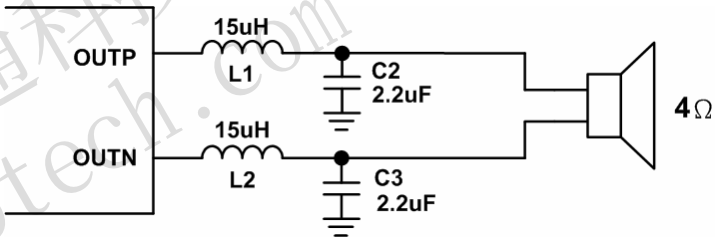


Figure34.

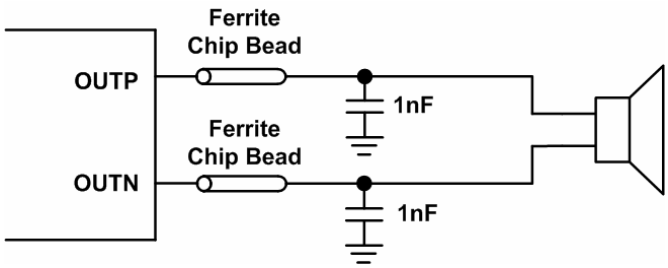


Figure35.

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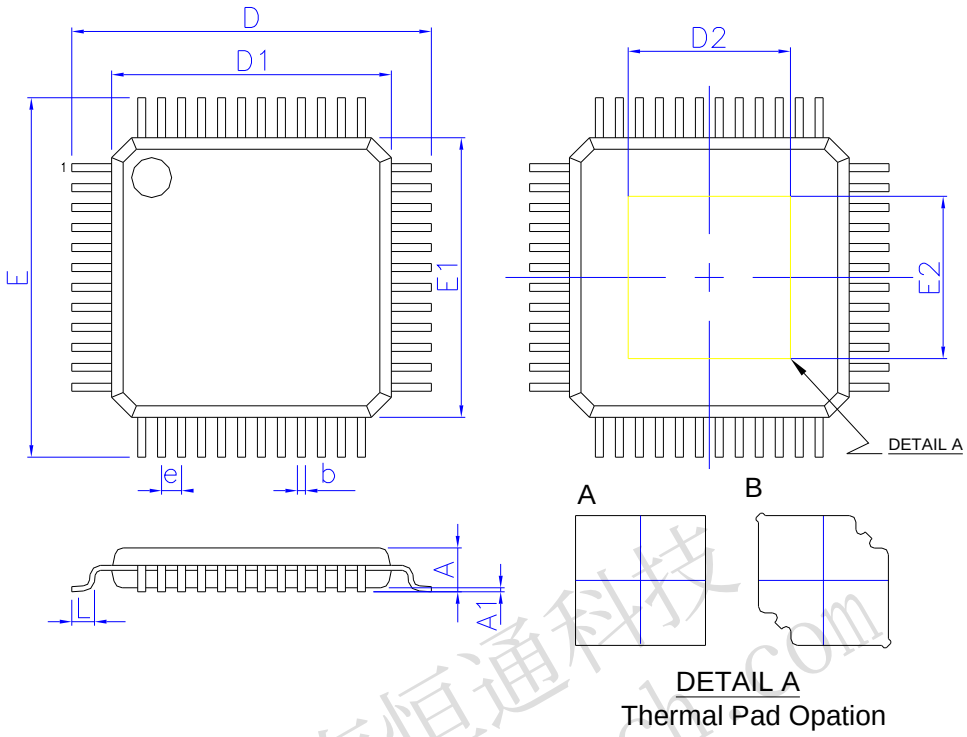
Package Information

TQFP-48



DETAIL A
Thermal Pad Opation

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SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.20	-	0.047
A1	0.05	0.15	0.002	0.006
b	0.17	0.27	0.007	0.011
D	8.80	9.20	0.346	0.362
D1	7.00		0.275	
D2	2.00	-	0.079	-
E	8.80	9.20	0.346	0.362
E1	7.00		0.275	
E2	2.00	-	0.079	-
e	0.50		0.020	
L	0.45	0.75	0.018	0.030