EUTECH
MICROELECTRONICS

# 6.5-W Mono Class-D Audio Power Amplifier

## DESCRIPTION

The EUA2107 is a high efficiency, mono bridged-tied load (BTL), class-D audio power amplifier. Operating from a 12V power supply, EUA2107 is capable of delivering 6.5W of continuous output power to a 8Ω load with 10% THD+N. The EUA2107 features a differential input architecture offering improved noise immunity over a single-ended (SE) input amplifier. Amplifier gain is internally configured and can be selected to 12, 18, 23.6 or 35.5dB utilizing the Go and G1 gain select pins.

The EUA2107 also features short-circuit and thermal protection preventing the device from being damaged during a fault condition. The EUA2107 is available in thermally efficient 24-pin TSSOP package and does not require an external heat sink.

## FEATURES

- Wide Supply Voltage: 8V to 24V
- Unique Modulation Scheme Reduces EMI Emission
- 6.5W into 8Ω Load From 12V Supply (10% THD+N)
- Short circuit Protection (Save two Schottky Diodes.)
- Low Supply Current….8mA Typ at 12V
- Shutdown Current…...1μA Typ
- 24-pin TSSOP Package with Thermal Pad
- RoHS compliant and 100% lead(Pb)-free

## APPLICATIONS

- 2.1 Notebook PCs
- LCD Monitors/TVs
- PC Surround Speakers
- Hands-Free Car Kits

## Typical Application Circuit

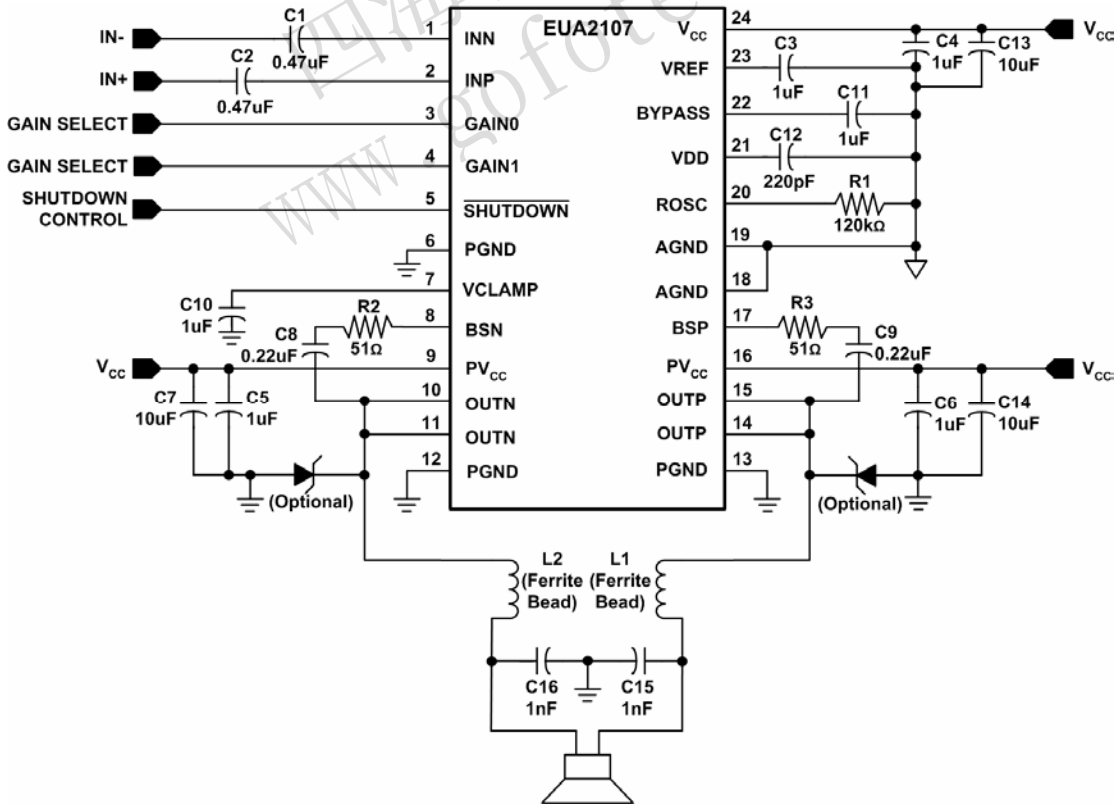
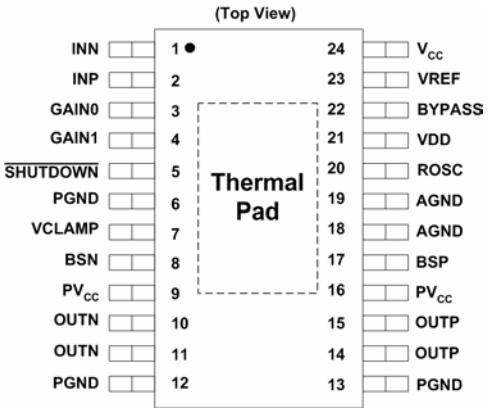



**Figure1.**

## Pin Configurations

| Package Type | Pin Configurations |
|---|---|
| TSSOP-24 |  |



## Pin Description

| PIN | TSSOP-24 | I/O | DESCRIPTION |
|---|---|---|---|
| INN | 1 | I | Negative differential input |
| INP | 2 | I | Positive differential input |
| GAIN0 | 3 | I | Bit 0 of gain control (see Table 1 for gain settings) |
| GAIN1 | 4 | I | Bit 1 of gain control (see Table 1 for gain settings) |
| $\overline{\text{SHUTDOWN}}$ | 5 | I | Shutdown terminal (active low), TTL compatible, 21V compliant |
| PGND | 6,12,13 | | Power ground |
| VCLAMP | 7 | O | Connect 1μF capacitor to ground to provide reference voltage for H-bridge gates |
| BSN | 8 | I | Bootstrap terminal for high-side gate drive of negative BTL output (connect a 0.22μF capacitor with a 51Ω resistor in series from OUTN to BSN) |
| $PV_{CC}$ | 9,16 | I | High-voltage power supply (for output stages) |
| OUTN | 10,11 | O | Negative BTL output, connect Schottky diode from PGND to OUTN for short-circuit protection |
| OUTP | 14,15 | O | Positive BTL output, connect Schottky diode from PGND to OUTP for short-circuit protection |
| BSP | 17 | I | Bootstrap terminal for high-side gate drive of positive BTL output (connect a 0.22μF capacitor with a 51Ω resistor in series from OUTP to BSP) |
| AGND | 18,19 | I | Analog ground terminal |
| ROSC | 20 | I | Connect 120kΩ resistor to ground to set oscillation frequency |
| VDD | 21 | I | 4V internal regulator (connect a 220pF capacitor to ground) |
| BYPASS | 22 | I | Connect 1μF capacitor to ground for BYPASS voltage filtering |
| VREF | 23 | O | 4V internal regulator for control circuitry (connect a 0.1μF to 1μF capacitor to ground) |
| $V_{CC}$ | 24 | I | Analog high-voltage power supply |

## Ordering Information

| Order Number | Package Type | Marking | Operating Temperature Range |
|---|---|---|---|
| EUA2107QIR1 | TSSOP-24 | xxxxx<br>EUA2107 | -40 °C to +85°C |

EUA2107 □ □ □ □

- Lead Free Code
  1: Lead Free 0: Lead
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  Q:TSSOP

## Block Diagram

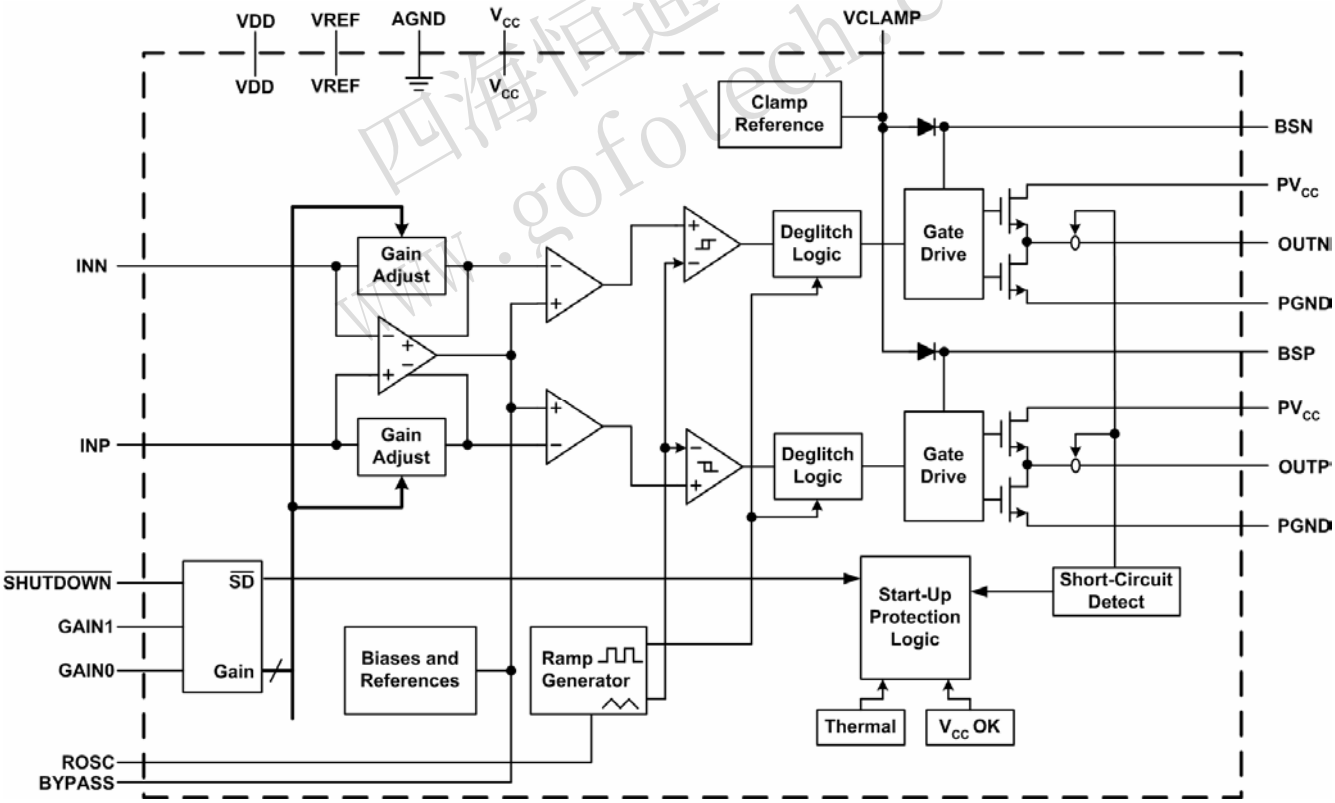



**Figure2.**

## Absolute Maximum Ratings

- Supply Voltage, $V_{CC}$,$PV_{CC}$ ---------- -0.3 V to 26V
- Load impedance, $R_L$ ---------- ≥7Ω
- Input Voltage, $\overline{SHUTDOWN}$ ---------- -0.3 V to $V_{CC}$ +0.3V
- Input Voltage,GAIN0,GAIN1---------- -0.3 V to 5.5V
- Input Voltage, INN, INP---------- -0.3 V to 6V
- Free-air Temperature Range, $T_A$ ---------- -40°C to +85°C
- Junction Temperature Range, $T_J$ ---------- -40°C to +150°C
- Storage Temperature Rang, $T_{stg}$ ---------- -65°C to +85°C
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ---------- +260°C
- ESD Susceptibility (HBM) ---------- >2kV

## Recommended Operating Conditions

| | | | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$, $PV_{CC}$ | $R_L$ ≥ 7Ω | 8 | 24 | V |
| Load Impedance, $R_L$ | | | 7 | | Ω |
| High-level input voltage, $V_{IH}$ | $\overline{SHUTDOWN}$ ,GAIN0,GAIN1 | | 2 | | V |
| Low-level input voltage, $V_{IL}$ | $\overline{SHUTDOWN}$ ,GAIN0,GAIN1 | | | 0.8 | V |
| Operating free-air temperature, $T_A$ | | | -40 | 85 | °C |

## Electrical Characteristics $T_A$ = +25°C , $PV_{CC}$=$V_{CC}$=12V (Unless otherwise noted)

| Symbol | Parameter | Conditions | | EUA2107 Min | EUA2107 Typ | EUA2107 Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\lvert V_{OS} \rvert$ | Output offset voltage (measured differentially) | $V_I$= 0 V, $A_V$=12dB, 18,23.6dB | | | | 50 | mV |
| | | $V_I$= 0 V, $A_V$=36dB | | | | 100 | |
| PSRR | Power supply rejection ratio | $PV_{CC}$ = 12 V to 15 V, inputs ac coupled to AGND, Gain = 32 dB | | | -60 | | dB |
| $\lvert I_{IL} \rvert$ | High-level input current | $PV_{CC}$ = 12 V, $V_I$= $PV_{CC}$ | | | | 1 | μA |
| $\lvert I_{IH} \rvert$ | Low-level input current | $PV_{CC}$ = 12 V, $V_I$= 0 V | | | | 1 | μA |
| ICC | Supply current | $\overline{SHUTDOWN}$ =2V, no load | | | 8 | 15 | mA |
| | | $\overline{SHUTDOWN}$ =$V_{CC}$, $V_{CC}$=18V, $P_O$=6.5W, $R_L$=8Ω | | | 0.42 | | A |
| $ICC_{(SD)}$ | Supply current , shutdown mode | $\overline{SHUTDOWN}$ =0.8V | | | 1 | 2 | μA |
| $f_S$ | Switching frequency | $R_{OSC}$=120kΩ | | | 250 | | kHz |
| $r_{DS}$(on) | Output transistor on resistance (total) | $I_O$=1A, $T_J$=+25°C | | | | 1.4 | Ω |
| G | Gain | GAIN1=0.8V | GAIN0=0.8V | 10.9 | 12 | 12.8 | dB |
| | | | GAIN0=2V | 17.1 | 18 | 18.5 | |
| | | GAIN1=2V | GAIN0=0.8V | 23 | 23.6 | 24.3 | dB |
| | | | GAIN0=2V | 34.7 | 35.5 | 36.3 | |

**Operating Characteristics $PV_{CC}=V_{CC}=12V$, Gain=12dB, $T_A$ = +25°C (Unless otherwise noted)**

| Symbol | Parameter | Conditions | EUA2107 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $P_O$ | Continuous output power | THD+N=10%, f=1kHz, $R_L$=8Ω | | 6.5 | | W |
| | | THD+N=1%, f=1kHz, $R_L$=8Ω | | 5 | | |
| THD+N | Total harmonic distortion +noise | $P_O$=3.25W ,$R_L$=8Ω, f=1 kHz | | 0.08% | | |
| $B_{OM}$ | Maximum output power bandwidth | THD=1% | | 20 | | kHz |
| $k_{SVR}$ | Supply ripple rejection ratio | f=1kHz, $C_{(BYPASS)}$=1uF | | -65 | | dB |
| SNR | Signal-to-noise ratio | $P_O$=3.25W ,$R_L$=8Ω | | 92 | | dB |
| Vn | Noise output voltage | $C_{(BYPASS)}$=1uF, f=20Hz to 22kHz, A-weighting filter | | 180 | | μV(rms) |
| | | | | 75 | | dBV |
| $Z_I$ | Input impedance | See Table 1 | | >35 | | kΩ |

**Operating Characteristics $PV_{CC}=V_{CC}=18V$, Gain=12dB, $T_A$ = +25°C (Unless otherwise noted)**

| Symbol | Parameter | Conditions | EUA2107 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| THD+N | Total harmonic distortion +noise | $P_O$=3.25W ,$R_L$=8Ω, f=1 kHz | | 0.16% | | |
| $B_{OM}$ | Maximum output power bandwidth | THD=1% | | 20 | | kHz |
| $k_{SVR}$ | Supply ripple rejection ratio | f=1kHz, $C_{(BYPASS)}$=1uF | | -65 | | dB |
| SNR | Signal-to-noise ratio | $P_O$=3.25W ,$R_L$=8Ω | | 92 | | dB |
| Vn | Noise output voltage | $C_{(BYPASS)}$=1uF, f=20Hz to 22kHz, A-weighting filter | | 200 | | μV(rms) |
| | | | | 74 | | dBV |
| $Z_I$ | Input impedance | See Table 1 | | >35 | | kΩ |

## Typical Characteristics

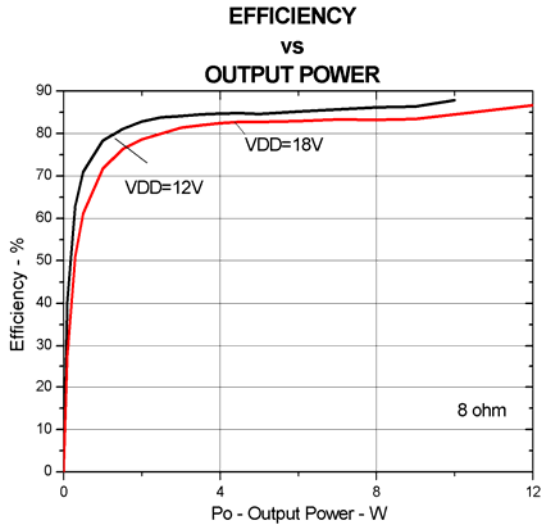



**Figure3.**

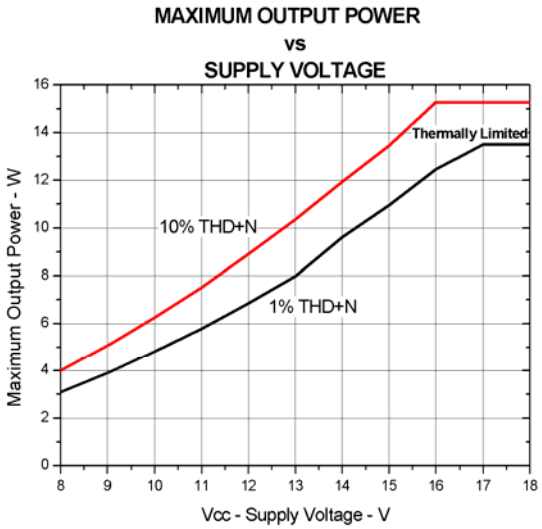



**Figure4.**

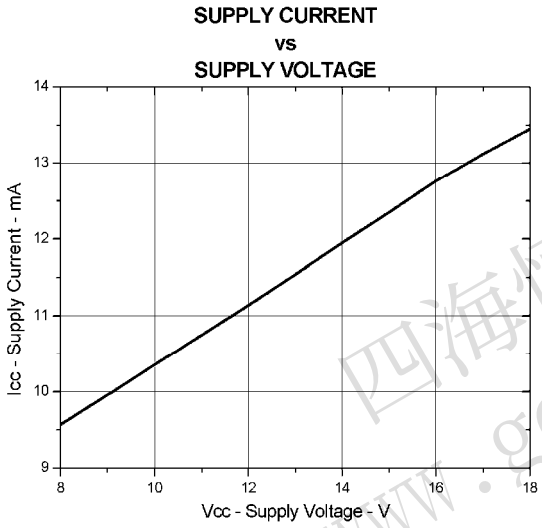



**Figure5.**

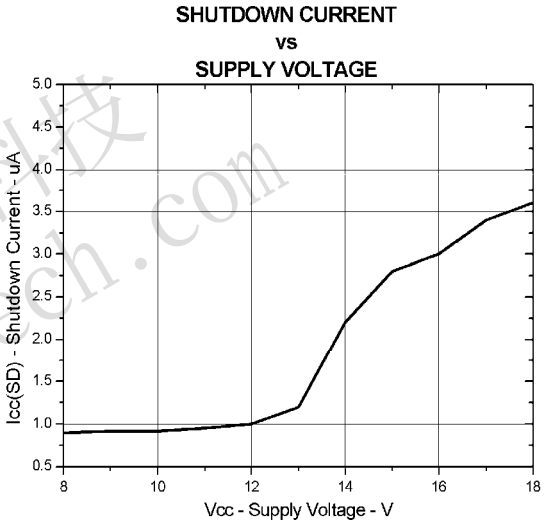



**Figure6**

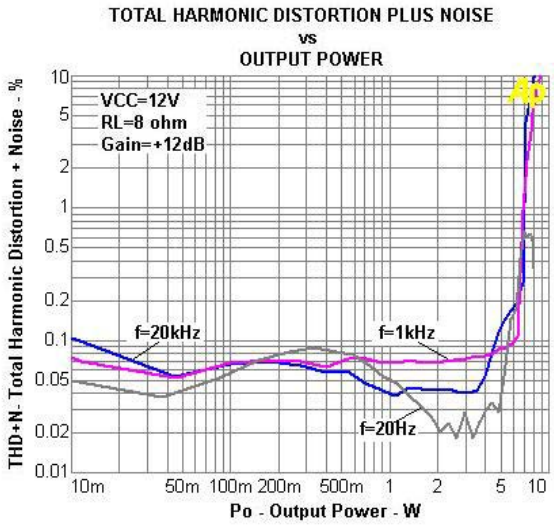



**Figure7.**

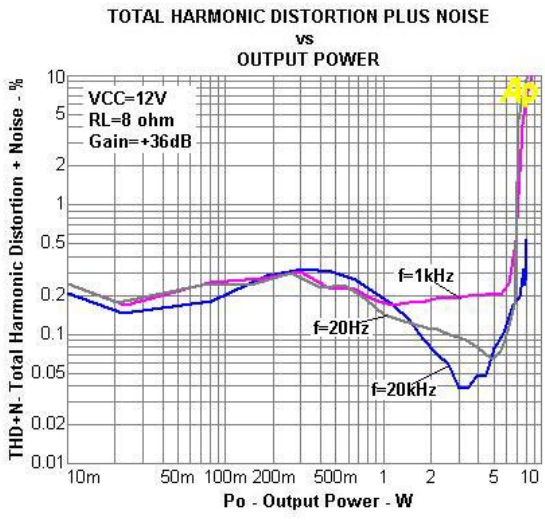



**Figure8.**

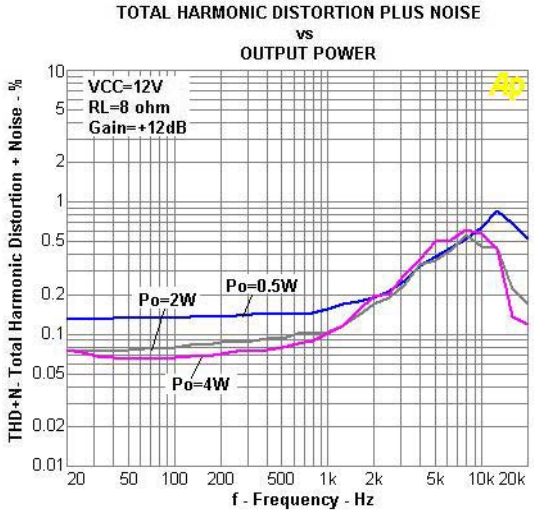



**Figure9.**

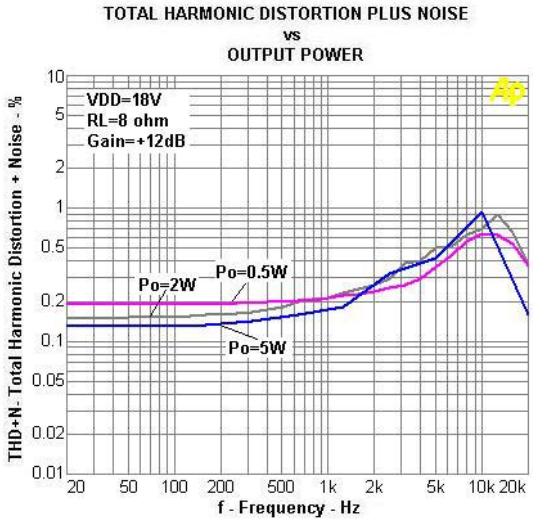



**Figure10.**

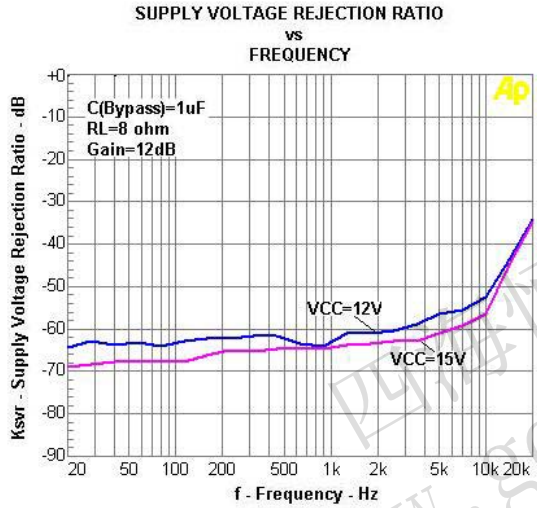



**Figure11.**

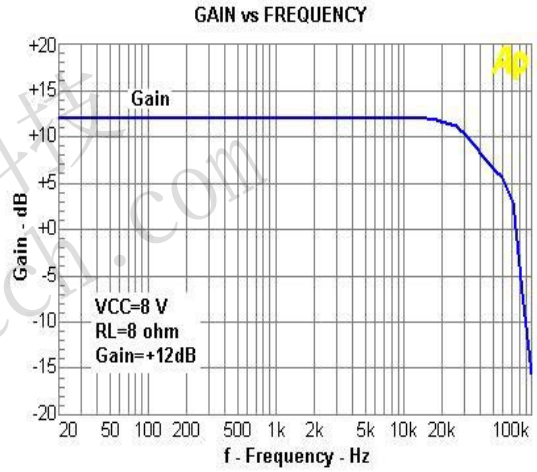



**Figure12.**

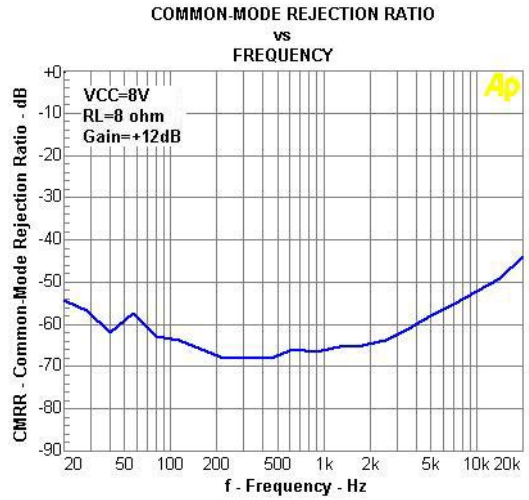



**Figure13.**

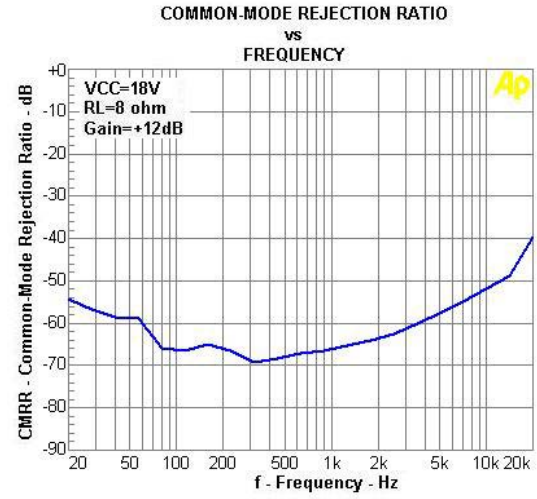



**Figure14.**

## Application Information

### Gain Selection

The gain of the EUA2107 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance ($Z_I$) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance may shift by 30% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 35 kΩ, which is the absolute minimum input impedance of the EUA2107. At the lower gain settings, the input impedance could increase as high as 260 kΩ.

**Table.1 Gain Setting**

| GAIN1 | GAIN0 | AMPLIFIER GAIN (dB) | INPUT IMPEDANCE (kΩ) |
|---|---|---|---|
| | | TYP | TYP |
| 0 | 0 | 12 | 200 |
| 0 | 1 | 18 | 100 |
| 1 | 0 | 24 | 100 |
| 1 | 1 | 36 | 50 |

### $\overline{\text{SHUTDOWN}}$ Operation

The EUA2107 employs a shutdown mode of operation designed to reduce supply current ($I_{CC}$) to the absolute minimum level during periods of non-use for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, $I_{CC(SD)}$ = 1μA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected, because amplifier operation would be unpredictable. Ideally, the device should be held in shutdown when the system powers up and brought out of shutdown once any digital circuitry has settled. However, if $\overline{\text{SHUTDOWN}}$ is to be left unused, the terminal may be connected directly to $V_{CC}$.

### Short-Circuit Protection

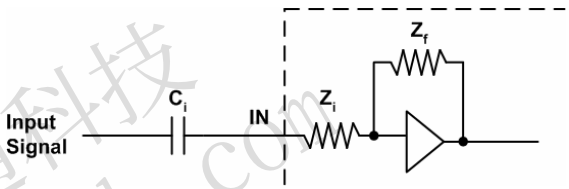
The EUA2107 has short circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-VCC shorts. When a short-circuit is detected on the outputs, the part immediately disables the output drive and enters into shutdown mode. This is a latched fault and must be reset by cycling the voltage on the SHUTDOWN pin to a logic low and back to the logic high state for normal operation. This clears the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry again activates.

### Thermal Protection

Thermal protection on the EUA2107 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 40°C. The device begins normal operation at this point with no external system interaction.

### Input Resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the -3 B or cutoff frequency also changes by over six times.

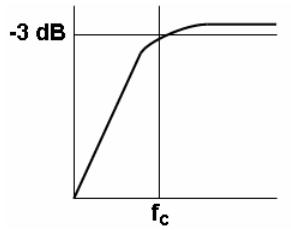



The -3 dB frequency can be calculated using Equation 1. Use Table 1 for $Z_I$ values.

$$f = \frac{1}{2\pi Z_i C_i} \quad \text{---------- (1)}$$

### Input Capacitor, $C_I$

In the typical application, an input capacitor ($C_I$) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, $C_I$ and the input impedance of the amplifier ($Z_I$) form a high-pass filter with the corner frequency determined in Equation 2.




$$f_c = \frac{1}{2\pi Z_i C_i} \quad \text{----------(2)}$$

The value of $C_I$ is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where $Z_I$ is 35 kΩ and the

specification calls for a flat bass response down to 20 Hz. Equation 2 is reconfigured as Equation 3.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad \text{----------(3)}$$

In this example, $C_I$ is 0.22µF, so one would likely choose a value of 0.47µF, as this value is commonly used. If the gain is known and will be constant, use $Z_I$ from Table 1 to calculate $C_I$. A further consideration for this capacitor is the leakage path from the input source through the input network and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice.

### Power Supply Decoupling

The EUA2107 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads.

For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1µF placed as close as possible to the device $V_{CC}$ lead works best. For filtering lower-frequency noise signals, a larger capacitor of 10µF or greater placed near the audio power amplifier is recommended.

### BSN and BSP Capacitors

The full H-bridge output stage uses only NMOS transistors. It therefore requires bootstrap capacitors for the high side of each output to turn on correctly. A 0.22µF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22µF capacitor must be connected from OUTP to BSP, and one 0.22µF capacitor must be connected from OUTN to BSN. (See Figure 1.)

### VCLAMP Capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, an internal regulator clamps the gate voltage. A 1µF capacitor must be connected from VCLAMP (pin 7) to ground and must be rated for at least 25V. The voltage at VCLAMP (pin 7) varies with $V_{CC}$ and may not be used for powering any other circuitry.

### Bypass Capacitor

The bypass capacitor (C11 of Figure 1) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, $C_{BYPASS}$ determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor (C11) values of 1µF ceramic low-ESR capacitors is recommended for the best THD noise and de-pop performance. The bypass capacitor **must** be a value greater than the input capacitors for optimum de-pop performance.

### VREF Decoupling Capacitor

The VREF terminal (pin 23) is the output of an internally-generated 4V supply, used for the oscillator and gain setting logic. It requires a 0.1µF to 1µF capacitor to ground to keep the regulator stable. The regulator may not be used to power any additional circuitry.

### VDD Decoupling Capacitor

The VDD terminal (pin 21) is the output of an internally-generated 4V supply, used for un-shutdown logic circuit. It requires 1µF capacitor to ground to keep the regulator stable.

### Differential Input

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the EUA2107 EVM with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the EUA2107 with a single-ended source, ac ground the INN input through a capacitor and apply the audio signal to the INP input. In a single-ended input application, the INN input should be ac-grounded at the audio source instead of at the device input for best noise performance.

### Switching Frequency

The switching frequency is determined using the values of the components connected to $R_{OSC}$ (pin 20) and the frequency can be varied from 200 kHz to 300 kHz by adjusting the values chosen for $R_{OSC}$ .

### Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

## Output Filter Considerations

A ferrite bead filter (shown in Figure 15) should be used in order to pass FCC and/or CE radiated emissions specifications and if a frequency sensitive circuit operating higher than 1 MHz is nearby. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies. Use an additional LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and/or there are long wires (greater than 11 inches) from the amplifier to the speaker, as shown in Figure 16.

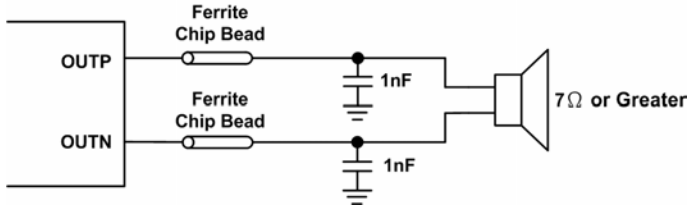



**Figure 15. Typical Ferrite Chip Bead Filter**

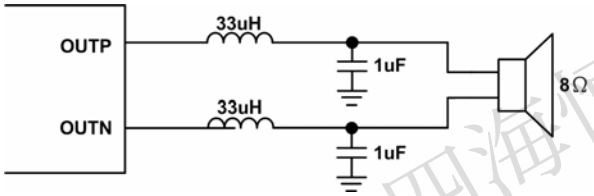
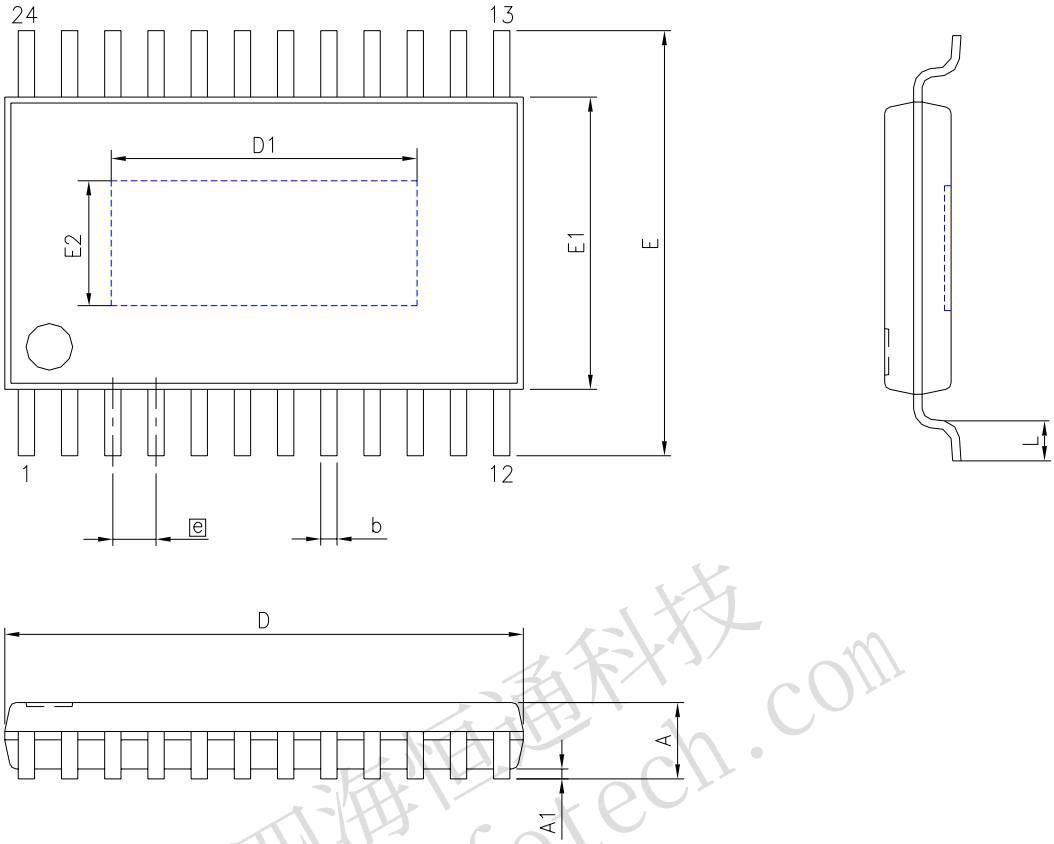



**Figure 16. Typical LC Output Ferrite for 8Ω Speaker**

## Package Information

**TSSOP-24**






| SYMBOLS | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | - | 1.20 | - | 0.047 |
| A1 | 0.00 | 0.15 | 0.000 | 0.006 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| E1 | 4.40 | | 0.173 | |
| D | 7.80 | | 0.307 | |
| D1 | 4.60 | | 0.181 | |
| E | 6.20 | 6.60 | 0.244 | 0.260 |
| E2 | 1.88 | | 0.074 | |
| e | 0.65 | | 0.026 | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |