EUTECH
MICROELECTRONICS

25-W Mono Class-D Audio Power Amplifier with Speaker Protection

DESCRIPTION

The EUA2112 is a high efficiency, one channel bridged-tied load (BTL), class-D audio power amplifier. Operating from a 24V power supply, EUA2112 is capable of delivering 25W of continuous output power to a 8Ω load with 10% THD+N. The EUA2112 features a differential input architecture offering improved noise immunity over a single-ended (SE) input amplifier. Amplifier gain is internally configured and can be selected to 20, 26, 32 or 36dB utilizing the Go and G1 gain select pins. Advanced EMI suppression technology enables the use of inexpensive ferrite bead at the outputs while meeting EMC requirements.

The speaker protection circuitry is integrated into EUA2112 to limit the amount of current through the speaker. The EUA2112 also features short-circuit and thermal protection preventing the device from being damaged during a fault condition. The EUA2112 is available in thermally efficient 28-pin TSSOP package.

FEATURES

- Wide Supply Voltage: 8V to 26V
- Unique Modulation Scheme Reduces EMI Emission
- 25W into an 8-Ω Load From a 24-V Supply
- 20W into a 4-Ω Load From a 12-V Supply
- 94% Efficient Class-D Operation Eliminates Need for Heat Sinks
- Four Selectable, Gain Settings
- Differential Inputs
- Speaker Protection Circuitry
- Thermal and Short-Circuit Protection
- 28-pin TSSOP Package with Thermal Pad
- RoHS compliant and 100% lead(Pb)-free Halogen-Free

APPLICATIONS

- Televisions

Typical Application Circuit

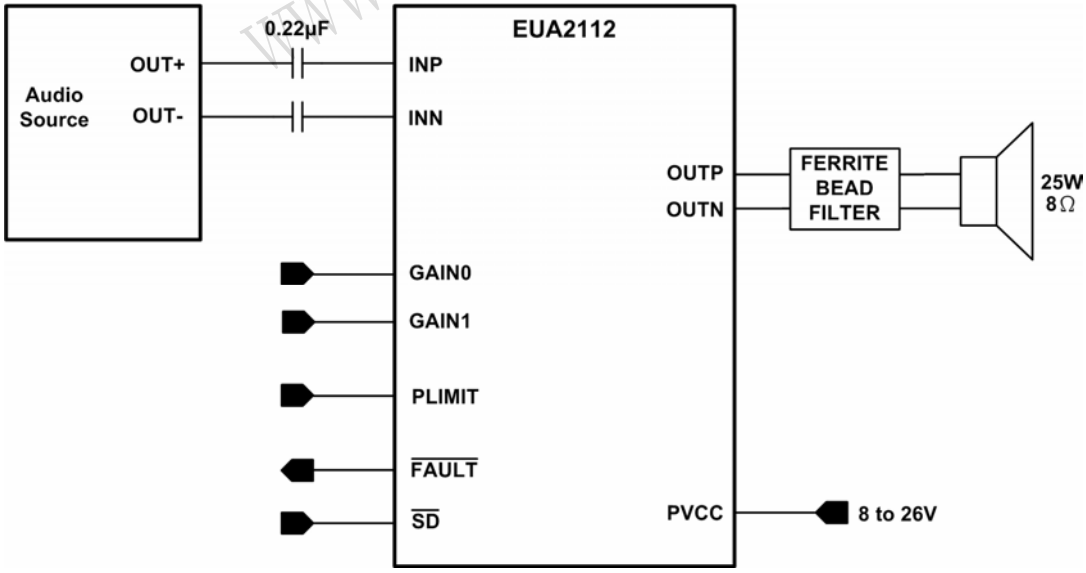
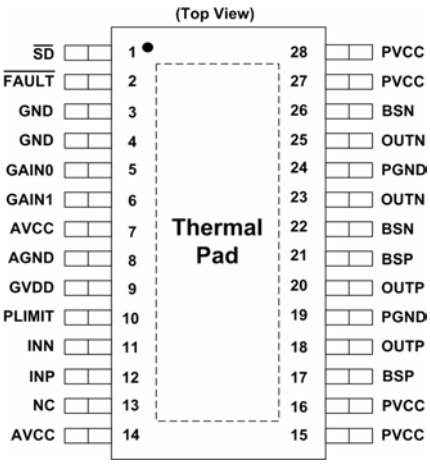


Figure1. Simplified Application Schematic

Pin Configurations

Package Type	Pin Configurations
TSSOP-28	

Pin Description

PIN	TSSOP-28	I/O/P	DESCRIPTION
$\overline{SD}$	1	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
$\overline{FAULT}$	2	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{FAULT}$ pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVCC.
GND	3,4	I	Connect to local ground.
GAIN0	5	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
GAIN1	6	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
AVCC	7,14	P	Analog supply
AGND	8	P	Analog signal ground. Connect to the thermal pad.
GVDD	9	O	High-side FET gate drive supply. Nominal voltage is 4.5V. Also should be used as supply for PLIMIT function.
PLIMIT	10	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
INN	11	I	Negative audio input. Biased at 2.25V.
INP	12	I	Positive audio input. Biased at 2.25V.
NC	13	P	Not connected
PVCC	15,16,27,28	P	Power supply H-bridge. PVCC pins are connect internally.
BSP	17,21	I	Bootstrap I/O for positive high-side FET.
OUTP	18,20	O	Class-D H-bridge positive output.
PGND	19,24		Power ground for the H-bridges.
BSN	22,26	I	Bootstrap I/O for negative high-side FET.
OUTN	23,25	O	Class-D H-bridge negative output.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUA2112QIR1	TSSOP-28	xxxxx EUA2112	-40 °C to +85°C

EUA2112 □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen Free 0: Lead
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  Q:TSSOP

Absolute Maximum Ratings

- Supply Voltage, AVCC,PVCC, ---------- -0.3 V to 30V
- Input Voltage, $\overline{SD}$,GAIN0,GAIN1,PBTL, $\overline{FAULT}$ ---------- -0.3 V to V_{CC} +0.3V
- Input Voltage, PLIMIT ---------- -0.3 V to GVDD +0.3V
- Input Voltage, RINN,RINP,LINN,LINP ---------- -0.3 V to 6.3V
- Thermal Resistance θ_{JA} (TSSOP-28) ---------- 34℃/W
- Free-air Temperature Range, T_A ---------- -40°C to +85°C
- Junction Temperature Range, T_J ---------- -40°C to +150°C
- Storage Temperature Rang, T_{stg} ---------- -65°C to +150°C
- Lead Temperature ---------- 260°C
- Load Resistance, R_{LOAD} ---------- 3.2Ω Minimum
- ESD Susceptibility (HBM) ---------- 2kV

Recommended Operating Conditions

		Min	Max	Unit
Supply voltage, V_{CC}	PVCC,AVCC	8	26	V
High-level input voltage, V_{IH}	$\overline{SD}$,GAIN0,GAIN1,PBTL	2		V
Low-level input voltage, V_{IL}	$\overline{SD}$,GAIN0,GAIN1,PBTL		0.8	V
High-level input current, I_{IH}	$\overline{SD}$,GAIN0,GAIN1,PBTL,V_I=2V,V_{CC}=18V		50	μA
Low-level input current, I_{IL}	$\overline{SD}$,GAIN0,GAIN1,PBTL,V_I=0.8V,V_{CC}=18V		5	μA
Low-level output voltage, V_{OL}	$\overline{FAULT}$, $R_{PULL-UP}$=100k, V_{CC}=26V		0.8	V
Oscillator frequency, f_{OSC}		230	330	kHz
Operating free-air temperature, T_A		-40	85	°C

DC Characteristics T_A = +25°C ,V_{CC}=24V, R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions		EUA2112			Unit
				Min	Typ	Max.	
$\|V_{OS}\|$	Class-D output offset voltage (measured differentially)	V_I= 0V, Gain = 36dB			5	50	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ =2V, no load, PV_{CC}=24V			32	50	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ =0.8V, no load, PV_{CC}=24V			250	400	μA
r_{DS}(on)	Drain-source on-state resistance	V_{CC}=12V, I_O=500mA, T_J=25°C	High Side		240		mΩ
			Low Side		240		
G	Gain	GAIN1=0.8V	GAIN0=0.8V	19	20	21	dB
			GAIN0=2V	25	26	27	
		GAIN1=2V	GAIN0=0.8V	31	32	33	dB
			GAIN0=2V	35	36	37	
t_{ON}	Turn-on time	$\overline{SD}$ =2V			28		ms
t_{OFF}	Turn-off time	$\overline{SD}$ =0.8V			28		ms
GVDD	Gate Drive Supply	I_{GVDD}=100μA		4.2	4.5	4.8	V
t_{DCDET}	DC Detect time	$V_{(RINN)}$=5V, VRINP=0V			420		ms

DC Characteristics T_A = +25°C ,V_{CC}=12V, R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions		EUA2112			Unit
				Min	Typ	Max.	
$\|V_{OS}\|$	Class-D output offset voltage (measured differentially)	V_I= 0V,Gain =36dB			5	50	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ =2V, no load, PV_{CC}=12V			20	35	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ =0.8V, no load, PV_{CC}=12V			200	1000	μA
r_{DS}(on)	Drain-source on-state resistance	V_{CC}=12V, I_O=500mA, T_J=25°C	High Side		240		mΩ
			Low Side		240		
G	Gain	GAIN1=0.8V	GAIN0=0.8V	19	20	21	dB
			GAIN0=2V	25	26	27	
		GAIN1=2V	GAIN0=0.8V	31	32	33	dB
			GAIN0=2V	35	36	37	
t_{ON}	Turn-on time	$\overline{SD}$ =2V			28		ms
t_{OFF}	Turn-off time	$\overline{SD}$ =0.8V			28		ms
GVDD	Gate Drive Supply	I_{GVDD}=2mA		4.2	4.5	4.8	V
V_O	Output voltage maximum under PLIMIT control	$V_{(PLIMIT)}$=1.3V, V_I=1Vrms		6.75	7.90	8.75	V

AC Characteristics T_A = +25°C ,V_{CC}=24V, R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2112			Unit
			Min	Typ	Max.	
K_{SVR}	Power supply ripple rejection	200mV_{PP} ripple at 1kHz, Gain= 20dB, Inputs ac-coupled to AGND		-60		dB
P_O	Continuous output power	THD+N=10%, f=1kHz, V_{CC}=24V		25		W
THD+N	Total harmonic distortion +noise	V_{CC}=24V, f=1kHz, Po=12.5W(half-power)		0.25		%
Vn	Output integrated noise	20Hz to 22kHz, A-weighted filter, Gain=20dB		255		μV
				-71		dBV
SNR	Signal-to-noise ratio	P_O=12.5W, f=1kHz,Gain=20dB, A-weighted		91		dB
f_{OSC}	Oscillator frequency		230	280	330	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			30		°C

AC Characteristics T_A = +25°C ,V_{CC}=12V, R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2112			Unit
			Min	Typ	Max.	
K_{SVR}	Power supply ripple rejection	200mV_{PP} ripple from 20Hz ~1kHz, Gain= 20dB, Inputs ac-coupled to AGND		-60		dB
P_O	Continuous output power	THD+N=10%, f=1kHz, V_{CC}=12V, R_L=4Ω		20		W
		THD+N=10%, f=1kHz, V_{CC}=12V, R_L=8Ω		10		
THD+N	Total harmonic distortion +noise	R_L=8Ω, f=1kHz, Po=5W(half-power)		0.25		%
Vn	Output integrated noise	20Hz to 22kHz, A-weighted filter, Gain=20dB		255		μV
				-71		dBV
SNR	Signal-to-noise ratio	Maximum output at THD+N< 1%, f=1kHz,Gain=20dB, A-weighted		90		dB
f_{OSC}	Oscillator frequency		230	280	330	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			30		°C

Block Diagram

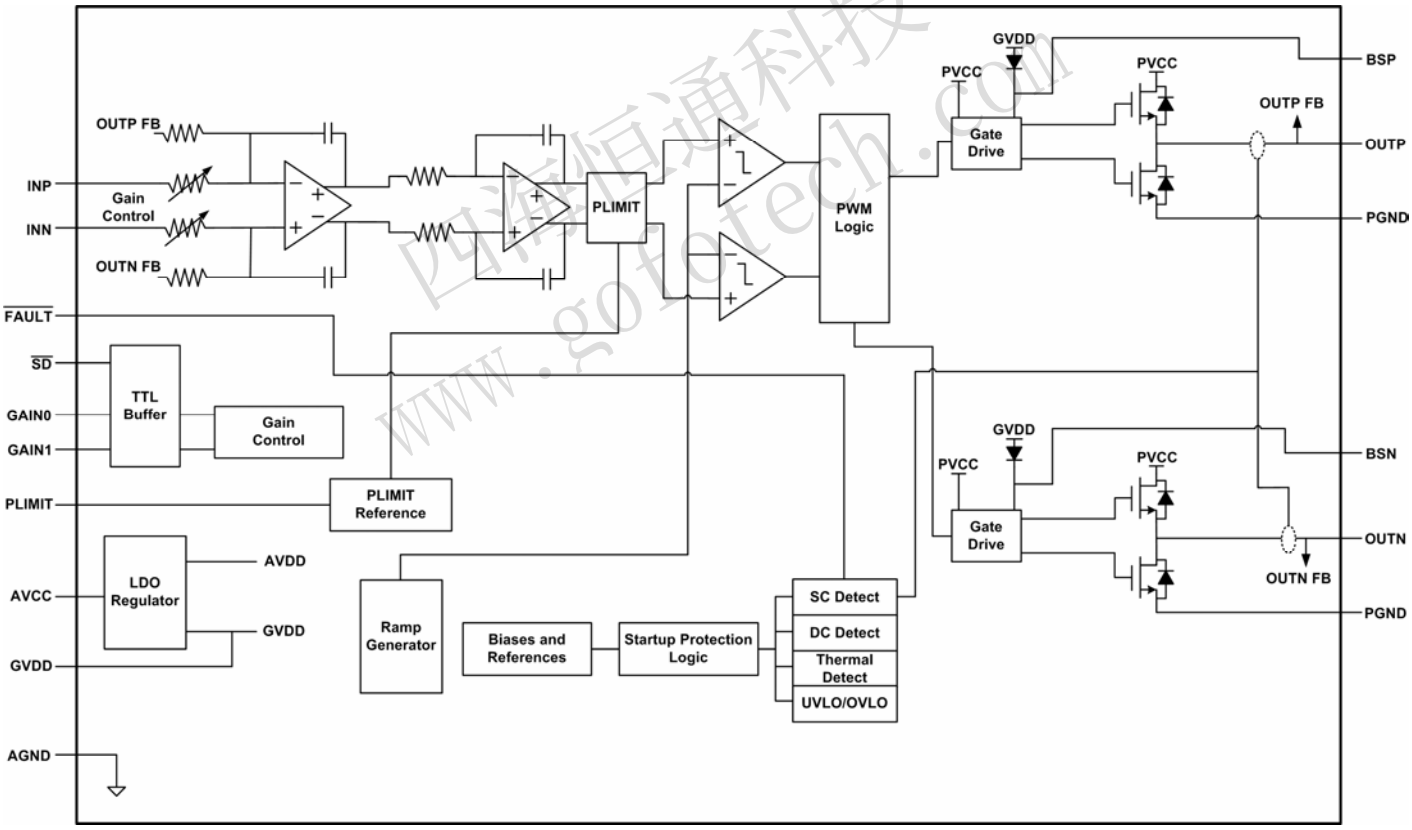


Figure2.

Typical Characteristics

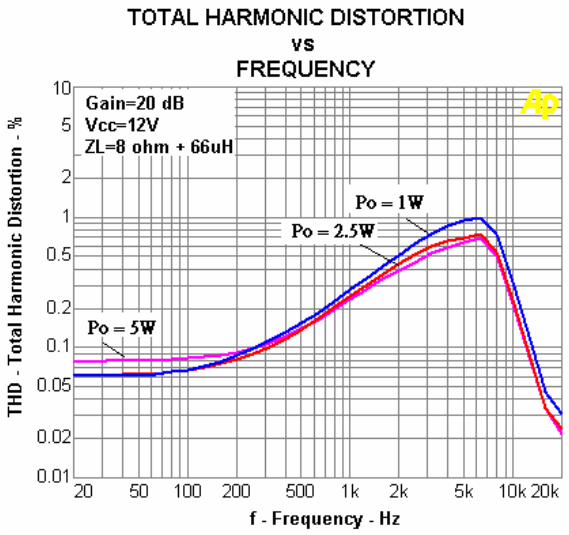


Figure3.

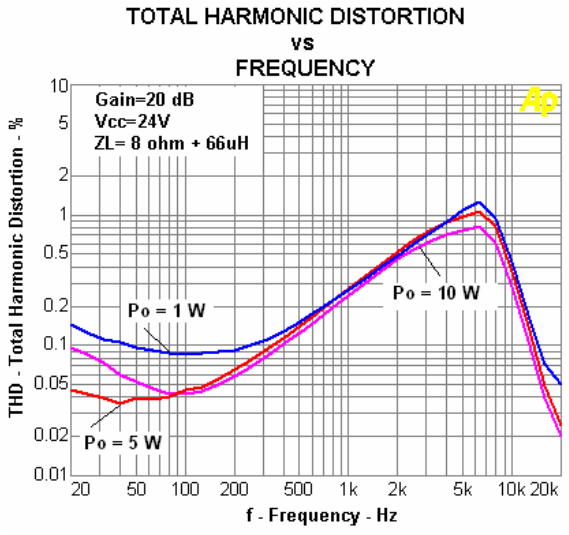


Figure4.

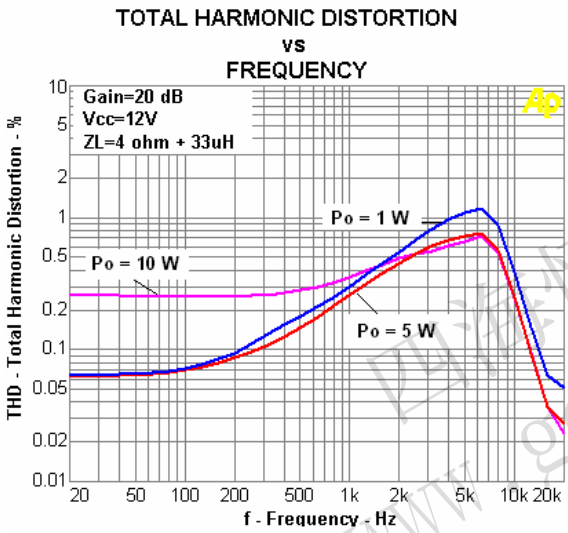


Figure5.

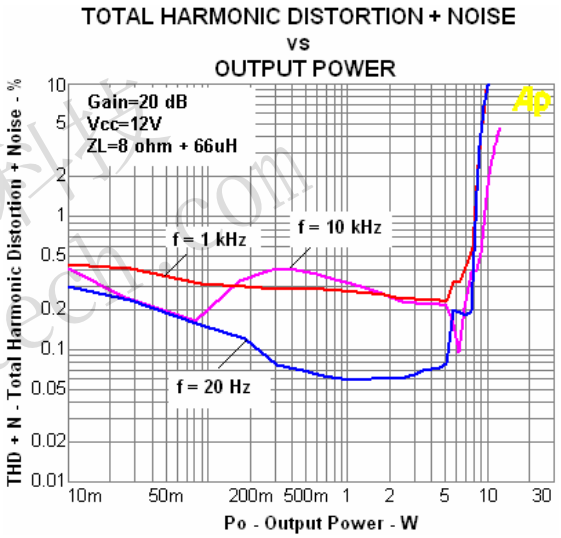


Figure6.

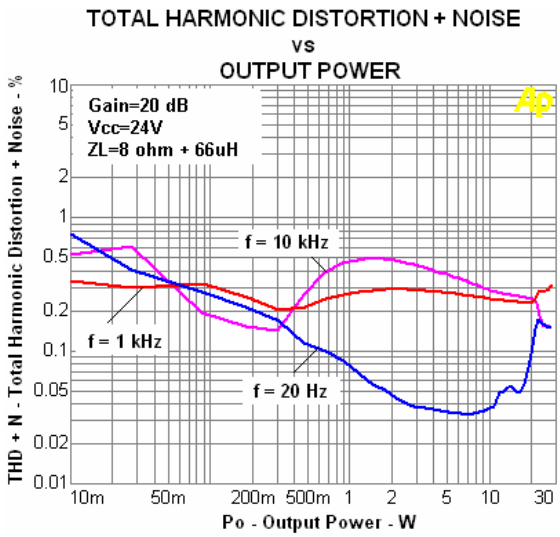


Figure7.

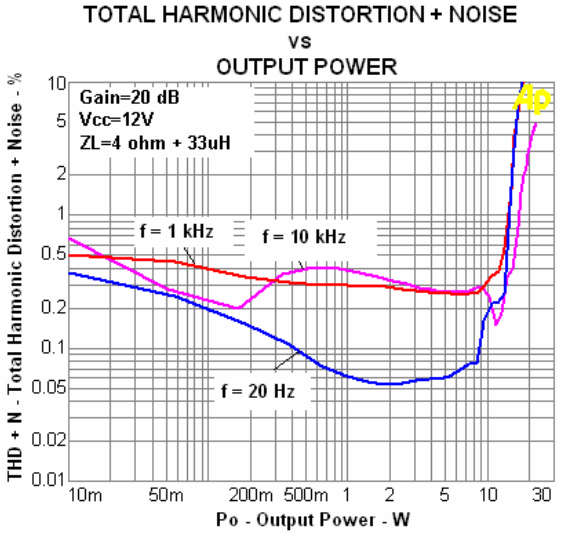


Figure8.

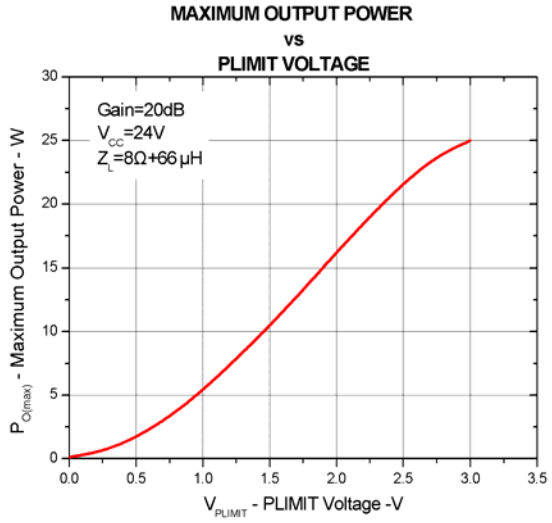


Figure9.

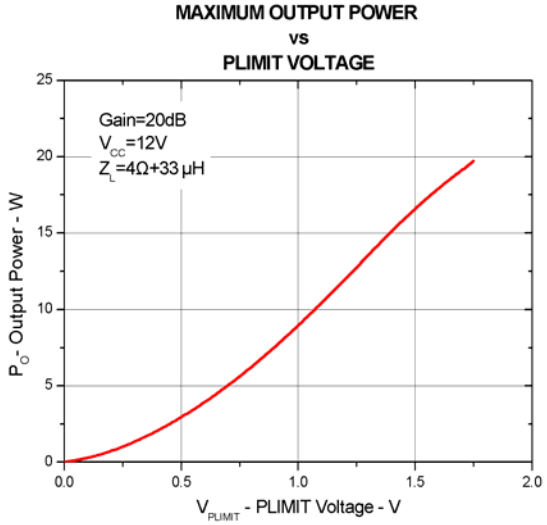


Figure10.

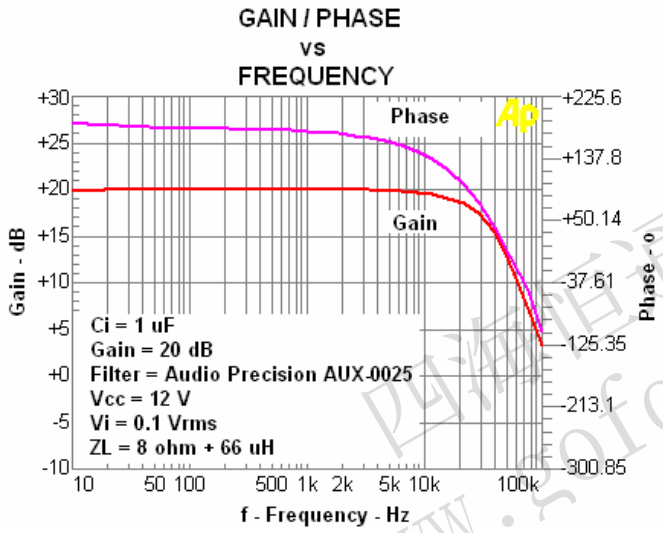


Figure11.

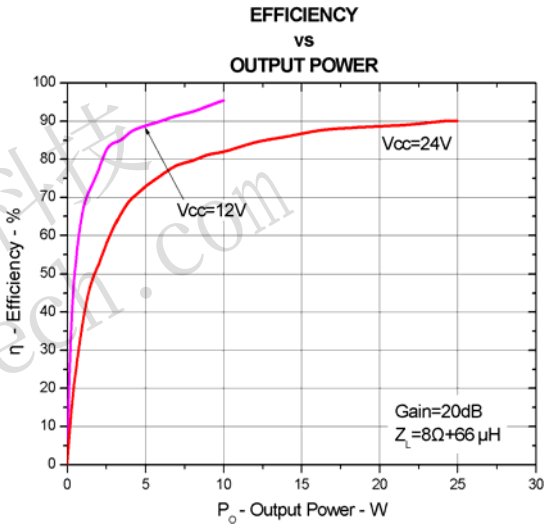


Figure12.

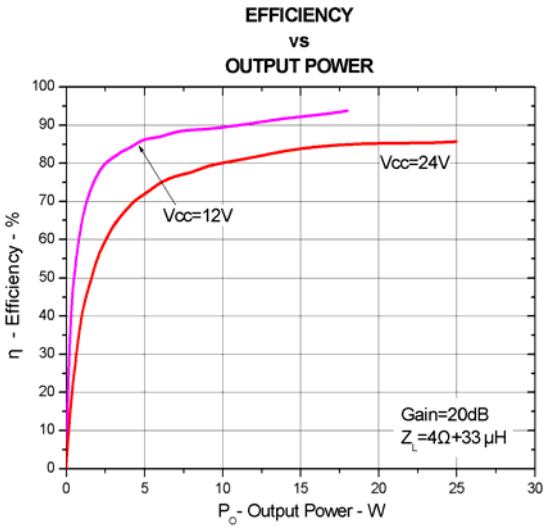


Figure13.

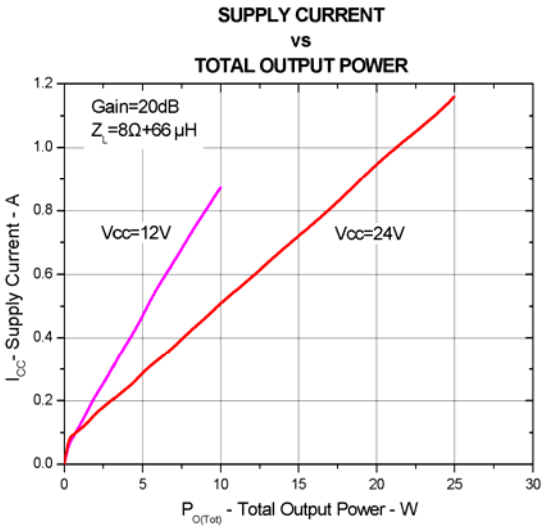


Figure14.

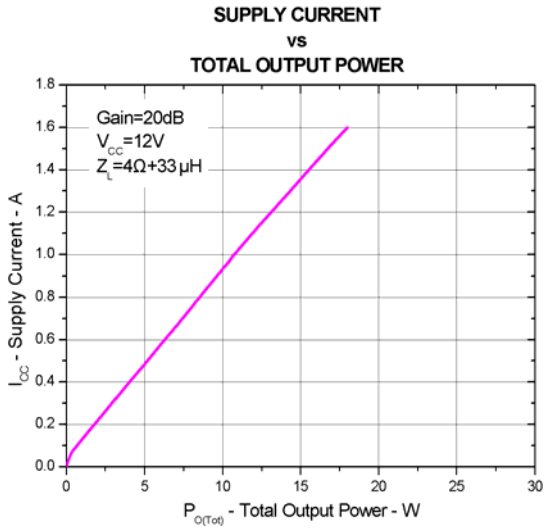


Figure15.

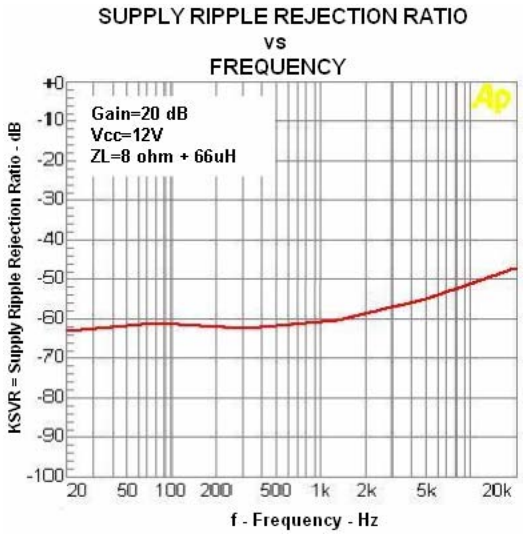


Figure16.

Application Information

Differential Input

The differential input stage of the amplifier cancels any common-mode noise that appears on both input lines of the audio channel. To use the EUA2112 with a differential source, connect the positive signal of the audio source to the INP pin and the negative signal from the audio source to the INN pin (Figure 17).

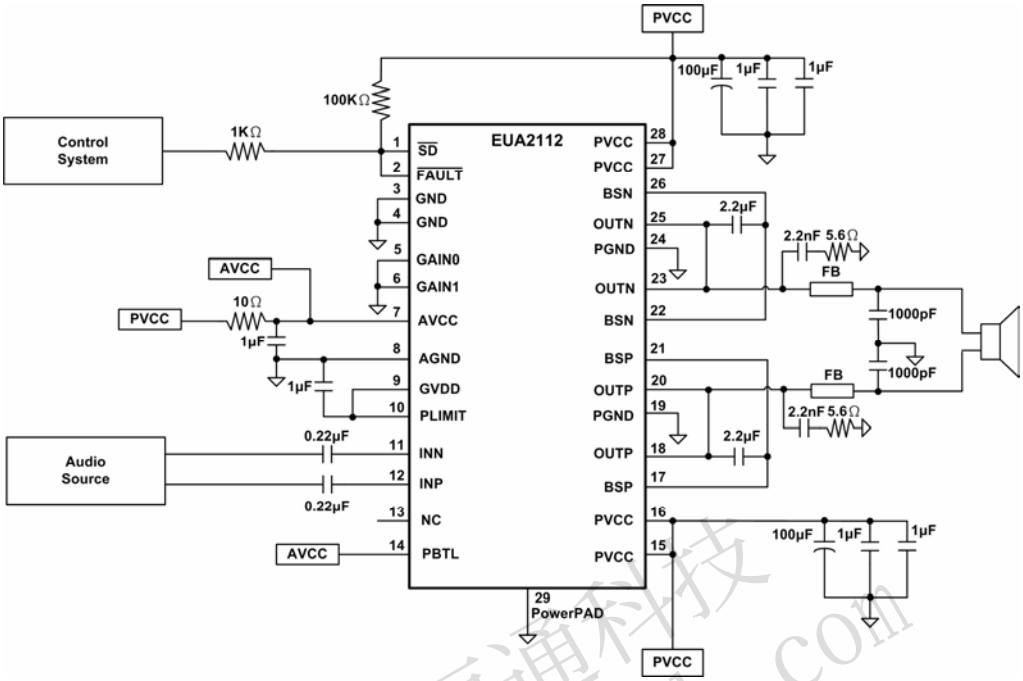


Figure 17. Differential Input

Single-Ended Input

When using an audio source with a single-ended “out”, it is important to connect the RINN and LINN pins to the GND of the audio source with coupling capacitors. (Figure 18).

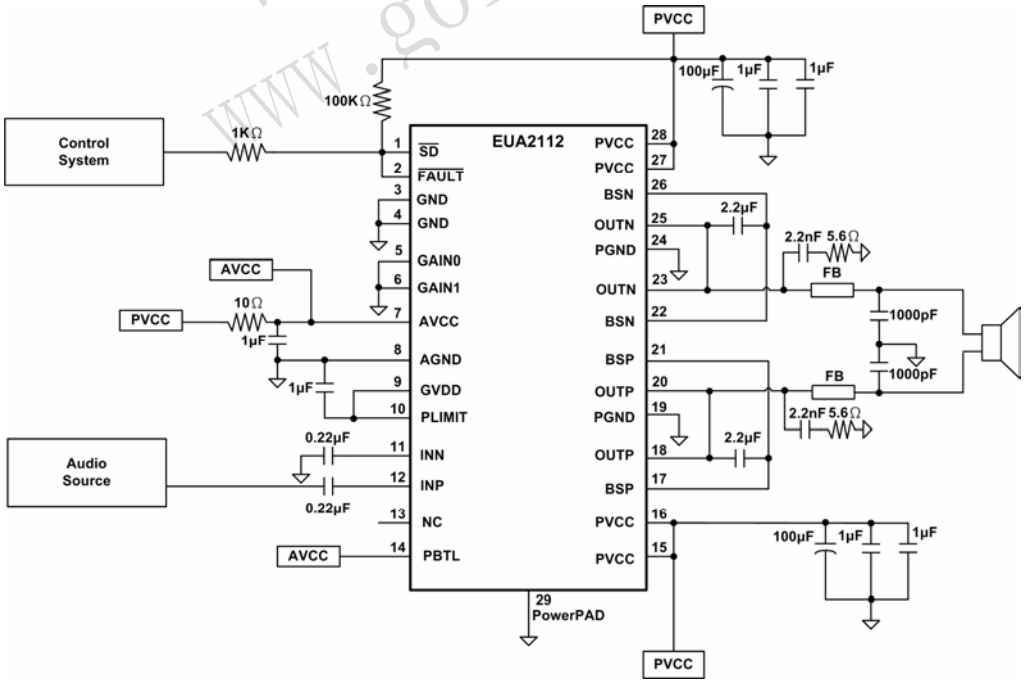


Figure 18. Single Ended Input

Gain Selection

The gain of the EUA2112 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 1 are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network should be designed assuming an input impedance of 40 kΩ, which is the absolute minimum input impedance of the EUA2112. At the lower gain settings, the input impedance could increase as high as 120 kΩ.

Table.1 Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	20	100
0	1	26	50
1	0	32	50
1	1	36	50

$\overline{SD}$ Operation

Connect $\overline{SD}$ to a logic high for normal operation. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{SD}$ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown prior to removing the power supply voltage.

PLIMIT

The voltage at pin 10 can used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also add a 1µF capacitor from pin 10 to ground.

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. This "virtual" rail is 6 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{---------- (1)}$$

For unclipped power

Where:

R_S is the total series resistance including $R_{DS(on)}$, and any resistance in the output filter.

R_L is the load resistance.

V_P is the peak amplitude of the output possible within the supply rail.

V_P = 6.6 × PLIMIT voltage if PLIMIT < 6.6 × V_P

P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)

Table.2 PLIMIT Typical Operation

Test Conditions()	PLIMIT Voltage	Output Power (W)	Output Voltage Amplitude (V_{P-P})
PVCC=24V, VIN=1Vrms, R_L=4Ω, Gain=20dB	4.5	25.87	28.8
PVCC=24V, VIN=1Vrms, R_L=4Ω, Gain=20dB	1.24	13.48	20.7
PVCC=24V, VIN=1Vrms, R_L=4Ω, Gain=20dB	0.8	6.46	18.2
PVCC=12V, VIN=1Vrms, R_L=4Ω, Gain=20dB	4.5	18.72	24.4
PVCC=12V, VIN=1Vrms, R_L=4Ω, Gain=20dB	1.13	11.7	19.3
PVCC=12V, VIN=1Vrms, R_L=4Ω, Gain=20dB	0.77	6.08	13.9

GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also be used to supply the PLIMIT voltage divider circuit. Add a 1µF capacitor to ground at this pin.

DC Detect

EUA2112 has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the FAULT pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z. To clear the DC Detect it is necessary to cycle the PVCC supply. Cycling SD will NOT clear a DC detect fault.

A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 20% (for example, +60%, -40%) for more than 420 msec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2Hz. To avoid nuisance faults due to the DC detect circuit, hold the SD pin low at

power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

Short-Circuit Protection and Automatic Recovery Feature

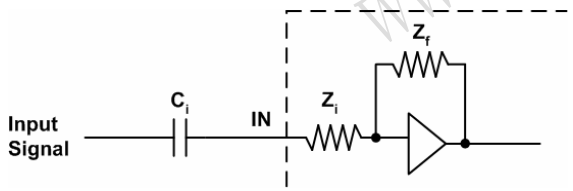
The EUA2112 has short-circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-VCC shorts. When a short circuit is detected on the outputs, the part immediately disables the output drive. This is a latched fault and must be reset by cycling the voltage on the $\overline{\text{SHUTDOWN}}$ pin or MUTE pin. This clears the short-circuit flag and allows for normal operation if the short was removed. If the short was not removed, the protection circuitry again activates.

Thermal Protection

Thermal protection on the EUA2112 prevents damage to the device when the internal die temperature exceeds 150°C. There is a 10°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30°C. The device begins normal operation at this point with no external system interaction.

Input Resistance

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 50 kΩ ±20%, to the largest value, 100 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.

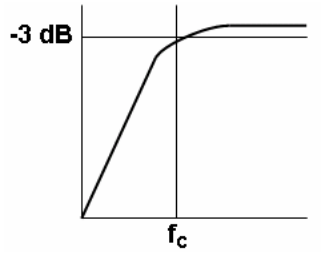


The -3dB frequency can be calculated using Equation 2. Use the Z_I values given in Table 1.

$$f = \frac{1}{2\pi Z_i C_i} \qquad \text{---------- (2)}$$

Input Capacitor, C_I

In the typical application, an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 3.



$$f_c = \frac{1}{2\pi Z_i C_i} \qquad \text{----------(3)}$$

The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_I is 50 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 3 is reconfigured as Equation 4.

$$C_i = \frac{1}{2\pi Z_i f_c} \qquad \text{----------(4)}$$

In this example, C_I is 0.16µF; so, one would likely choose a value of 0.22µF as this value is commonly used. If the gain is known and is constant, use Z_I from Table 1 to calculate C_I.

Power Supply Decoupling, C_S

The EUA2112 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF to 1µF placed as close as possible to the device VCC lead works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220µF or greater placed near the audio power amplifier is recommended. The 220µF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220µF or larger capacitor should be placed on each PVCC terminal. A 10µF capacitor on the AVCC terminal is adequate.

BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors, that require bootstrap capacitors for the high side of each output to turn on correctly. A 220nF~2.2uF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. (See application circuit diagram in Figure 17,18.)

The bootstrap capacitors connected between the BSx pins

and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

Using Low-ESR Capacitors

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance. For best performance over the extended temperature range, select X7R capacitors.

Output Filter

Most applications require a ferrite bead filter. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency (<1 MHz) EMI-sensitive circuits and/or there are long wires from the amplifier to the speaker.

When both an LC filter and a ferrite bead filter are used, the LC filter should be placed as close as possible to the IC followed by the ferrite bead filter.

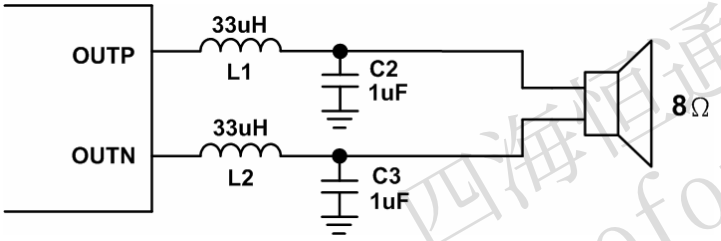


Figure19.

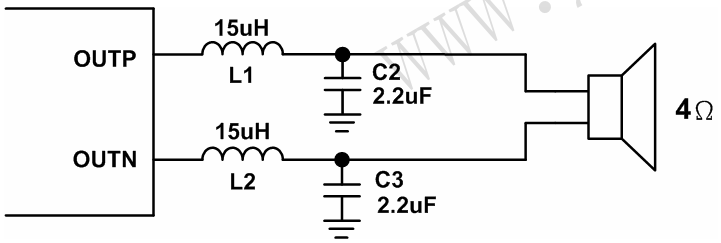


Figure20.

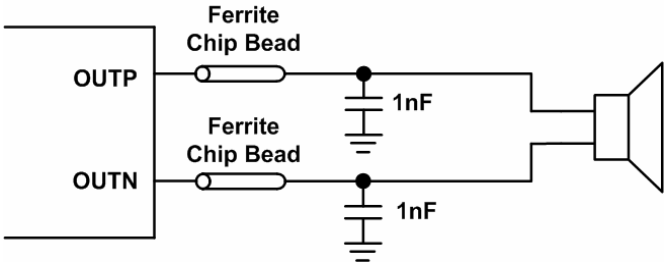
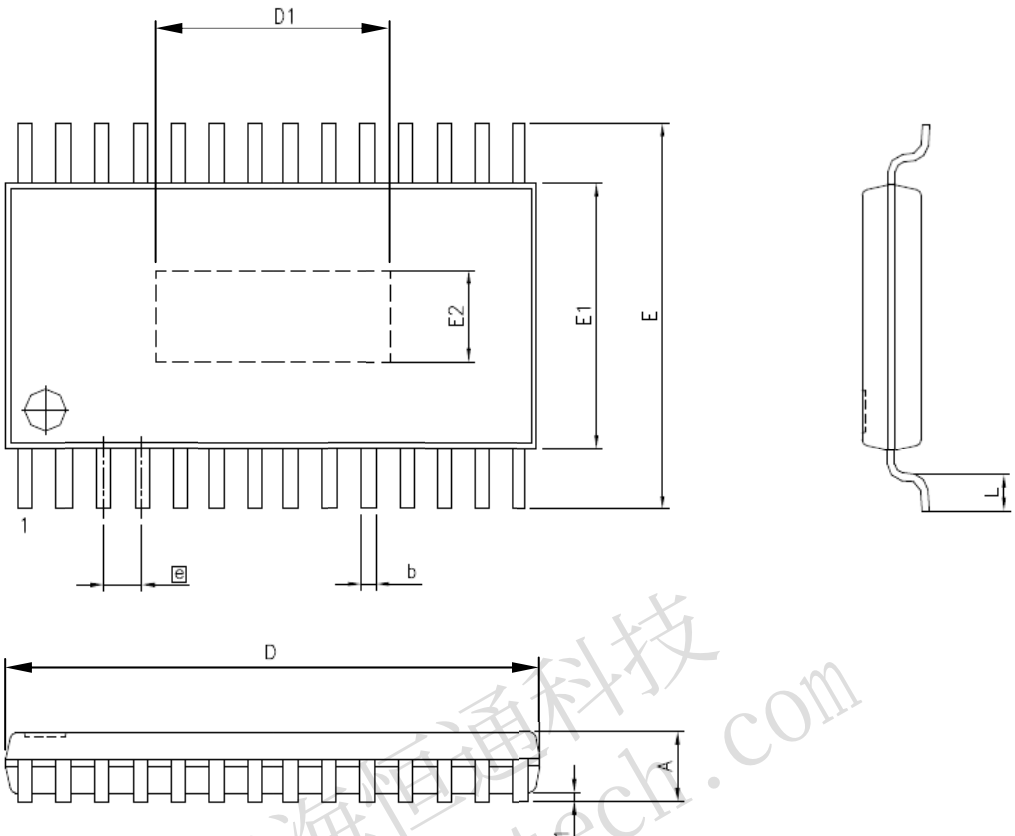


Figure21.

Package Information

TSSOP-28



	MILLIMETERS		INCHES	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	-	1.20	-	0.047
A1	0.00	0.15	0.000	0.006
b	0.19	0.30	0.007	0.012
E1	4.40		0.173	
D	9.60	9.80	0.378	0.386
D1	3.05	3.55	0.120	0.139
E	6.20	6.60	0.244	0.260
E2	2.62	3.12	0.103	0.122
e	0.65		0.026	
L	0.45	0.75	0.018	0.030