20-W Stereo Class-D Audio Power Amplifier

DESCRIPTION

The EUA2123 is a high efficient Class-D audio power amplifier for delivering up to 2×20W into a 4Ω stereo mode with a single-ended (SE) configuration or 1×40W into an 8Ω mono mode with a bridge-tied-load (BTL) configuration. The high efficiency of the EUA2123 eliminates the need for an external heat sink when playing music.

The gain of the amplifier is controlled by two gain select pins. The gain selections are 20, 26, 32, 36 dB. Short circuit and thermal-overload protection prevent the device from being damaged during a fault condition.

FEATURES

- 2×20W, THD=10% at 4Ω Load from a 24V Supply
- 2×10W, THD=10% at 8Ω Load from a 24V Supply
- 1×40W, THD=10% at 8Ω Load from a 24V Supply
- Operates from 10V to 30V
- Unique Modulation Scheme
- High Efficiency up to 90%
- Four Selectable Gain Settings
- Internal Oscillator
- Single-Ended Analog Inputs
- Mute and Shutdown Control
- Integrated On/Off /Mute Pop Suppression
- Thermal Protection with Auto Recovery
- Short-Circuit Latch-off Protection
- Space-Saving Surface-Mount 24-pin TSSOP Package
- RoHS compliant and 100% lead(Pb)-free

APPLICATIONS

- Televisions

Typical Application Circuit

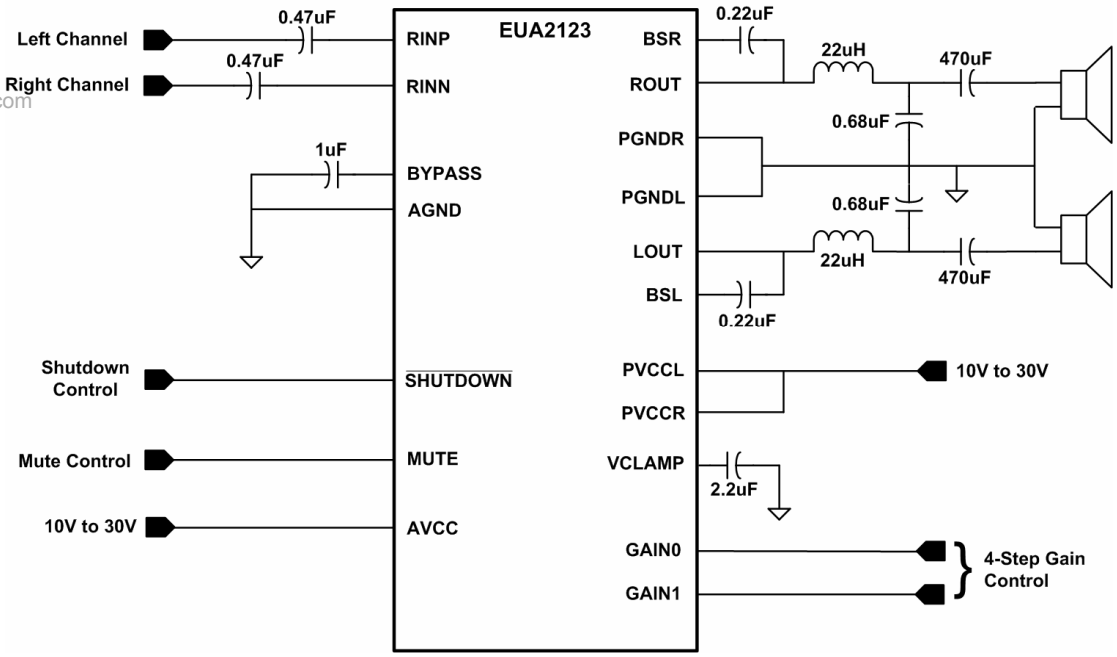
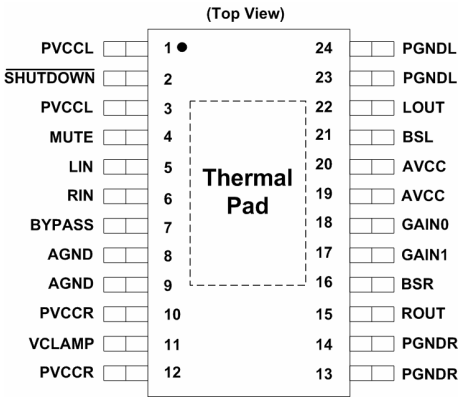


Figure1.

Pin Configurations

Package Type	Pin Configurations
TSSOP-24	

Pin Description

PIN	TSSOP-24	I/O/P	DESCRIPTION
PVCCL	1,3	P	Power supply for left-channel half-bridge, not internally connected to PVCCR or AVCC
$\overline{\text{SHUTDOWN}}$	2	I	Shutdown signal for IC (low = disabled, high = operational). TTL logic levels with compliance to AVCC
MUTE	4	I	Mute signal for quick disable/enable of outputs (high = outputs switch at 50% duty cycle, low =outputs enabled). TTL logic levels with compliance to AVCC
LIN	5	I	Audio input for left channel
RIN	6	I	Audio input for right channel
BYPASS	7	O	Reference for preamplifier inputs. Nominally equal to AVCC/12. Also controls start-up time via external capacitor sizing.
AGND	8	P	Analog ground for analog cells in core
AGND	9	P	Analog ground for digital/analog cells in core
PVCCR	10,12	P	Power supply for right-channel half-bridge, not connected to PVCCL or AVCC
VCLAMP	11	P	Internally generated voltage supply for bootstrap capacitors
PGNDR	13,14	P	Power ground for right-channel half-bridge.
ROUT	15	O	Class-D 1/2-H-bridge output for right channel
BSR	16	I/O	Bootstrap I/O for right channel
GAIN1	17	I	Gain select most-significant bit. TTL logic levels with compliance to AVCC
GAIN0	18	I	Gain select least-significant bit. TTL logic levels with compliance to AVCC
AVCC	19,20	P	High-voltage analog power supply. Not internally connected to PVCCR or PVCCL
BSL	21	I/O	Bootstrap I/O for left channel
LOUT	22	O	Class-D 1/2- half-bridge output for left channel
PGNDL	23,24	P	Power ground for left-channel half-bridge

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUA2123QIR1	TSSOP-24	xxxxx EUA2123	-40 °C to +85°C

EUA2123 □ □ □ □

- Lead Free Code
  1: Lead Free 0: Lead
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  Q:TSSOP

Block Diagram

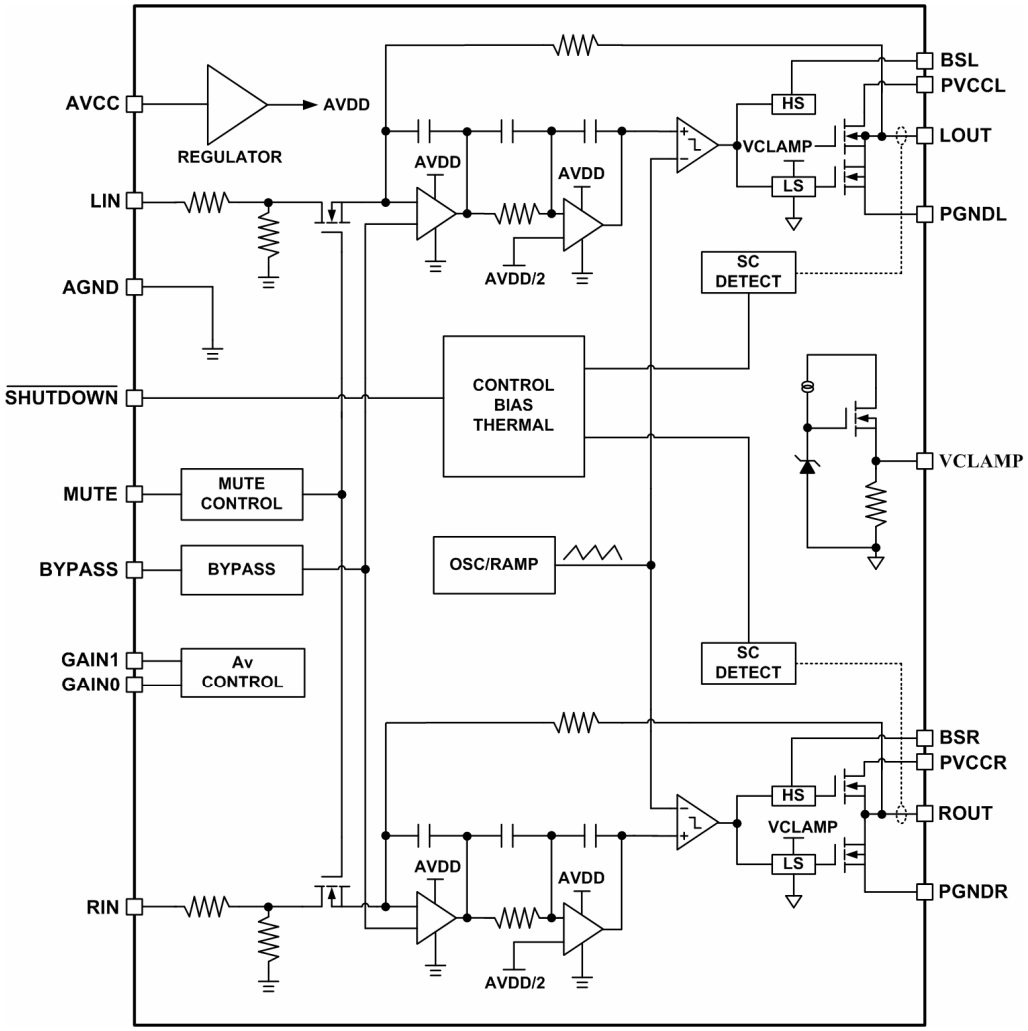


Figure2.

Absolute Maximum Ratings

- Supply Voltage, AVCC,PVCC ---------- -0.3 V to 36V
- Input Voltage, $\overline{\text{SHUTDOWN}}$,MUTE,GAIN0, GAIN1 ---------- -0.3 V to V_{CC} +0.3V
- Input Voltage, RIN, LIN ---------- -0.3 V to 7V
- Free-air Temperature Range, T_A ---------- -40°C to +85°C
- Junction Temperature Range, T_J ---------- -40°C to +150°C
- Storage Temperature Rang, T_{stg} ---------- -65°C to +150°C
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ---------- +260°C
- Load impedance, R_L ---------- 3.2Ω

Recommended Operating Conditions

		Min	Max	Unit
Supply voltage, V_{CC}	PVCC,AVCC	10	30	V
High-level input voltage, V_{IH}	$\overline{\text{SHUTDOWN}}$,MUTE,GAIN0,GAIN1	2		V
Low-level input voltage, V_{IL}	$\overline{\text{SHUTDOWN}}$,MUTE,GAIN0,GAIN1		0.8	V
High-level input current, I_{IH}	$\overline{\text{SHUTDOWN}}$,V_I=V_{CC},V_{CC}=30V		125	μA
	MUTE,V_I=V_{CC}, V_{CC}=30V		125	
	GAIN0,GAIN1, V_I= V_{CC}, V_{CC}=24V		125	
Low-level input current, I_{IL}	$\overline{\text{SHUTDOWN}}$,V_I=0V,V_{CC}=30V		1	μA
	MUTE,V_I=0V, V_{CC}=30V		1	
	GAIN0,GAIN1, V_I= 0V, V_{CC}=24V		1	
Operating free-air temperature, T_A		-40	85	°C

DC Characteristics T_A = +25°C ,V_{CC}= 24V, R_L=4Ω (Unless otherwise noted)

Symbol	Parameter	Conditions		EUA2123			Unit
				Min	Typ	Max	
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I= 0 V, Gain = 36 dB			7.5	50	mV
$V_{(BYPASS)}$	Bypass output voltage	No load			AVCC/ 12		V
ICC	Quiescent supply current	$\overline{\text{SHUTDOWN}}$ =2V, MUTE=0V, no load			27	37	mA
$ICC_{(SD)}$	Quiescent supply current in shutdown mode	$\overline{\text{SHUTDOWN}}$ =0.8V, no load			0.8	1.5	mA
$ICC_{(MUTE)}$	Quiescent supply current in mute mode	MUTE=0.8V, no load			27		mA
r_{DS}(on)	Drain-source on-state resistance				200		mΩ
G	Gain	GAIN1=0.8V	GAIN0=0.8V	18	20	22	dB
			GAIN0=2V	24	26	28	
		GAIN1=2V	GAIN0=0.8V	30	32	34	dB
			GAIN0=2V	34	36	38	
	Mute Attenuation	V_I=1 Vrms			-55		dB

AC Characteristics T_A = 25°C ,V_{CC}=24V, R_L=4Ω (Unless otherwise noted)

Symbol	Parameter	Conditions		EUA2123			Unit
				Min	Typ	Max	
K_{SVR}	Supply ripple rejection	V_{CC}=24V, V_{RIPPLE}=200 mV_{PP} Gain= 20dB	100Hz		-58		dB
			1kHz		-58		
P_O	Output power at 1% THD+N	V_{CC}=24V, R_L=4Ω, f=1kHz			15		W
		V_{CC}=24V, R_L=8Ω, f=1kHz			8		
	Output power at 10% THD+N	V_{CC}=24V, R_L=4Ω, f=1kHz			20		
		V_{CC}=24V, R_L=8Ω, f=1kHz			10		
THD+N	Total harmonic distortion +noise	R_L=4Ω, f=1 kHz, P_O=10W			0.8%		
		R_L=8Ω, f=1 kHz, P_O=5W			0.4%		
Vn	Output integrated noise floor	20Hz to 22kHz, A-weighted filter, Gain=20dB			130		μV
					-77.5		dBV
	Crosstalk	P_O=1 W, f=1 kHz ,Gain=20dB			-80		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N< 1%, f=1kHz,Gain=20dB,R_L=8Ω,P_O=5W			92		dB
	Thermal trip point				150		℃
	Thermal hysteresis				40		℃
fOSC	Oscillator frequency			220	250	280	kHz
△t	Mute delay	Time from mute input switches high until outputs muted			30		μsec
	Unmute delay	Time from mute input switches low until outputs unmuted			30		μsec

Typical Characteristics

TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY

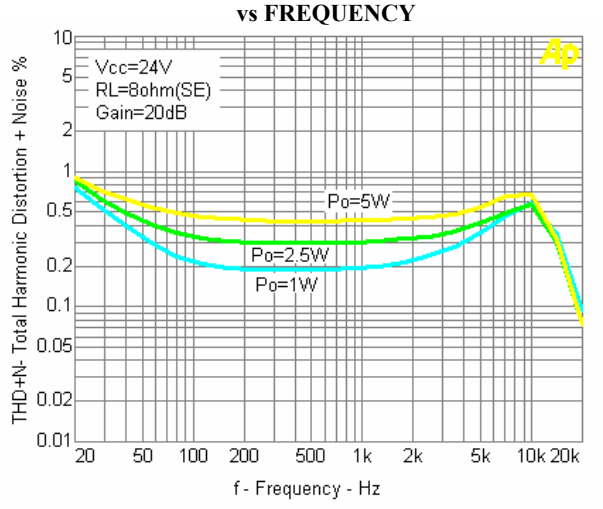


Figure3.

TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY

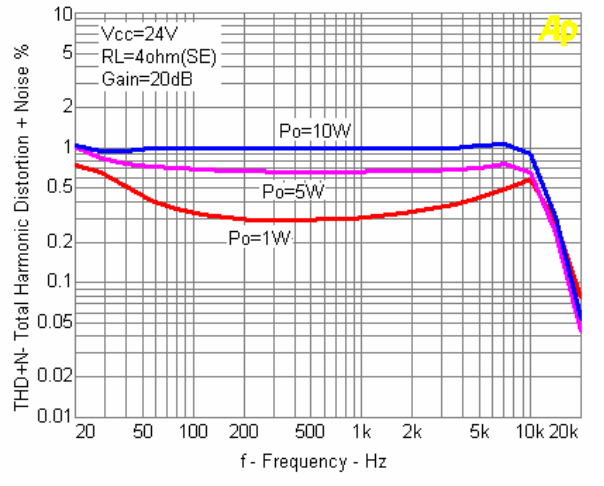


Figure4.

TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY

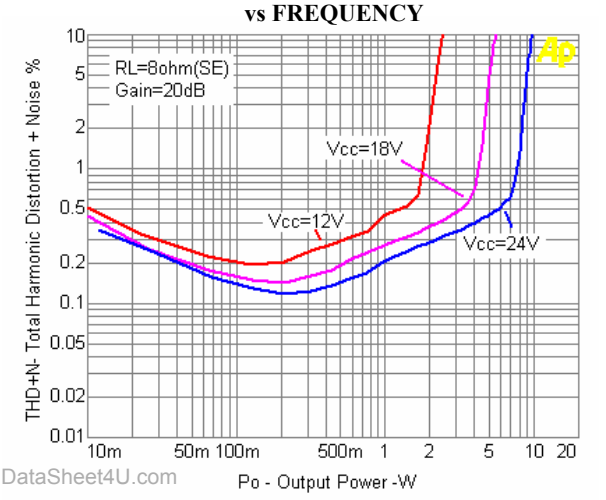


Figure5.

TOTAL HARMONIC DISTORTION+NOISE vs OUTPUT POWER

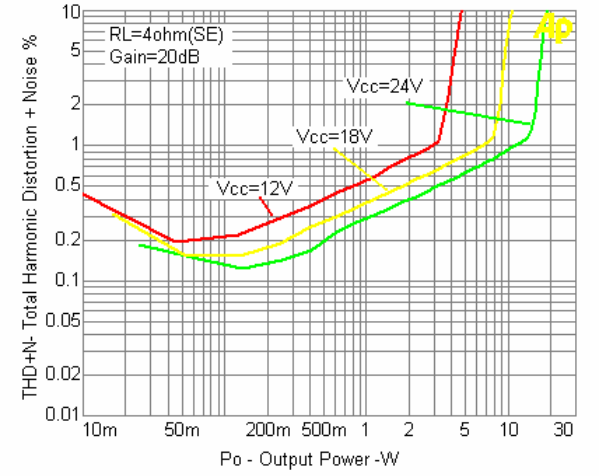


Figure6

CROSSTALK vs FREQUENCY

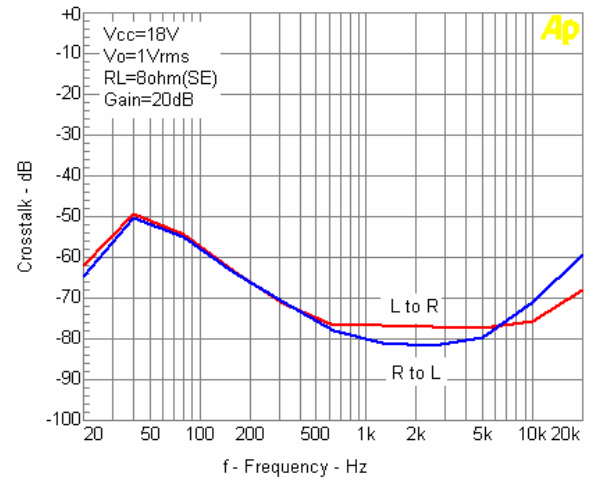


Figure7.

CROSSTALK vs FREQUENCY

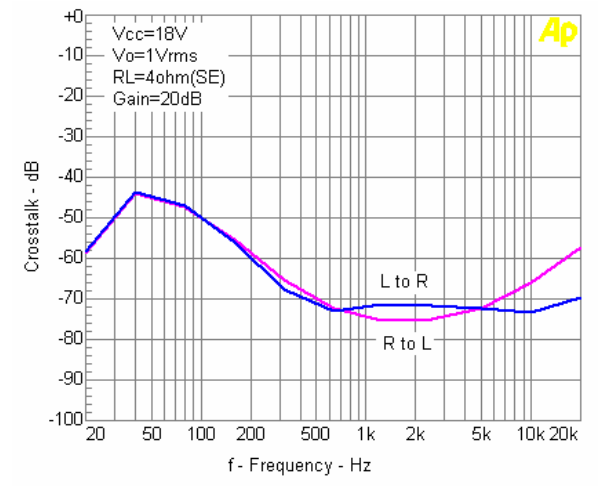


Figure8.

GAIN/PHASE vs FREQUENCY

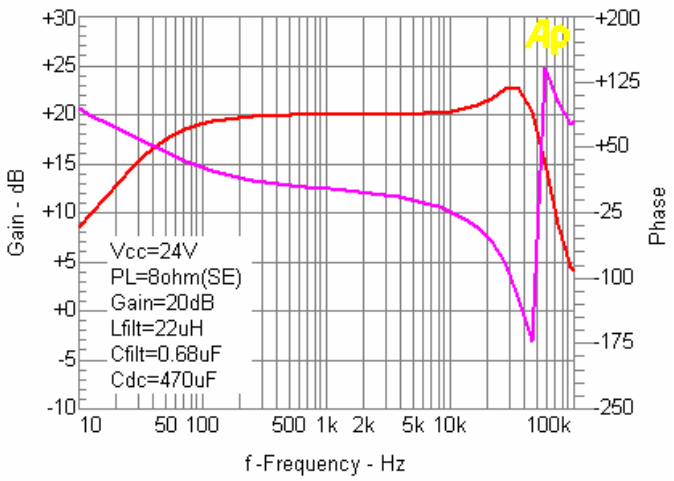


Figure9.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

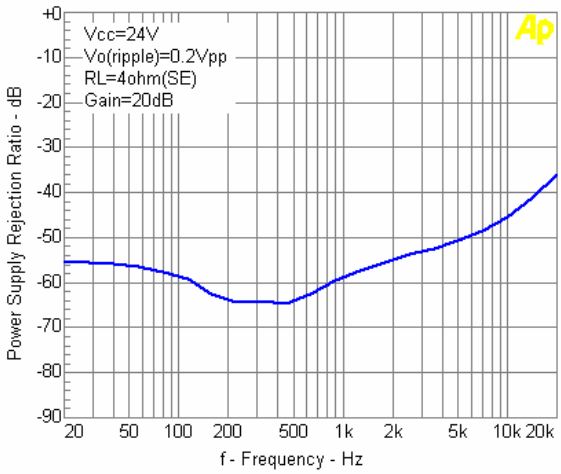


Figure10.

NOISE FLOOR vs FREQUENCY

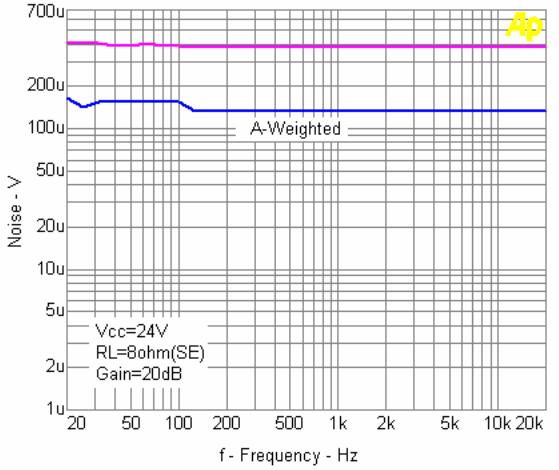


Figure11.

ATTENUATION

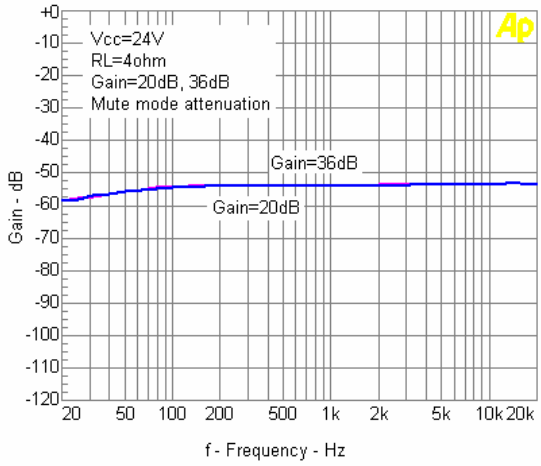


Figure12.

OUTPUT POWER vs SUPPLY VOLTAGE

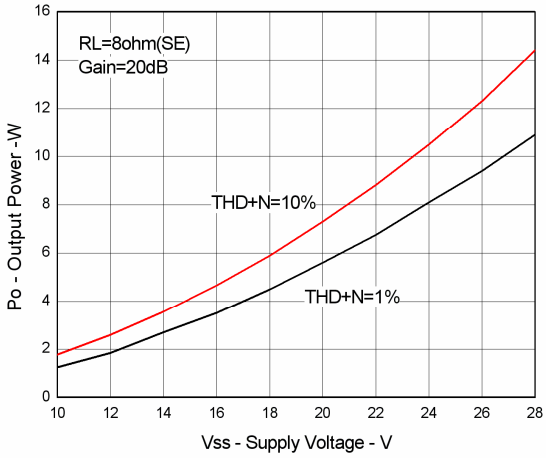


Figure13.

OUTPUT POWER vs SUPPLY VOLTAGE

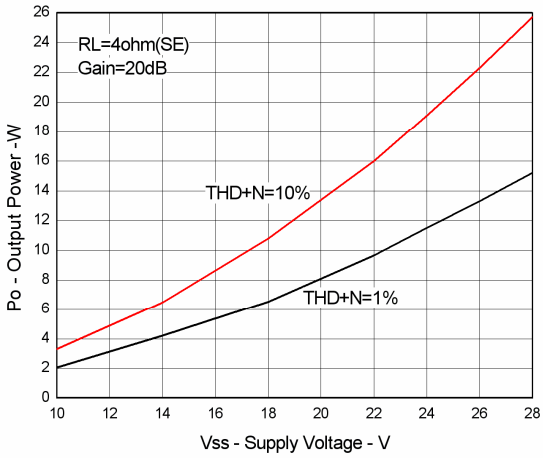


Figure14.

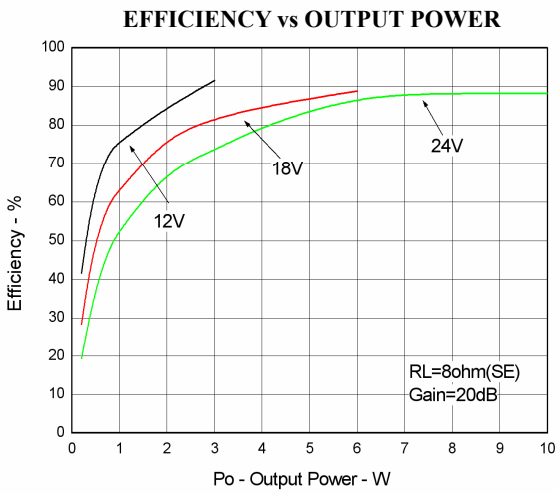


Figure15.

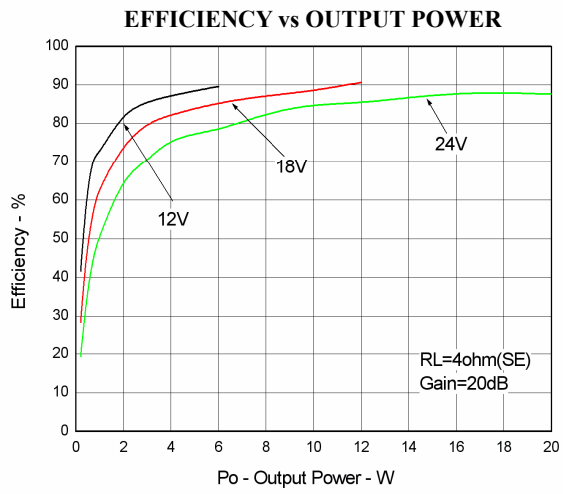


Figure16.

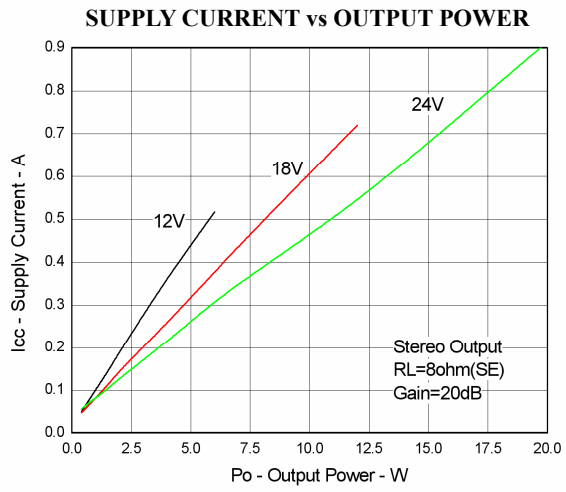


Figure17.

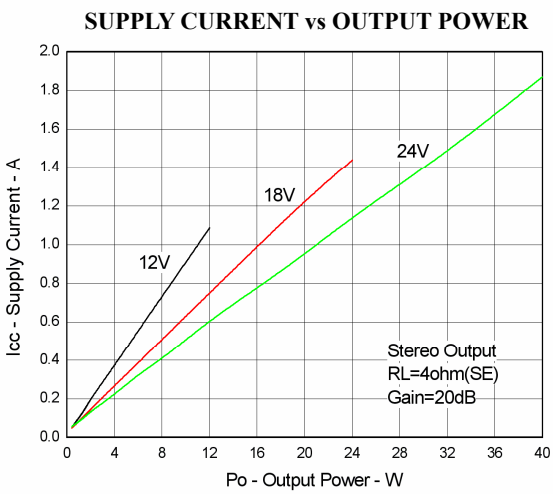


Figure18.

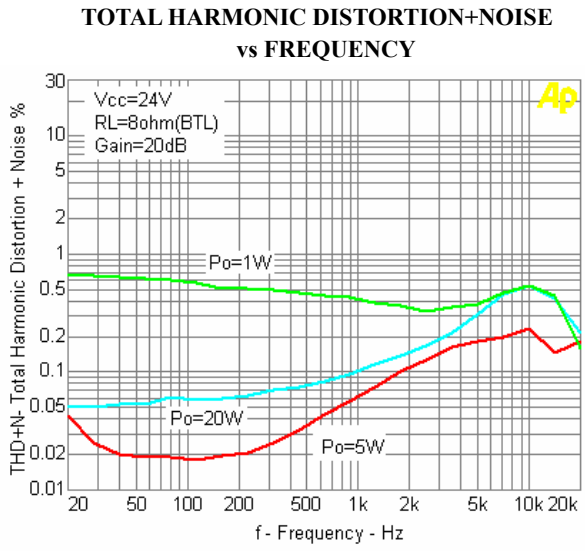


Figure19.

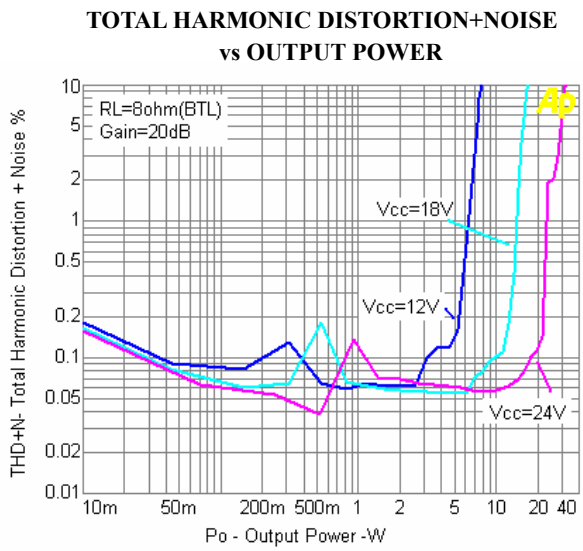


Figure20.

GAIN/PHASE vs FREQUENCY

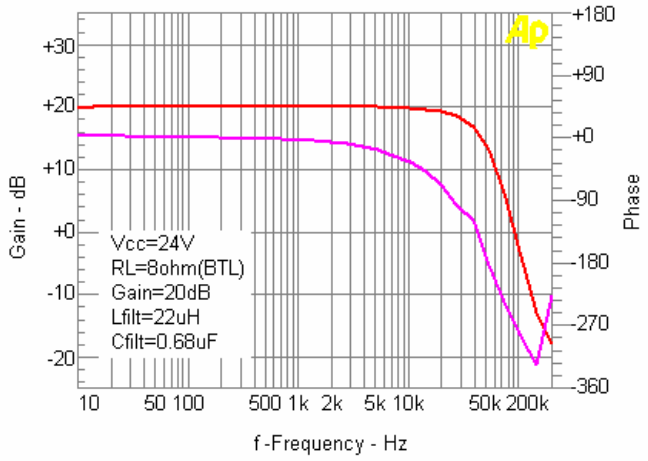


Figure21.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

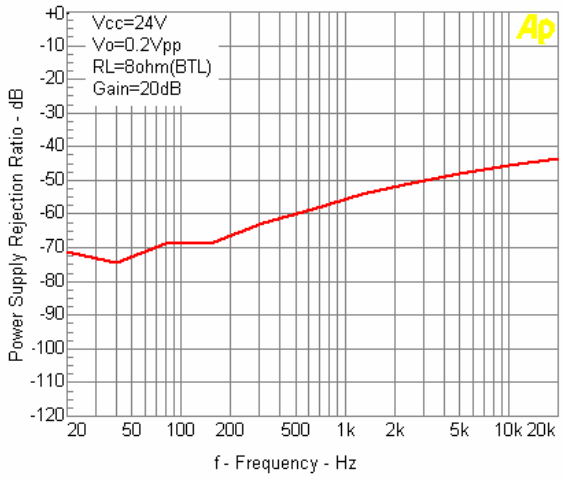


Figure22.

OUTPUT POWER vs SUPPLY VOLTAGE

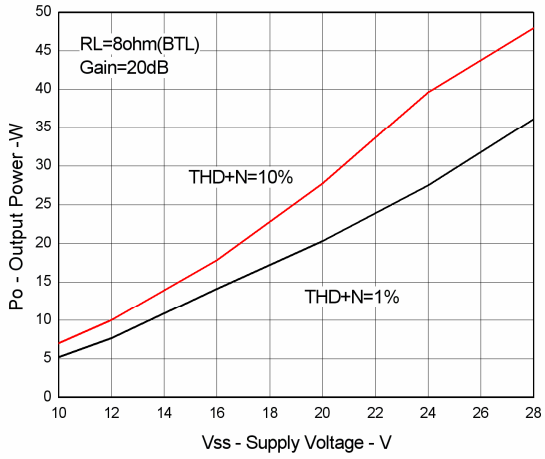


Figure23.

EFFICIENCY vs OUTPUT POWER

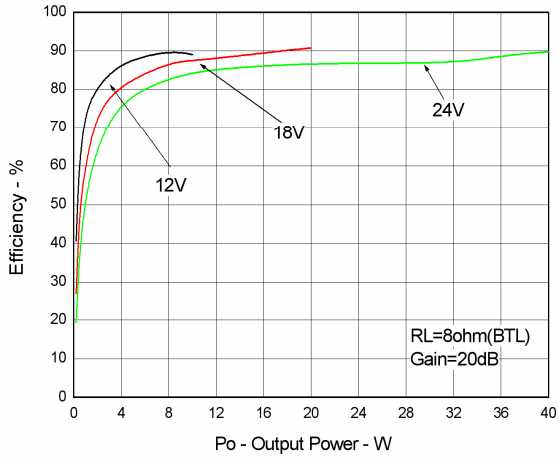


Figure24.

SUPPLY CURRENT vs OUTPUT POWER

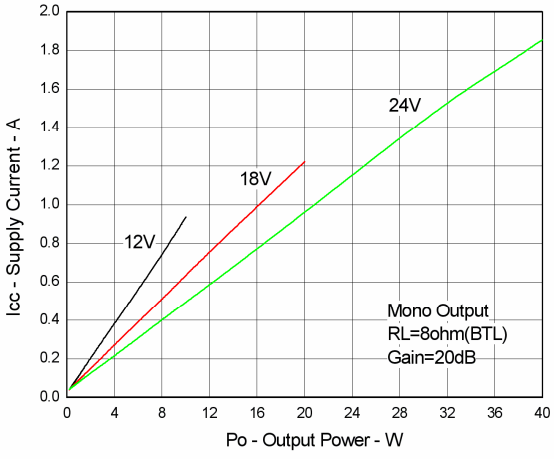


Figure25.

Application Information

Supply Pumping

Supply pumping occurs in single-ended class D amplifiers, and is caused by rapid switch transitions where current is pumped back into the supply line. This phenomenon is most evident at low audio frequencies and when both channels are operating at the same frequency and phase. At low levels, power-supply pumping results in distortion in the audio output due to fluctuations in supply voltage. At higher levels, pumping can cause the overvoltage protection to operate, which temporarily shuts down the audio output. The large capacitor is necessary to relieve power supply pumping. Also, improvement is realized by hooking other supplies to this node, thereby sinking some of the excess current. Power supply pumping should be tested by operating the amplifier at low frequencies and high output levels.

Gain Setting via GAIN0 and GAIN1 Inputs

The gain of the EUA2123 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 1 are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

Table.1 Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	20	240
0	1	26	120
1	0	32	60
1	1	36	36

$\overline{\text{SHUTDOWN}}$ Operation

Connect $\overline{\text{SHUTDOWN}}$ to a logic high for normal operation. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{\text{SHUTDOWN}}$ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown or mute mode prior to removing the power supply voltage.

MUTE Operation

The MUTE pin only control the output state and does not shutdown the EUA2123. A logic high on this terminal disables the outputs. A logic low on this pin enables the outputs. This terminal may be used as a quick disable/enable of outputs when changing channels on a television or transitioning between different audio sources. Do not leave MUTE terminal floating.

Short-Circuit Protection

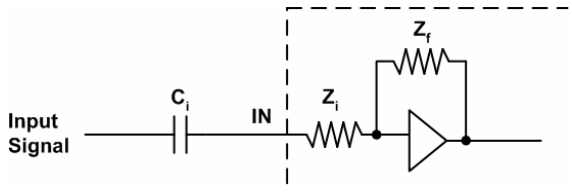
The EUA2123 has short-circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts and output-to-GND shorts after the filter and output capacitor (at the speaker terminal.) Directly at the device terminals, the protection circuitry prevents damage to device during output-to-output, output-to-ground, and output-to-supply. When a short circuit is detected on the outputs, the part immediately disables the output drive. This is an latched fault. Normal operation is restored when the fault is removed. The latched-off fault will be released when amplifier enter shutdown mode.

Thermal Protection

Thermal protection on the EUA2123 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 40°C. The device begins normal operation at this point with no external system interaction.

Input Resistance

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 36 kΩ ±20%, to the largest value, 240 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB cutoff frequency may change when changing gain steps.

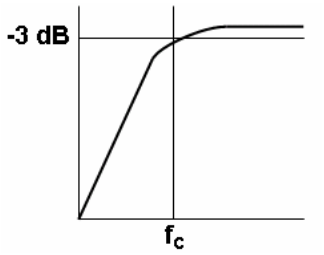


The -3 dB frequency can be calculated using Equation 1. Use Table 1 for Z_I values.

$$f = \frac{1}{2\pi Z_i C_i} \quad \text{---------- (1)}$$

Input Capacitor, C_I

In the typical application, an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 2.



$$f_c = \frac{1}{2\pi Z_i C_i} \quad \text{----------(2)}$$

The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_I is 36kΩ and the specification calls for a flat bass response down to 20Hz. Equation 2 is reconfigured as Equation 3.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad \text{----------(3)}$$

In this example, C_I is 0.22μF; so, one would likely choose a value of 0.47μF, as this value is commonly used. If the gain is known and is constant, use Z_I from Table 1 to calculate C_I. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at V_{BYP} (VCC/12), which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages, and it is important to ensure that boards are cleaned properly.

Single-Ended Output Capacitor, C_O

In single-ended (SE) applications, the dc blocking capacitor forms a high-pass filter with the speaker impedance. The frequency response rolls of with decreasing frequency at a rate of 20dB/decade. The cutoff frequency is determined by:

$$f_c = 1/2\pi C_O Z_L \quad \text{----------(4)}$$

Table 2 shows some common component values and the associated cutoff frequencies:

Table.2 Gain Setting

Speaker Impedance (Ω)	C_{SE}-DC Blocking Capacitor (μF)		
	f_c=60Hz (-3dB)	f_c=40Hz (-3dB)	f_c=20Hz (-3dB)
4	680	1000	2200
8	330	470	1000

Output Filter and Frequency Response

To get better frequency response, a flat-passband output filter (second-order Butterworth) may be used. The output filter components consist of the series inductor and capacitor to ground at the LOUT and ROUT pins. There are some possible combinations depending on the speaker impedance, and whether the output configuration is single ended (SE) or bridge-tied load (BTL). The values for the filter components are recommended in Table 3. It is important to use a high-quality capacitor in this application. A rating of at least X7R is required.

Table.3 Recommended Filter Output Components

Output Configuration	Speaker Impedance (Ω)	Filter Inductor (μH)	Filter Capacitor (nF)
Single Ended (SE)	4	22	680
	8	47	390
Bridge Tied Load (BTL)	4	10	1500
	8	22	680

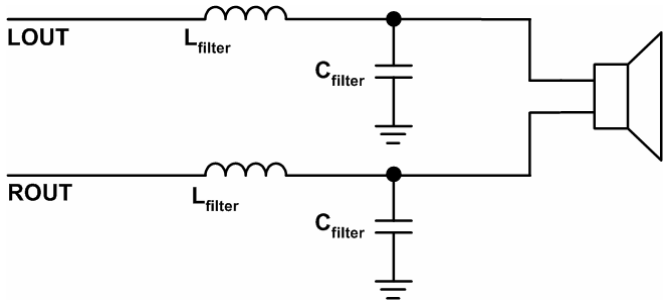


Figure 26. BTL Filter Configuration

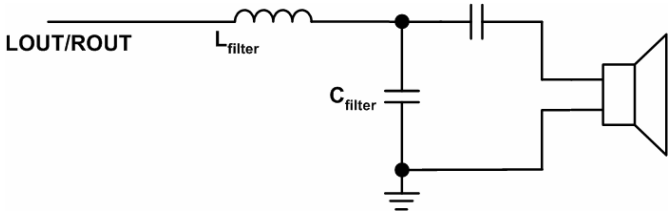


Figure 27. SE Filter Configuration

Power-Supply Decoupling, C_S

The EUA2123 is a high-performance CMOS audio amplifier that requires adequate power-supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power-supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power-supply leads.

For higher-frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF to 1μF, placed as close as possible to the device V_{CC} lead works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 470μF or greater placed near the audio power amplifier is recommended. The 470μF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 470μF or larger capacitor should be placed on each PVCC terminal. A 10μF capacitor on the AVCC terminal is adequate. These capacitors must be properly derated for voltage and ripple current rating to ensure reliability.

BSN and BSP Capacitors

The half H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220nF capacitor must be connected from LOUT to BSL, and one 220nF capacitor must be connected from ROUT to BSR. The bootstrap capacitors connected between the BSx pins and their corresponding outputs function as a floating power supply for the high-side N-channel power MOSFET gate-drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

VCLAMP Capacitor

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, one internal regulator clamps the gate voltage. One 2.2μF capacitor must be connected from VCLAMP (pin 11) to ground and must be rated for at least 16V. The voltages at the VCLAMP terminal may vary with V_{CC} and may not be used for powering any other circuitry.

VBYP Capacitor Selection

The scaled supply reference (VBYP) nominally provides an AVCC/12 internal bias for the preamplifier stages. The external capacitor for this reference (C_{BYP}) is a critical component and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts. The start up time is proportional to 0.12s per microfarad. Thus, the recommended 1μF capacitor results in a start-up time of approximately 120ms. The second function is to reduce noise produced by the power supply caused by coupling with the output drive signal. This noise could result in degraded power-supply rejection and THD+N.

The circuit is designed for a C_{BYP} value of 1μF for best pop performance. The input capacitors should have the same value. A ceramic or tantalum low-ESR capacitor is recommended.

Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

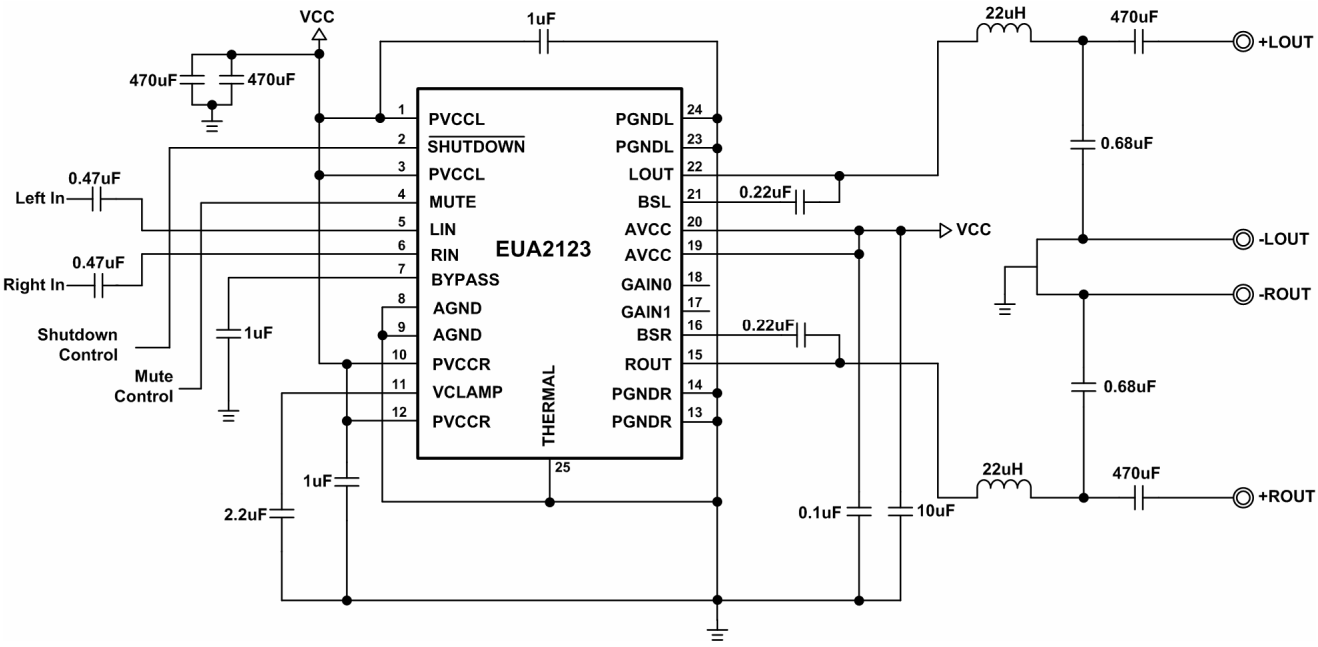


Figure 28. Schematic for Single Ended (SE)

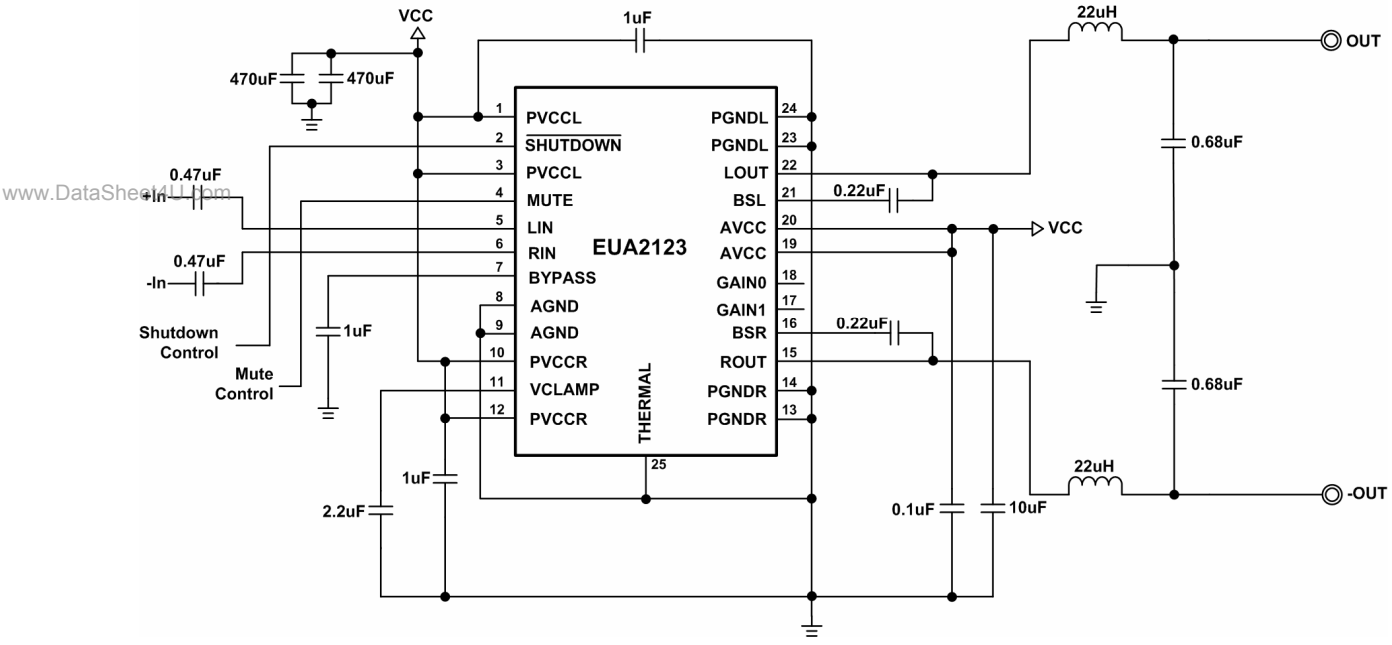
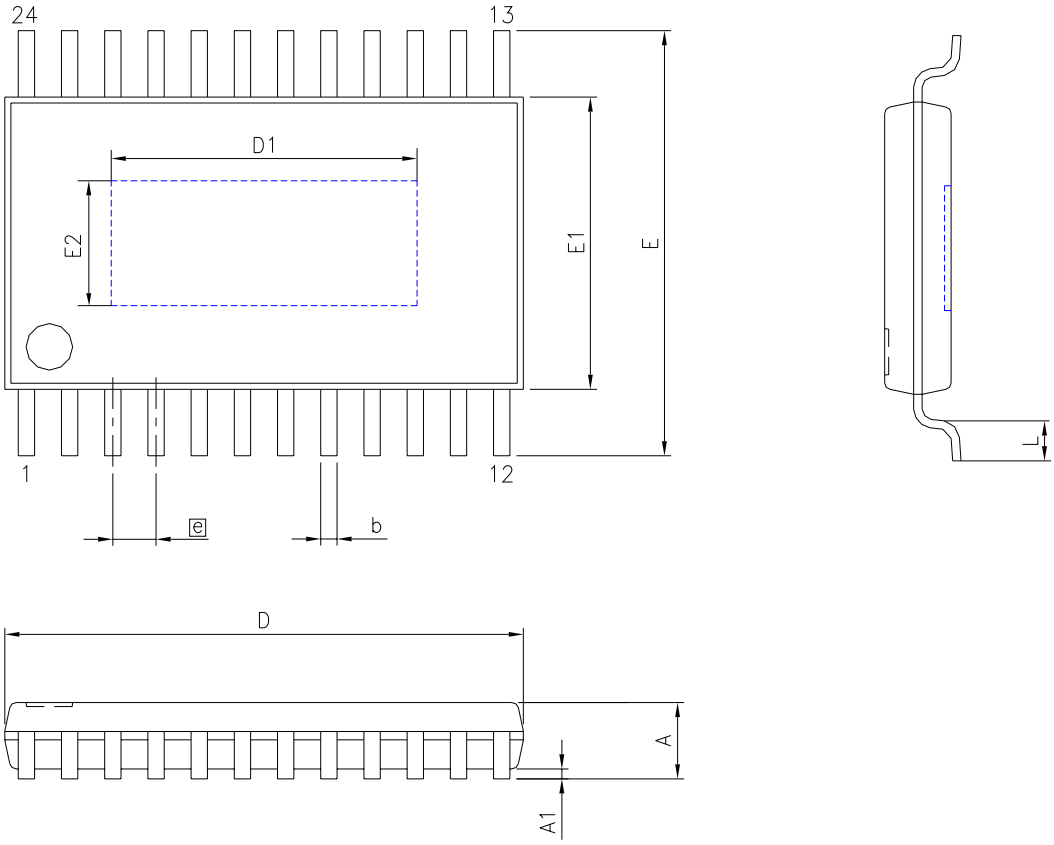


Figure 29. Schematic for Bridge Tied (BTL) Configuration

Package Information

TSSOP-24



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.20	-	0.047
A1	0.00	0.15	0.000	0.006
b	0.19	0.30	0.007	0.012
E1	4.40		0.173	
D	7.80		0.307	
D1	4.60		0.181	
E	6.20	6.60	0.244	0.260
E2	1.88		0.074	
e	0.65		0.026	
L	0.45	0.75	0.018	0.030