

## 2-W Stereo Audio Power Amplifier with Mute

### DESCRIPTION

The EUA5202 is a stereo audio power amplifier that delivering 2W of continuous RMS power per channel into 3-Ω loads. When driving 1W into 8-Ω speakers, the EUA5202 has less than 0.04% THD+N across its specified frequency range. Included within this device is integrated de-pop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 2 to 20 in BTL mode (1 to 10 in SE mode). An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line (often headphone drive) outputs are required to be SE, the EUA5202 automatically switches into SE mode when the SE/BTL inputs is activated. Consume only 7mA of supply current during normal operation, and the EUA5202 also features a shutdown function for power sensitive applications, holding the supply current at 1μA.

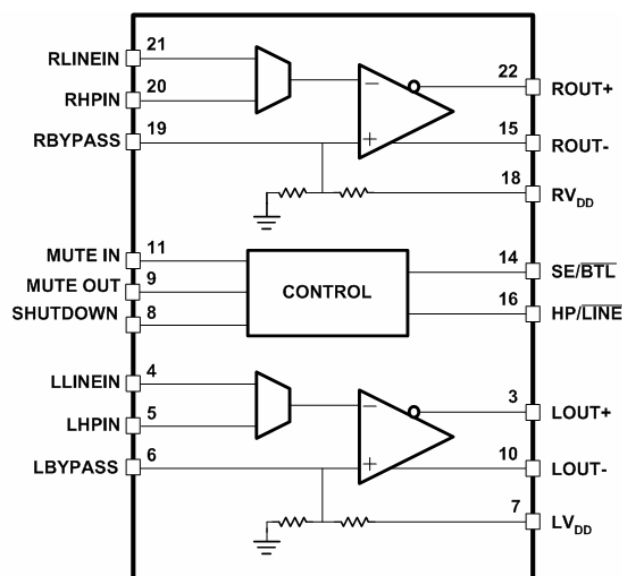
### FEATURES

- Output Power at 3Ω Load
  - 2W/ch at  $V_{DD}=5V$
  - 800mW/ch at 3V
- Low Supply Current and Shutdown Current
- Integrated Depop Circuit
- Mute and Shutdown Control Function
- Thermal Shutdown Protection
- Stereo Input MUX
- Bridge-Tied Load (BTL) or Single-Ended (SE) Modes.
- TSSOP-24 with Thermal Pad
- RoHS Compliant and 100% Lead (Pb)-Free

### APPLICATIONS

- Notebook Computers
- Multimedia Monitors
- Digital Radios and Portable TVs

### Block Diagram



Typical Application Circuit

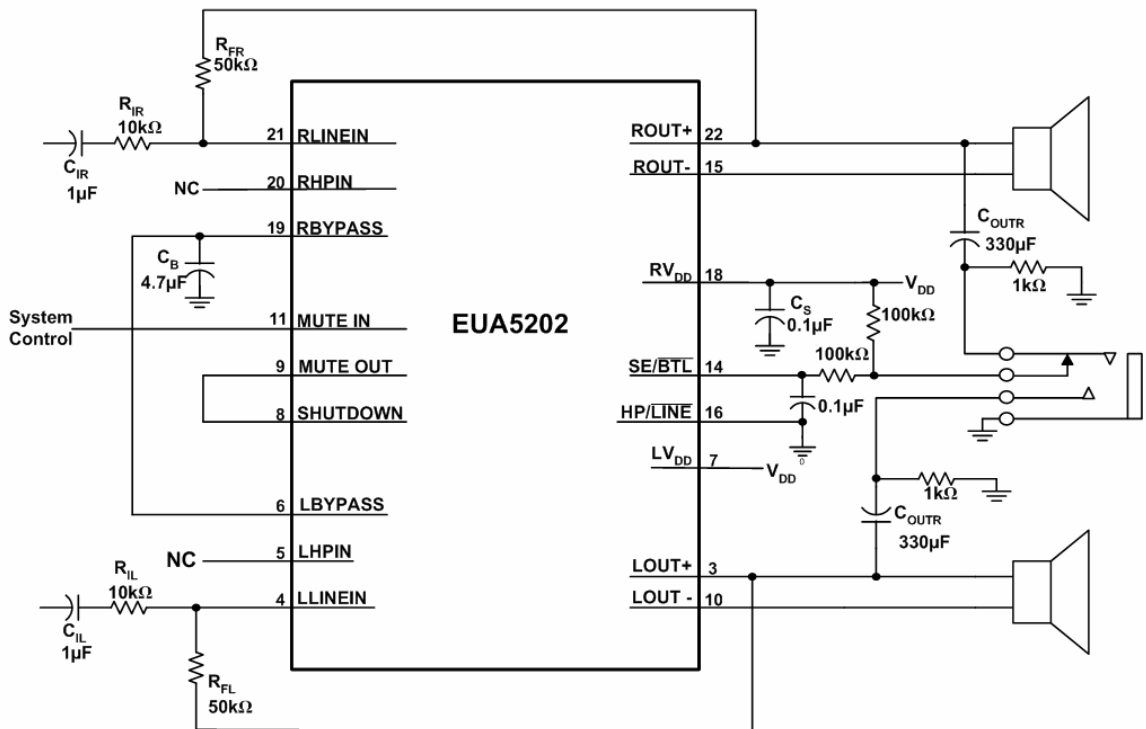


Figure 1. EUA5202 Minimum Configuration Application Circuit

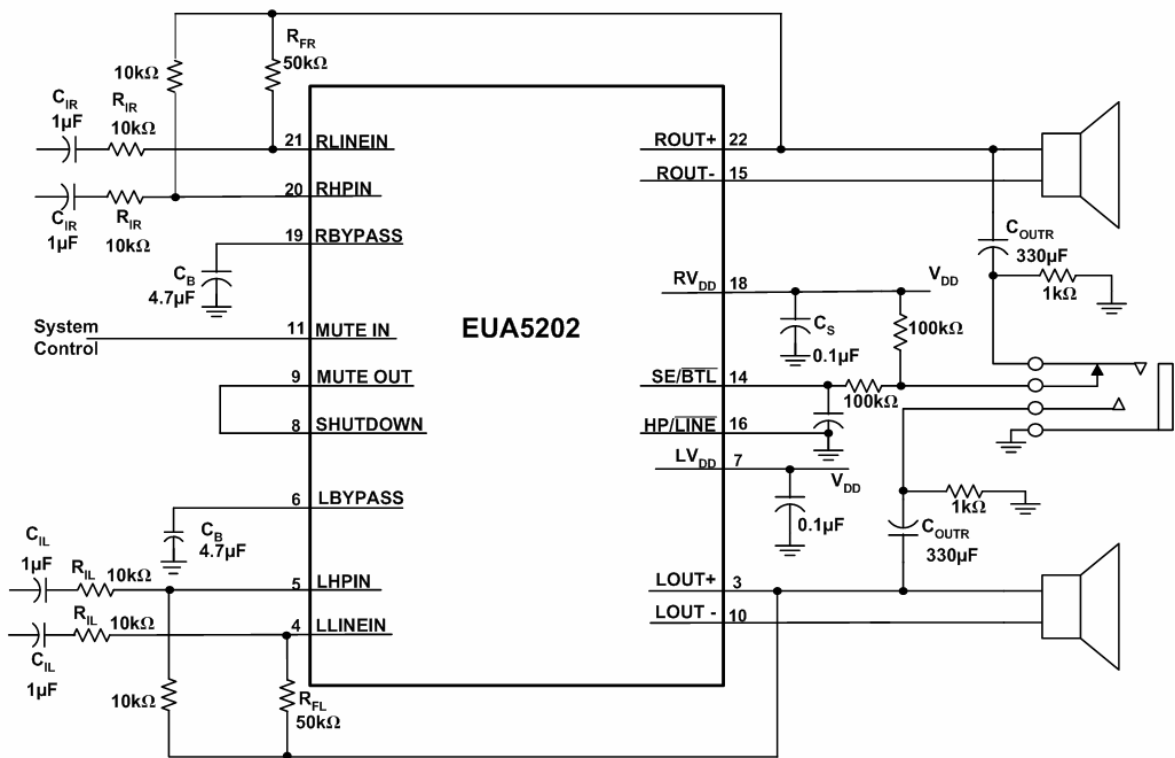


Figure 2. EUA5202 Full Configuration Application Circuit





## Pin Configurations

Package	Pin Configurations
TSSOP-24 with Thermal Pad, exposure on the bottom of the package	<p>Pin 1: GND/HS</p> <p>Pin 2: T<sub>J</sub></p> <p>Pin 3: LOUT+</p> <p>Pin 4: LLINEIN</p> <p>Pin 5: LHPIN</p> <p>Pin 6: LBYPASS</p> <p>Pin 7: LV<sub>DD</sub></p> <p>Pin 8: SHUTDOWN</p> <p>Pin 9: MUTE OUT</p> <p>Pin 10: LOUT-</p> <p>Pin 11: MUTE IN</p> <p>Pin 12: GND/HS</p> <p>Pin 13: GND/HS</p> <p>Pin 14: SE/BTL</p> <p>Pin 15: ROUT-</p> <p>Pin 16: HP/LINE</p> <p>Pin 17: NC</p> <p>Pin 18: RV<sub>DD</sub></p> <p>Pin 19: RBYPASS</p> <p>Pin 20: RHPIN</p> <p>Pin 21: RLINEIN</p> <p>Pin 22: ROUT+</p> <p>Pin 23: NC</p> <p>Pin 24: GND/HS</p>

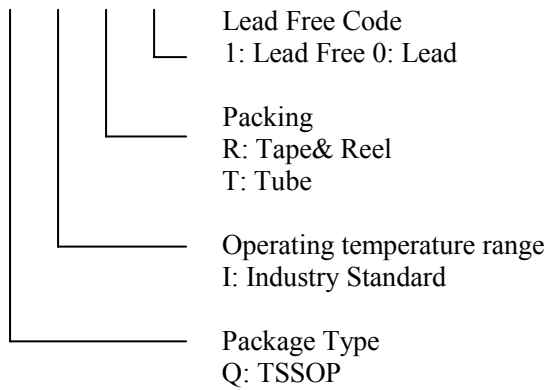
## Pin Description

PIN	PIN	I/O	DESCRIPTION
HP/LINE	16	I	Input MUX control input, hold high to select LHP IN or RHP IN (5, 20), hold low to select LLINE IN or RLINE IN (4, 21)
LBYPASS	6		Tap to voltage divider for left channel internal mid-supply bias
LHPIN	5	I	Left channel headphone input, selected when HP/LINE terminal (16) is held high
LLINE IN	4	I	Left channel line input, selected when HP/LINE terminal (16) is held low
LOUT+	3	O	Left channel + output in BTL mode, + output in SE mode
LOUT-	10	O	Left channel - output in BTL mode, high-impedance state in SE mode
GND/HS	1,12,13,24		Ground connection for circuitry, directly connected to thermal pad
LV <sub>DD</sub>	7	I	Supply voltage input for left channel and for primary bias circuits
MUTE IN	11	I	Mute all amplifiers, hold low for normal operation, hold high to mute
MUTE OUT	9	O	Follows MUTE IN terminal (11), provides buffered output
NC	17,23		No internal connection
RBYPASS	19		Tap to voltage divider for right channel internal mid-supply bias
RHPIN	20	I	Right channel headphone input, selected when HP/LINE terminal (16) is held high
RLINEIN	21	I	Right channel line input, selected when HP/LINE terminal (16) is held low
ROUT+	22	O	Right channel + output in BTL mode, + output in SE mode
ROUT-	15	O	Right channel - output in BTL mode, high-impedance state in SE mode
RV <sub>DD</sub>	18	I	Supply voltage input for high channel
SE/BTL	14	I	Hold low for BTL mod, hold high for SE mode
SHUTDOWN	8	I	Places entire IC in shutdown mode when held high, I <sub>DD</sub> =5μA
T <sub>J</sub>	2	O	Sources a current proportional to the junction temperature. This terminal should be left unconnected during normal operation.

**Ordering Information**

Order Number	Package Type	Marking	Operating Temperature range
EUA5202QIR1	TSSOP 24	 xxxx EUA5202	-40°C to 85°C
EUA5202QIR0	TSSOP 24	 xxxx EUA5202	-40°C to 85°C
EUA5202QIT1	TSSOP 24	 xxxx EUA5202	-40°C to 85°C
EUA5202QIT0	TSSOP 24	 xxxx EUA5202	-40°C to 85°C

EUA5202



**Absolute Maximum Ratings**

- Supply voltage,  $V_{DD}$ ----- 6V
- Input voltage,  $V_I$ ----- -0.3V to  $V_{DD}+0.3V$
- Continuous total power dissipation----- internally limited
- Operating free-air temperature range,  $T_A$  ----- -40°C to 85°C
- Operating junction temperature range,  $T_J$  ----- -40°C to 150°C
- Storage temperature range,  $T_{stg}$  ----- -65°C to 150°C
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds----- 260°C

**Recommended Operating Conditions**

		MIN	NOM	MAX	UNIT
Supply Voltage, $V_{DD}$		3	5	5.5	V
Operating free-air temperature, $T_A$	$V_{DD} = 5V$ , 250m W/Ch average power, 4-Ω stereo BTL drive, with proper PCB design	-40		85	°C
	$V_{DD} = 5V$ , 2 W/Ch average power, 3-Ω stereo BTL drive, with proper PCB design and 300 CFM forced-air cooling	-40		85	
Common mode input voltage, $V_{ICM}$	$V_{DD} = 5V$	1.25		4.5	V
	$V_{DD} = 3.3V$	1.25		2.7	

**DC Electrical Characteristics,  $T_A=25^\circ C$**

Symbol	Parameter	Conditions	EUA5202			Unit
			Min.	Typ	Max.	
$I_{DD}$	Supply Current	$V_{DD}=5V$	Stereo BTL	7.1	11	mA
			Stereo SE	3.9	6	mA
		$V_{DD}=3.3V$	Stereo BTL	5.7	9	mA
			Stereo SE	3.1	5	mA
$V_{OO}$	Output Offset Voltage (measured differentially)	$V_{DD}=5V$ , Gain=2		5	25	mV
$I_{DD(Mute)}$	Supply Current in Mute Mode	$V_{DD}=5V$		1.55		mA
$I_{DD(SD)}$	$I_{DD}$ in Shutdown	$V_{DD}=5V$		1	5	μA

**Typical Ac Operating Characteristics,  $V_{DD}=5V$ ,  $T_A=25^\circ C$ ,  $R_L=3\Omega$** 

Symbol	Parameter	Conditions	Typ.	Unit
$P_O$	Output Power(each channel) <sup>*1</sup>	THD=0.2%, BTL, See Figure 3	2	W
		THD=1%, BTL, See Figure 3	2.2	
THD+N	Total Harmonic Distortion Plus Noise	$P_O=2W$ , $f=1KHz$ , See Figure5	200	m%
		$V_I=1V$ , $R_L=10k\Omega$ , $A_V=1V/V$	100	m%
$B_{OM}$	Maximum Output Power Bandwidth	$A_V=10V/V$ THD <1%, See Figure5	>20	KHz
	Supply Ripple Rejection Ratio	$f=1KHz$ , See Figure37	65	dB
		$f=20-20KHz$ , See Figure37	40	
	Mute Attenuation		85	dB
	Channel-to- Channel Output Separation	$f=1KHz$ , See Figure 39	85	dB
	Line/HP Input Separation		88	dB
	BTL Attenuation in SE Mode		86	dB
$Z_I$	Input Impedance		2	M $\Omega$
	Signal-to-Noise Ratio	$P_O=2W$ , BTL, 5V	101	dB
$V_N$	Output Noise Voltage	See Figure 35	22	$\mu V$ (rms)

\*1: Output Power is measured at the output terminals of the IC at 1 KHz

**Typical Ac Operating Characteristics,  $V_{DD}=3.3V$ ,  $T_A=25^\circ C$ ,  $R_L=3\Omega$** 

Symbol	Parameter	Conditions	Typ.	Unit
$P_O$	Output Power(each channel) <sup>*1</sup>	THD=0.2%, BTL, See Figure 10	800	W
		THD=1%, BTL, See Figure 10	900	
THD+N	Total Harmonic Distortion Plus Noise	$P_O=2W$ , $f=1KHz$ , See Figure11	350	m%
		$V_I=1V$ , $R_L=10k\Omega$ , $A_V=1V/V$	200	m%
$B_{OM}$	Maximum Output Power Bandwidth	$A_V=10V/V$ THD <1%, See Figure11	>20	KHz
	Supply Ripple Rejection Ratio	$f=1KHz$ , See Figure37	60	dB
		$f=20-20KHz$ , See Figure37	40	
	Mute Attenuation		85	dB
	Channel-to- Channel Output Separation	$f=1KHz$ , See Figure 40	80	dB
	Line/HP Input Separation		88	dB
	BTL Attenuation in SE Mode		86	dB
$Z_I$	Input Impedance		2	M $\Omega$
	Signal - to - Noise Ratio	$P_O=700mW$ , BTL, 5V	96	dB
$V_N$	Output Noise Voltage	See Figure 36	22	$\mu V$ (rms)

\*1: Output Power is measured at the output terminals of the IC at 1 KHz

## Typical Operating Characteristics

(Table of Graphs)

No	Item	Conditions	Figure	Page
1	THD+N vs. Output Power	VDD=5V , RL=3 & 8 ohm , BTL , f=1KHz	3	9
2	THD+N vs. Frequency	VDD=5V , RL=4 ohm , BTL , Po=1.5W f=20 to 20KHz , Av= -2 & -10 & -20V/V	4	9
3	THD+N vs. Frequency	VDD=5V , RL=3 & 4 ohm , BTL , Po=1.5W , f=20 to 20KHz	5	9
4	THD+N vs. Output Power	VDD=5V , RL=3 ohm , BTL , f=20 & 1K & 20KHz	6	9
5	THD+N vs. Frequency	VDD=5V , RL=8 ohm , BTL , f=20 to 20KHz , Av=-2V/V	7	9
6	THD+N vs. Output Power	VDD=5V , RL=8 ohm , BTL , Po=1W , Av= -2 & -10 & -20V/V , f=20 to 20KHz	8	9
7	THD+N vs. Output Power	VDD=5V , RL=8 ohm , BTL , f=20 & 1K & 20KHz	9	10
8	THD+N vs. Output Power	VDD=3.3V , RL=3 & 8 ohm , BTL , f=1KHz	10	10
9	THD+N vs. Frequency	VDD=3.3V , RL=4 ohm , BTL , Po=0.75W , Av= -2 & -10 & -20V/V , f=20 to 20KHz	11	10
10	THD+N vs. Frequency	VDD=3.3V , RL=4 ohm , BTL , Av=-2V/V , Po=0.1 & 0.35 & 0.75W & 800mW(RL=3 ohm)	12	10
11	THD+N vs. Output Power	VDD=3.3V , RL=3 ohm , BTL , Av=-2V/V , f=20 & 1K & 20KHz	13	10
12	THD+N vs. Frequency	VDD=3.3V , RL=8 ohm , BTL , Po=0.4W , Av=-2 & -10 & -20V/V	14	10
13	THD+N vs. Frequency	VDD=3.3V , RL=8 ohm , BTL , Av=-2V/V , Po=0.1 & 0.25 & 0.4W	15	11
14	THD+N vs. Output Power	VDD=3.3V , RL=8 ohm , BTL , Av= -2V/V , f=20 & 1K & 20KHz	16	11
15	THD+N vs. Frequency	VDD=5V , RL=4 ohm , SE , Po=0.5W , Av= -1&-5&-10V/V	17	11
16	THD+N vs. Frequency	VDD=5V , RL=4 ohm , SE , Av= -2V/V , Po=0.1 & 0.25 & 0.5W	18	11
17	THD+N vs. Output Power	VDD=5V , RL=4 ohm , SE , Av= -2V/V , f=100 & 1K & 20KHz	19	11
18	THD+N vs. Frequency	VDD=5V , RL=8 ohm , SE , Po=0.25W , Av= -1 & -5 & -10V/V	20	11
19	THD+N vs. Frequency	VDD=5V , RL=8 ohm , SE , Av= -2V/V , Po=0.05 & 0.1 & 0.25W	21	12
20	THD+N vs. Output Power	VDD=5V , RL=8 ohm , SE , Av= -2V/V , f=100 & 1K & 20KHz	22	12
21	THD+N vs. Frequency	VDD=5V , RL=32 ohm , SE , Po=0.075W , Av= -1 & -5 & -10V/V	23	12
22	THD+N vs. Frequency	VDD=5V , RL=32 ohm , SE , Av= -1V/V , Po=25 & 50 & 75mW	24	12
23	THD+N vs. Output Power	VDD=5V , RL=32 ohm , SE , Av= -1V/V , f=20 & 1K & 20KHz	25	12
24	THD+N vs. Frequency	VDD=3.3V , RL=4 ohm , SE , Po=0.2W , Av= -1 & -5 & -10V/V	26	12
25	THD+N vs. Frequency	VDD=3.3V , RL=4 ohm , SE , Av= -1V/V , Po=0.05 & 0.1 & 0.2W	27	13
26	THD+N vs. Output Power	VDD=3.3V , RL=4 ohm , SE , Av= -2V/V , f=100 & 1K & 20KHz	28	13
27	THD+N vs. Frequency	VDD=3.3V , RL=8 ohm , SE , Po=100mW , Av= -1 & -5 & -10V/V	29	13
28	THD+N vs. Frequency	VDD=3.3V , RL=8 ohm , SE , Av= -1V/V , Po=25 & 50 & 100mW	30	13
29	THD+N vs. Output Power	VDD=3.3V , RL=8 ohm , SE , Av= -1V/V , f=100 & 1K & 20KHz	31	13
30	THD+N vs. Frequency	VDD=3.3V , RL=32 ohm , SE , Po=30mW , Av= -1 & -5 & -10V/V	32	13
31	THD+N vs. Frequency	VDD=3.3V , RL=32 ohm , SE , Av= -1V/V , Po=10 & 20 & 30mW	33	14
32	THD+N vs. Output Power	VDD=3.3V , RL=32 ohm , SE , Av=-1V/V , f=20 & 1K & 20KHz	34	14
33	Output Noise Voltage vs. Frequency	VDD=5V , BW=22Hz to 22kHz , RL=4	35	14

34	Output Noise Voltage vs. Frequency	VDD=3.3V , BW=22Hz to 22kHz , RL=4	36	14
35	Supply Ripple Rejection Ratio vs. Frequency	RL=4 ohm , CB=4.7uF , BTL , VDD=3.3 & 5V	37	14
36	Supply Ripple Rejection Ratio vs. Frequency	RL=4 ohm , CB=4.7uF , SE , VDD=3.3 & 5V	38	14
37	Crosstalk vs .Frequency	VDD=5V , Po=1.5W , RL=4 ohm , BTL , Right to Left & Left to Right	39	15
38	Crosstalk vs .Frequency	VDD=3.3V , Po=0.75W , RL=4 ohm , BTL , Right to Left & Left to Right	40	15
39	Crosstalk vs .Frequency	VDD=5V , Po=75mW , RL=32 ohm , SE , Right to Left & Left to Right	41	15
40	Crosstalk vs .Frequency	VDD=3.3V , Po=35mW , RL=32 ohm , SE , Right to Left & Left to Right	42	15
41	Closed Loop Response	VDD=5V , Av=-2V/V , Po=1.5W , BTL , Gain & Phase	43	15
42	Closed Loop Response	VDD=3.3V , Av= -2V/V , Po=0.75W , BTL , Gain &Phase	44	15
43	Closed Loop Response	VDD=5V , Av=-1V/V , Po=0.5W , SE , Gain &Phase	45	16
44	Closed Loop Response	VDD=3.3V , Av= -1V/V , Po=0.25W , SE , Gain &Phase	46	16
45	Supply Current vs. Supply Voltage	Stereo BTL & Stereo SE	47	16
46	Output Power vs. Supply Voltage	THD+N=1% , BTL , Each Channel , RL=3 & 4 & 8 ohm	48	16
47	Output Power vs. Supply Voltage	THD+N=1% , SE , Each Channel , RL=3 & 4 & 8 ohm	49	16
48	Output Power vs. Load Resistance	THD+N=1% , BTL , Each Channel , VDD=3.3 & 5V	50	16
49	Output Power vs. Load Resistance	THD+N=1% , SE , Each Channel , VDD=3.3 & 5V	51	17
50	Power Dissipation vs. Output Power	VDD=5V , BTL , Each Channel , RL=3 & 4 & 8ohm	52	17
51	Power Dissipation vs. Output Power	VDD=3.3V , BTL , Each Channel , RL=3 & 4 & 8ohm	53	17
52	Power Dissipation vs. Output Power	VDD=5V , SE , Each Channel , RL=4 & 8 & 32 ohm	54	17
53	Power Dissipation vs. Output Power	VDD=3.3V , SE , Each Channel , RL=4 & 8 & 32 ohm	55	17



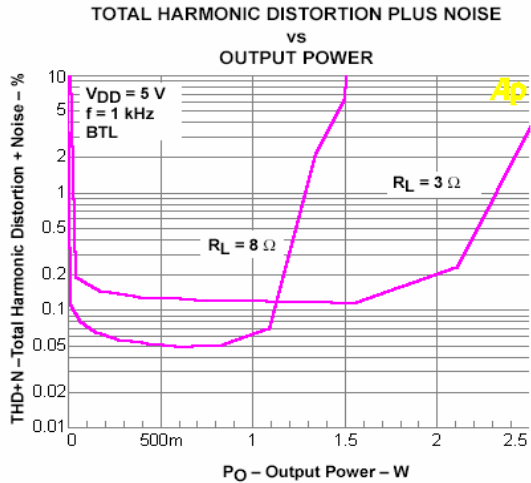


Figure 3.

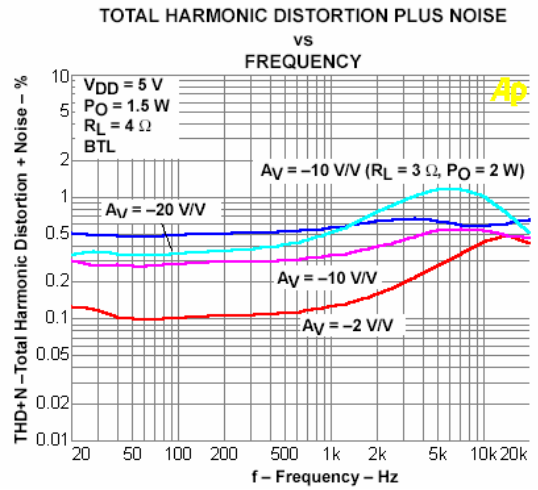


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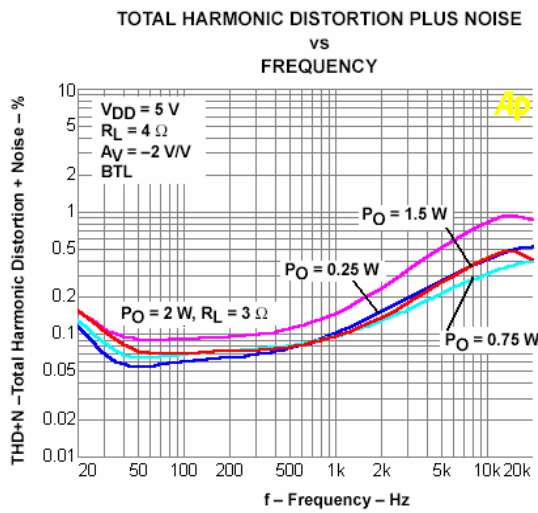


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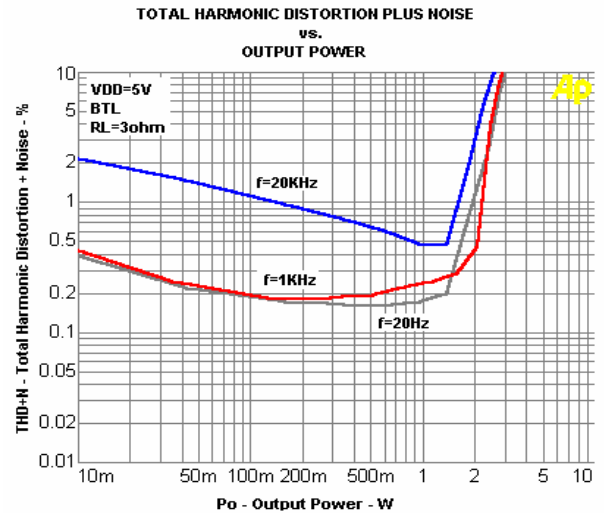


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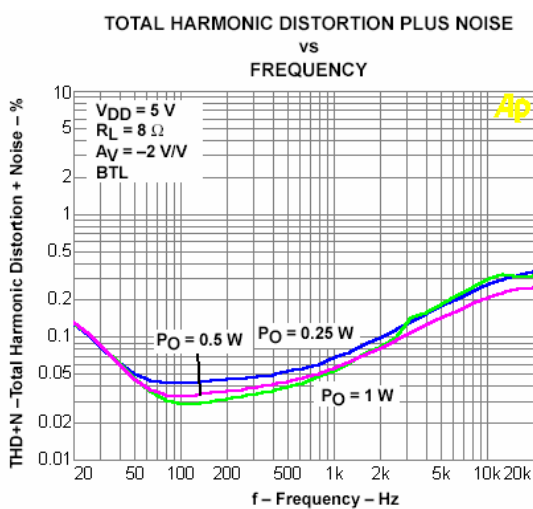


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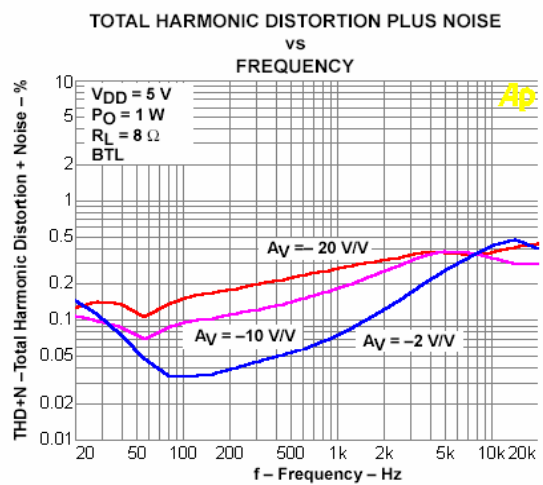


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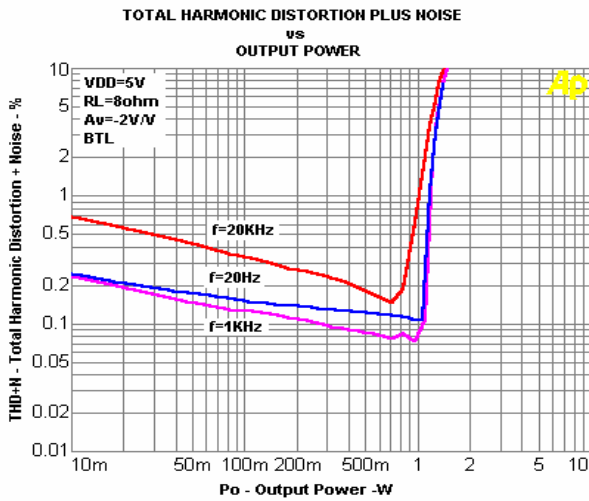


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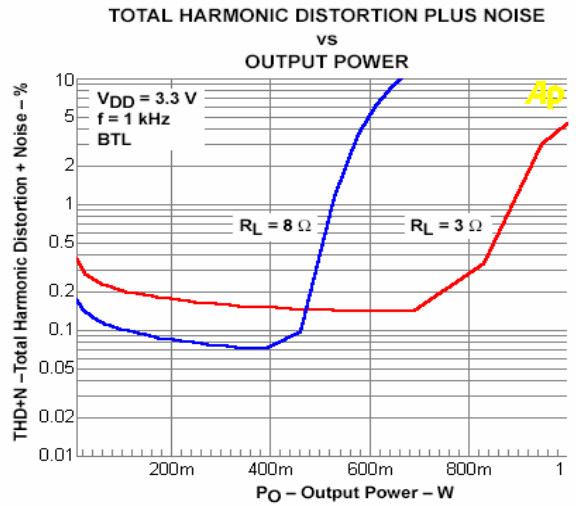


Figure10.

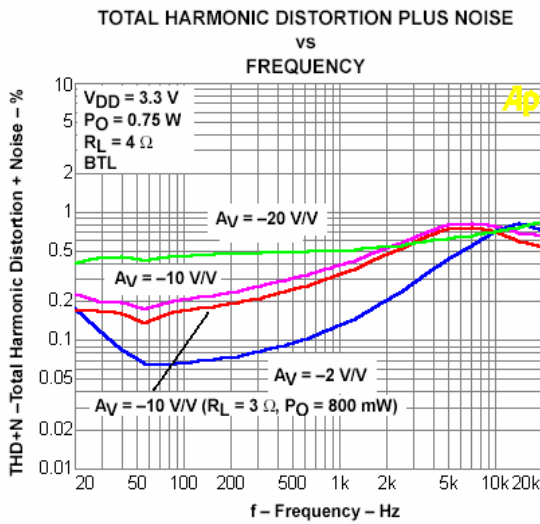


Figure11.

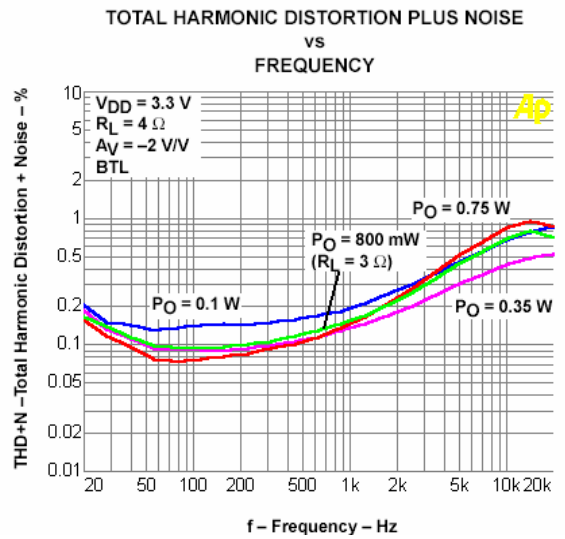


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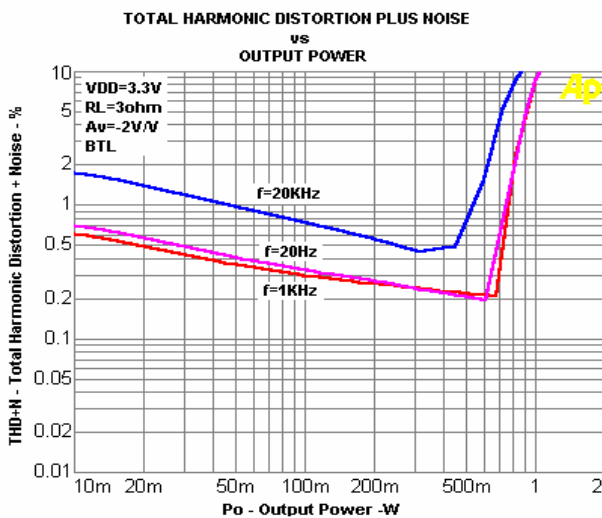


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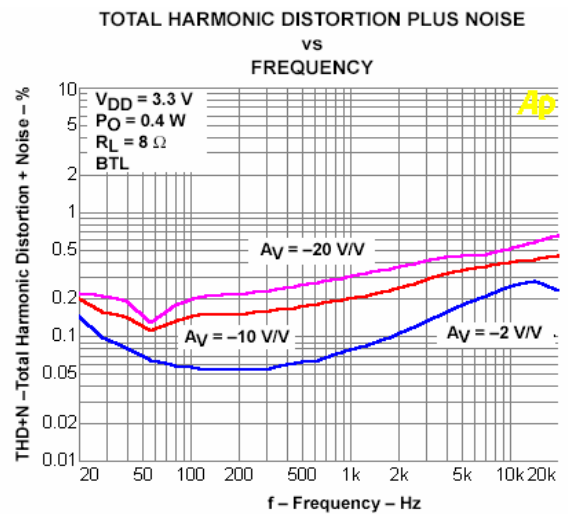


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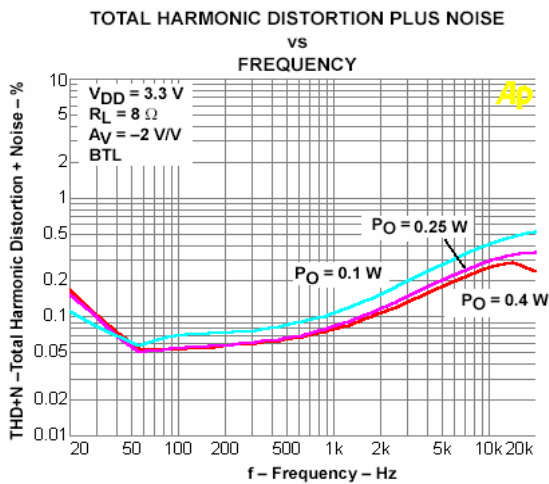


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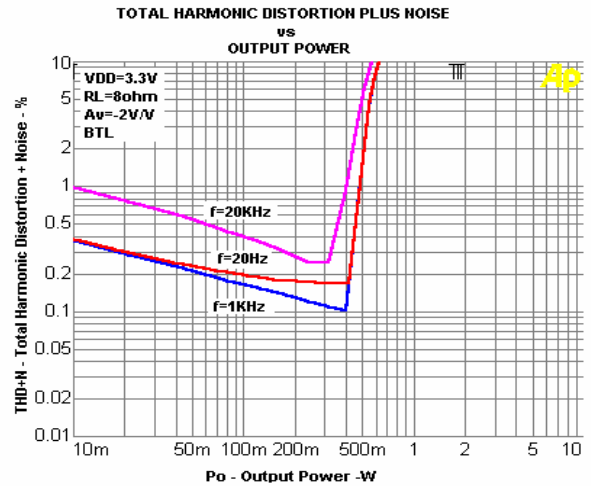


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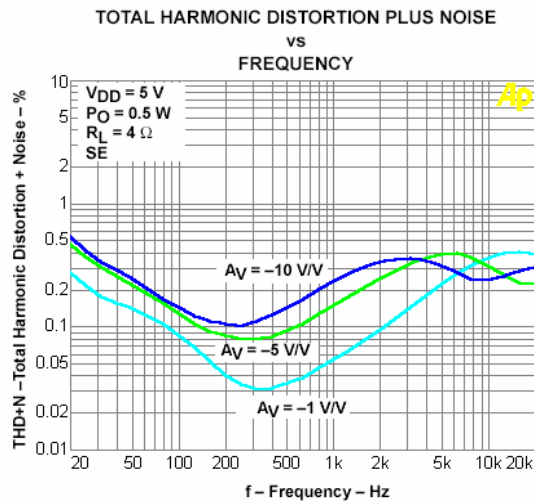


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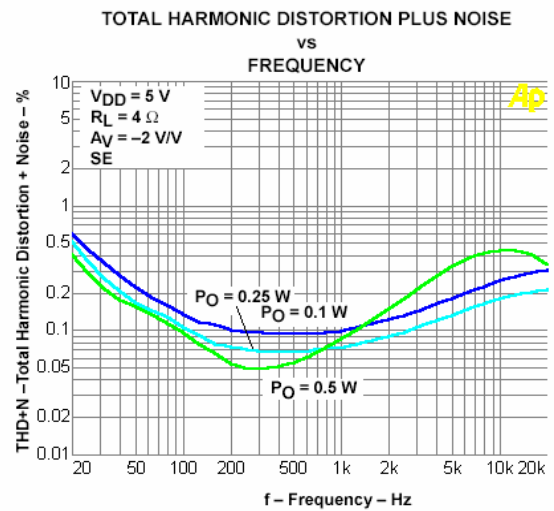


Figure18.

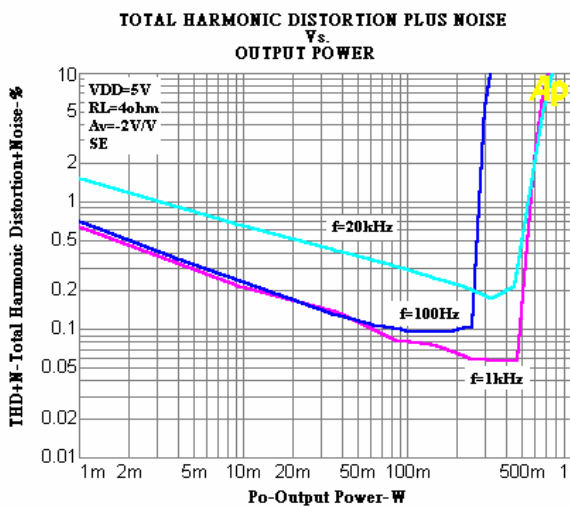


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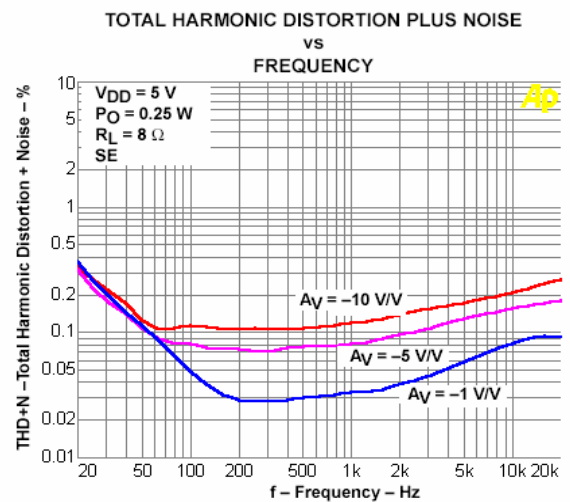


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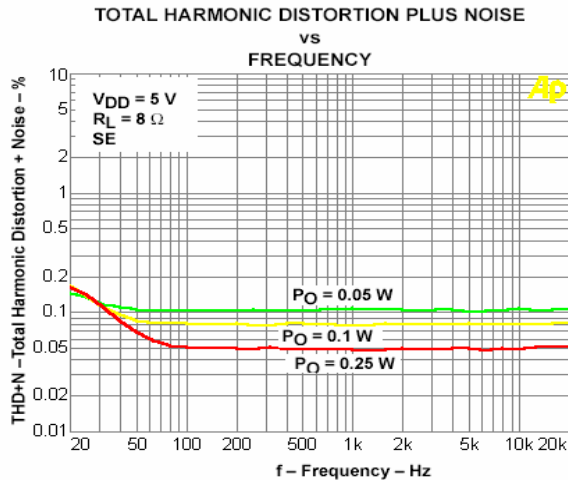


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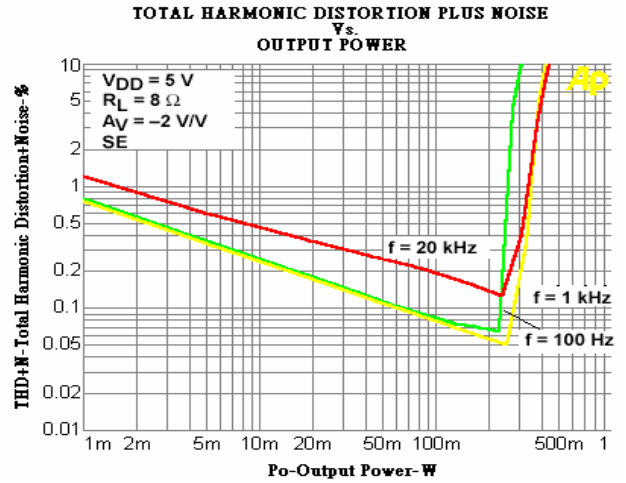


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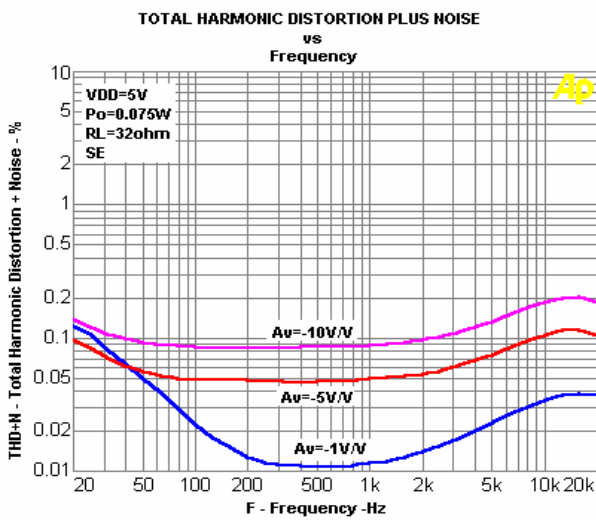


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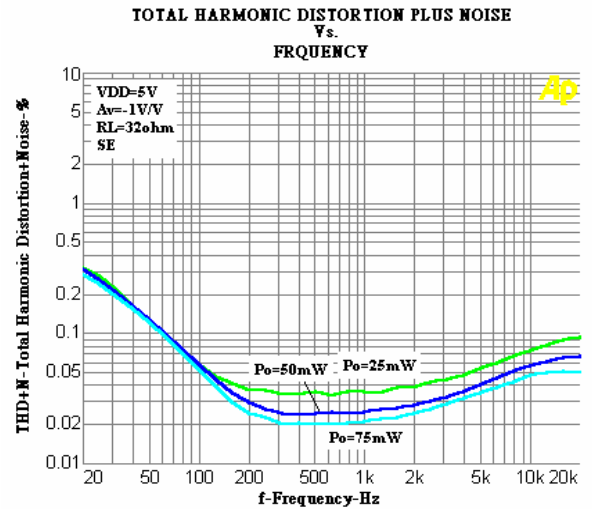


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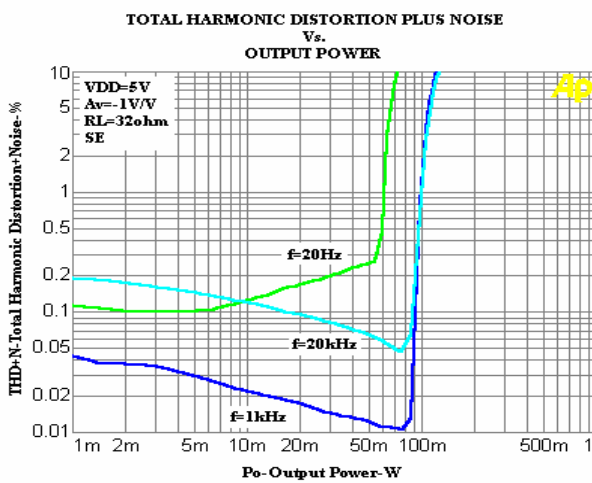


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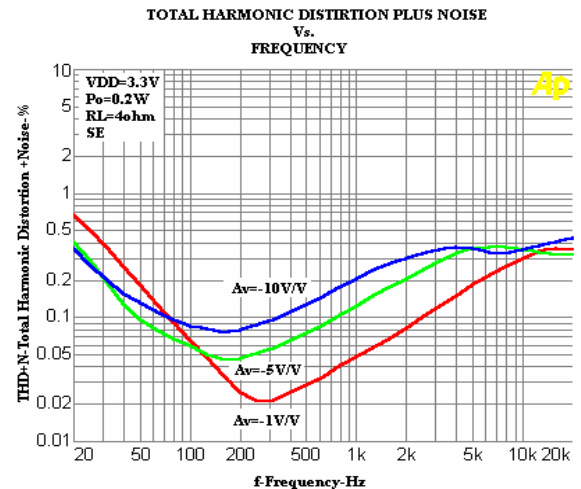


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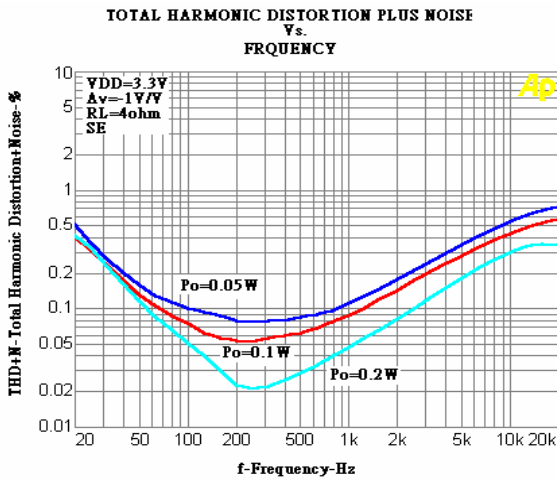


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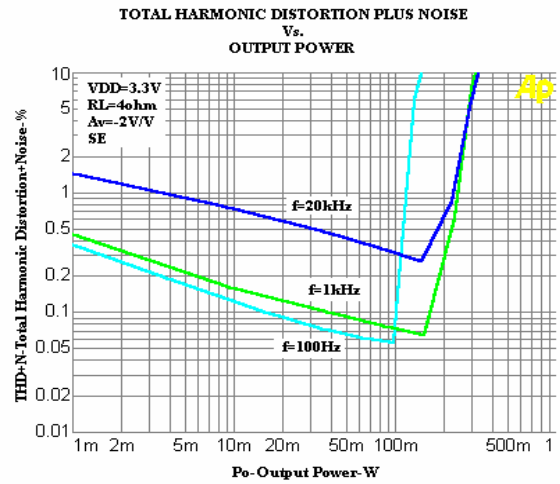


Figure28.

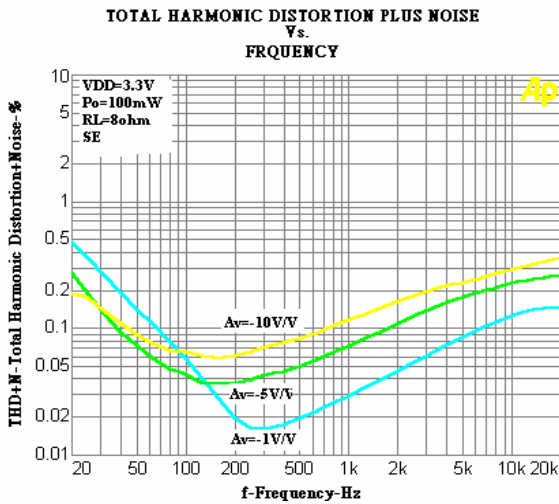


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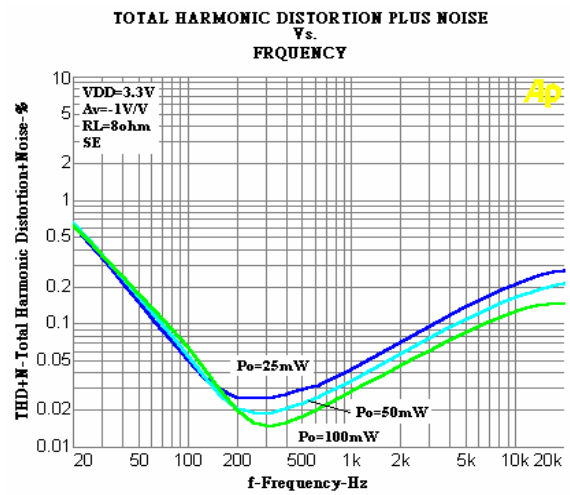


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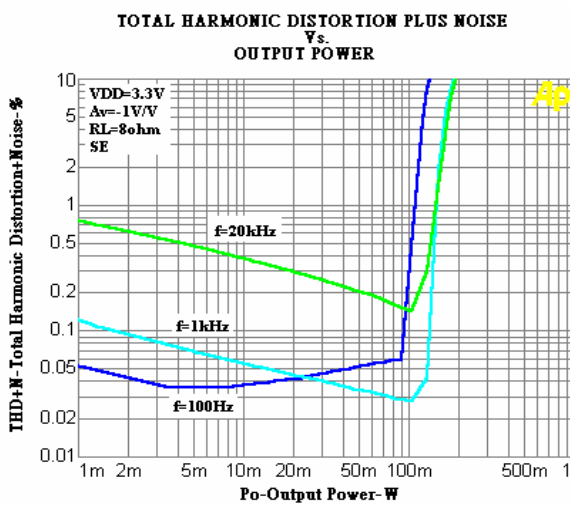


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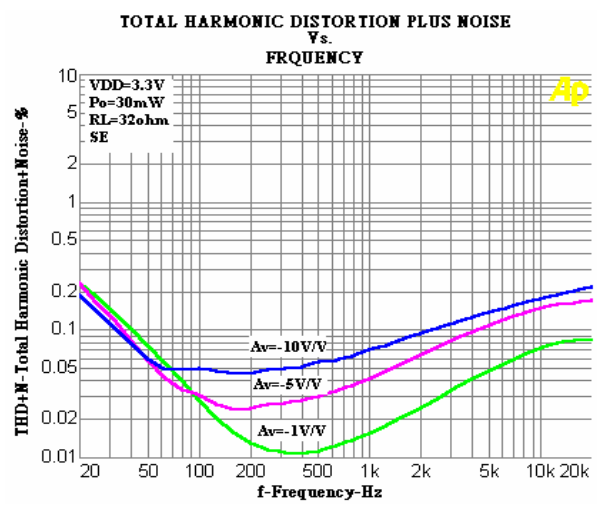


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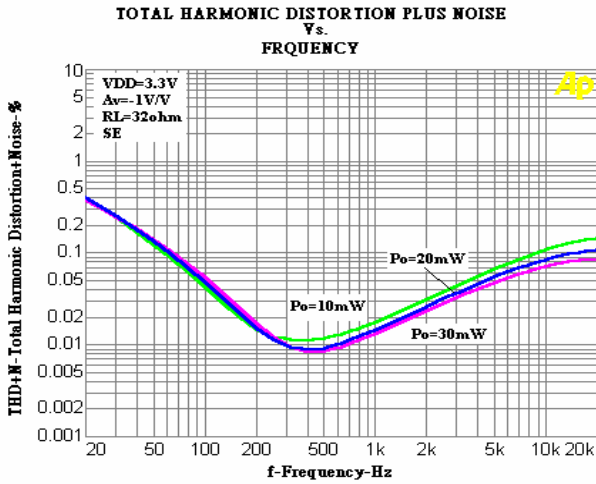


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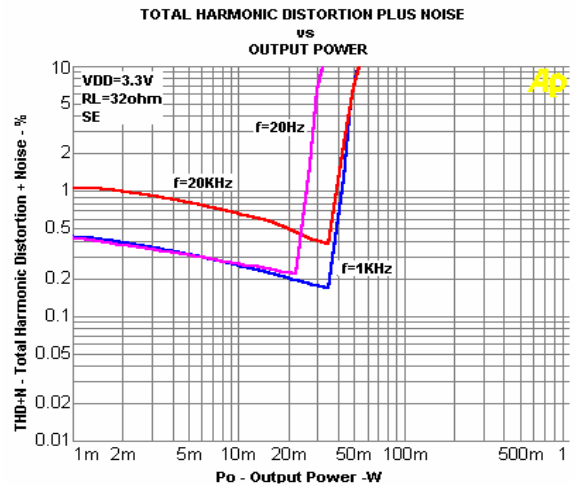


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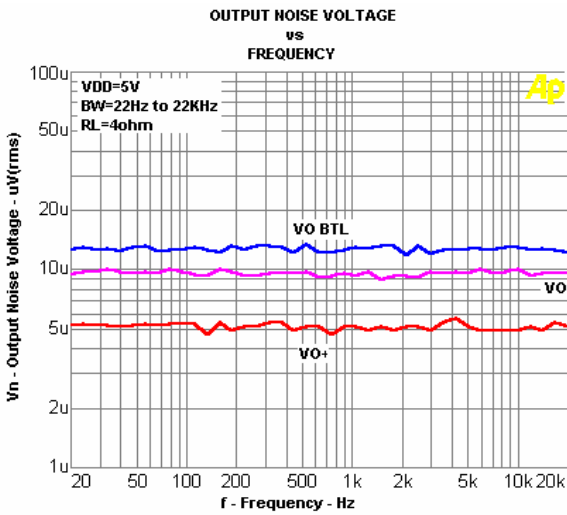


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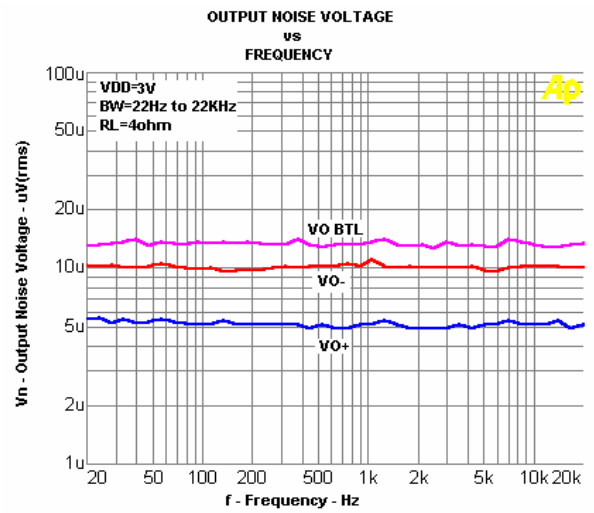


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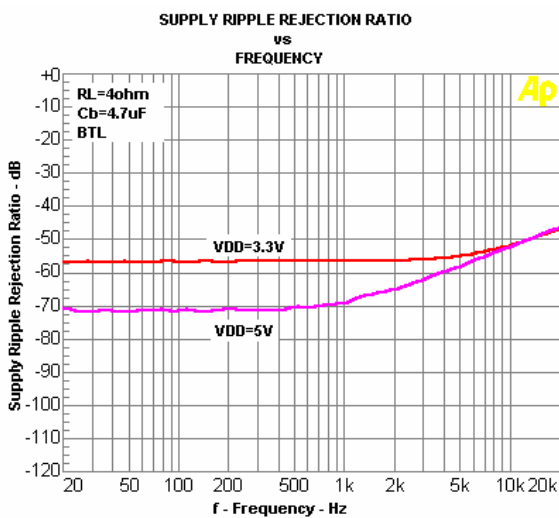


Figure37.

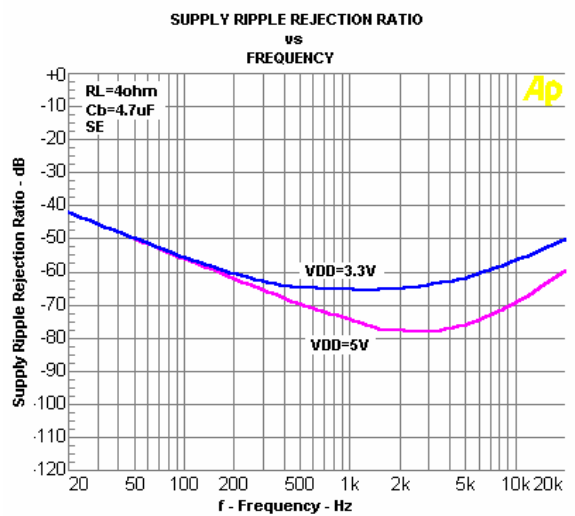


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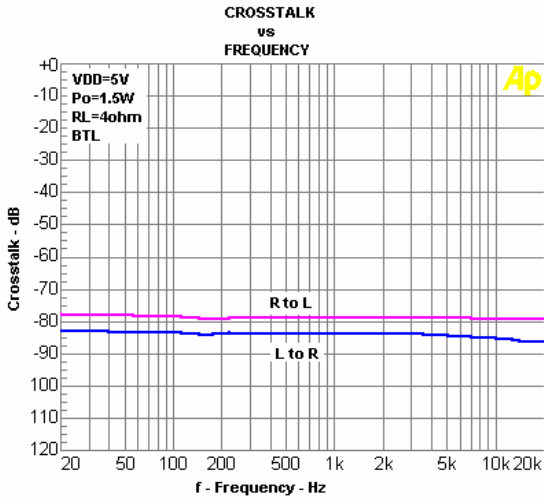


Figure39.

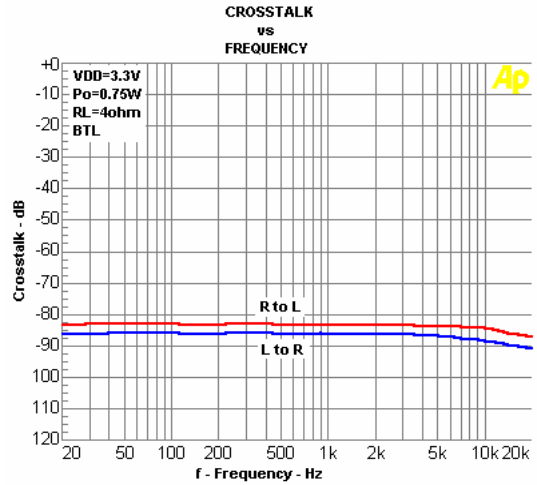


Figure40.

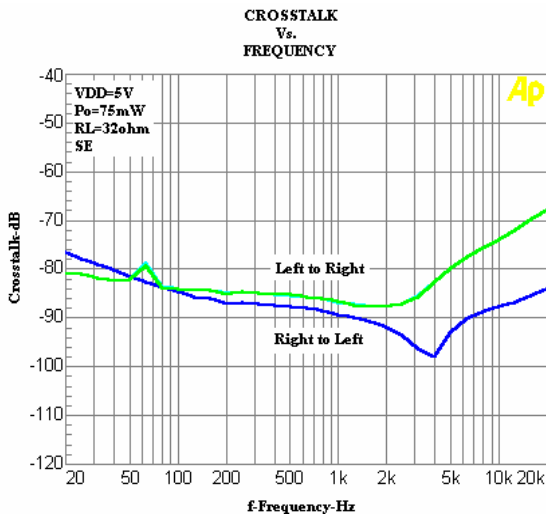


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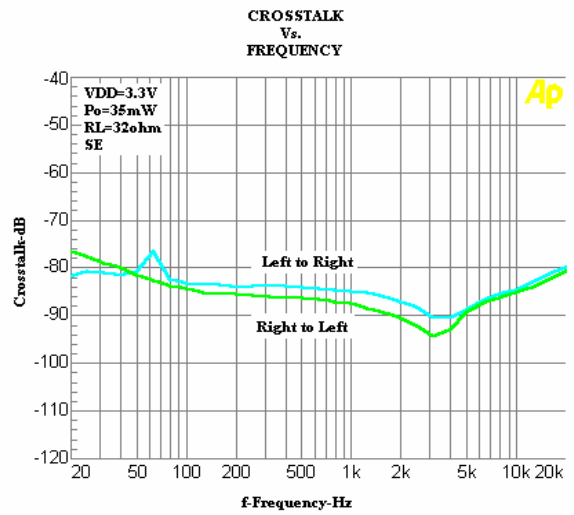


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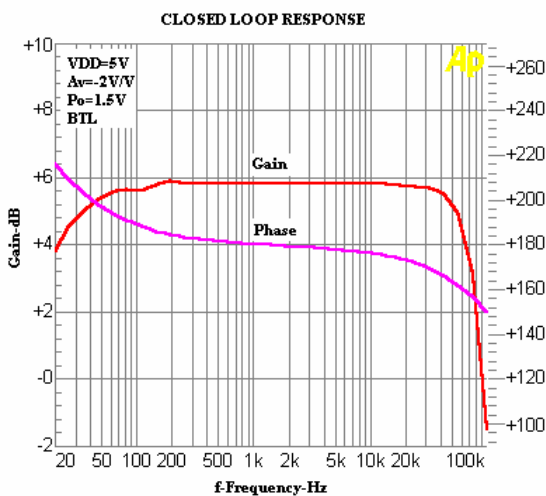


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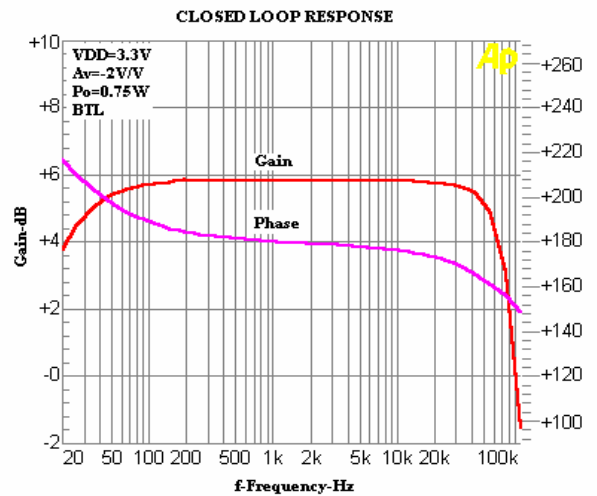


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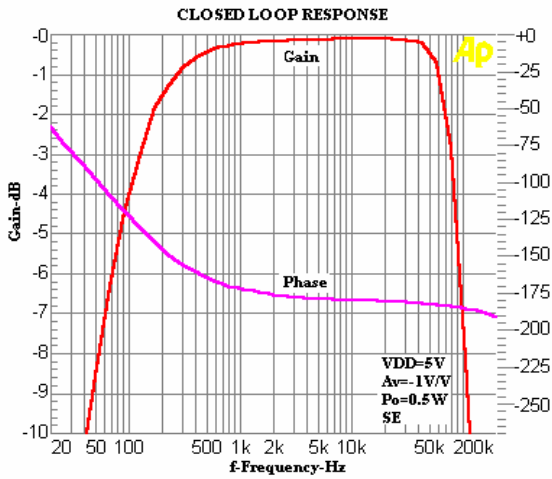


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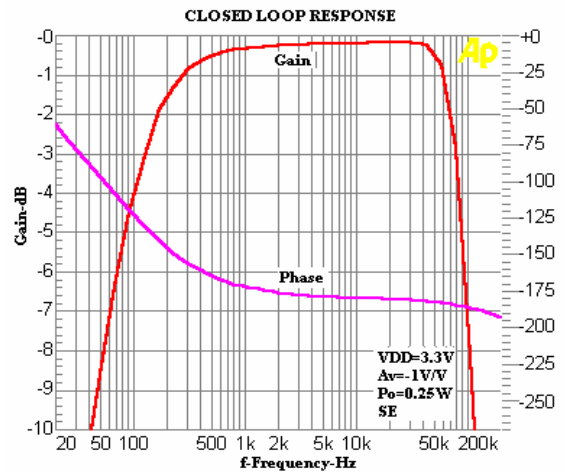


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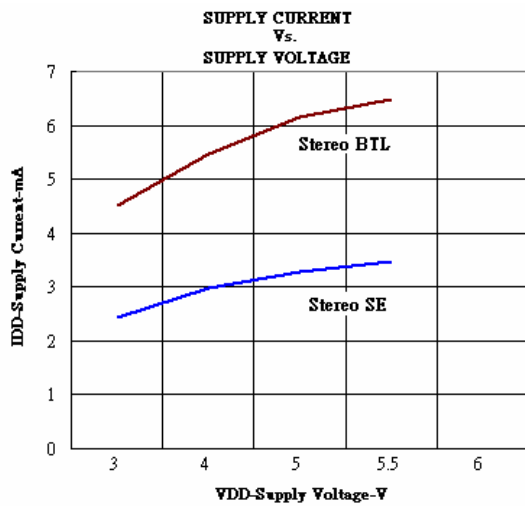


Figure47.

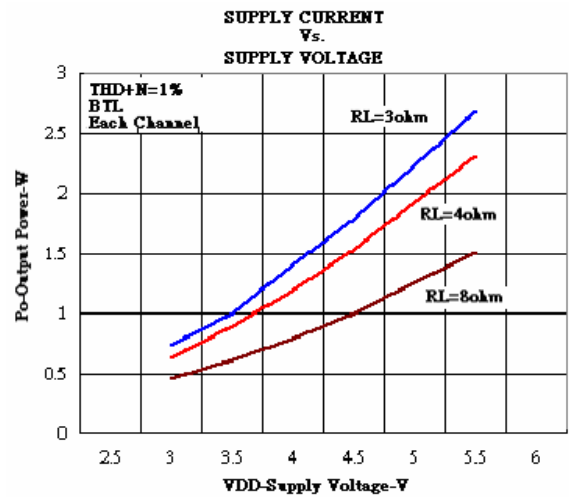


Figure48.

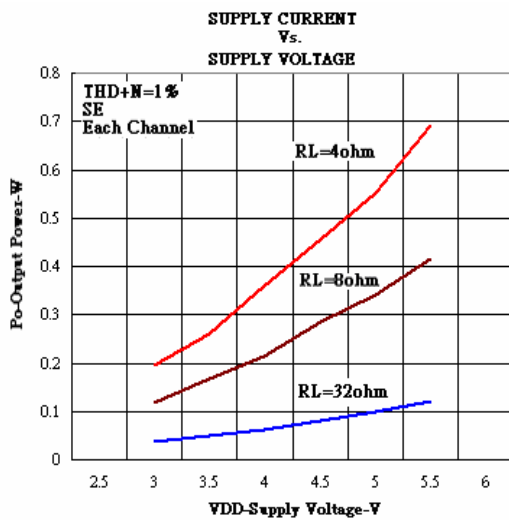


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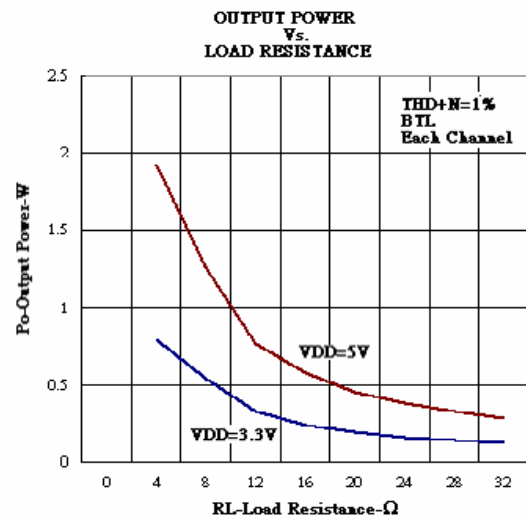


Figure50.



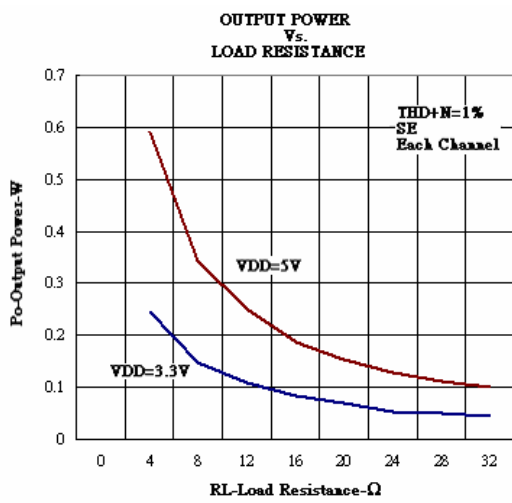


Figure51.

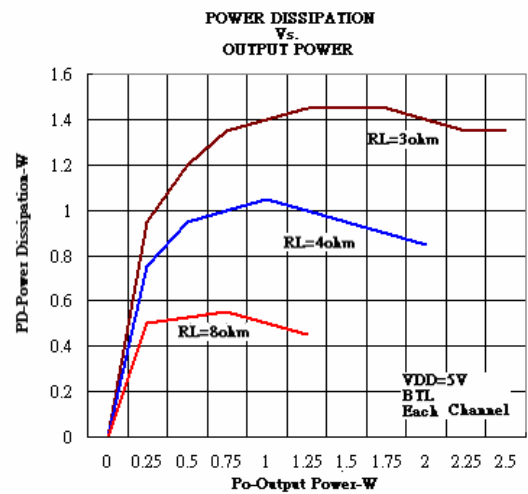


Figure52.

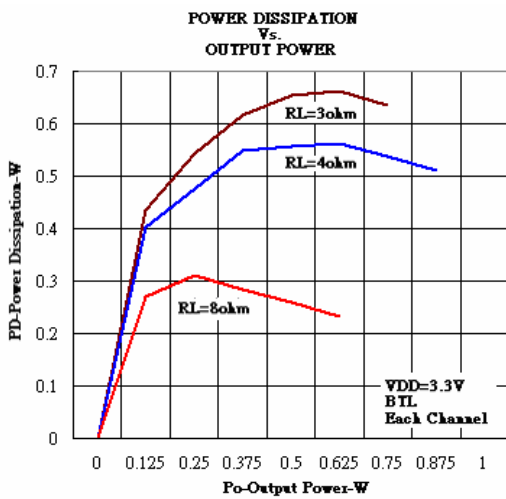


Figure53.

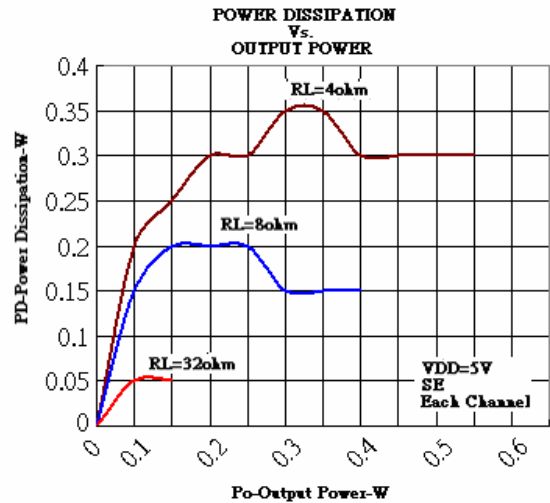


Figure54.

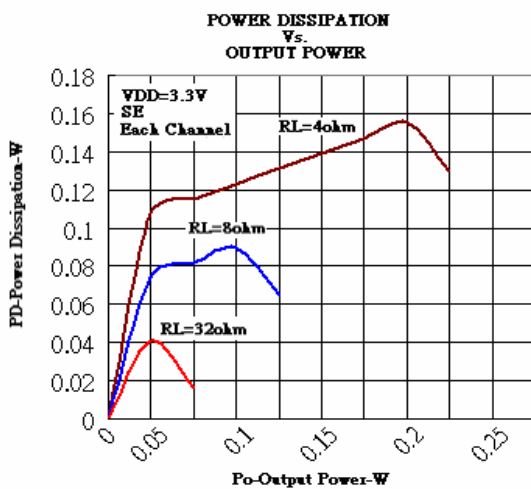


Figure55.

**Application Information**

**Gain Setting Resistors,  $R_F$  and  $R_I$**

The gain for each audio input of the EUA5202 is set by resistors by resistors  $R_F$  and  $R_I$  according to equation 1 for BTL mode.

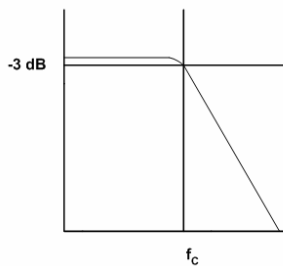
$$\text{BTL Gain} = -2 \left( \frac{R_F}{R_I} \right) \text{----- (1)}$$

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the EUA5202 is a MOS amplifier, the input impedance is very high, value of  $R_F$  increases. In addition, a certain range of  $R_F$  values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5kΩ and 20kΩ .The effective impedance is calculated in equation 2.

$$\text{EffectiveImpedance} = \frac{R_F R_I}{R_F + R_I} \text{----- (2)}$$

As an example consider an input resistance of 10kΩ and a feedback resistor of 50kΩ. The BTL gain of the amplifier would be -10 and the effective impedance at the inverting terminal would be 8.3kΩ, which is well within the recommended range. For high performance applications metal film resistors are recommended because they tent to have lower noise levels than carbon resistors. For values of  $R_F$  above 50kΩ the amplifier tends to become unstable due to a pole formed from  $R_F$  and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5pF should be places in parallel with  $R_F$  when  $R_F$  is greater than 50kΩ. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 3.

$$f_c (\text{lowpass}) = \frac{1}{2 \pi R_F C_F} \text{----- (3)}$$

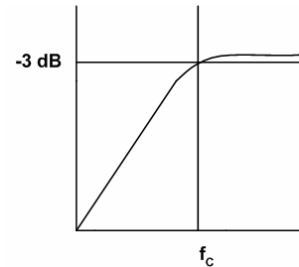


For example, if  $R_F$  is 100kΩ and  $C_F$  is 5 pF then  $f_c$  is 318 KHz, which is well outside of the audio range.

**Input Capacitor,  $C_I$**

In the typical application an input capacitor,  $C_I$ , is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case,  $C_I$  and  $R_I$  form a high-pass filter with the corner frequency determined in equation 4.

$$f_c (\text{highpass}) = \frac{1}{2 \pi R_I C_I} \text{----- (4)}$$



The value of  $C_I$  is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where  $R_I$  is 10kΩ and the specification calls for a flat bass response down to 40Hz. Equation 8 is reconfigured as equation 5.

$$C_I = \frac{1}{2 \pi R_I f_c} \text{----- (5)}$$

In this example,  $C_I$  is 0.40 μF so one would likely choose a value in the range of 0.47μF to 1μF. A further consideration for this capacitor is the leakage path from the input source through the input network ( $R_I$ ,  $C_I$ ) and the feedback resistor ( $R_F$ ) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at  $V_{DD}/2$ , which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

**Power Supply Decoupling, C<sub>s</sub>**

The EUA5202 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent – series - resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device V<sub>DD</sub> lead works best. For filtering lower – frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

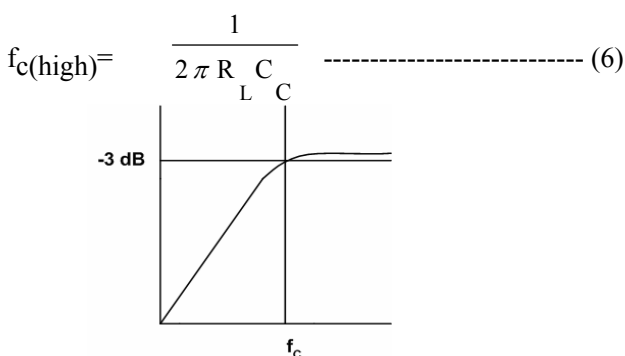
**Bypass Capacitor, C<sub>B</sub>**

The bypass capacitor, C<sub>B</sub>, is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, C<sub>B</sub> determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N. Bypass capacitor, C<sub>B</sub>, values of 0.1 µF to 1 µF ceramic of tantalum low-ESR capacitors are recommended for the best THD and noise performance.

In Figure 2, the full feature configuration, two bypass capacitors are used. This provides the maximum separation between right and left drive circuits. When absolute minimum cost and/or component space is required, one bypass capacitor can be used as shown in Figure 1. It is critical that terminals 6 and 19 be tied together in this configuration.

**Output Coupling Capacitor, C<sub>C</sub>**

In the typical single-supply SE configuration, and output coupling capacitor (C<sub>C</sub>) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor and impedance of the load form a high-pass filter governed by equation 6



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C<sub>C</sub> are required to pass low frequencies into the load. Consider the example where a C<sub>C</sub> of 330 µF is chosen and loads vary from 3Ω, 4Ω, 8Ω, 32Ω, 10kΩ, to 47kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

**Table1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode**

R <sub>L</sub>	C <sub>C</sub>	Lowest Frequency
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10000 Ω	330 µF	0.05 Hz
47000 Ω	330 µF	0.01 Hz

As Table 1 indicates, most of the bass response is attenuated into 4–Ω load, an 8–Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

**Using Low-ESR Capacitors**

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

**Bridged-Tied Load Versus Single-Ended Mode**

Figure 56 show a linear audio power amplifier (APA) in a BTL configuration. The EUA 5202 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging 2 × V<sub>O(PP)</sub> into the power equation, where voltage is squared, yields 4 × the output power from the same supply rail and load impedance (see equation 7)

$$V_{(\text{rms})} = \frac{V_{O(\text{PP})}}{2\sqrt{2}} \quad \text{Power} = \frac{V_{(\text{rms})}^2}{R_L} \quad \text{----- (7)}$$

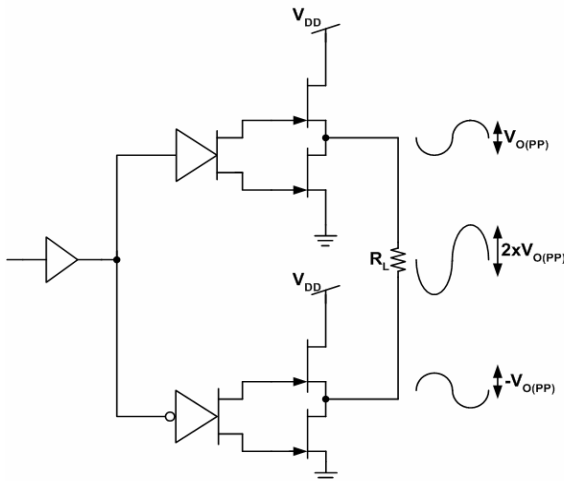


Figure 56. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5V, bridging raises the power into an 8-Ω speaker from a single-ended (SE, ground reference) limit of 250 mW to 1W. In sound power that is a 6-dB improvement—which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 57. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33μF to 1000μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 8.

$$f_C = \frac{1}{2 \pi R_L C_C} \text{----- (8)}$$

For example, a 68μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

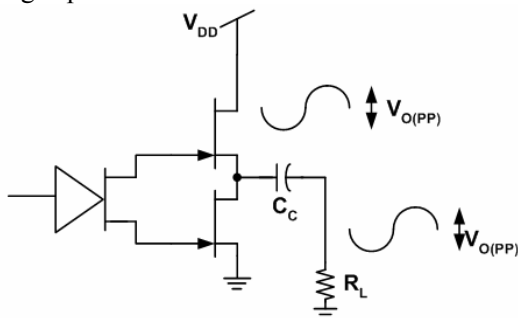


Figure 57. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4 × the output power of the SE configuration. Internal dissipation versus output power is discussed further in the crest factor and thermal considerations section.

**Single-Ended Operation**

In SE mode (see Figure56 and Figure57), the load is driven from the primary amplifier output for each channel (OUT+, terminals 22 and 3).

In SE mode the gain is set by the RF and RI resistors and is shown in equation 9. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2, from equation 5, is not included.

$$\text{SE Gain} = - \left( \frac{R_F}{R_I} \right) \text{----- (9)}$$

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship (see equation 10):

$$\frac{1}{(C_B \times 25k)} \leq \frac{1}{(C_I R_I)} < \frac{1}{R_L C_C} \text{----- (10)}$$

**Input MUX Operation**

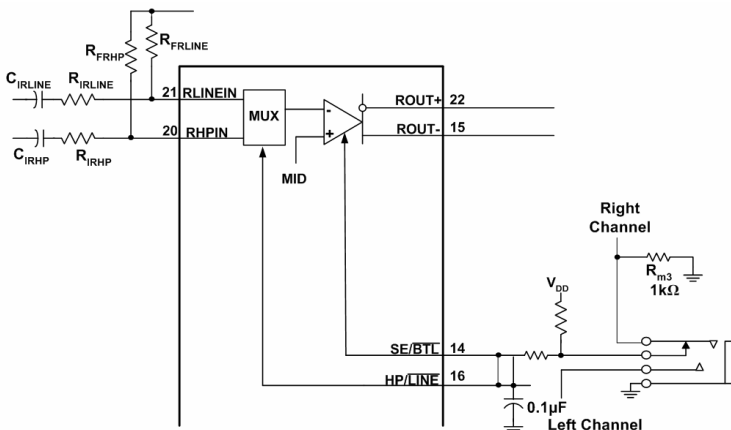
Working in concert with the SE/BTL feature, the HP/LINE MUX feature gives the audio designer the flexibility of a multichip design in a single IC (see Figure 58). The primary function of the MUX is to allow different gain settings for BTL versus SE mode. Speakers typically require approximately a factor of 10 more gain for similar volume listening levels as compared to headphones. To achieve headphone and speaker listening parity, the resistor values would need to be set as follows:

$$SE\ Gain_{(HP)} = -\left(\frac{R_{F(HP)}}{R_{I(HP)}}\right) \text{ ----- (11)}$$

If, for example  $R_{I(HP)} = 10\text{ k}\Omega$  and  $R_{F(HP)} = 10\text{ k}\Omega$  then  $SE\ Gain_{(HP)} = -1$

$$BTL\ Gain_{(LINE)} = -2\left(\frac{R_{F(LINE)}}{R_{I(LINE)}}\right) \text{ ----- (12)}$$

If, for example  $R_{I(LINE)} = 10\text{ k}\Omega$  and  $R_{F(LINE)} = 50\text{ k}\Omega$  then  $BTL\ Gain_{(LINE)} = -10$

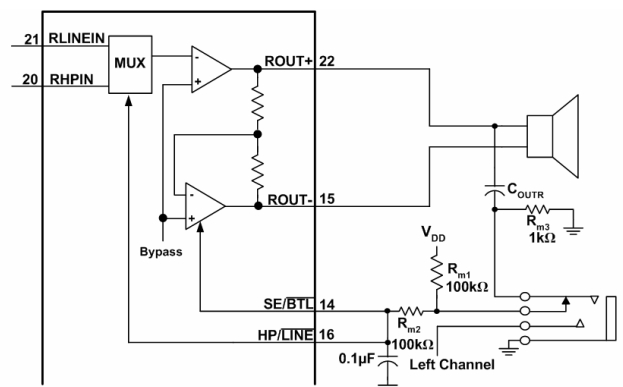


**Figure 58. EUA5202 Example Input MUX Circuit**

Another advantage of using the MUX feature is setting the gain of the headphone channel to -1. This provides the optimum distortion performance into the headphones where clear sound is more important. Refer to the SE/BTL operation section for a description of the headphone hack control circuit.

**SE/BTL Operation**

The ability of the EUA5202 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the EUA5202, two separate amplifiers drive LOUT- and ROUT- (terminals 10 and 15). When SE/BTL is held high, the OUT- amplifier are in high output impedance state, which configures the EUA5202 as an SE driver from LOUT + and ROUT + (terminal 3 and 22).  $I_{DD}$  is reduced by approximately one-half in SE mode. Control of the SE/BTL input can be from a logic-level CMOS source, or, more typically, from a resistor divider network as shown in Figure 59.



**Figure 59. EUA5202 Resistor Divider Network Circuit**

Using a readily available 1/8-in. (3.5mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/BTL input low. When a plug is inserted, the OUT- amplifier is shutdown causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (CO) into the headphone jack. As shown in the full feature application (Figure 2), the input MUX control can be tied to the SE/BTL input. The benefits of doing this are described in the following input MUX operation section.

**Mute and Shutdown Mode**

The EUA5202 employs both a mute and a shutdown mode of operation designed to reduce supply current,  $I_{DD}$ , to the absolute minimum level during periods of nonuse for battery-power conservation. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state,  $I_{DD} = 5\ \mu\text{A}$ . SHUTDOWN or MUTE IN should never be left unconnected because amplifier operation would be unpredictable. Mute mode alone reduces  $I_{DD}$  to 1.5 mA.

## Thermal Pad Considerations

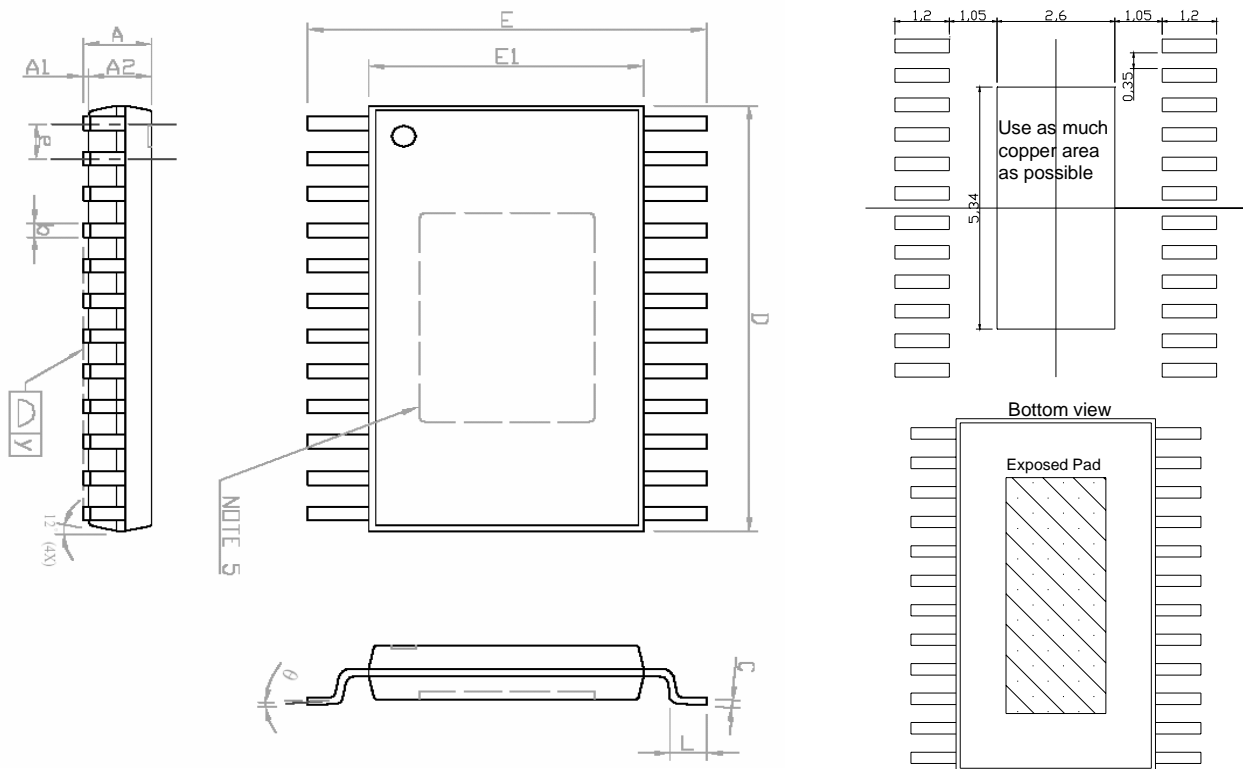
The thermal pad must be connected to ground. The package with thermal pad of the EUA5202 requires special attention on thermal design. If the thermal design issues are not properly addressed, the EUA5202 will go into thermal shutdown when driving a heavy load.

The thermal pad on the bottom of the EUA5202 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 13 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane.

For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25 °C, a larger copper plane or forced-air cooling will be required to keep the EUA5202 junction temperature below the thermal shutdown temperature (150 °C). In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.

## Package Information



## NOTE

1. Package body sizes exclude mold flash protrusions or gate burrs
2. Tolerance  $\pm 0.1\text{mm}$  unless otherwise specified
3. Coplanarity :0.1mm
4. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.
5. Die pad exposure size is according to lead frame design.
6. Standard Solder Map dimension is millimeter.
7. Followed from JEDEC MO-153

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-----	-----	1.15	-----	-----	0.045
A1	0.00	-----	0.10	0.000	-----	0.004
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	-----	0.30	0.007	-----	0.012
C	0.09	-----	0.20	0.004	-----	0.008
D	7.70	7.80	7.90	0.303	0.307	0.311
E	-----	6.40	-----	-----	0.252	-----
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	-----	0.65	-----	-----	0.026	-----
L	0.45	0.60	0.75	0.018	0.024	0.030
y	-----	-----	0.10	-----	-----	0.004
$\theta$	0	-----	8	0	-----	8