2-W Stereo Audio Power Amplifier with Selectable Gain and Shutdown

DESCRIPTOIN

The EUA6027A is a stereo audio speaker amplifier in a 20-pin TSSOP thermally enhanced package. Operating on a single 5V supply, EUA6027A is capable of delivering 2W of output power per channel into 3Ω loads with less than 1% THD+N.

Amplifier gain is internally configured and controlled by way of two terminals (GAIN0 and GAIN1). Gain settings of 6 dB, 10 dB, 15.6 dB, and 21.6 dB (inverting) are provided. Internal gain control requires few external components.

Other features include an active-low shutdown mode input and thermal shutdown protection.

FEATURES

- 2W/Ch Output Power Into 3-Ω Load From 5-V Supply
- Internal Gain Control
- Fully Differential Input
- Depop Circuitry
- Thermal Shutdown Protection
- TSSOP-20 with Thermal Pad
- RoHS Compliant and 100% Lead (Pb)-Free

APPLICATIONS

- Notebook Computers, PDAs, and Other Portable Audio Devices

Typical Application

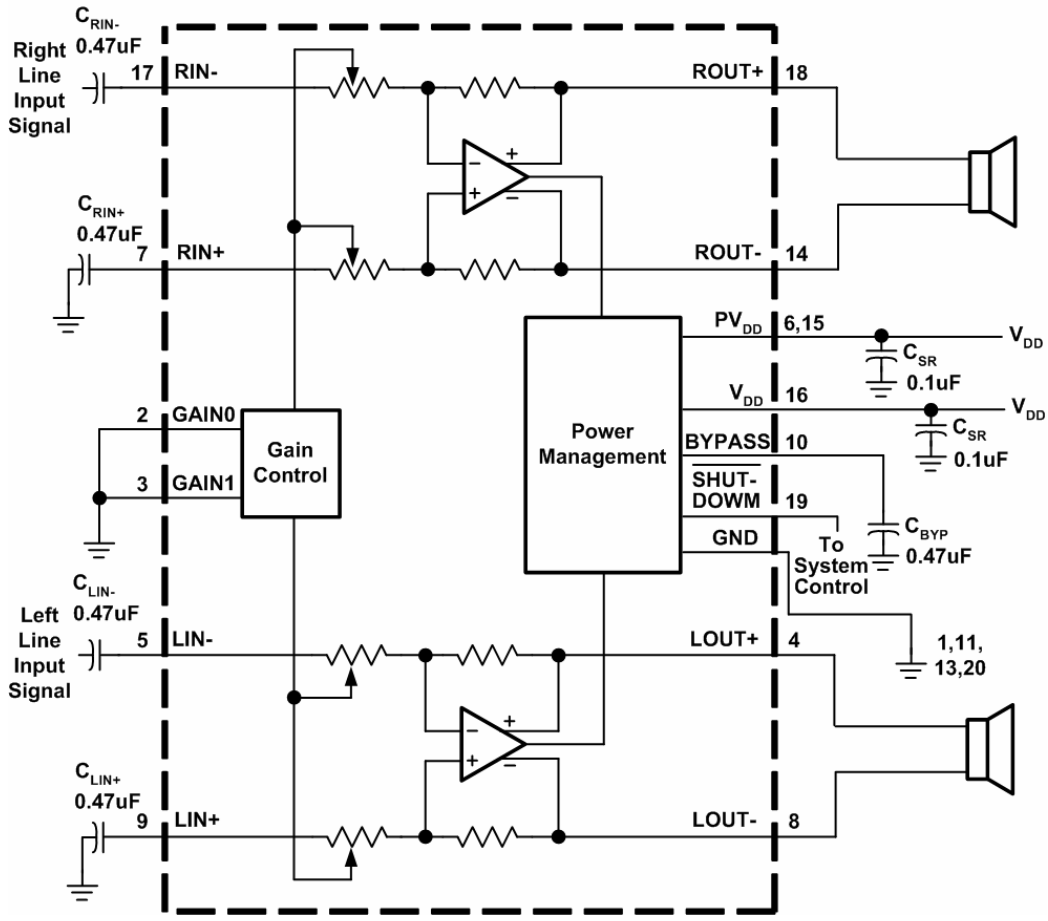


Figure 1.

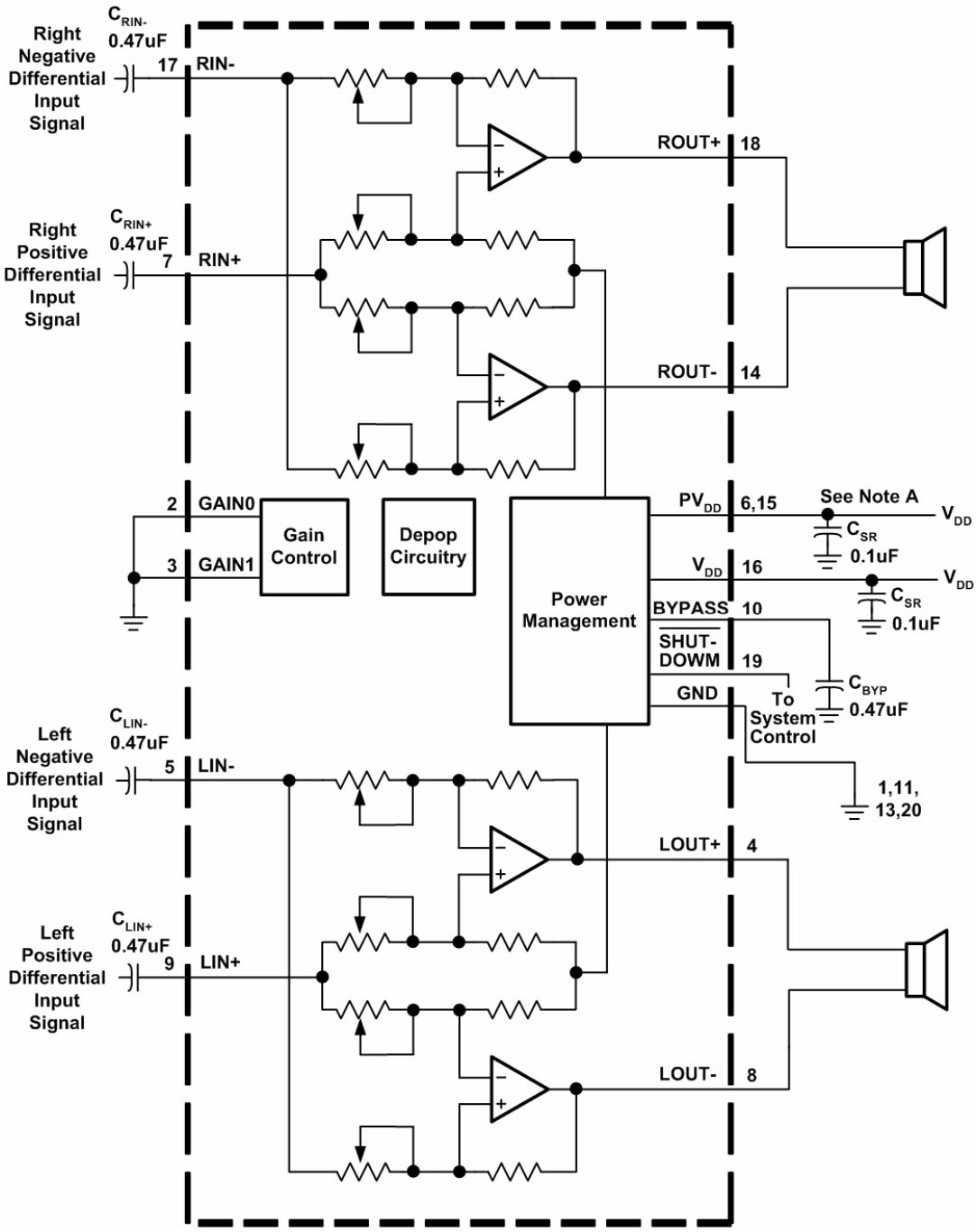
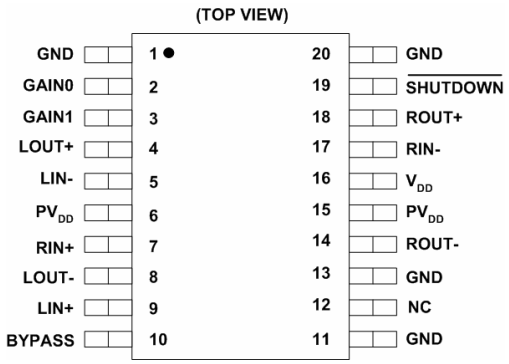


Figure 2. Application Circuit Using Differential Inputs

Note A: A 0.1µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower frequency noise signals, a larger electrolytic capacitor of 10µF or greater should be placed near the audio power amplifier.

Pin Configurations

Package Type	Pin Configurations
TSSOP-20 (FD)	

Pin Description

PIN	PIN	I/O	DESCRIPTION
BYPASS	10	-	Tap to voltage divider for internal midsupply bias generator
GAIN0	2	I	Bit 0 of gain control
GAIN1	3	I	Bit 1 of gain control
GND	1,11 13,20	-	Ground
LIN-	5	I	Left channel negative differential input
LIN+	9	I	Left channel positive differential input
LOUT-	8	O	Left channel negative output
LOUT+	4	O	Left channel positive output
NC	12	-	No connection
PV_{DD}	6,15	I	Supply voltage terminal
ROUT-	14	O	Right channel negative output
ROUT+	18	O	Right channel positive output
RIN-	17	I	Right channel negative differential input
RIN+	7	I	Right channel positive differential input
$\overline{SHUTDOWN}$	19	I	Places IC in shutdown mode when held low
V_{DD}	16	-	Supply voltage terminal

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUA6027AQIR1	TSSOP-20	xxxxx 6027A	-40 °C to 85°C

EUA6027A □ □ □ □

Lead Free Code
1: Lead Free 0: Lead

Packing
R: Tape& Reel

Operating temperature range
I: Industry Standard

Package Type
Q: TSSOP

Absolute Maximum Ratings

- Supply voltage, V_{DD} ---------- 6V
- Input voltage, V_I ---------- –0.3 V to V_{DD} +0.3 V
- Operating free-air temperature range, T_A ---------- –40°C to 85° C
- Operating junction temperature range, T_J ---------- –40°C to 150°C
- Storage temperature range, T_{stg} ---------- –65°C to 150°C
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ---------- 260°C
- Thermal Resistance

  θ_{JA} (TSSOP) ---------- 87.9°C/W

Recommended Operating Conditions

		Min	Max	Unit
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	$\overline{SHUTDOWN}$	2		V
Low-level input voltage, V_{IL}	$\overline{SHUTDOWN}$		0.8	V
Operating free-air temperature, T_A		-40	85	°C

Electrical Characteristics at Specified Free-air Temperature, V_{DD} = 5V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	EUA6027A			Unit
			Min.	Typ.	Max.	
$\|V_{OO}\|$	Output offset voltage (measured differentially)	V_I= 0, A_V=-2V/V,BTL,no load			25	mV
PSRR	Power supply rejection ratio	V_{DD}= 4.5 V to 5.5 V		79		dB
$\|I_{IH}\|$	High-level input current	V_{DD}= 5.5V, V_I = V_{DD}			1	μA
$\|I_{IL}\|$	Low-level input current	V_{DD}=5.5V, V_I = 0V			1	μA
I_{DD}	Supply current, no load	$\overline{SHUTDOWN}$ =2V		10	14	mA
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ =0.8V		145	300	μA

Operating Characteristics, V_{DD} = 5V, T_A = 25°C, R_L = 8Ω, Gain =-2V/V(unless otherwise noted)

Symbol	Parameter	Conditions	EUA6027A			Unit
			Min.	Typ.	Max.	
P_O	Output power	THD=1%, R_L=4Ω,f=1kHz		1.95		W
THD+N	Total harmonic distortion plus noise	P_O=1W, R_L=8Ω, f=20Hz to 15kHz		0.045 @1KHz		%
B_{OM}	Maximum output power bandwidth	THD=5%, R_L=8Ω		＞15		kHz
KSVR	Supply ripple rejection ratio	f =1kHz, C_B=0.47μF		-80		dB
SNR	Signal-to-noise ratio			103		dB
Vn	Noise output voltage	C_B=0.47μF,f=20 Hz to 20 kHz,		17		μV_{RMS}

Typical Characteristics

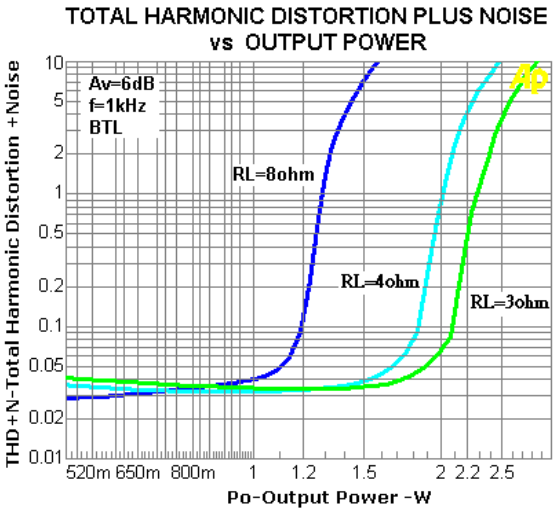
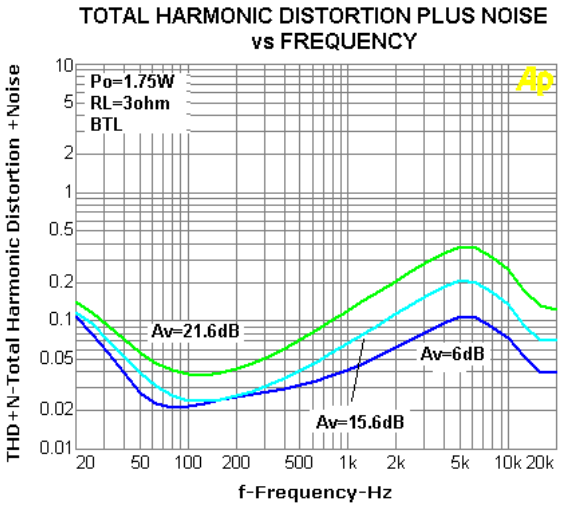


Figure 3



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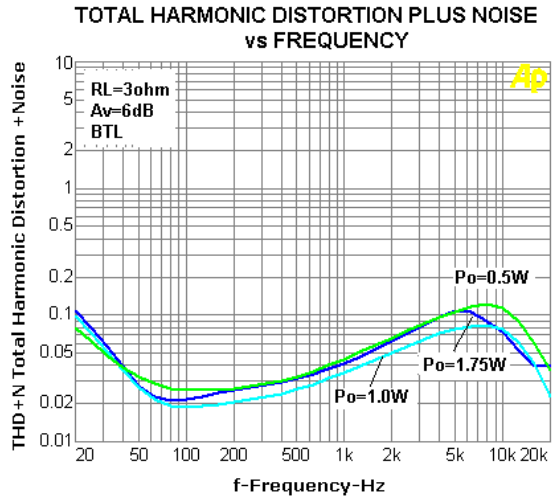

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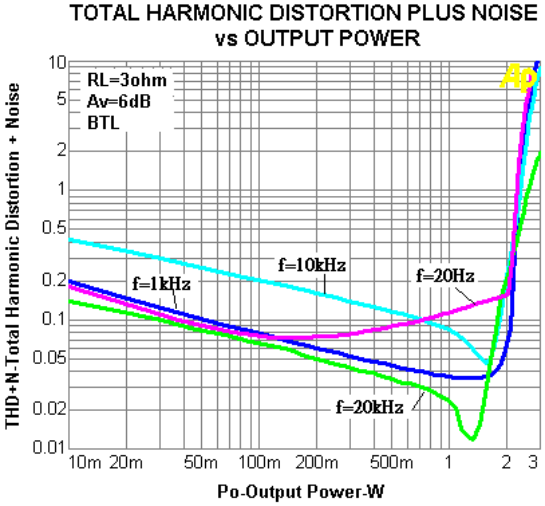

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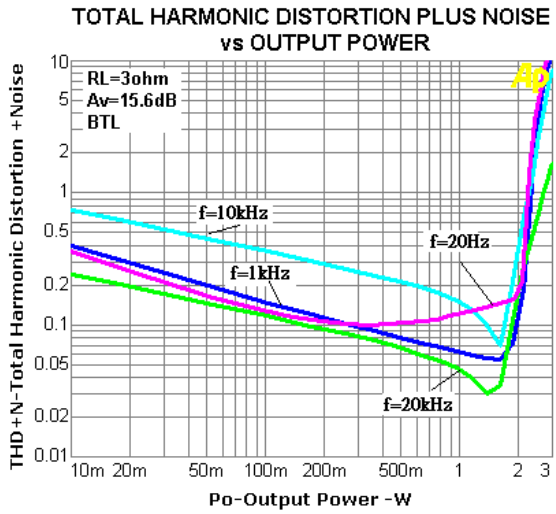
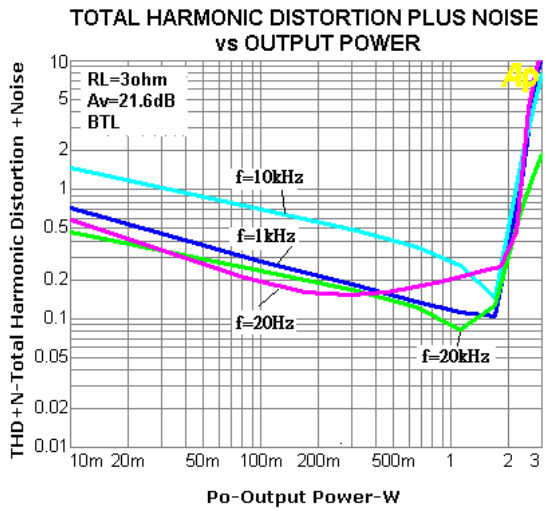


Figure 7



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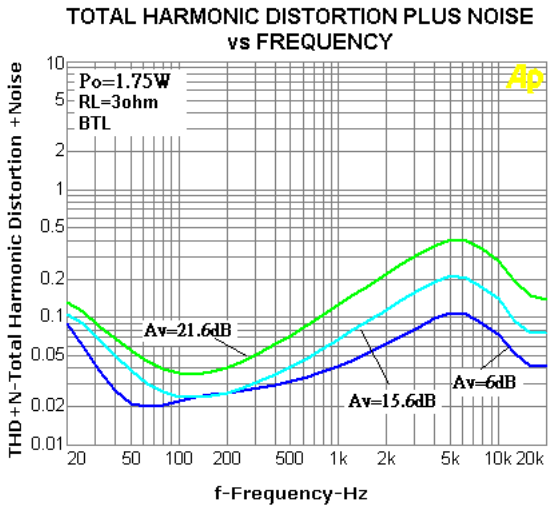

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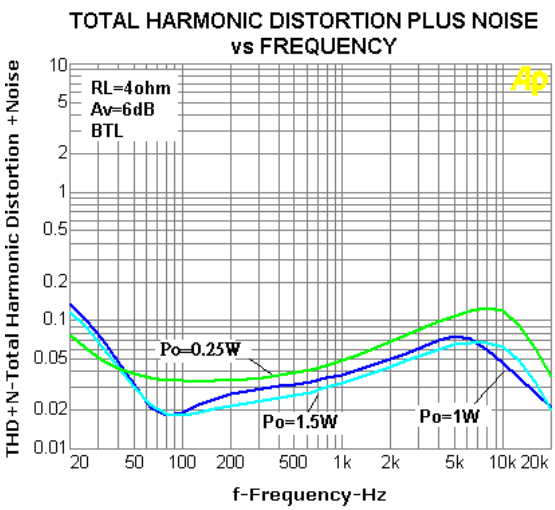

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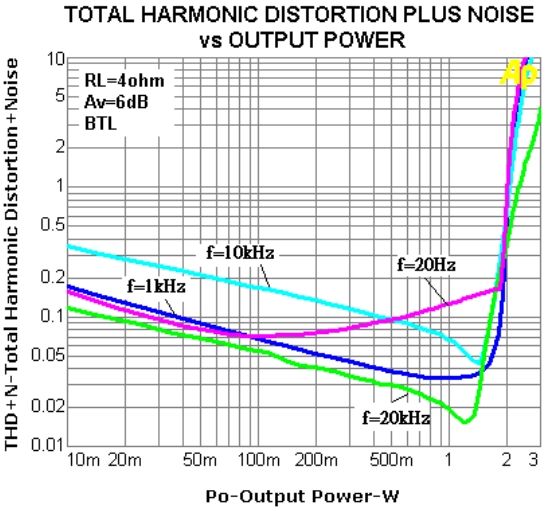

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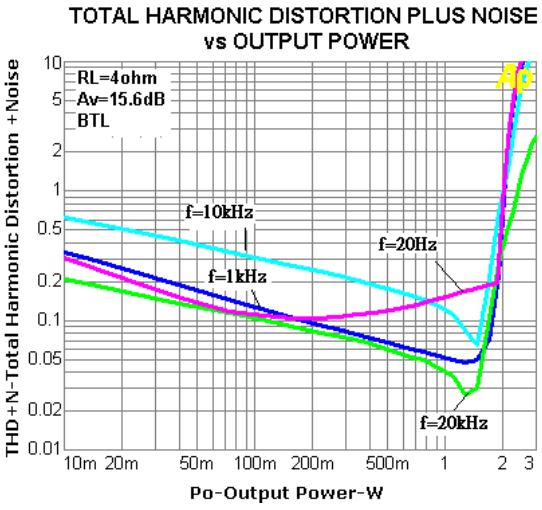

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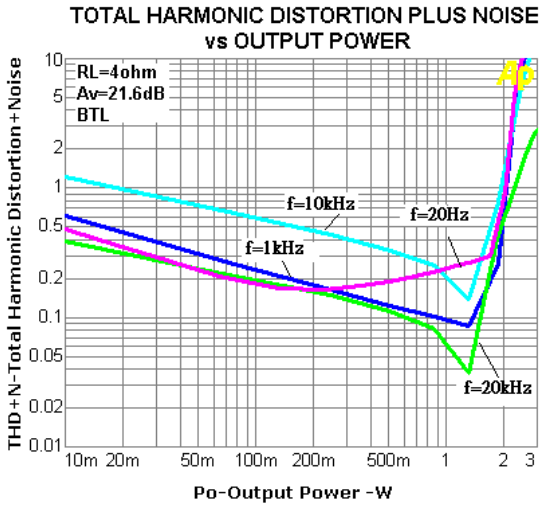

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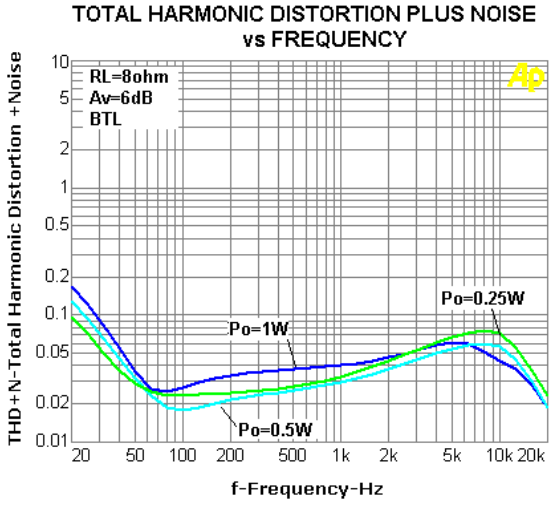

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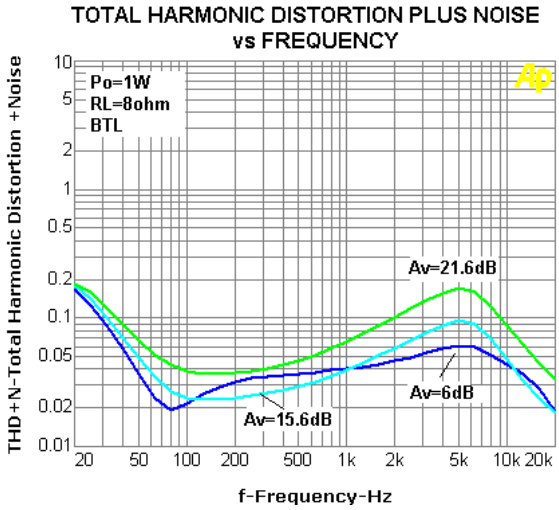

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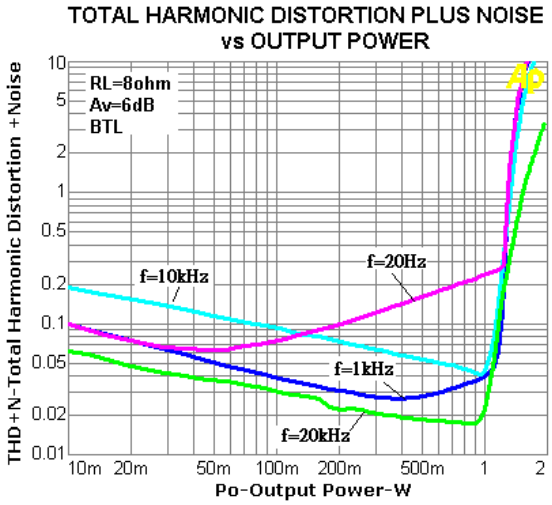

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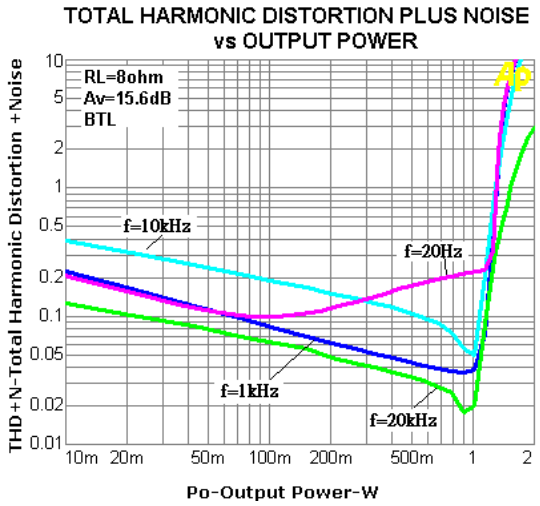

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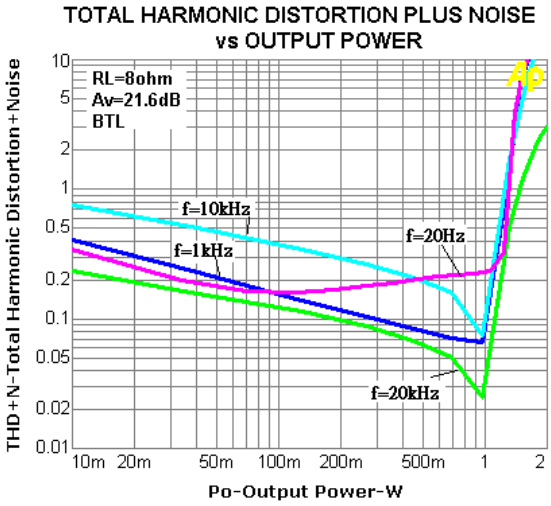

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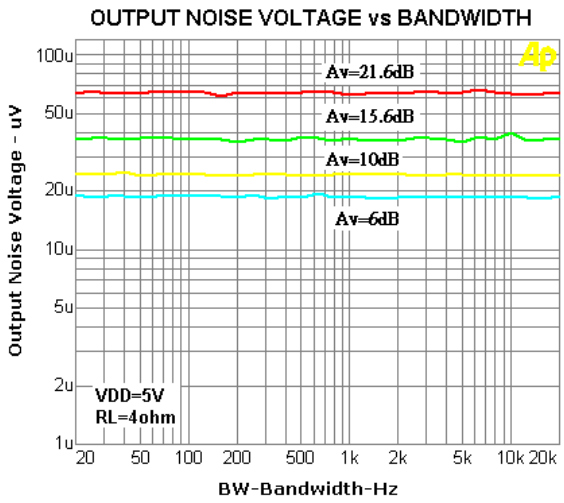

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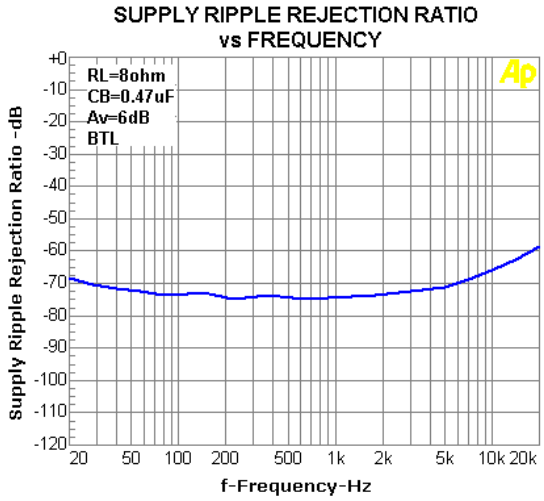

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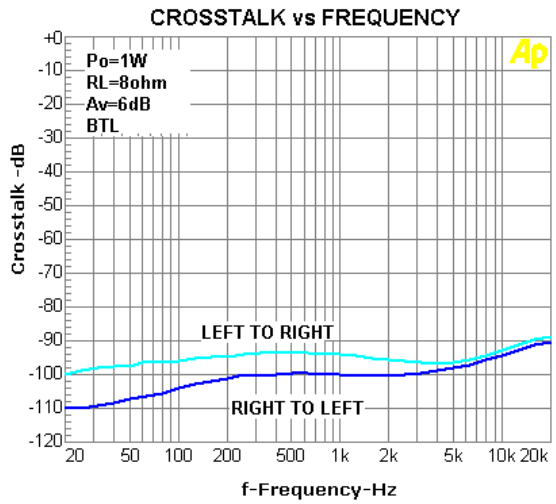

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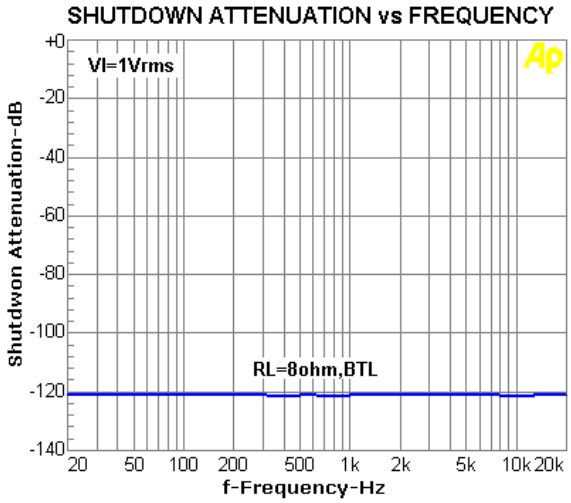

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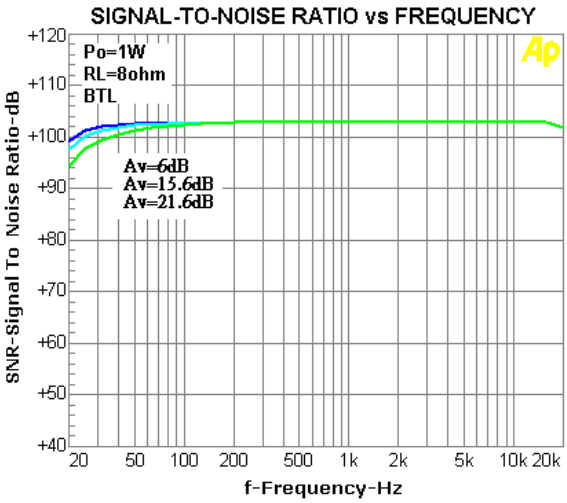

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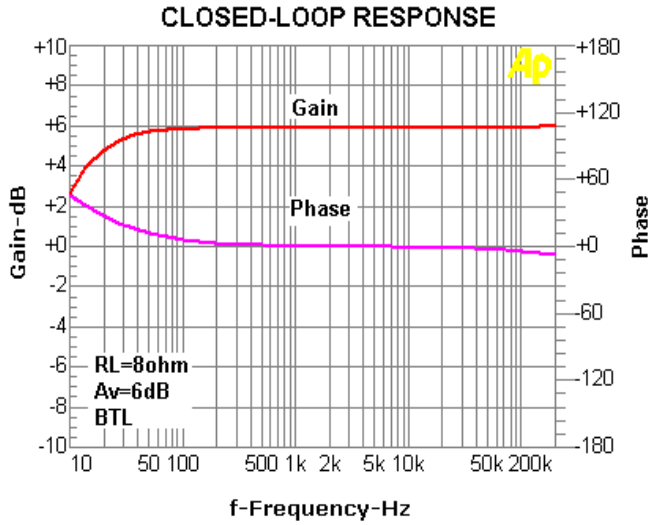


Figure 24

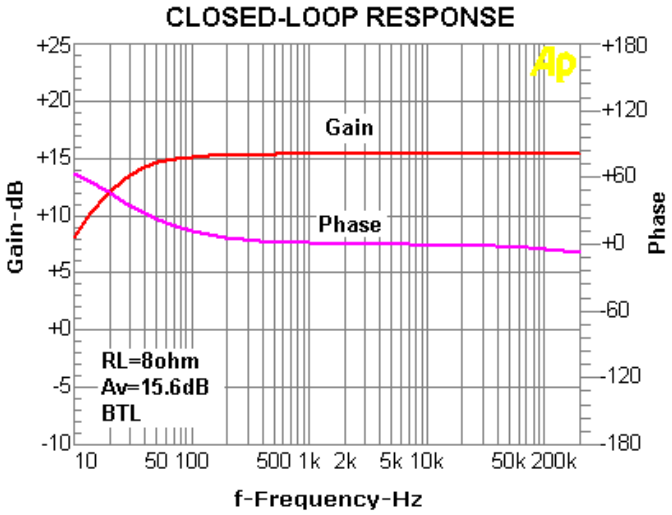


Figure 25

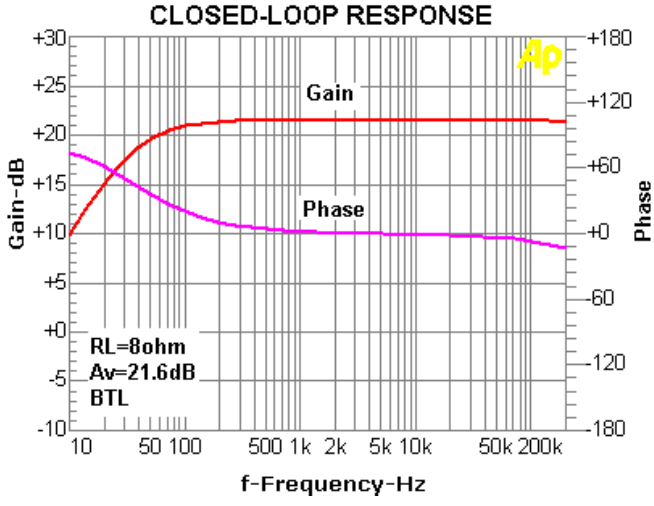


Figure 26

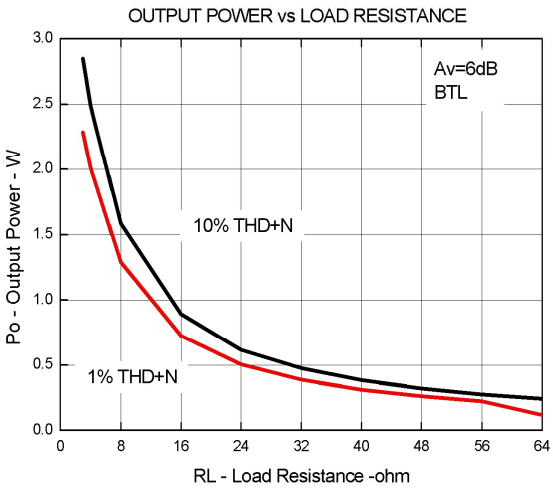


Figure 27

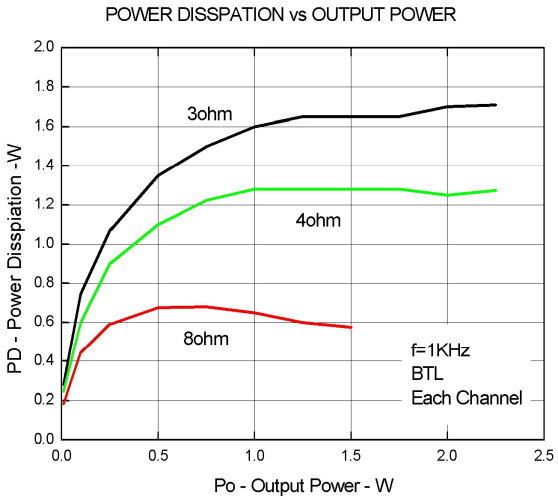


Figure 28

Application Information

Shutdown Modes

The EUA6027A employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{SHUTDOWN}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{SHUTDOWN}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD}=150μA. $\overline{SHUTDOWN}$ should never be left unconnected because amplifier operation would be unpredictable.

Gain Setting via GAIN0 and GAIN1 Inputs

The gain of the EUA6027A is set by two input terminals, GAIN0 and GAIN1.

Table 1 .Gain Settings

GAIN0	GAIN1	AV(inv)	Input Impedance
0	0	6dB	90kΩ
0	1	10dB	70kΩ
1	0	15.6dB	45kΩ
1	1	21.6dB	25kΩ

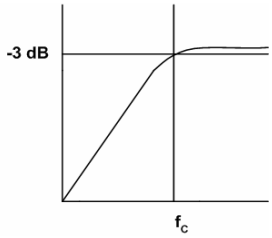
The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance, ZI, to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the actual gain distribution from part-to-part is quite good. However, the input impedance will shift by 30% due to shifts in the actual resistance of the input impedance.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 10 kΩ, which is the absolute minimum input impedance of the EUA6027A. At the higher gain settings, the input impedance could increase to as high as 115 kΩ. The typical input impedance at each gain setting is given in Table 1.

Input Capacitor, C_i

In the typical application an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier, Z_i, form a high-pass filter with the corner frequency determined in equation 1.

$$f_{c(highpass)} = \frac{1}{2\pi Z_i C_i} \text{----------(1)}$$



The value of C_i is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_i is 70kΩ and the specification calls for a flat bass response down to 40Hz. Equation 2 is reconfigured as equation 2.

$$C_i = \frac{1}{2\pi Z_i f_C} \text{----------(2)}$$

In this example, C_i is 56nF so one would likely choose a value in the range of 56nF to 1μF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

Power Supply Decoupling, (C_S)

The EUA6027A is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10μF or greater placed near the audio power amplifier is recommended.

Midrail Bypass Capacitor, (C_{BYP})

The midrail bypass capacitor, C_{BYP}, the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor, C_{BYP}, values of 0.47µF to 1µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

Using Low- ESR Capacitors

Low- ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

Bridged-Tied Load Versus Single-Ended Mode

Figure 29 show a Class-AB audio power amplifier (APA) in a BTL configuration. The EUA6027A BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2\times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance(see equation 3)

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad \text{Power} = \frac{V_{(rms)}^2}{R_L} \qquad \text{------(3)}$$

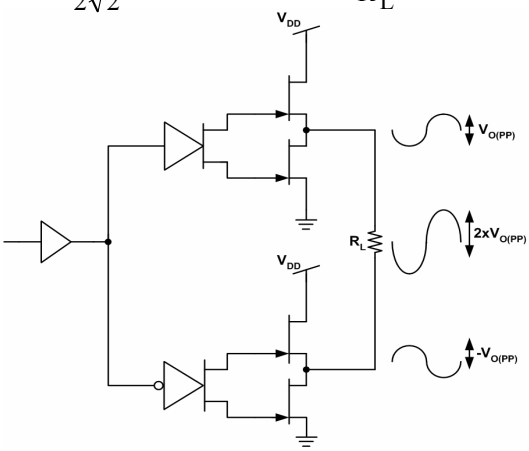


Figure 29.Bridge-Tied Load configuration

In a typical computer sound channel operating at 5V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1W. In sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 30.

A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 4.

$$f_C = \frac{1}{2\pi R_L C_C} \text{----------(4)}$$

For example, a 68µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

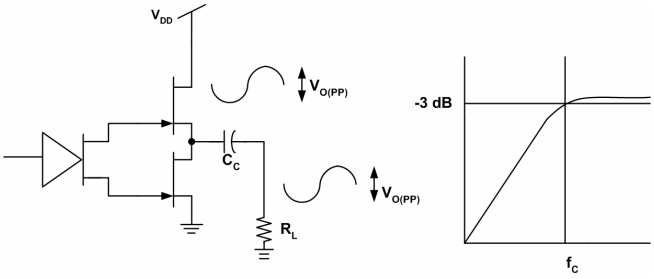


Figure 30. Single-Ended configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4 X the output power of the SE configuration. Internal dissipation versus output power is discussed further in the crest factor and thermal considerations section.

Thermal Pad Considerations

The thermal pad must be connected to ground. The package with thermal pad of the EUA6027A requires special attention on thermal design. If the thermal design issues are not properly addressed, the EUA6027A will go into thermal shutdown when driving a heavy load.

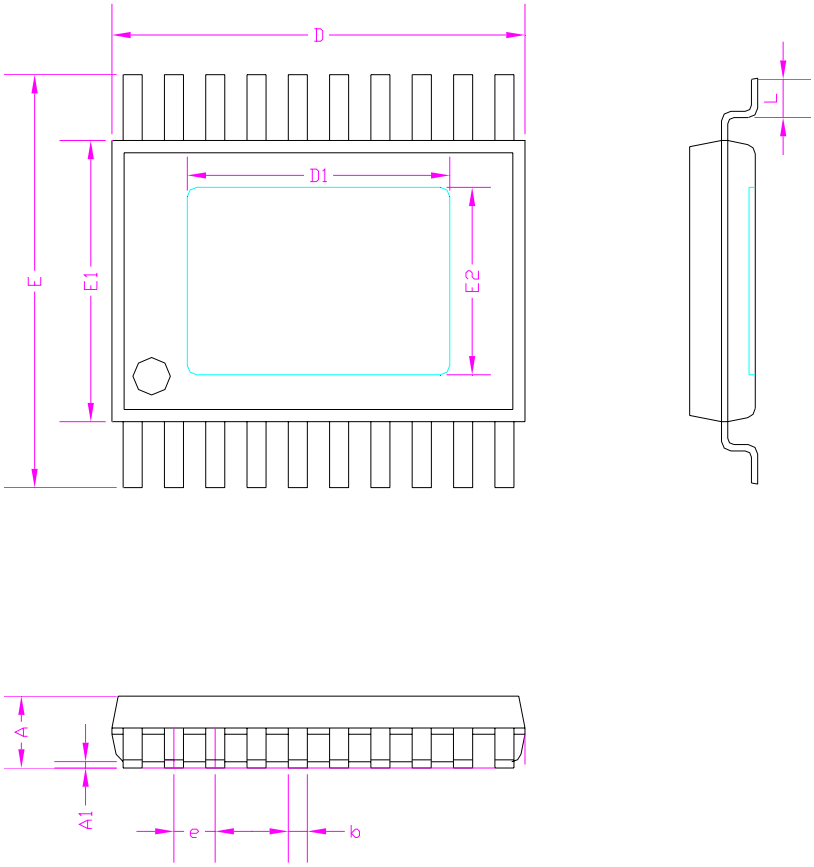
The thermal pad on the bottom of the EUA6027A should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 13 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane.

For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25℃,a larger copper plane or forced-air cooling will be required to keep the EUA6027A junction temperature below the thermal shutdown temperature (150℃). In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.

Package Information

TSSOP-20 (FD)



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.20	-	0.047
A1	0.00	0.15	0.000	0.006
b	0.19	0.30	0.007	0.012
E1	4.40		0.173	
D	6.50		0.256	
D1	3.77		0.148	
E	6.20	6.60	0.244	0.260
E2	2.70		0.106	
e	0.65		0.026	
L	0.45	0.75	0.018	0.030