

## 500kHz Synchronous Step-Up Converter with 600mA LDO

### DESCRIPTION

The EUP2412 provides a high efficiency 500kHz synchronous step-up converter and a low noise, high PSRR, low dropout (LDO) fixed output linear regulator with independent enable pins. EUP2412 input voltage range is 2.2V to 5.5V, making it ideal for applications with either a 2-cell NiMH/NiCd or a single-cell lithium-ion/polymer batteries.

The EUP2412 500kHz fixed frequency synchronous step-up converter uses smaller external components producing a compact solution for a wide range of load currents. Integrated N-Channel main switch and P-Channel synchronous rectifier greatly improve converter efficiency. Internal soft-start function reduces inrush current. The EUP2412 synchronous step-up convert regulates the output voltage up to 6V. When the synchronous step-up convert is disabled, the internal conduction path from SW to OUT is fully blocked. This output disconnect feature isolates the output from the input and reduces the shutdown current less than 0.1 $\mu$ A.

The EUP2412 LDO linear regulator has an independent input supply pin and is capable of delivering up to 600mA load current. It offers high output accuracy, extremely low dropout voltage, low quiescent current and fast start-up time. LDO is designed to work with low-ESR ceramic capacitors. Only a 2.2 $\mu$ F ceramic output capacitor can make the device stable over the entire load range. Optionally connecting a capacitor from BYPASS pin to GND gets high PSRR. The EUP2412 LDO output voltage is factory pre-set 1.2V, 1.8V, 2.5V, 2.8V or 3.3V.

The EUP2412 is available in a 10pin 3mm  $\times$  3mm TDFN-10 package.

### FEATURES

- Wide Input Voltage Range: 2.2V to 5.5V
- Synchronous Step-Up Converter:
  - 1.6Amp Peak Current Limit
  - 500kHz Fixed Switching Frequency
  - Output is Disconnected from the Input in Shutdown
  - Built-in Main Switch and Synchronous Rectifier
  - Internal Soft-Start
- Linear Regulator:
  - 600mA Output Current
  - 300mV Dropout Voltage at 600mA
  - 2% Initial Accuracy
  - Fast Line / Load Transient Response
  - 70dB PSRR at 1kHz
  - Stable with a 2.2 $\mu$ F Ceramic Output Capacitor
  - Output is Discharged to GND in Shutdown
  - Fixed Output Voltage: 1.2V to 3.6V
- Thermal Shutdown
- RoHS Compliant and 100% Lead (Pb)-Free
- Available in TDFN33-10 Package

### APPLICATIONS

- Portable Media Players
- Cellular Phones
- Bluetooth portable radios and Accessories
- Battery-Powered Equipments

### Typical Application Circuit

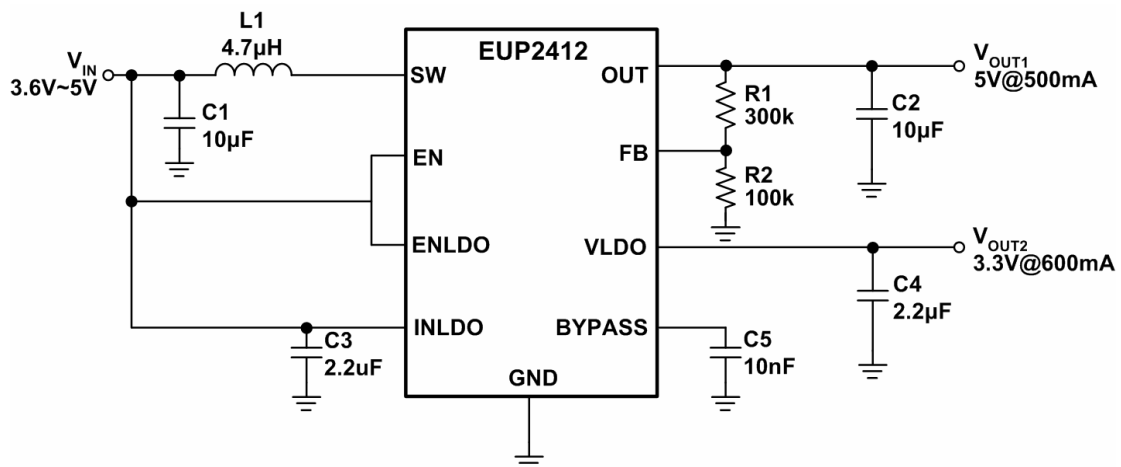


Figure 1. Application Circuit 1

Typical Application Circuit (continued)

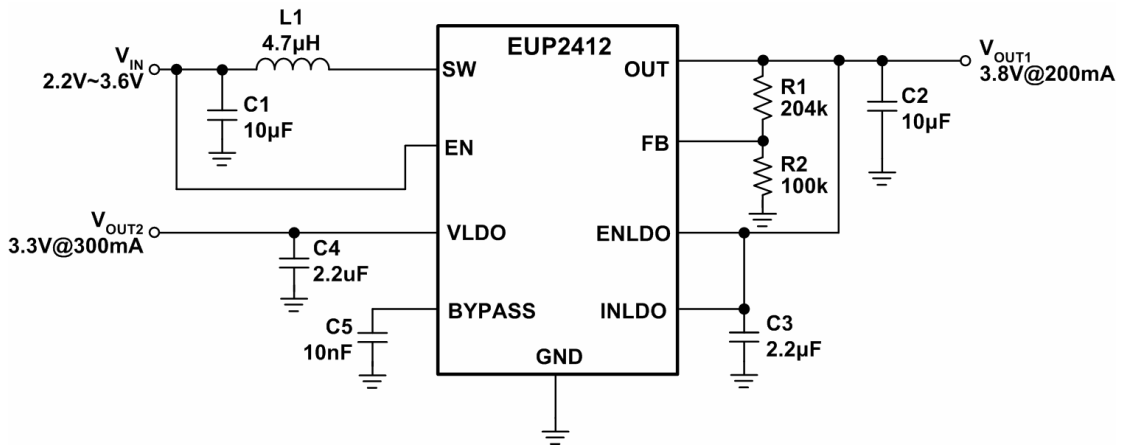


Figure 2. Application Circuit 2

Function Block Diagram

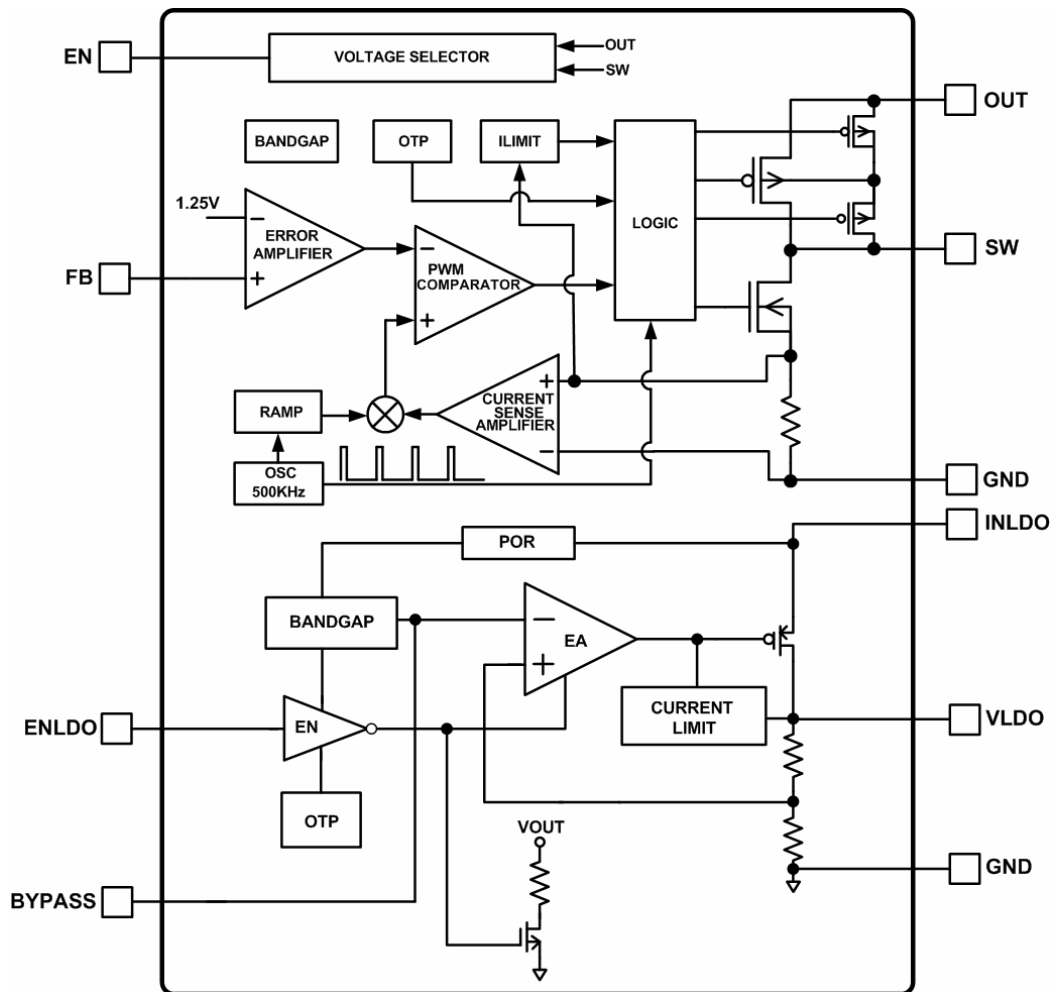


Figure 3. Functional Block Diagram

## Pin Configurations

Package Type	Pin Configurations
TDFN-10	<p>(TOP VIEW)</p> <p>Diagram showing the pin configurations for the TDFN-10 package (TOP VIEW). The pins are numbered 1 through 10, with their corresponding functions listed:</p> <ul style="list-style-type: none"> <li>1: GND</li> <li>2: SW</li> <li>3: OUT</li> <li>4: INLDO</li> <li>5: VLDO</li> <li>6: BYPASS</li> <li>7: ENLDO</li> <li>8: FB</li> <li>9: GND</li> <li>10: EN</li> </ul>

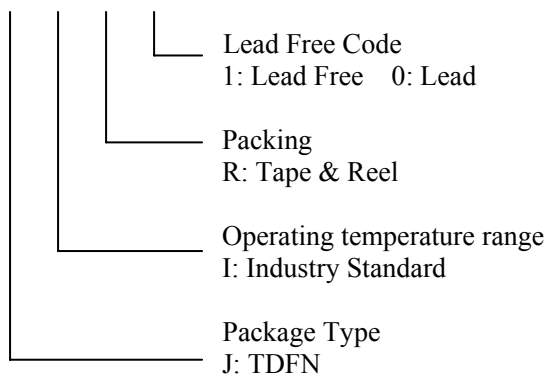
## Pin Description

PIN	NAME	DESCRIPTION
1,9	GND	Ground pins.
2	SW	Step-up converter switching node. SW is the drain of the internal low-side N-Channel MOSFET and high-side P-Channel MOSFET. Connect the inductor between input supply and SW.
3	OUT	Step-up converter output.
4	INLDO	LDO Input voltage. Bypass INLDO to GND with a 2.2 $\mu$ F or greater capacitor.
5	VLDO	LDO Output voltage. Bypass VLDO to GND with a 2.2 $\mu$ F or greater capacitor.
6	BYPASS	LDO internal reference bypass pin for ultra low noise and high PSRR application.
7	ENLDO	LDO Enable Pin. Connect this pin to ground or less than 0.4V to disable the device.
8	FB	Step-up converter feedback input (1.25V Nominal). Connect the external resistor divider tap to FB pin. The output voltage can be adjusted from 1.25V to 5.5V.
10	EN	Step-up converter Enable Pin. Connect this pin to ground or less than 0.4V to disable the device.

**Ordering Information**

Order Number	Package Type	Marking	Operating Temperature Range
EUP2412-12JIR1	TDFN-10	XXXXX P2412 1T	-40 °C to +85°C
EUP2412-15JIR1	TDFN-10	XXXXX P2412 1C	-40 °C to +85°C
EUP2412-18JIR1	TDFN-10	XXXXX P2412 1D	-40 °C to +85°C
EUP2412-25JIR1	TDFN-10	XXXXX P2412 1B	-40 °C to +85°C
EUP2412-28JIR1	TDFN-10	XXXXX P2412 1E	-40 °C to +85°C
EUP2412-33JIR1	TDFN-10	XXXXX P2412 1H	-40 °C to +85°C

EUP2412



**Absolute Maximum Ratings (1)**

- OUT, EN, FB to GND ----- -0.3V to 6V
- INLDO, ENLDO to GND ----- -0.3V to 6V
- VLDO to GND ----- -0.3V to (V<sub>INLDO</sub>+0.3V)
- SW Current (2) ----- -1.6A to +1.6A
- Junction Temperature ----- 150
- Storage Temperature Range ----- -65 to +150
- Lead Temperature ----- 260
- Thermal Resistance  $\theta_{JA}$  (TDFN-10) ----- 48 /W
- ESD Rating  
Human Body Model ----- 2kV

**Recommended Operating Conditions (3)**

- V<sub>IN</sub> ----- 2.2 to 5.5V
- V<sub>EN</sub>, V<sub>ENLDO</sub> ----- 0 to 5.5V
- Operating Temperature Range ----- -40 to +85

Note (1): Stress beyond those listed under “Absolute Maximum Ratings” may damage the device.

Note (2): SW has internal clamp diodes between GND-SW and SW-OUT. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Note (3): The device is not guaranteed to function outside the recommended operating conditions.

**Electrical Characteristics**

T<sub>A</sub>=+25 , V<sub>IN</sub>= V<sub>EN</sub>=2.4V, V<sub>INLDO</sub>=V<sub>ENLDO</sub>=4.3V, unless otherwise specified.

Parameter	Conditions	EUP2412			Unit
		Min.	Typ.	Max.	
<b>LDO Linear Regulator</b>					
Input Voltage INLDO		2.5		5.5	V
POR Threshold			2.1		V
POR hysteresis			0.4		V
Quiescent Current	I <sub>LOAD</sub> =0mA		120	180	μA
Shutdown Current	V <sub>ENLDO</sub> =0V		0.1	1	μA
Power Supply Ripple Rejection	V <sub>IN</sub> =3.3V+1V <sub>P-P</sub> , f=1kHz, I <sub>LOAD</sub> =10mA		70		dB
	V <sub>IN</sub> =3.3V+1V <sub>P-P</sub> , f=10kHz, I <sub>LOAD</sub> =10mA		70		
ENLDO Logic High Voltage	T <sub>A</sub> =-40 to +85	1.5			V
ENLDO Logic Lo Voltage	T <sub>A</sub> =-40 to +85			0.4	V
ENLDO Input Current	V <sub>IN</sub> =5V, V <sub>EN</sub> =5V or 0V	-1		1	μA
Start-up Time	C <sub>BYPASS</sub> =10nF		120		μs
VLDO Output Voltage Accuracy	I <sub>OUT</sub> =10mA	-2		+2	%
	I <sub>OUT</sub> =10mA, T <sub>A</sub> =-40 to +85	-3		+3	
Output Line Regulation	3.8V<V <sub>INLDO</sub> <5.5V, I <sub>OUT</sub> =10mA		0.04	0.1	%/V
Output Load Regulation	1 mA <I <sub>OUT</sub> <600mA		17	30	mV
Dropout Voltage (4)	I <sub>LOAD</sub> =300mA		180	240	mV
	I <sub>LOAD</sub> =600mA		360	450	
Maximum Output Current		600			mA
Short Circuit Current Limit		600	900		mA

**Electrical Characteristics**

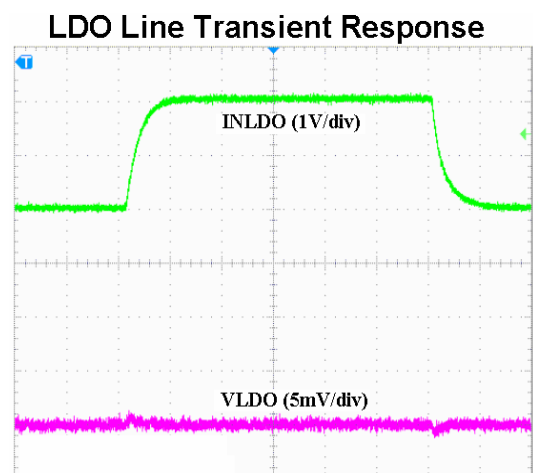
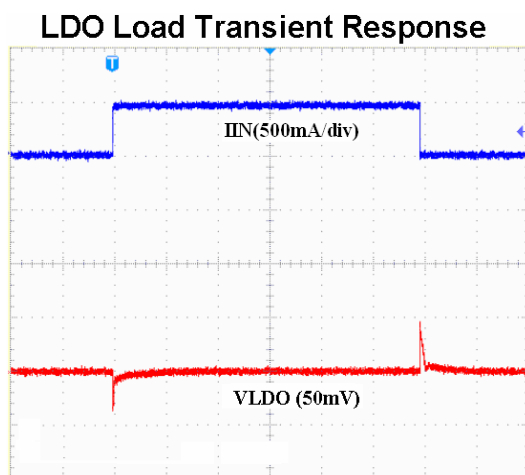
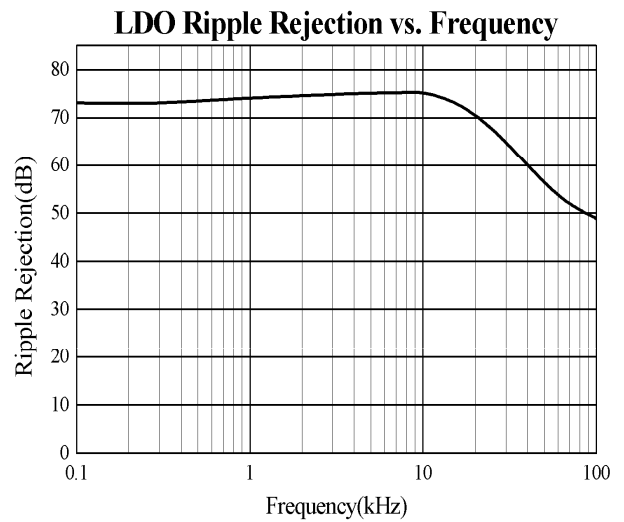
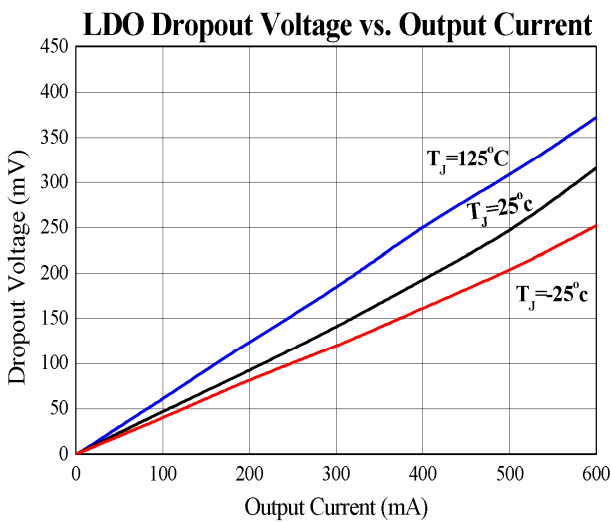
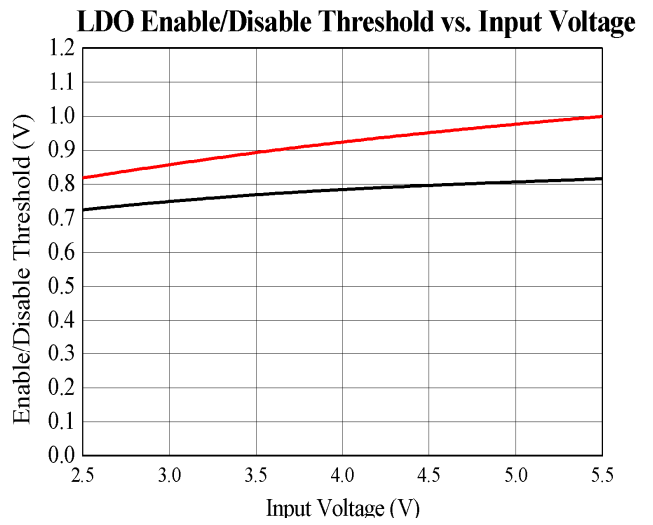
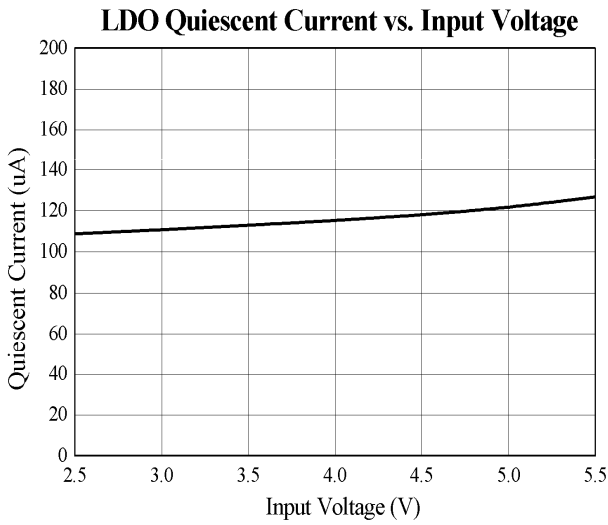
$T_A=+25$  ,  $V_{IN}=V_{EN}=2.4V$ ,  $V_{INLDO}=V_{ENLDO}=4.3V$ , unless otherwise specified.

Parameter	Conditions	EUP2412			Unit
		Min	Typ	Max.	
<b>Step-up Converter</b>					
Supply Voltage $V_{IN}$		2.2		5	V
Output Voltage Range $V_{OUT}$		2.5		6	V
Shutdown Current	$V_{EN}=V_{OUT}=0V$ , $V_{SW}=5V$		0.05	1	$\mu A$
Supply Current	$V_{FB}=1.3V$		390		$\mu A$
Feedback Voltage FB		1.2	1.25	1.3	V
Feedback Input Current	$V_{FB}=1.2V$		50		nA
Switching Frequency		310	500	690	KHz
Maximum Duty Cycle		80	85	90	%
EN Input Logic Lo Voltage				0.4	V
EN Input Logic Hi Voltage		1.4			V
EN Pull Down Resistor			1		$M\Omega$
Low-Side On Resistance	$V_{OUT}=3.3V$		450		$m\Omega$
Low-Side Switch Peak Current Limit		1	1.6	2	A
High-Side On Resistance	$V_{OUT}=3.3V$		650		$m\Omega$
<b>Over Temperature Protection</b>					
Thermal Shutdown			160		$^{\circ}C$
Thermal Shutdown Hysteresis			30		$^{\circ}C$

Note (4): Dropout is defined as  $V_{IN}-V_{OUT}$  when  $V_{OUT}$  is 100mV below the value of  $V_{OUT}$  for  $V_{IN}=V_{OUT}+0.5V$ .

**Typical Operating Characteristics**

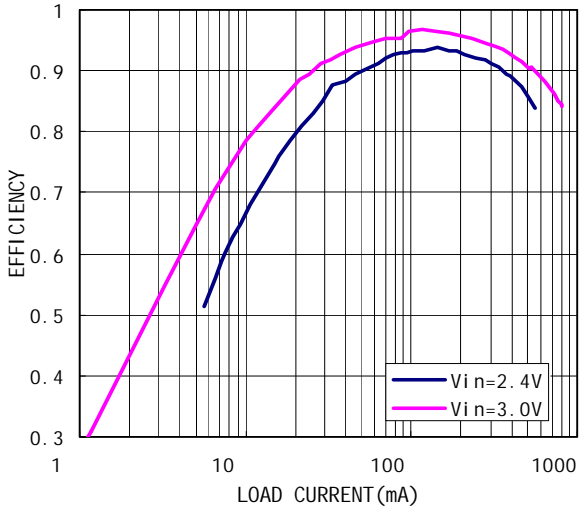
$V_{IN} = 2.4V$ ,  $V_{OUT} = 3.5V$ ,  $V_{INLDO} = 4.3V$ ,  $C1=C2=10\mu F$ ,  $L1=4.7\mu H$ ,  $R1 = 178K\Omega$ ,  $R2 = 100K\Omega$ ,  $C3=C4=2.2\mu F$ ,  $C5=10nF$  (See Figure 1).



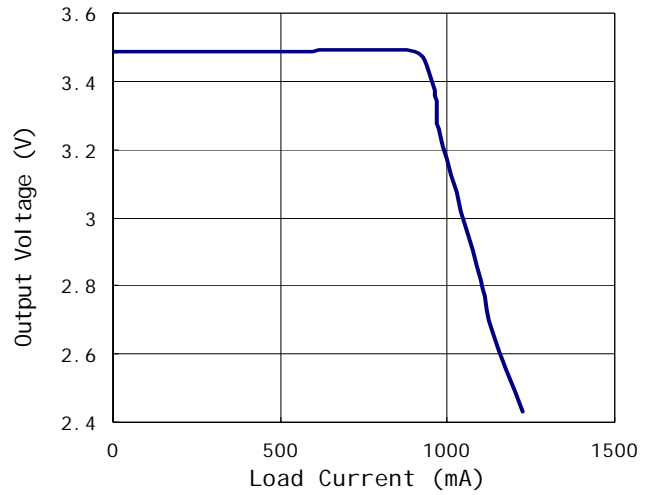
**Typical Operating Characteristics (Continued)**

$V_{IN} = 2.4V$ ,  $V_{OUT} = 3.5V$ ,  $V_{INLDO} = 4.3V$ ,  $C1=C2=10\mu F$ ,  $L1=4.7\mu H$ ,  $R1 = 178K\Omega$ ,  $R2 = 100K\Omega$ ,  $C3=C4=2.2\mu F$ ,  $C5=10nF$  (See Figure 1).

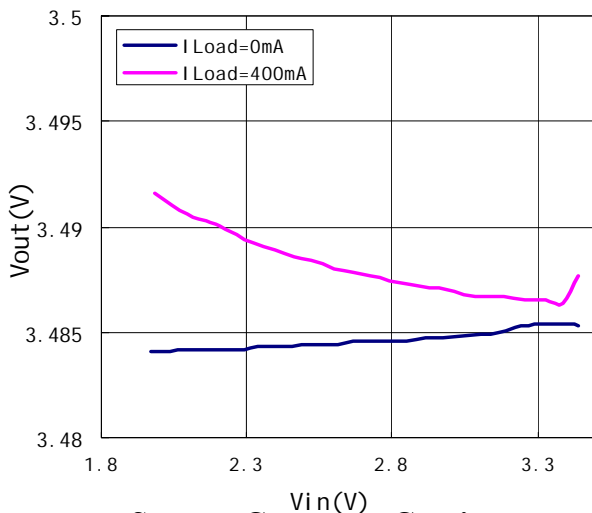
**Step-up Converter Efficiency vs Load Current**



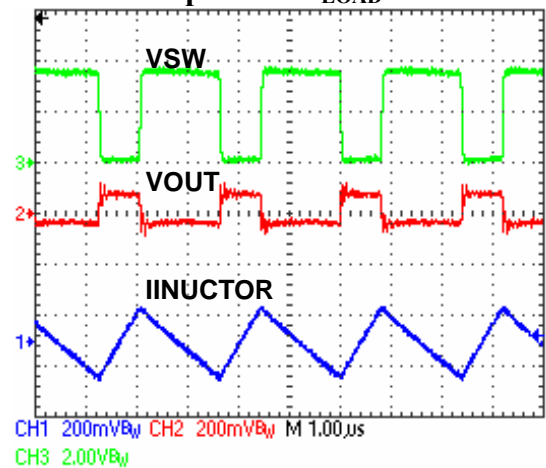
**Step-up Converter Load Regulation**



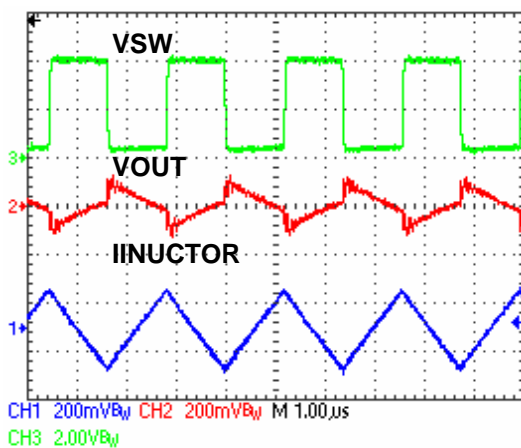
**Step-up Converter Line Regulation**



**Step-up Converter Continuous Mode Operation  $I_{LOAD}=20mA$**



**Step-up Converter Continuous Mode Operation  $I_{LOAD}=400mA$**

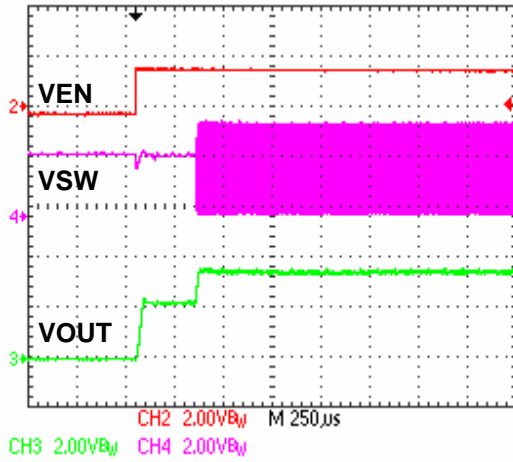




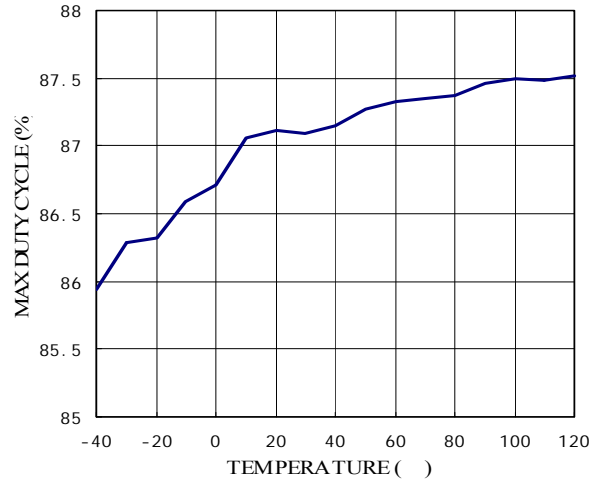
**Typical Operating Characteristics (continued)**

Operating Conditions :  $V_{IN} = 2.4V$ ,  $V_{OUT} = 3.5V$ ,  $C_{IN} = 10\mu F$ ,  $C_{OUT} = 10\mu F$ ,  $L1 = 4.7\mu H$ ,  $R1 = 178K\Omega$ ,  $R2 = 100K\Omega$

**Step-up Converter Startup**  
 $R_{LOAD} = 16\Omega$



**Step-up Converter Maximum Duty Cycle vs Temperature**



## LDO Linear Regulator Function Descriptions

The EUP2412 LDO is a high output current, low dropout linear regulator with fast transient response and high PSRR. It offers high output accuracy, extremely low dropout voltage, low quiescent current and fast start-up time. It is designed to work with low-ESR ceramic capacitor, reducing the amount of the PCB area. Only a 2.2 $\mu$ F ceramic capacitor can make the device stable over the whole load range.

As shown in the function block diagram, the LDO is composed of the bandgap reference voltage, the error amplifier, P-channel MOSFET pass transistor, internal resistor divider and some additional protection circuits. The reference voltage, connected to the cathode terminal of the error amplifier, compares with the feedback voltage to regulate the output voltage to make it constant over the whole load range. If the feedback voltage is lower than the reference voltage, the pass transistor gate is pulled low to increase its conductivity. This allows more current to flow to the output and increases the output voltage. If the feedback voltage is higher than the reference voltage, the pass transistor allows less current to flow to the output. The feedback point is the output of the internal or external resistor divider connected to the VLDO pin.

### Supply Input Power on Reset

The input voltage supplies current to the output and the operation voltage of the internal circuit. The input voltage is monitored for power on reset (POR) to ensure the LDO is disabled when the input voltage is not high enough for normal operation. The POR threshold voltage is 2.1V at VIN rising typically.

### Enable/Shutdown

The LDO is disabled when the ENLDO pin is connected to ground or the voltage less than 0.4V, reducing the quiescent current to less than 1 $\mu$ A. In the shutdown mode the error amplifier, the reference voltage, the driver and the pass transistor are all disabled. Make this pin higher than 1.5V to enable the device. ENLDO can not be floated.

### Soft Stop

When the LDO is disabled, an internal 400 $\Omega$  resistor is connected between VLDO and GND. This is intended to discharge C<sub>OUT</sub>. The internal resistor is not used when the device turns on.

### Current Limit

The LDO includes a current limit circuit to monitor the gate voltage of the pass transistor to limit the output current. When the output current is higher than the over-current limit, the circuit will clamp the gate voltage of the pass transistor to keep the current flowing to the output. The typical value is 0.9A.

## Step-up Converter Function Descriptions

The EUP2412 step-up converter uses 500kHz fixed-frequency, current-mode regulation architecture to regulate the output voltage. The Step-up converter measures the output voltage through an external resistive voltage divider and compares that to the internal 1.25V reference to generate the error voltage. The current-mode regulator compares the error voltage to the inductor current to regulate the output voltage. When the step-up converter is disabled (EN = Low), both power switches are off. There is no current path from SW to OUT. Therefore, the output voltage discharges to ground. When the step-up converter is enabled (EN = High), a limited start-current charges the output capacitor through the P-Channel MOSFET until the output voltage rising close to input voltage, then the part operates in force PWM mode to regulate the output voltage to the final value.

The EUP2412 step-up converter features a soft-start timer to limit the error amplifier output voltage during startup. to prevent. This prevents excessive inrush current causing premature termination of the source voltage at startup. The soft-start also limits the inductor current at startup, forcing the input current to rise slowly to regulate the output voltage.

## Application Information (See Figure 1 and 2)

### LDO Input Capacitor C3

A 2.2uF capacitor is required between the INLDO pin and the GND pin. Place it as close as possible to the device. There are no requirements for the ESR on the input capacitor, but the tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be 2.2uF over the whole operating temperature range.

### LDO Output Capacitor C4

The EUP2412 LDO is designed specifically to work with very small ceramic output capacitors. A 2.2uF to 10uF with 5mΩ to 500mΩ ESR range is suitable in the EUP2412 LDO application circuit. The ESR of a typical 2.2uF ceramic capacitor is about 20mΩ, which easily meets the ESR requirement for stability. The EUP2412 LDO will remain stable and in regulation with no external load. This is special important in CMOS RAM keep-alive applications.

### Step-up Converter Input Capacitor C1

An input capacitor is required to supply the AC ripple current to the inductor, while limiting noise at the input source. Multi-layer ceramic capacitors are the best choice as they have extremely low ESR and are available in small footprints. Use an input capacitor value of 4.7μF or greater. This capacitor must be placed physically close to the device.

### Step-up Converter Output Capacitor C2

A single 4.7μF to 10μF ceramic capacitor usually provides sufficient output capacitance for most applications. Larger values up to 22μF may be used to obtain extremely low output voltage ripple and improve transient response. The impedance of the ceramic capacitor at the switching frequency is dominated by the capacitance, and so the output voltage ripple is mostly independent of the ESR. The output voltage ripple  $V_{RIPPLE}$  is calculated as:

$$V_{RIPPLE} = \frac{I_{LOAD}(V_{OUT} - V_{IN})}{V_{OUT} \times C2 \times f_{SW}}$$

Where  $V_{IN}$  is the input voltage,  $I_{LOAD}$  is the load current,  $C2$  is the capacitance of the output capacitor and  $f_{SW}$  is the 500KHz switching frequency.

### Capacitor Characteristics

More consideration should be taken when selecting the capacitor because its capacitance can vary with temperature. The capacitor type X7R or X5R, which operates over a temperature range of -40 to +85, will only vary within ±15%. Some large value ceramic capacitors are manufactured with Z5U or T5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature goes from 25 to 85. Therefore the capacitor type X7R or X5R is recommended in applications where the ambient temperature will change significantly above or below 25.

### Step-up Converter Inductor L1

The inductor is required to force the output voltage higher while being driven by the lower input voltage. A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 30%-50% of the maximum input current. Make sure that the peak inductor current is below the minimum current limit at the duty cycle used (to prevent loss of regulation due to the current limit variations).

Calculate the required inductance value  $L$  using the equations:

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{sw} \times \Delta I}$$

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{LOAD(MAX)}}{V_{IN} \times \eta}$$

$$\Delta I = (30\% - 50\%) I_{IN(MAX)}$$

Where  $I_{LOAD(MAX)}$  is the maximum load current,  $\Delta I$  is the peak-to-peak inductor ripple current and  $\eta$  is efficiency. For the EUP2412, typically, 4.7μH is recommended for most applications. Choose an inductor that does not saturate at the peak switch current as calculated above with additional margin to cover heavy load transients and extreme startup conditions.

### Setting the Step-up Converter Output Voltage

Set the step-up regulator output voltage by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the 1.25V feedback voltage. Use a 100kΩ resistor for  $R2$  of the voltage divider. Determine the high-side resistor  $R1$  by the equation:

$$R1 = \frac{V_{OUT} - V_{FB}}{\left(\frac{V_{FB}}{R2}\right)}$$

Where  $V_{OUT}$  is the output voltage,  $V_{FB}$  is the 1.25V feedback voltage and  $R2=100k\Omega$ .

**Thermal Considerations**

Thermal protection limits power dissipation in EUP2412. When the operation junction temperature exceeds 160°C, the OTP circuit starts the thermal shutdown function and turns off both LDO and step-up regulator. The device turns on again after the junction temperature cools by 30°C.

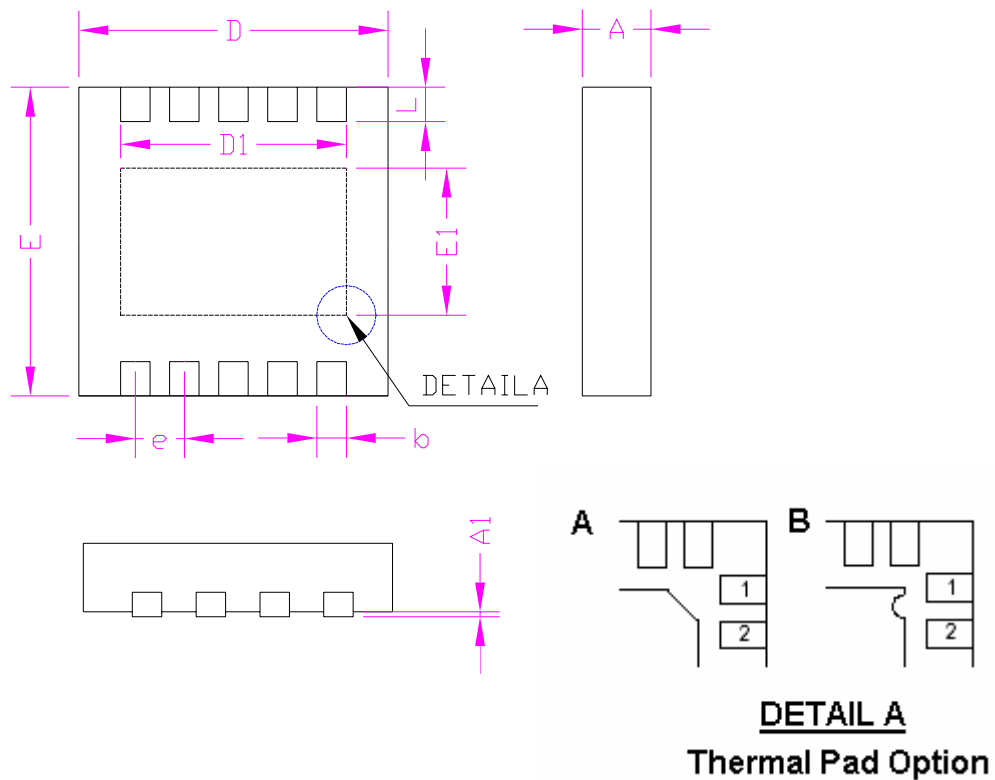
For continuous operation, do not exceed absolute maximum operation junction temperature 150°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where  $T_{J(MAX)}$  is the maximum operation junction temperature 150°C,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance.

Package Information

TDFN-10



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
D1	2.50		0.098	
D	2.90	3.10	0.114	0.122
E1	1.70		0.067	
E	2.90	3.10	0.114	0.122
L	0.30	0.50	0.012	0.020
b	0.18	0.30	0.007	0.012
e	0.50		0.020	
D1	2.40		0.094	