EUTECH
MICROELECTRONICS

EUP2592

8-String White LED Driver for LCD Panel Application

DESCRIPTION

The EUP2592 is an 8-channel WLED driver that controls WLED current for LCD backlight application. The EUP2592 is capable of driving up to eight strings in parallel and 12 LEDs per string. Each string is terminated with ballast that achieves ±1.5% current regulation accuracy between strings, ensuring even LED brightness. The EUP2592 have wide input voltage range from 4.5V to 28V, and provide adjustable 5mA to 50mA LED current. EUP2592 uses an external PWM signal to control WLED dimming. EUP2592 has built in many fault protections.

The EUP2592 step-up controller features an internal 150mΩ (typ.), 48V (max.) power MOSFET with local current-sense amplifier for accurate cycle-by-cycle current limit. This architecture greatly simplifies the external circuitry and saves PCB space. The EUP2592 minimizes the headroom voltage of output and power loss by detecting the highest LED forward voltage dynamically. Low-feedback voltage at each LED string 360mV (typ.) at 20mA LED current helps reduce power loss and improve efficiency.

The EUP2592 internally generates a PWM signal for accurate WLED dimming control. The PWM frequency is resistor programmable, while PWM duty cycle is controlled directly from an external PWM signal or through an adjustable resistor at PWMO pin. This internal PWM dimming control provides a dimming range with 8-bit resolution to maximize battery life. The EUP2592 WLED brightness can also be directly modulated with an external PWM signal from 100Hz to 10kHz.

The EUP2592 have extensive protection that include string open and short detection, over voltage protection, over-temperature protection and an optional input over-current protection with an external fault disconnect switch.

FEATURES

- Up to 8 strings in parallel and 12 LEDs per string Maximum number of LEDs that can be driven is 96 (8x12) WLEDs
- Accurate PWM Dimming Control with 8-bit Resolutions
- External Direct PWM Dimming Control Mode
- Wide Input Voltage Range 4.5V to 28V
- Internal 0.15Ω 48V Power MOSFET
- ±1.5% LED Current Regulation Accuracy Between Strings
- Dynamic Headroom Control for LED Outputs
- Low String Feedback Voltage: 360mV at 20mA LED Current
- User Selectable Switching Frequency 500kHz and 1200kHz
- Multiple Fault Protections
  -LED Open Circuit Detection
  -LED Short Circuit Detection
  -Over-Temperature Protection
  -Output Over-Voltage Protection
  -Input over current protection
- Small 24-Pin, 4mm x 4mm, Thin TQFN Package
- RoHS Compliant and 100% Lead (Pb)-Free

APPLICATIONS

- Notebook Displays LED Backlighting
- LCD Monitor LED Backlighting

Typical Application Circuit

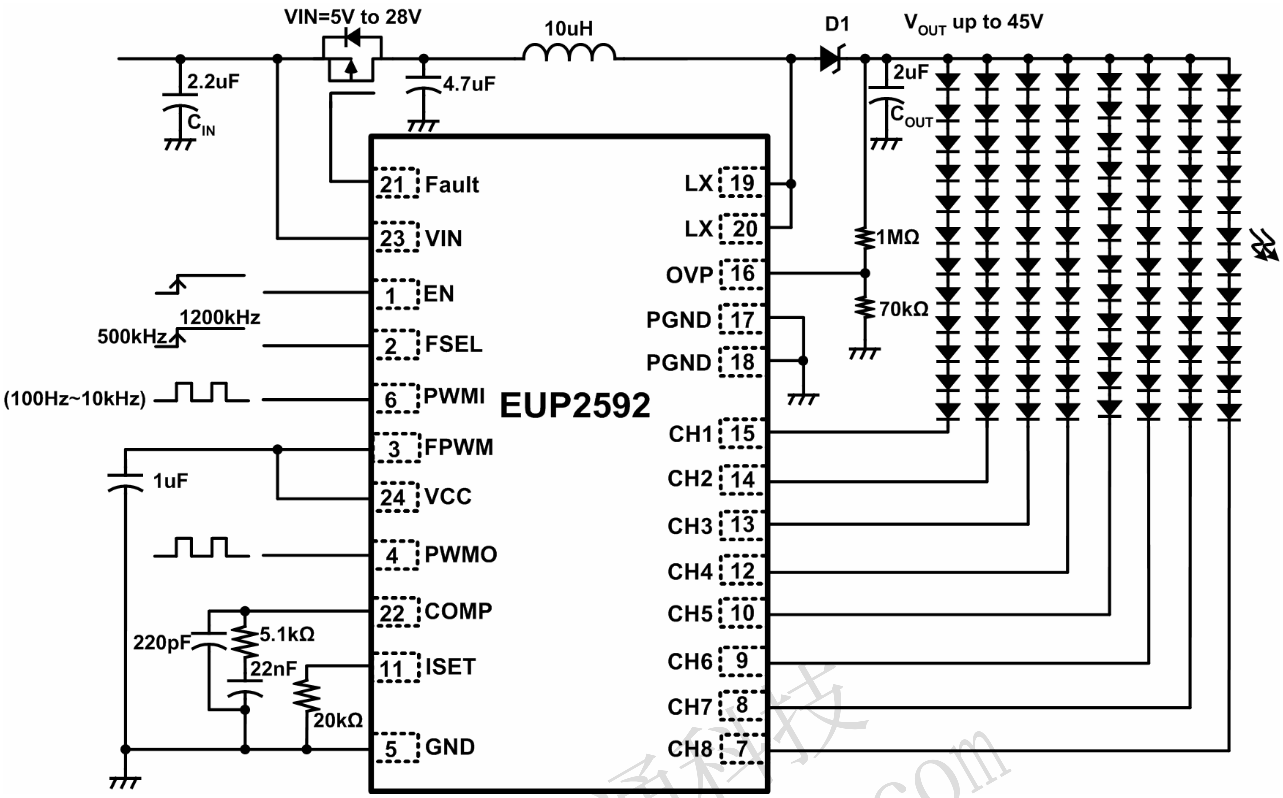


Figure 1. External Direct PWM Dimming Control with An External PWM Signal

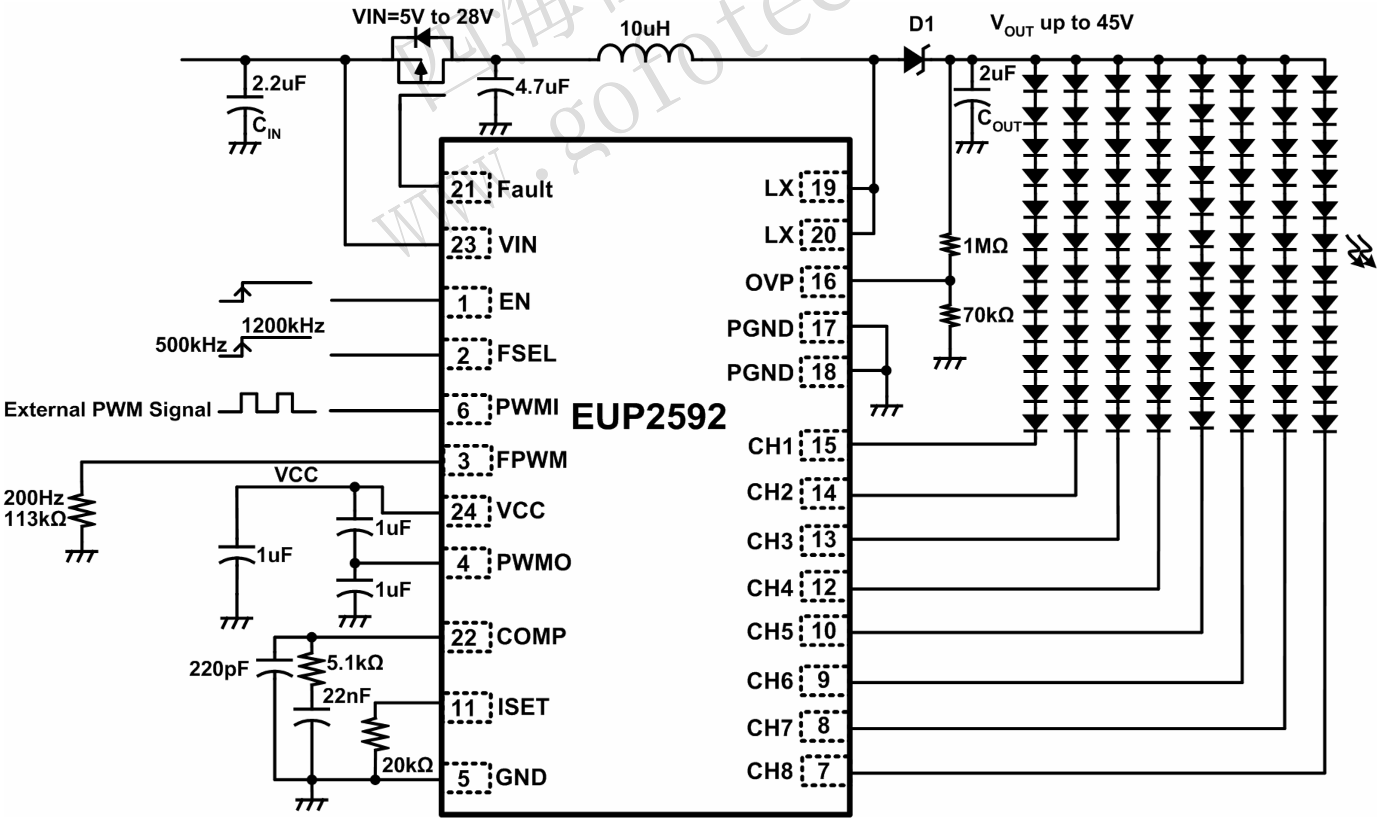


Figure 2. Internal PWM Dimming Control with An External PWM Signal

Typical Application Circuit (continued)

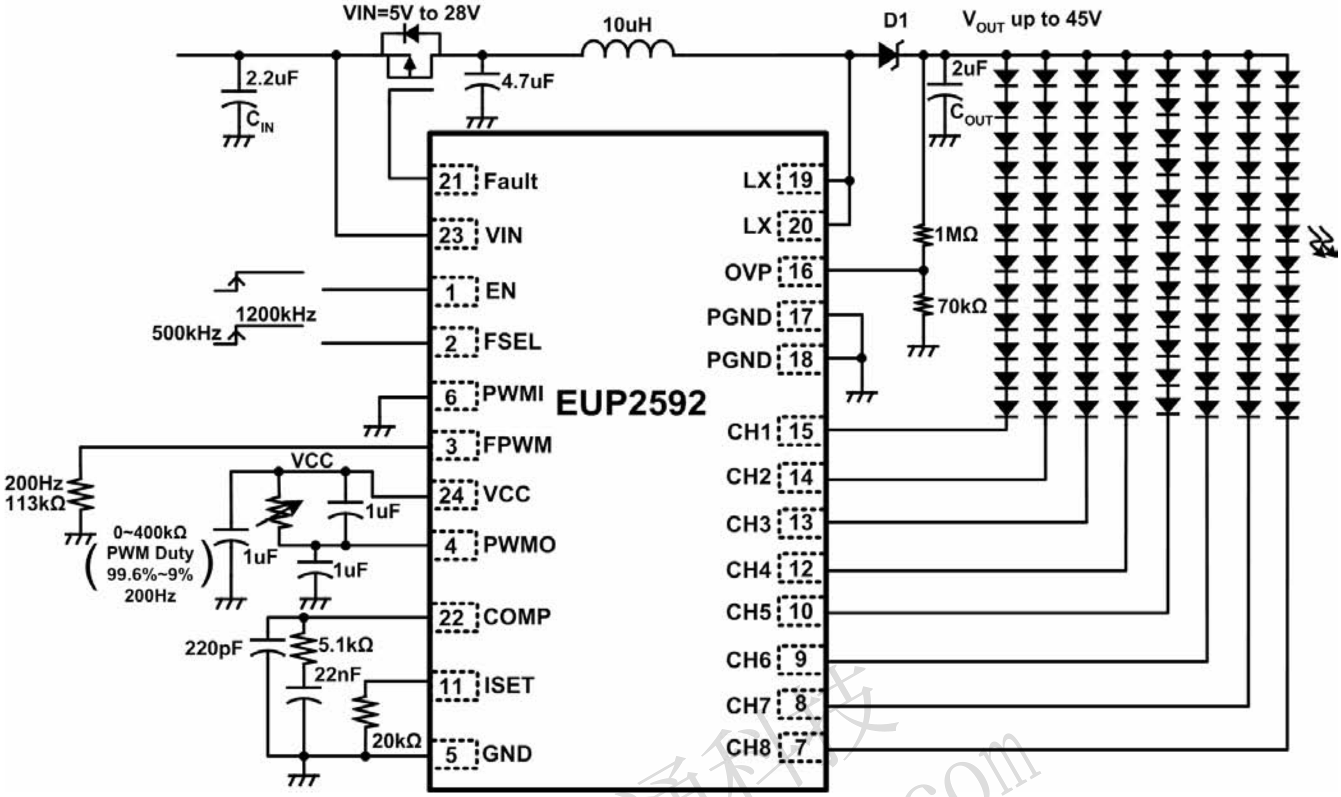


Figure 3. Internal PWM Dimming Control with An External Adjustable Resistor

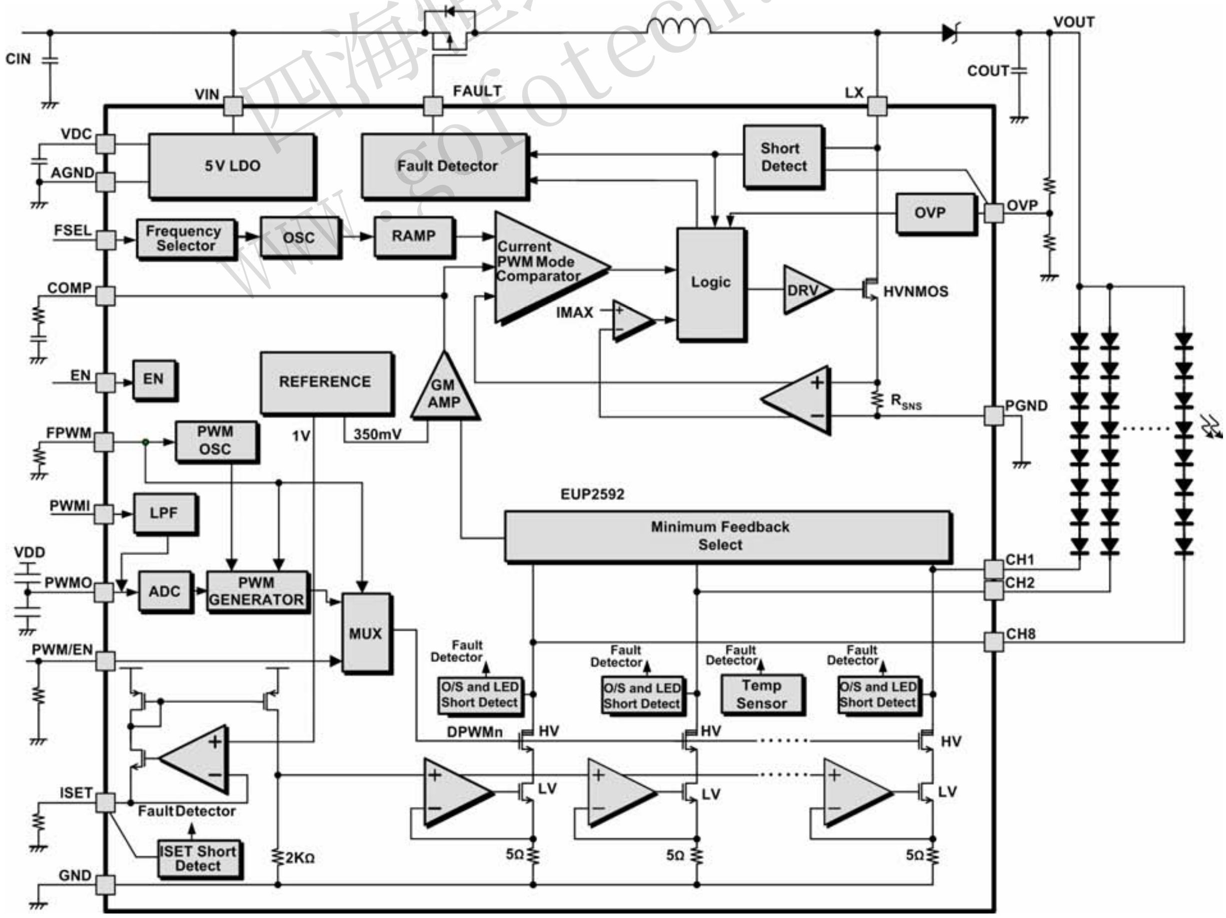
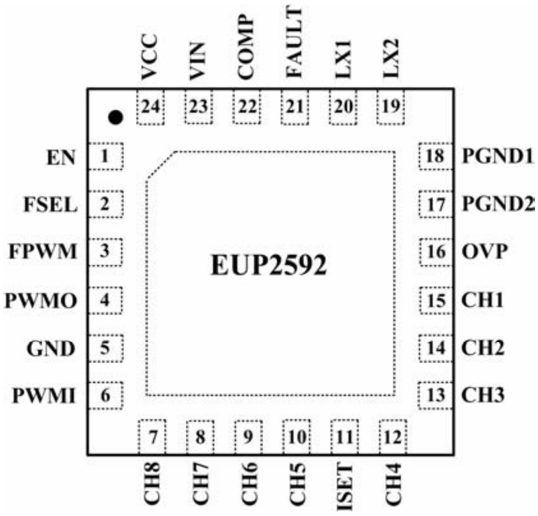


Figure 4. EUP2592 Functional Block Diagram

Pin Configurations

Package Type	Pin Configurations
TQFN-24	

Pin Description

PIN	TQFN-24	DESCRIPTION
1	EN	EN: Device Enable pin, active high. Connect EN to VCC to enable IC automatically.
2	FSEL	FSEL: Switching Frequency selection pin. Lo: 500kHz, Hi: 1.2MHz.
3	FPWM	DPMW Frequency set pin, connect a resistor to ground. f_{DPWM}=200Hz*113kΩ/R_{FPWM} Connect FPWM pin to VCC to enable PWMI direct control (See PWMI pin description 1. External Direct PWM Mode).
4	PWMO	Filtered PWM Signal Output. Connect 1uF capacitors from PWMO to VCC and GND. The capacitor forms a low-pass filter with an internal 40kΩ (typ.) resistor to filter the PWM signal into an analog signal whose level represents the duty cycle information of the input PWM signal. PWMO is input of the internal 8-bit ADC. The higher PWMO voltage is, and the bigger PWM duty cycle is. In the internal ADC PWM mode, the maximum PWM duty cycle is 99.6%.
5	GND	Analog ground.
6	PWMI	PWM Dimming Signal Input. This PWM signal is used for LED brightness control. This PWM signal is used for brightness control in 2 ways: 1. External Direct PWM Mode (FPWM=VCC). The PWM signal directly controls the dimming duty cycle and frequency. The input PWM signal frequency range is normally 100HZ to 10kHz. 2. Internal PWM mode (through the internal 8bit ADC, maximum duty 99.6%) The input PWMI signal is filtered out and converted to the PWMO DC voltage which is proportional to the internal PWM signal duty cycle. The PWMO voltage sets EUP2592 dimming duty cycle. The EUP2592 dimming frequency is programmed by the resistor value at the FPWM pin.
7	CH8	String 8 LED current source. Leave it floating if not used.
8	CH7	String 7 LED current source. Leave it floating if not used.
9	CH6	String 6 LED current source. Leave it floating if not used.
10	CH5	String 5 LED current source. Leave it floating if not used.
11	ISET	Full-Scale LED Current Adjustment Pin. The resistance from ISET to GND controls the full-scale current in each LED string. The acceptable resistance range is 8kΩ < RISET <80kΩ, which corresponds to full-scale LED current of 50mA>ICH_MAX>5mA. ISET voltage is around 1.0V. There is a short protection at this pin to prevent LED current too large (ISET UVLO threshold 0.85V).

Pin Description (continued)

PIN	TQFN-24	DESCRIPTION
12	CH4	String 4 LED current source. Leave it floating if not used.
13	CH3	String 3 LED current source. Leave it floating if not used.
14	CH2	String 2 LED current source. Leave it floating if not used.
15	CH1	String 1 LED current source. Leave it floating if not used.
16	OVP	Output over-voltage feedback input. Connect OVP to the tap point of the resistor divider between output and ground.
17, 18	PGND1, PGND2	Step-up converter Power Ground.
19, 20	LX1,LX2	Step-up converter Power MOSFET Drain.
21	FAULT	Gate control output of the fault disconnect switch.
22	COMP	Step-Up Converter Compensation Pin. Connect a 22nF ceramic capacitor in series with a 5.1k resistor from COMP to GND. When the EUP2592 shuts down, COMP is discharged to GND.
23	VIN	Input supply for the device and LED power.
24	VCC	5V Linear Regulator Output to power internal circuitry. If 4.5V<VIN < 5.5V, connect VCC directly to supply voltage of VIN. Bypass VCC to GND with a ceramic capacitor of 0.47µF or greater.
-	Thermal pad	Exposed Backside Pad. Solder to the circuit board ground plane with sufficient copper connection to ensure low thermal resistance.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP2592JIR1	TQFN-24	xxxxx P2592	-40 °C to +85°C

EUP2592 □ □ □ □

- Lead Free Code
  1: Lead Free 0: Lead
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  J: TQFN

Absolute Maximum Ratings (1)

- VIN to GND -- -0.3V to 30V
- FAULT to GND --- -0.3V to VIN+0.3V
- CH_, LX to GND--- -0.3V to +48V
- PGND to GND --- -0.3V to +0.3V
- VCC, OVP, ISET, COMP, PWMI to GND-------------------------------------- -0.3V to +6V
- EN, FSEL,FPWM and PWMO to GND--- -0.3V to +6V
- Continuous Power Dissipation (TA = +70°C)
  24-Pin Thin QFN [derate 20.3mW/°C (JEDEC high-k 2s2p) above +70°C] 1624mW
- Junction Temperature -- 150°C
- Lead Temperature (Soldering, 10sec.) --- 260°C
- Storage Temperature Range -- -65°C to +150°C

Operating Conditions (2)

- Operating Temperature Range --- -40°C to +85°C
- Supply Voltage , VIN--- 5.5V to 28V

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.
Note (2): The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

(Circuit of Figure 1, VIN=12V, GND=PGND=0V, ISET=20kΩ, VPWMI=VEN=5V, T_A= 40°C to +85°C, unless otherwise noted. Typical values are at T_A= +25°C.)

Symbol	Parameter	Conditions	EUP2592			Unit
			Min	Typ	Max.	
VIN	VIN Supply voltage	VCC=OPEN	5.5		28	V
		VIN=VCC, External VCC mode	4.5		5.5	
I_IN	VIN Supply current	CH_=1V (Stop boost SW) or PWMI=0V		1.5	3	mA
ISHUT	VIN Shutdown Current	EN=0V,VIN=28V		10	25	µA
VENH	EN Logic Hi Level		2.1			V
VENL	EN Logic Lo Level				0.8	V
Linear Regulator						
VCC	VCC output voltage	5.5V< VIN <28V, CH_=1V	4.7	5.0	5.3	V
I_VCC	VCC Current Limit	VIN=12V,VCC is forced 4.5V, CH=1V	15	40	70	mA
VUVLO	VCC Under-voltage Lockout Threshold	Rising edge, typical hysteresis = 200mV	3.7	4.05	4.4	V
LED Current						
VISET	ISET Regulation Voltage	RISET=20kΩ		1		V
UVLO_ ISET	ISET UVLO Threshold			0.85		V
ILED1	CH_ Full Scale Current	RISET=11.4kΩ, TA=+25ºC	33.6	35	36.4	mA
ILED2		RISET=20kΩ, T_A=+25ºC	19.2	20	20.8	mA
Imatch1	Channel-to-Channel current matching1	RISET=11.4kΩ, ILED=35mA, TA=+25ºC	-1.5		+1.5	%
Imatch2	Channel-to-Channel current matching2	RISET=20kΩ, $ILED_{TYP}$=20mA, T_A=+25ºC	-1.5		+1.5	%
ICH_LKG	ILED_ Leakage Current	PWMI=L, $V_{CH\_}$=45V			5	uA
VCH_MIN	Minimum CH_ Regulation Voltage	RISET=20kΩ, $ILED_{TYP}$=20mA, T_A=+25ºC (VCH=360mV*ILED/20mA)		360		mV

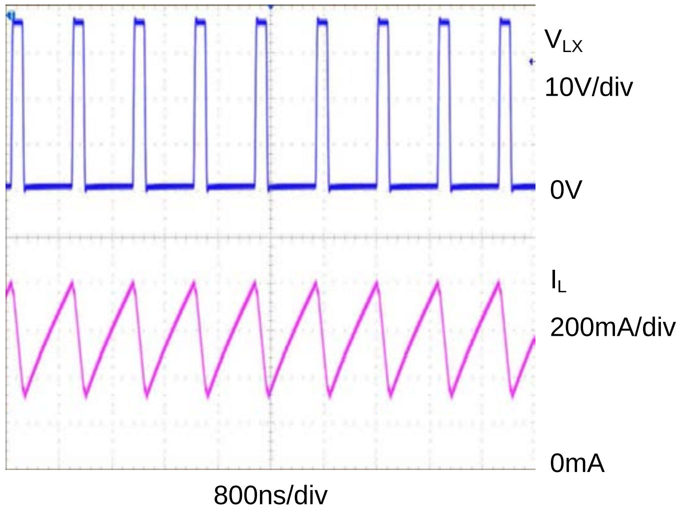
Electrical Characteristics (continued)

(Circuit of Figure 1, VIN=12V, GND=PGND=0V, ISET=20kΩ, VPWMI=VEN=5V, T_A= 40°C to +85°C, unless otherwise noted. Typical values are at T_A= +25°C.)

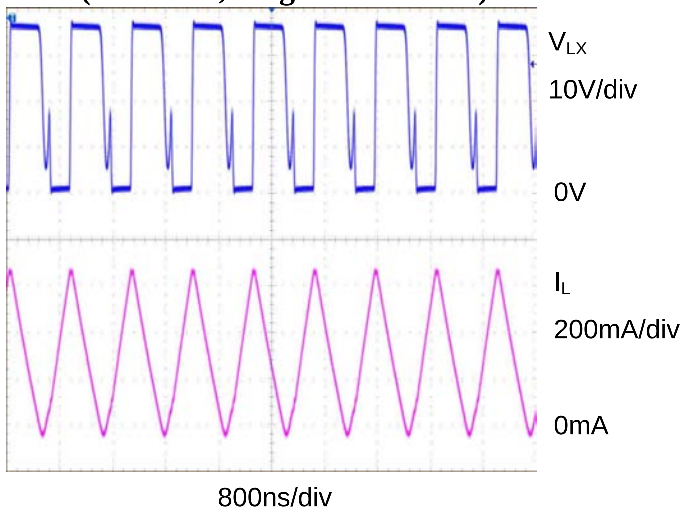
Symbol	Parameter	Conditions	EUP2592			Unit
			Min	Typ	Max.	
Boost converter						
GM	Error Amp Tansconductance			60		uA/V
Rds(on)	Internal Boost Switch On-resistance	ILX=200mA		150	250	mΩ
ILX_lkg	LX Leakage current	EN=Low, VLX=45V		5	10	uA
VFSELH	FSEL Logic Hi Level		2.1			V
VFSELL	FSEL Logic Lo Level				0.8	V
fosc0	Boost Switching Frequency	FSEL=GND	450	500	550	kHz
fosc1		FSEL=VCC	1080	1200	1320	
Dmax	Boost Maximum Duty Cycle		91	94	97	%
ISWlim	Boost FET Peak Current Limit	Duty=Dmax, TA =+25℃	2.8	3.5	4.2	A
PWM Dimming Controls						
tPWMImin	Minimum PWM Enable signal (PWMI)	An External Direct PWM Driving Signal		10		µs
VPWMIH	PWMI Input high level		2.1			V
VPWMIL	PWMI input low level				0.8	V
VPWMIhys	PWMI Trip Hysteresis			80		mV
	PWMI Input Frequency Range	Guaranteed by Design	0		1	MHz
R_PWMO	PWMO Output Impedance	PWMI=Lo or Hi	20	40	60	kΩ
FPWM	DPWM Oscillator Frequency	R_{FPWM}=113 kΩ	190	200	210	Hz
Fault Detections						
Tsd	Thermal Shutdown Threshold			150		ºC
Tsd_hys	Thermal shutdown hysteresis			30		ºC
Vovp	Over-voltage Threshold on OVP	Rising Edge	2.85	3.00	3.15	V
VSC_OVP	OVP Short Detection Level	VIN-VFAULT ≥ 5V or VFAULT<2V(VIN<5.5V)		220		mV
VSC_LX	LX Short Detection Level	VIN-VFAULT ≥ 5V or VFAULT< 2V(VIN<5.5V)		3		V
CH_OS	CH Over-voltage or LED Short			7		V
CH_UV	CH Under-voltage	PWMI=Hi		135		mV
Ifault	FAULT Pull-down current	No fault, VIN=12V, VFAULT=12V	15	20	25	uA
Vfault	FAULT Clamp voltage with respect to VIN	No fault, VIN=12V, VIN-VFAULT	6	8	10	V
I_pul _fault	FAULT Pulse Pull-up Current	LX or OVP Short Fault, VIN_VFAULT=1V		10		mA

Typical Operating Characteristic (Circuit of Figure 1, VIN = 12V, RISET =20kΩ, VPWMI = VCC, LEDs =12 series x 8 parallel strings, T_A = +25°C, unless otherwise noted.)

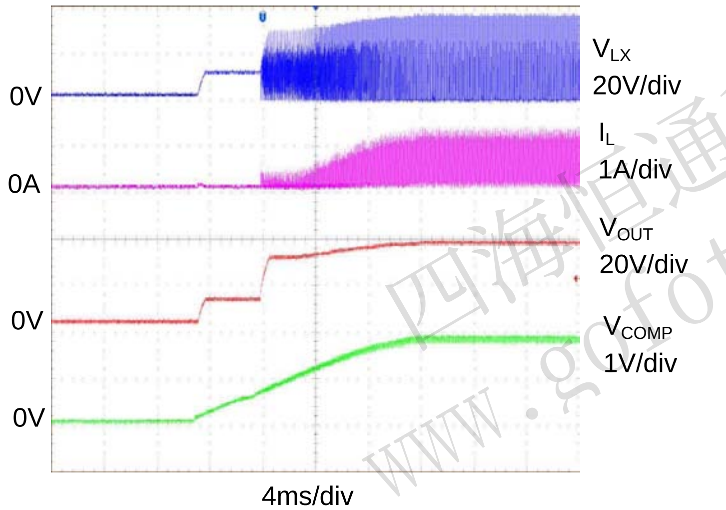
Switching Waveforms (VIN=7V, Brightness=100%)



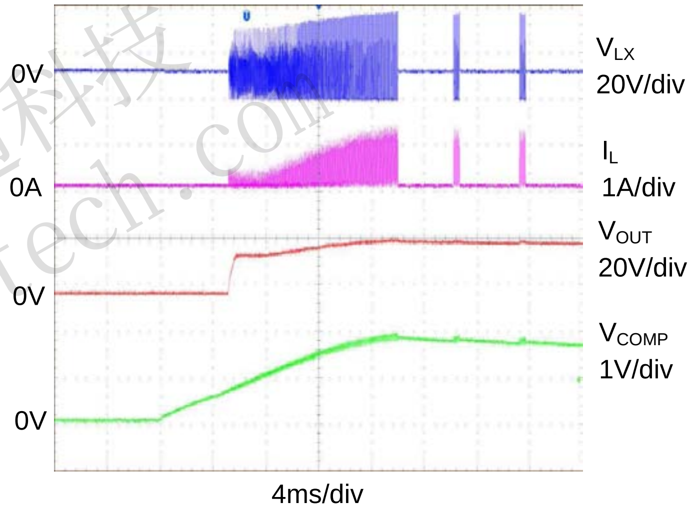
Switching Waveforms (VIN=20V, Brightness=100%)



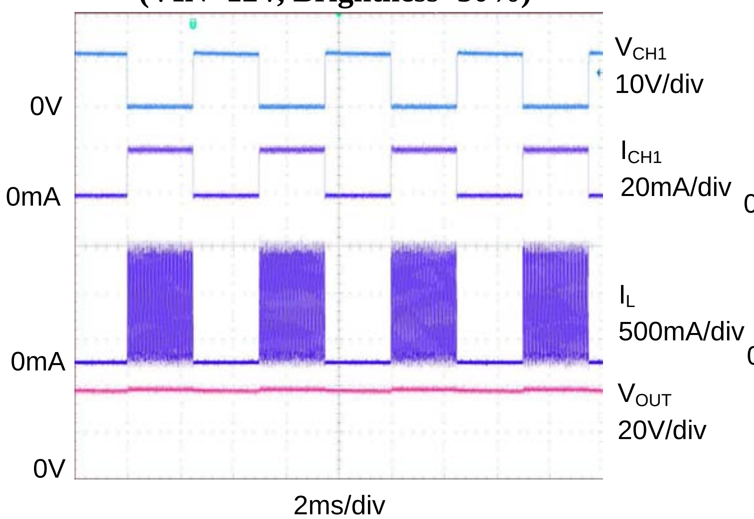
Start Waveforms (VIN=12V, Brightness=100%)



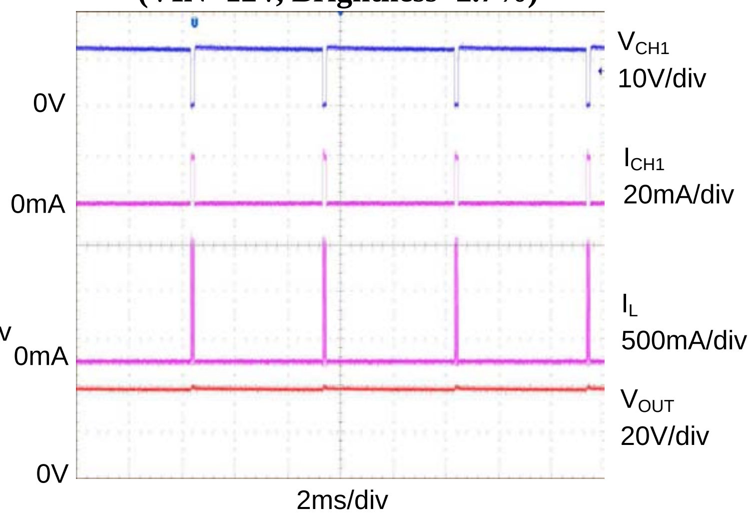
Start Waveforms (VIN=12V, Brightness=2.7%)



LED Current Waveforms (VIN=12V, Brightness=50%)

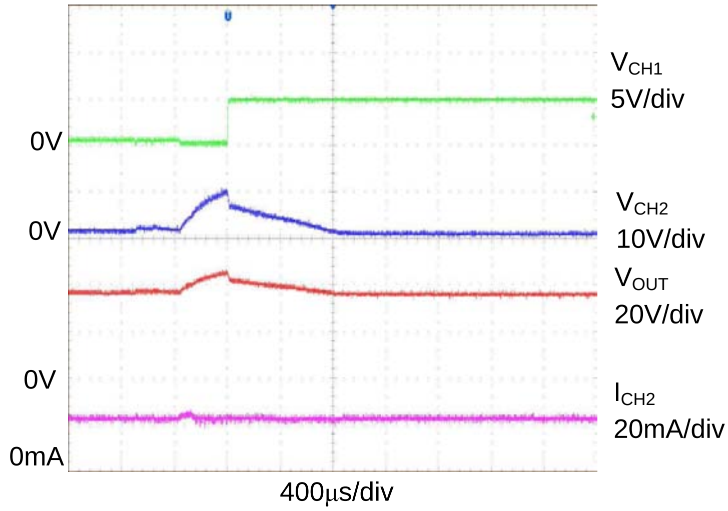


LED Current Waveforms (VIN=12V, Brightness=2.7%)

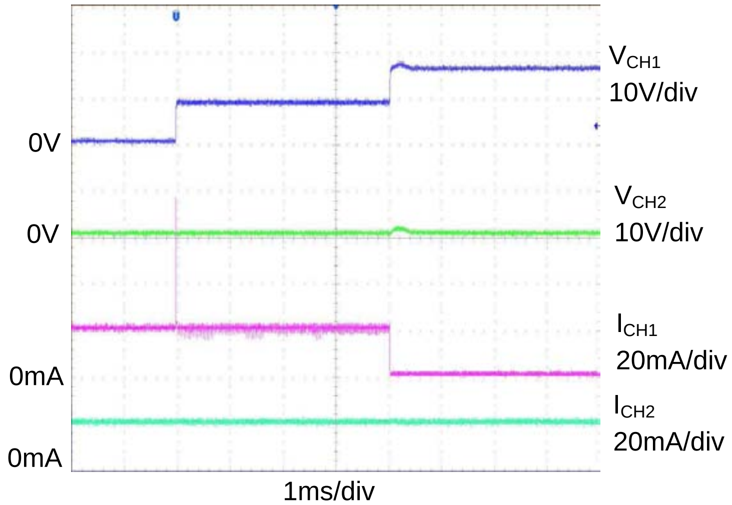


Typical Operating Characteristic (continued)

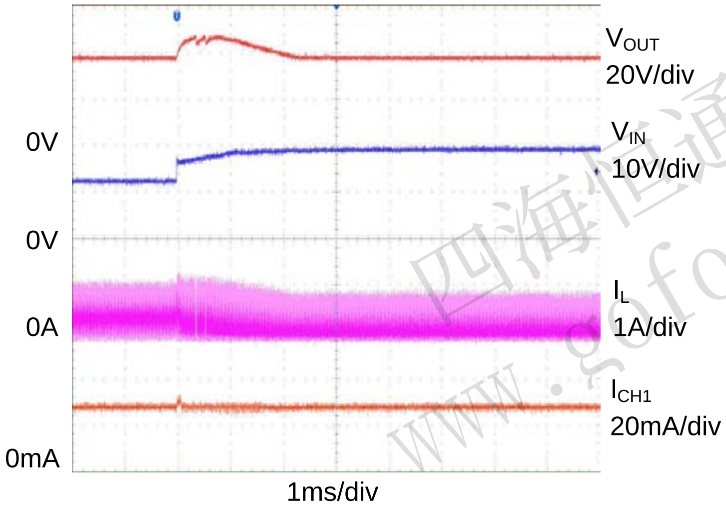
LED-Open Fault Protection
(VIN=12V, BRT=100%,LED Open On CH1)



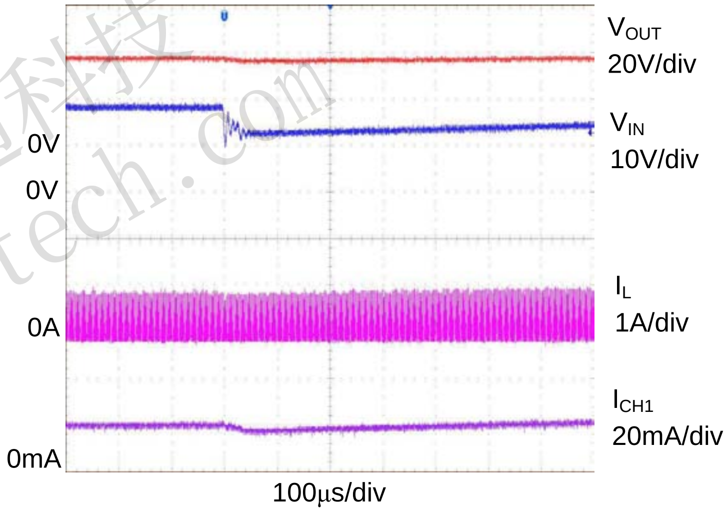
LED-Short Fault Protection
(VIN=12V, BRT=100%, 2 LEDs Short On CH1)



Line Transient Response
(VIN=12V→19V , Brightness=100%)



Line Transient Response
(VIN=12V→19V , Brightness=100%)



Detailed Description

The EUP2592 is a high-efficiency driver for arrays of white LEDs. It contains a fixed-frequency current- mode PWM step-up controller, dimming control circuit, internal power MOSFET, and eight regulated current sources (see Figure 1). When enabled, the step-up converter boosts the output voltage to provide sufficient headroom for the current sources to regulate their respective string currents. The EUP2592 features selectable switching frequency (500kHz or 1.2MHz), which allows trade-offs between external component size and operating efficiency.

WLED brightness is controlled by turning the WLEDs on and off with an external PWM signal. The EUP2592 has multiple features to protect the device from fault conditions. The EUP2592 checks each CH_ voltage during the operation. If one or more strings are open, the corresponding CH_ voltages are pulled below 135mV (typ), and the open-circuit fault is detected. As a result, the respective current sources are disabled. When one or more LEDs are shorted and the CH_ voltage exceeds 7V short fault is detected and the respective current source is disabled. In either LED open or short conditions, the fault strings are disabled while other strings can still operate normally. The step-up converter features cycle-by-cycle current limit to provide stable operation and soft-start protection. A thermal-shutdown circuit provides another level of protection.

5V Supply VCC and UVLO

The EUP2592 has built in 5V linear regulator VCC supply for internal control voltage. The EUP2592 includes the power on reset (POR) and under-voltage lockout (UVLO) features. POR resets the fault latchs. POR occurs when VCC rises above 2.8V (typ). The controller is disabled until VCC exceeds the UVLO threshold of 4.05V (typ). Hysteresis on UVLO is approximately 150mV. The VCC should be bypassed to GND with a 0.47µF or greater ceramic capacitor.

Shutdown

The EUP2592 can be placed into shutdown by set logic Low at EN pin. When a critical failure is detected, the IC also enters shutdown mode. In shutdown mode, all functions of the IC are turned off. The fault/status register is set accordingly in shutdown. When set EN logic Hi, the EUP2592 exits shutdown mode and starts. The fault/status register is reset at startup.

Fixed-Frequency Step-Up Converter

The EUP2592's fixed-frequency, current-mode, step-up converter automatically chooses the lowest active CH_ voltage to regulate the output voltage. The error signal is compared to the external switch current plus slope compensation to determine the switch on-time. As the load changes, the error amplifier sources or sinks current to the COMP output to deliver the required peak-inductor current. The slope-compensation signal is added to the current-sense signal to improve stability at high duty cycles.

Frequency Selection

The logic input FSEL input sets the internal oscillator frequency for step-up converter, as shown in Table 1. High-frequency (1.2MHz) operation optimizes the regulator for the smallest component size, at the expense of efficiency due to increased switching losses. Low-frequency (500kHz) operation offers the best overall efficiency but requires larger components and PCB area.

Table 1. Frequency Selection

FSEL PIN CONNECTION	SWITCHING FREQUENCY (kHz)
GND	500
VCC	1200

LED Current Sources

The EUP2592 is equipped with a bank of eight matched current sources. These specialized current sources are accurate to within ±1.5% between strings and can be switched on and off within 10µs, enabling PWM frequencies of up to 10kHz. All LED full-scale currents are identical and are set through the ISET pin (5mA < I_{LED} < 50mA). The full-scale LED current in the PWM dimming is determined by resistance from the ISET pin to ground:

$$I_{LEDMAX} = \frac{20mA \times 20k\Omega}{R_{ISET}}$$

The acceptable resistance range is 8kΩ< R_{ISET}< 80kΩ, which corresponds to full-scale LED current of 50mA > I_{LEDMAX} > 5mA. The current source output is pulse-width modulated and synchronized with an external PWM signal to reduce jitter and flicker noise in the display.

The minimum voltage drop across each current source is approximately 360mV when the LED current is 20mA. The low-voltage drop helps reduce dissipation while maintaining sufficient compliance to control the LED current within the required tolerances.

EUP2592 current source can be set even up to 50mA per-string, in this setting, a delicate circuit and PCB design is necessary to achieve good thermal diffusion, the application shown as below:

In this application, the design procedure as:

A: Sets CHx current: ICHx(mA)=400/RISET(KΩ), if set ICHx=40mA, RISET=10KΩ, and the maximum ICHx<50mA;

B:Connects per-CHx with 2 LED cathode legs to improve LED life;

C: When setting ICHx>35mA, guarantee all LED strings forward voltage drop difference as small as possible, which will keep LEDs light uniformity and decrease heat generation in EUP2592 current source;

D:During PCB layout, generate large heat sink connection with EUP2592 exposed pad to improve the heat exchange between EUP2592 and ambience;

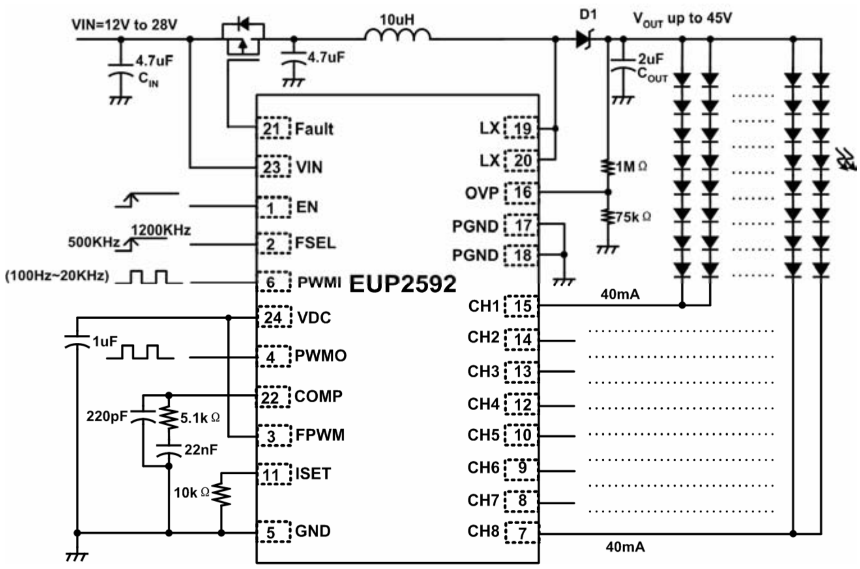


Figure 5. ICHx=40mA Application Circuit

The un-used LED current sources can be floated. When the IC is powered up, the device scans settings for all CH_ pins. All CH_ pins in use are combined to extract a lowest CH_voltage which is fed into the step-up converter's error amplifier and is used to set the output voltage.

LED Brightness PWM Dimming Control

The EUP2592 allows users to accurately control PWM dimming in two ways with an external PWM input signal.

(1)External Direct PWM Mode: Connect FPWM pin to VCC pin and enter the external direct PWM mode. The ISET pin sets the amplitude of the current sources for each LED string. The external PWM signal directly controls the PWM dimming frequency and duty cycle of 8 channel LED current sources. The resulting current is chopped and synchronized to the PWM input signal. When filtered by the slow response time of the human eye, the overall brightness is modulated in a consistent flicker-free manner.

(2)Internal PWM Mode: Connect a resistor from FPWM to GND and internally set PWM dimming frequency.

$$f_{PWM} = \frac{200\text{Hz} \times 113\text{k}\Omega}{R_{FPWM}}$$

The internal PWM signal controls the duty cycle of 8 channel current sources. The duty cycle of this PWM signal is proportional to the PWMO voltage. PWMO is a filtered PWMI signal output. Connect two 1μF capacitors from PWMO to VCC and GND. The capacitors form a lowpass filter with an internal 40kΩ (typ) resistor to convert the external PWM signal into an analog PWMO signal whose level represents the duty-cycle information of the external PWM signal. The internal PWM dimming signal duty cycle relationship with the external PWM duty cycle is shown in Figure 6. The maximum internal PWM dimming signal duty cycle is 99.6%.

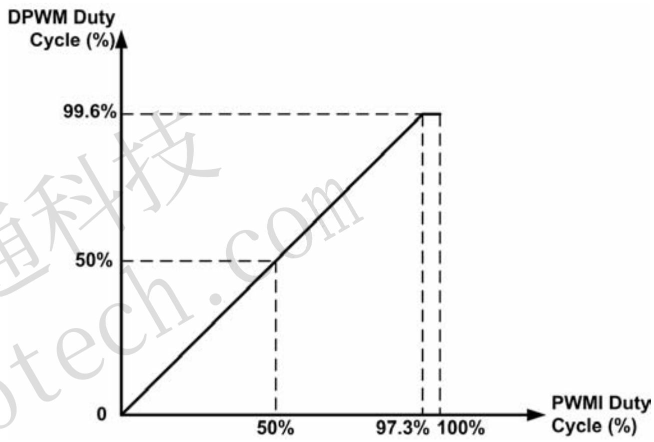


Figure 6. The Internal PWM Duty Cycle vs The External PWM Signal Duty Cycle

If the external PWM signal is not available, users can use an adjustable resistor to set the internal PWM dimming signal duty cycle. Connect PWMI input to GND and connect an external adjustable resistor between PWMO and VCC. The external adjustable resistor and the internal 40kΩ resistor form a resistor divider and set PWMO voltage level (Figure 7).

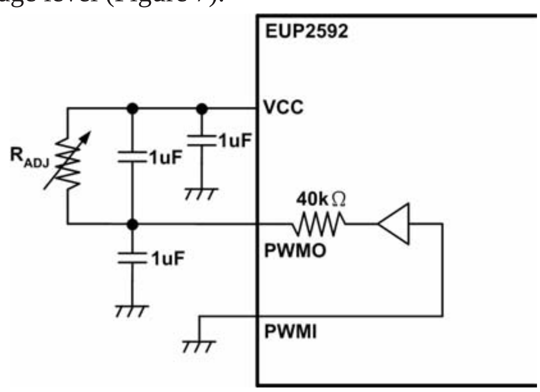


Figure 7. Internal PWM Dimming Duty Cycle Control with An External Adjustable Resistor Circuit Diagram

The duty cycle of the internal PWM dimming signal is set by the following formula.

$$Duty_{PWM} = \frac{40k\Omega}{R_{ADJ} + 40k\Omega} \times 100\%$$

Fault Protection

The EUP2592 has multiple features to protect the device from fault conditions. Separate feedback loops limit the output voltage under any circumstance, ensuring safe operation. Once an open string is detected, the string is disabled while other strings operate normally. The EUP2592 also features short LED detection. Table 2 lists all EUP2592 fault protection control.

Table 2. EUP2592 Fault Protection

Faults	FAULT Output (HV)	IC Operation Mode	Boost DC-DC	WLED Current Mirrors
Input Over Current LX shorted to GND (V_{LX}<3V)	Pull Hi, Disable PCH	VCC Alive. EUP2592 is latched off until recycle power or toggle EN	Off	Off
Input Over Current OVP shorted to GND or Boost Schottky Diode Malfunction (V_{OVP}<0.22V)	Pull Hi, Disable PCH	VCC Alive. EUP2592 is latched off until recycle power or toggle EN	Off	Off
DC-DC Boost Output Exceeds OVP Threshold (V_{OVP}=3V)	Pull Lo, Enable PCH	Normal	When V_{OVP} is greater than 3.0V, the internal N-CH Switch will be turned off until V_{OVP} drops to 2.85V.	On
Any WLED Current Mirror Open Circuit ($V_{CH\_}$<0.135V and can be pulled High)	Pull Lo, Enable PCH	Normal	On	Open CH_ will be turned off (Note: Leave un-used CH_ floating)
Any WLED Current Mirror CH_ shorted to GND ($V_{CH\_}$<0.135V and CAN'T be pulled High)	Pull Hi, Disable PCH	VCC Alive. EUP2592 is latched off until recycle power or toggle EN.	Off	Off
One or more LEDs of any WLED Current Mirror shorted ($V_{CH\_}$>7V)	Pull Lo, Enable PCH	Normal	On	LED shorted CH_ will be turned off after 2ms blanking. The rest CH_ remain ON.
Thermal Fault (TJ>+150ºC)	Pull Hi first, Then Enable PCH w/ 20uA pull down current after TJ falls below 120ºC	Normal	Off first, Then restart after TJ falls below 120ºC	Off first, Then restart after TJ falls below 120ºC
ISET UVLO (V_{ISET}<0.85V)	Pull Lo, Enable PCH	Normal	Off	Off

Startup Fault Diagnosis

At startup, the EUP2592 checks the OVP pin to see if the Schottky diode is open. If the OVP voltage is lower than 220mV (typ), the boost converter does not start. After the OVP test is done, the EUP2592 performs a diagnostic test of the LED array (See Fault Protection Table 1). After the LED string diagnostic phases are finished, the boost converter starts.

Overvoltage Protection

To protect the step-up converter when the load is open, or the output voltage becomes excessive for any reason, the EUP2592 features a dedicated overvoltage feedback input (OVP). The OVP pin is tied to the center tap of a resistive voltage-divider from the high-voltage output. When the OVP pin voltage, V_{OVP}, exceeds 3V, a comparator turns off the internal power MOSFET. This step-up converter switch is re-enabled after the V_{OVP} drops 220mV (typ) hysteresis below the protection threshold. This overvoltage-protection feature ensures the step-up converter fail-safe operation when the LED strings are disconnected from the output.

Current-Source Fault Protection

The EUP2592 performs a diagnostic test at startup. Open/short strings are disabled. LED fault open/short is also detected after startup. When one or more strings fails after startup, the corresponding current sources are disabled. The remaining LED strings still operate normally.

Open-Current Source Protection

The EUP2592 step-up converter output voltage is regulated according to the minimum CH_ voltages on all the strings in use. If one or more strings are open, the respective CH_ pins are pulled to ground. For any CH_ lower than 135mV, the corresponding current source is disabled. The unaffected LED strings still operate normally. If all strings in use are open, the EUP2592 shuts down the step-up converter. The EUP2592 can tolerate slight mismatch between LED strings. When severe mismatches or WLED shorts occur, the CH_ voltages will be uneven because mismatched voltage drops across strings. If a given CH_ voltage is higher than 7V (typ) after blanking time when LEDs are turned on, an LED short condition is detected on the respective string. When the short continues for greater than 2ms, the string is disabled. The controller allows the unaffected LED strings to operate normally. When only one string is in operation and there are shorts on some LEDs, then the converter does not shut down. Instead, the output voltage is adjusted accordingly. The LED short-protection feature is disabled during the soft-start phase of the step-up converter.

Thermal Shutdown

The EUP2592 includes a thermal-protection circuit. When the local IC temperature exceeds +150°C (typ), the controller and current sources shut down and do not restart until the die temperature drops by 30°C.

Design Procedure

External components are primarily dictated by the output voltage and the maximum load current, as well as maximum and minimum input voltages. Begin by selecting an inductor value. Once the inductor L value is chosen, select the diode and input and output capacitors.

Inductor Selection

The selection of the inductor should be based on its maximum current (I_{SAT}) characteristics, power dissipation (DCR), EMI susceptibility (shielded vs unshielded), and size. Inductor type and value influence many key parameters including ripple current, current limit, efficiency, transient performance and stability. The inductor maximum current capability must be adequate to handle the peak current at the worst case condition. A shielded inductor is usually more suitable for EMI susceptible applications, such as LED backlighting.

The peak current can be derived from the fact that the voltage across the inductor during the Off period can be shown as:

$$IL_{PEAK} = \left(V_O \times I_O\right) / \left(85\% \times V_I\right) + \tfrac{1}{2}\left[\left(V_O - V_I\right) / \left(L \times V_O \times f_{OSC}\right)\right]$$

The choice of 85% is just an average term for the efficiency approximation. The first term is average current that is inversely proportional to the input voltage. The second term is inductor current change that is inversely proportional to L and f_{OSC}. As a result, for a given switching frequency and minimum input voltage the system operates, the inductor I_{SAT} must be chosen carefully.

Output Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging on the output capacitor, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE(C)} \approx \frac{I_{OUT(MAX)}}{C_{OUT}}\left(\frac{V_{OUT(MAX)} - V_{IN(MIN)}}{V_{OUT(MAX)} f_{OSC}}\right)$$

and:

$$V_{RIPPLE(ESR)} \approx IL_{PEAK} R_{ESR(COUT)}$$

where IL_{PEAK} is the peak inductor current (see the Inductor Selection).The output voltage ripple should be low enough for the CH_ current-source regulation. The ripple voltage should be less than $200mV_{P-P}$. For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered. The actual capacitance of a ceramic capacitor is reduced by DC voltage biasing. Ensure the selected capacitor has enough capacitance at actual DC biasing. A 2.2uF to 10uF 50V rating ceramic capacitor can meet most application requirements.

Rectifier Diode Selection

The EUP2592's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. The diode should be rated to handle the output voltage and the peak switch current. Make sure that the diode's peak current rating is at least IL_{PEAK} calculated in the Inductor Selection section and that its breakdown voltage exceeds the output voltage.

Over-voltage Protection Determination

The OVP protection circuit should ensure the circuit safe operation; therefore, the controller should limit the output voltage within the ratings of all MOSFET, diode, and output capacitor components, while providing sufficient output voltage for LED current regulation. The OVP pin is tied to the center tap of a resistive voltage-divider (R1 and R2 in Figure 1) from the high-voltage output. When the controller detects the OVP pin voltage reaching the threshold V_{OVP_TH}, typically 3V, OVP protection is activated. Hence, the step-up converter output over-voltage protection point is:

$$V_{OUT(OVP)} = V_{OVP\_TH} \times \left(1 + \frac{R_{OVP1}}{R_{OVP2}}\right)$$

In Figure 1, the output OVP voltage is set to:

$$V_{OUT(OVP)} = 3V \times \left(1 + \frac{1M\Omega}{75k\Omega}\right) \approx 43V$$

Input Capacitor Selection

The input capacitor (C_{IN}) filters the current peaks drawn from the input supply and reduces noise injection into the IC. A 4.7µF ceramic capacitor is used in the Typical Operating Circuit (Figure 1) because of the high source impedance seen in the typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. In some applications, C_{IN} can be reduced below the values used in the Typical Operating Circuit (Figure 1). Ensure a low-noise supply at VIN by using adequate C_{IN}.

LED Selection and Bias

The series/parallel configurations of the LED load and the full-scale bias current have a significant effect on regulator performance. LED characteristics vary significantly from manufacturer to manufacturer. Consult the respective LED data sheets to determine the range of output voltages for a given brightness and LED current. In general, brightness increases as a function of bias current. This suggests that the number of LEDs could be decreased if higher bias current is chosen; however, high current increases LED temperature and reduces operating life. LED manufacturers specify LED color at a given LED current. With lower LED current, the color of the emitted light tends to shift toward the blue range of the spectrum. A blue bias is often acceptable for business applications but not for high-image-quality applications such as DVD players. PWM dimming is a viable solution for reducing power dissipation while maintaining LED color integrity. Careful attention should be paid to switching noise to avoid other display quality problems. Using fewer LEDs in a string improves step-up converter efficiency, and lowers breakdown voltage requirements of the output capacitor and diode. The minimum number of LEDs in series should always be greater than maximum input voltage. Between 8 and 12 LEDs in series are ideal for input voltages up to 20V.

Applications Information

LED CH_ Voltage Variation

The EUP2592 has accurate (±1.5%) matching for each current source. However, the forward voltage of each white LED can vary up to 25% from part to part. The accumulated voltage difference in each string equates to additional power loss within the IC. For the best efficiency, the voltage difference between strings should be minimized. The difference between lowest voltage string and highest voltage string should be less than 7V (typ). Otherwise, the internal LED short-protection circuit disables the high CH string.

CH_ Pin Maximum Voltage

The current through each CH_ pin is controlled only during the step-up converter's on-time. During the converter's off-time, the current sources are turned off. The output voltage does not discharge and stays high. The CH_ pin can withstand up to 48V.

Step-up Converter Loop Compensation

The EUP2592 uses current mode control architecture, which has a fast current sense loop and a slow voltage feedback loop. The fast current feedback loop does not require any compensation. The slow voltage loop must be compensated for stable operation. The compensation network is a series Rc, Cc1 network from COMP pin to ground and an optional Cc2 capacitor connected to the COMP pin. The Rc sets the high frequency integrator gain for fast transient response and the Cc1 sets the integrator pole and zero to ensure loop stability. For most applications, Rc is in the range of 1kΩ to 10kΩ and Cc1 is in the range of 10nF to 33nF. Depending on the PCB layout, a Cc2, in range of 220pF, may be needed to create a pole to cancel the output capacitor ESR's zero effect for stability. The EUP2592 evaluation board is configured with Rc1 of 5.1kΩ, Cc1 of 22nF, and Cc2 of 220pF, which achieves stability. In the actual applications, these values may need to be tuned empirically but these recommended values are usually a good starting point.

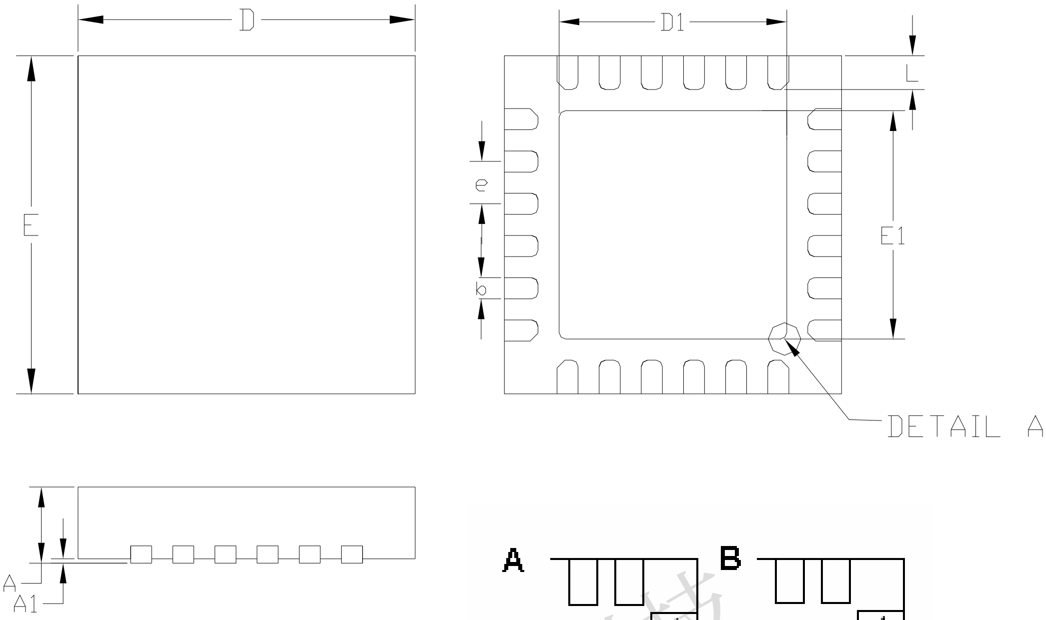
PCB Layout Guidelines

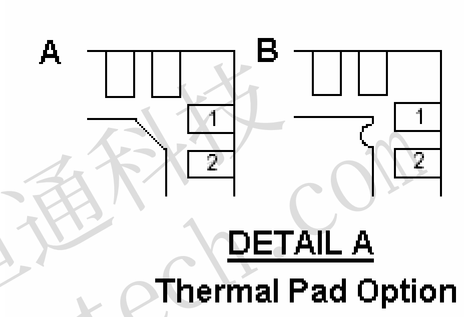
Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

1) Minimize the area of high current switching loop of rectifier diode, internal MOSFET, and output capacitor to avoid excessive switching noise.
2) Connect high-current input and output components with short and wide connections. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the internal MOSFET, then to the input capacitor’s negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the rectifier diode, to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Avoid using vias in the high-current paths. If vias are unavoidable, use multiple vias in parallel to reduce resistance and inductance.
3) Create a ground island (PGND) consisting of the input and output capacitor ground and negative terminal of the current-sense resistor. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output-voltage ripple and noise spikes. Create an analog ground island (AGND) consisting of the over-voltage detection divider ground connection, the ISET and FPWM resistor connections, CCV capacitor connections, and the device’s exposed backside pad. Connect the AGND and PGND islands by connecting the GND pins directly to the exposed backside pad. Make no other connections between these separate ground planes.
4) Place the over-voltage detection divider resistors as close as possible to the OVP pin. The divider’s center trace should be kept short. Placing the resistors far away causes the sensing trace to become antennas that can pick up switching noise. Avoid running the sensing traces near LX.
5) Place IN pin bypass capacitor as close as possible to the device. The ground connection of the IN bypass capacitor should be connected directly to GND pins with a wide trace.
6) Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node and ground. If possible, avoid running the LX node from one side of the PCB to the other. Use DC traces as shield if necessary. Refer to the EUP2592 evaluation kit for an example of proper board layout.

Packaging Information

TQFN-24





SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.18	0.30	0.007	0.012
E	3.90	4.10	0.154	0.161
D	3.90	4.10	0.154	0.161
D1	2.70		0.106	
E1	2.70		0.106	
e	0.50		0.020	
L	0.30	0.50	0.012	0.020