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TFT LCD DC-DC Converter with Integrated LDO, OP-AMP and GPM Switch

DESCRIPTION

The EUP2644 generates power supply rails for thin-film transistor (TFT) liquid-crystal display (LCD) panels in monitors and notebooks operation from 3V to 5.5V input supply. The device integrates a step-up converter, a high speed V_{COM} buffer, a 400mA low dropout (LDO) linear regulator, and a Gate Pulse Modulator (GPM).

The external compensated step up converter features an internal power MOSFET and high frequency operation allowing the use of small inductors and capacitors. The step up converter uses fixed-frequency, current mode control architecture which provides fast load-transient response and easy compensation. A 2.9A peak current limit for the internal switch protects power supply fault condition.

The GPM provides a modulated voltage to the gate driver circuitry of a TFT LCD display. It allows shaping of the gate high voltage to improve image quality. It also can delay the gate high voltage while power on. Both the power-on delay time and the falling time of the gate high voltage are programmable by external resistor and capacitor.

The high speed V_{COM} butter features continues output current (±100mA), 20MHz bandwidth, fast slew rate 70V/μs, and rail-to-rail inputs and outputs.

The LDO regulator provides up to 400mA current to the external digital circuitry.

FEATURES

- 3V to 5.5V Input Supply Range
- Current Mode Step Up Converter
  - Selectable Frequency (650kHz/1.2MHz)
  - Built-In 20V, 2.9A, 0.15Ω N-MOSFET
  - High Efficiency Up to 90%
  - Programmable Soft-Start
  - Fast Transient Response to Pulsed Load
- Gate Pulse Modulator Circuit
  - Adjustable Falling Time and Delay
  - Flicker Compensation
- High Speed High Output Current V_{COM} Buffer
  - 20MHz BW
  - 70V/μS Slew Rate
  - 400mA Peak Output Current
- 400mA LDO Regulator for V_{LOGIC}
  - Adjustable Output Voltage：2.5V, 2.85V, 3.3V
- Input Under Voltage Lockout and Thermal Protection
- 24 pin 4mm×4mm TQFN Package
- RoHS Compliant and 100% Lead (Pb)-Free

APPLICATIONS

- LCD Monitors
- Notebook Display

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Typical Application Circuit

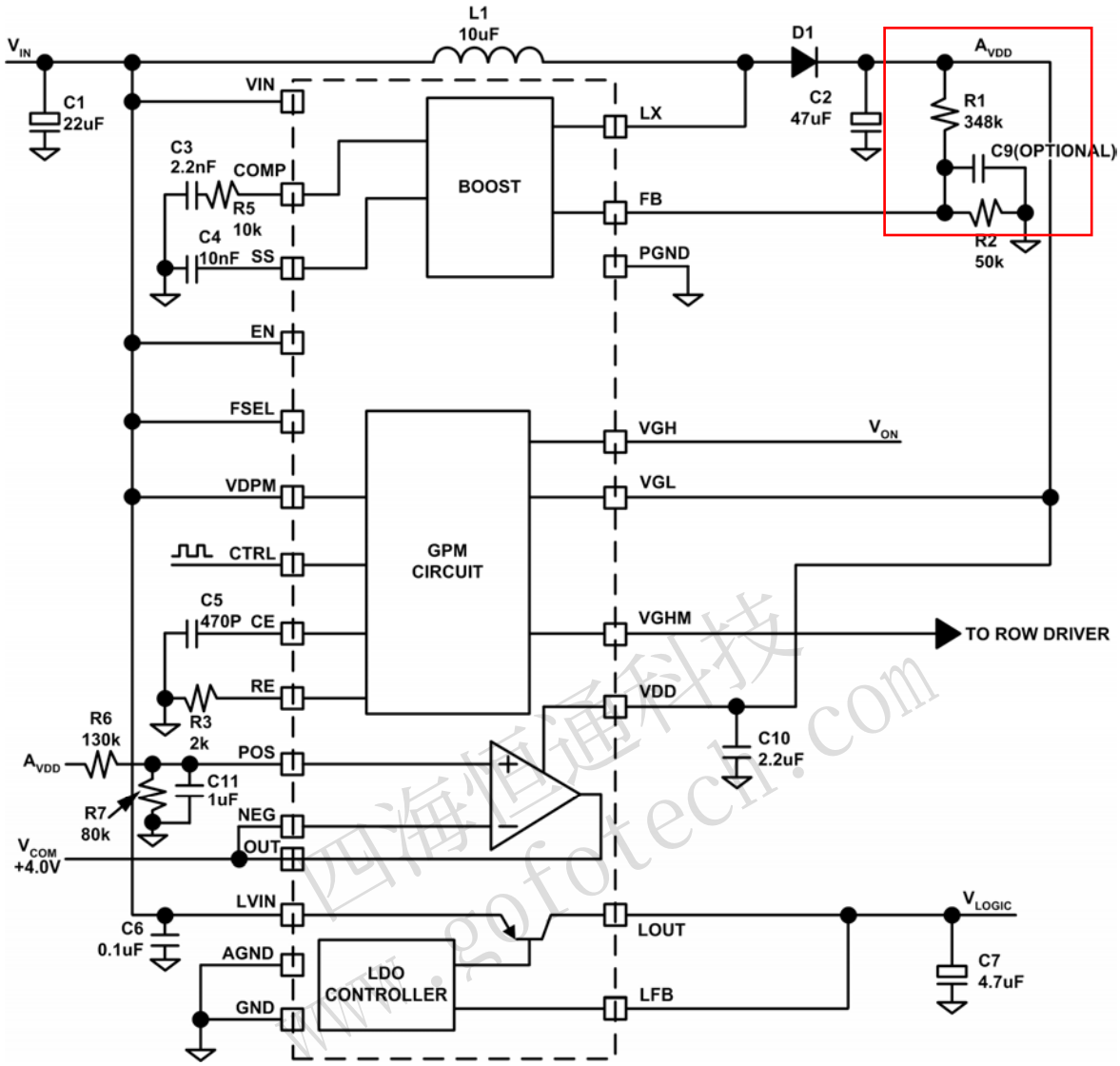
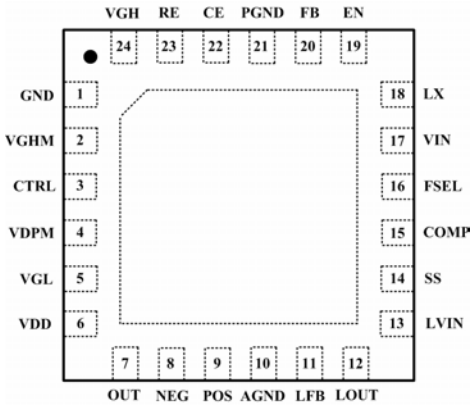


Figure 1.

Pin Configurations

Package Type	Pin Configurations
TQFN-24	

Pin Description

PIN	PIN	DESCRIPTION
1	GND	Ground
2	VGHM	Gate Pulse Modulation Output
3	CTRL	Gate Pulse Modulation Control Input
4	VDPM	Gate Pulse Modulation Enable
5	VGL	Gate Pulse Modulation Lower Voltage Input
6	VDD	V_{COM} Amplifier Supply
7	OUT	V_{COM} Amplifier Output
8	NEG	V_{COM} Amplifier Inverting Input
9	POS	V_{COM} Amplifier Noninverting Input
10	AGND	V_{COM} Amplifier Ground
11	LFB	LDO Output Adjust
12	LOUT	LDO Output
13	LVIN	LDO Power Supply
14	SS	Step up Converter Soft-start. Connect a capacitor between this pin and GND to set the soft-start time.
15	COMP	Step up Converter Compensation Pin. Connect a series resistor and capacitor between this pin and GND to optimize transient response.
16	FSEL	Step up Converter Frequency Select.
17	VIN	Step up Converter Power Supply
18	LX	Step up Converter Switching Node
19	EN	Chip Enable Pin. Connect to LVIN for normal operation, GND for shutdown.
20	FB	Step up Converter Feedback
21	PGND	Step up Converter Power Ground
22	CE	Gate Pulse Modulator Delay Control. Connect a capacitor between this pin and GND to set the delay time.
23	RE	Gate Pulse Modulator Slew Control. Connect a resistor between this pin and GND to set the falling slew rate.
24	VGH	Gate Pulse Modulator High Voltage Input.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP2644JIR1	TQFN-24	xxxxx P2644	-40 °C to 85°C

EUP2644 □ □ □ □

Lead Free Code
1: Lead Free 0: Lead

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
J: TQFN

Block Diagram

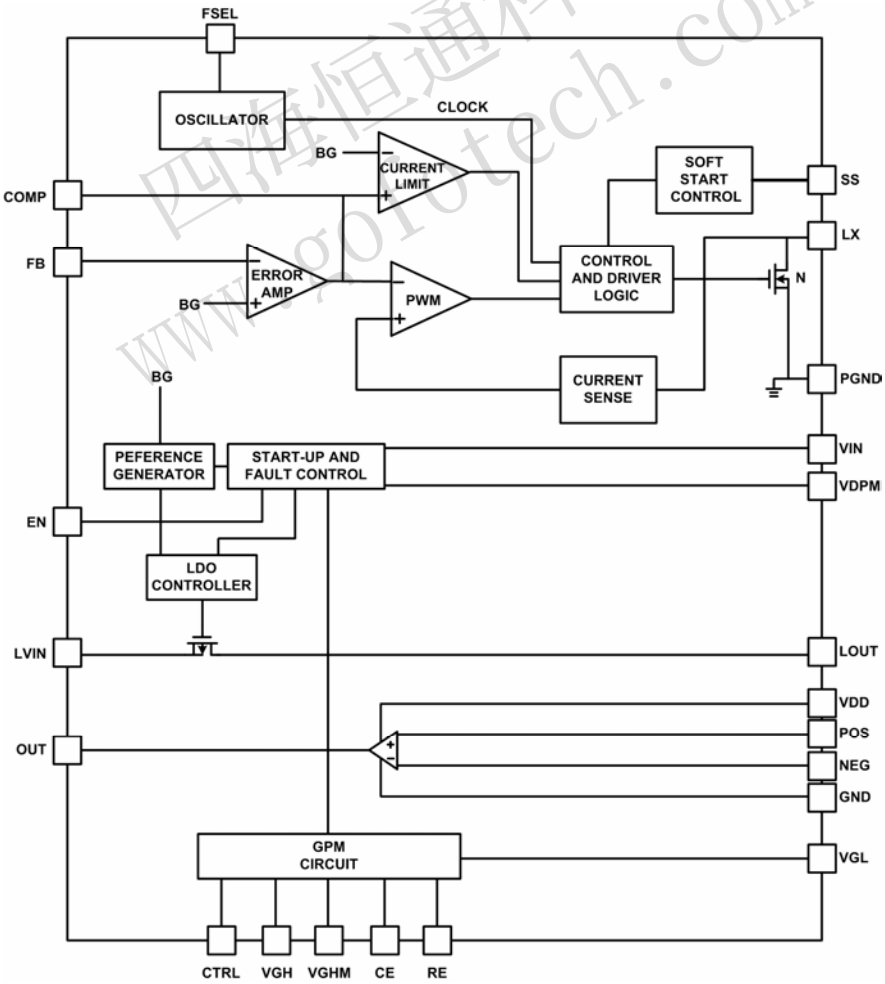


Figure 2.

Absolute Maximum Ratings

- LX to GND, AGND and PGND ---------- -0.5V to 25V
- VDD, OUT, NEG and POS to GND, AGND and PGND---------- -0.5V to 25V
- VGL, VGH and VGHM to GND, AGND and PGND---------- -0.5V to 32V
- Differential Voltage Between POS and NEG ---------- ±6V
- Voltage Between GND, AGND and PGND ---------- ±0.5V
- All Other Pins to GND, AGND and PGND ---------- -0.5V to 6.5V
- Input ,Output, or I/O Voltage ---------- GND-0.3V to VIN+0.3V
- Junction Temperature ---------- 150°C
- Lead Temp (Soldering, 10sec) --- ---------- 260°C

Operating Conditions

- Operating Temperature ---------- -40°C to 85°C
- Input Voltage Range, VIN ---------- 3V to 5.5V
- Step up Output Voltage Range---------- 8V to 20V

Electrical Characteristics

Specifications in standard type face are for T_A=25℃ and those with boldface type apply over the full Operating Temperature Range (T_A=-40℃ to +85℃), LVIN=VIN=5V,VGL=VDD=14V,VGH=25V,AVDD=10V, GND=AGND=PGND=0, unless otherwise noted.

Symbol	Parameter	Conditions	EUP2644			Unit
			Min.	Typ.	Max.	
GENERAL						
V_S	LVIN,V_{IN} Input Voltage Range	See separate LDO specifications	**3**	5	**5.5**	V
I_{S_DIS}	Sum Of LVIN, V_{IN} Supply Currents when Disabled	EN=0V		0.2	**2**	uA
I_S	Sum Of LVIN ,V_{IIN} Supply Currents	EN=5V,LX not switching, LDO not loaded		0.65		mA
UVLO	Undervoltage Lockout Threshold	Rising	**2.25**	2.45	**2.65**	V
		Falling	**2.15**	2.35	**2.55**	V
OT_R	Thermal Shutdown Temperature	Temperature Rising		160		℃
OT_F		Temperature Falling		120		℃
LOGIC INPUT CHARACTERISTICS-EN,CTRL,FSEL,VDPM						
V_{IL}	Low Voltage Threshold				**0.8**	V
V_{IH}	High Voltage Threshold		**2.2**			V
R_{IL}	Pull-Down Resistor	Enabled, Input at V_{IN}	**150**	250	**400**	V
STEP-UP SWITCHING REGULATOR						
A_{VDD}	Output Voltage Range				**20**	V
$\triangle A_{VDD}/VA_{VDD}$	Load Regulation	50mA<ILOAD<250mA		0.2		%
$\triangle A_{VDD}/\triangle V_{IN}$	Line Regulation	ILOAD=150mA, 3.0V<LVIN<5.5V		0.05	**0.12**	%/V
ACC_{AVDD}	Overall Accuracy (Line, Load, Temperature)	10mA<ILOAD<300mA, 3.0V< LVIN <5.5V,-40℃<T_A<85℃	**-3**		**3**	%
V_{FB}	Feedback Voltage(V_{FB})	ILOAD=100mA, T_A=25℃	**1.248**	1.260	**1.273**	V
		ILOAD=100mA, T_A=-40℃ to +85℃	**1.23**	1.26	**1.29**	V
I_{FB}	FB Input Bias Current			100	**200**	nA

Electrical Characteristics (continued)

Specifications in standard type face are for T_A=25℃ and those with boldface type apply over the full Operating Temperature Range (T_A=-40℃ to +85℃), LVIN=VIN=5V,VGL=VDD=14V,VGH=25V,AVDD=10V, GND=AGND=PGND=0, unless otherwise noted.

Symbol	Parameter	Conditions	EUP2644			Unit
			Min.	Typ.	Max.	
STEP-UP SWITCHING REGULATOR						
$R_{DS(ON)}$	Switch On Resistance			150	**300**	mΩ
EFF	Peak Efficiency			90		%
I_{LIM}	Switch Current Limit		**2.3**	2.9	**3.4**	A
D_{MAX}	Max Duty Cycle		**85**	96		%
F_{OSC}	Oscillator Frequency	FSEL=0V	**500**	650	**800**	kHz
		FSEL=V_{IN}	**0.95**	1.2	**1.4**	MHz
I_{SS}	Soft Start Slew Current	SS<1V,T_A=25℃		3		uA
LDO REGULATION						
V_{SL}	Input Voltage Range LVIN	LFB=LOUT	**3.0**		**5.5**	V
		LFB OPEN	**3.35**		**5.5**	V
		LFB =GND	**3.8**		**5.5**	V
V_{LOUT}	Output Voltage	LFB =GND, ILDO=1mA		3.31		V
		LFB =GND, ILDO=350mA		3.29		V
		LFB OPEN, ILDO=1mA		2.86		V
		LFB OPEN, ILDO=350mA		2.84		V
		LFB =LOUT, ILDO=1mA		2.51		V
		LFB = LOUT, ILDO=350mA		2.49		V
ACC_{LDO}	Overall Accuracy	1mA<ILDO<350mA	**-4**		**4**	%
$\triangle V_{LOUT}/V_{LVIN}$	Line Regulation	ILDO=1mA,3.0V<LVIN<5.5V		1		mV/V
$\triangle V_{LOUT}/V_{LOUT}$	Load Regulation	1mA<ILDO<350mA		1.36		%
V_{DO}	Dropout Voltage	Output drops by 2%, ILDO=350mA		300	**500**	mV
I_{LIML}	Current Limit	Output drops by 5%	**400**	550		mA
VCOM AMPLIFIER RLOAD=10K,CLOAD=10pF, Unless Otherwise Stated						
V_{SAMP}	Supply Voltage		**4.5**		**20**	V
I_{SAMP}	Supply Current			4.5		mA
V_{OS}	Offset Voltage			3	**20**	mV
I_B	Noninverting Input Bias Current			0	**100**	nA
CMIR	Common Mode Input Voltage Range		**0**		**VDD**	V
CMRR	Common Mode Rejection Ratio		**50**	90		dB
PSRR	Power Supply Rejection Ratio		**50**	90		dB
VOH	Output Voltage Swing High	Iout(source)=5mA		VDD-50		mV
VOH	Output Voltage Swing High	Iout(source)=50mA		VDD-450		mV
VOL	Output Voltage Swing Low	Iout(sink)=5mA		35		mV
VOL	Output Voltage Swing Low	Iout(sink)=50mA		350		mV
I_{SC}	Output Short Circuit Current		**250**	400		mA
SR	Slew Rate			70		V/us
BW	Gain Bandwidth	-3dB gain point		20		MHz

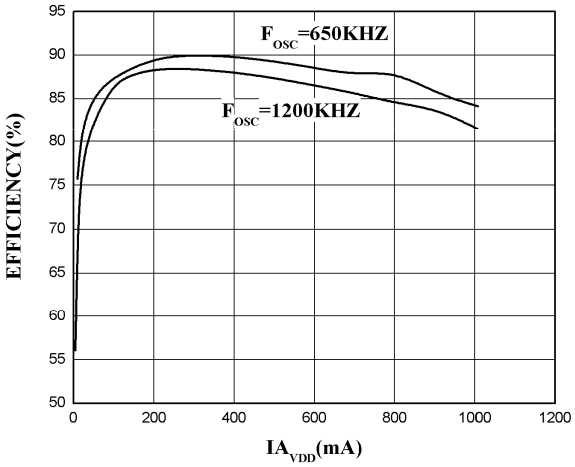
Electrical Characteristics (continued)

Specifications in standard type face are for T_A =25℃ and those with boldface type apply over the full Operating Temperature Range (T_A=-40℃ to +85℃), LVIN=VIN=5V,VGL=VDD=14V,VGH=25V,AVDD=10V, GND=AGND=PGND=0, unless otherwise noted.

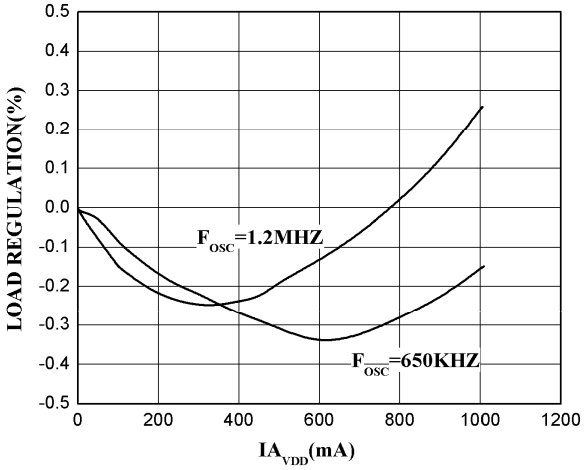
Symbol	Parameter	Conditions	EUP2644			Unit
			Min.	Typ.	Max.	
GATE PULSE MODULATOR						
VGH	VGH Voltage		**7**		**30**	V
I_{VGH}	VGH Input Current			130		uA
				50		uA
V_{GL}	VGL Voltage		**3**		**VGH-2**	V
I_{VGL}	VGL Input Current		**-2**	0.1	**2**	uA
R_{ONVGH}	VGH to VGHM On Resistance			70		Ω
I_{DIS_VGH}	VGHM Discharge current	RE=33kΩ		8		mA
T_{DEL}	DELAY Time	CE=470pF,RE=33kΩ		1.9		us

Typical Operating Characteristics

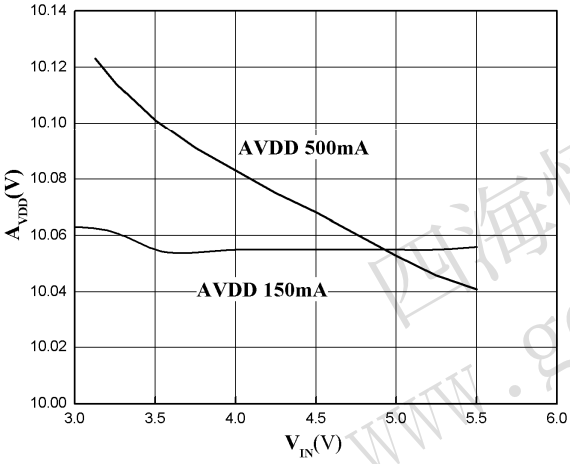
A_{VDD} Efficiency vs IA_{VDD}



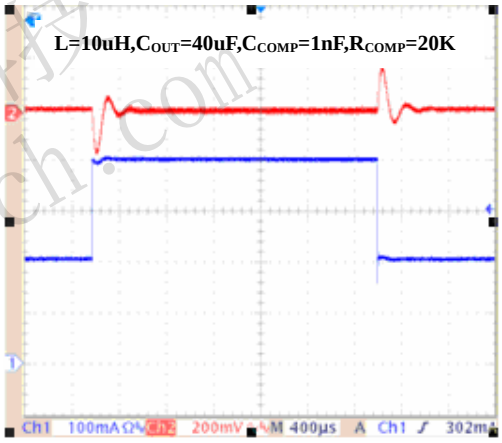
A_{VDD} Load Regulation vs IA_{VDD}



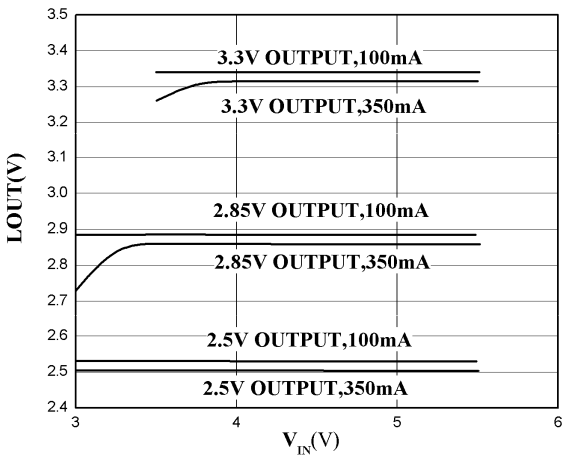
Line Regulation A_{VDD} vs V_{IN}



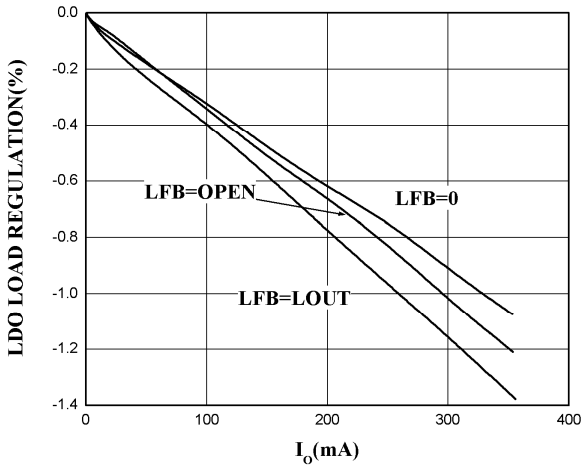
Step Up Converter Transient Response



Line Regulation LOUT vs V_{IN}

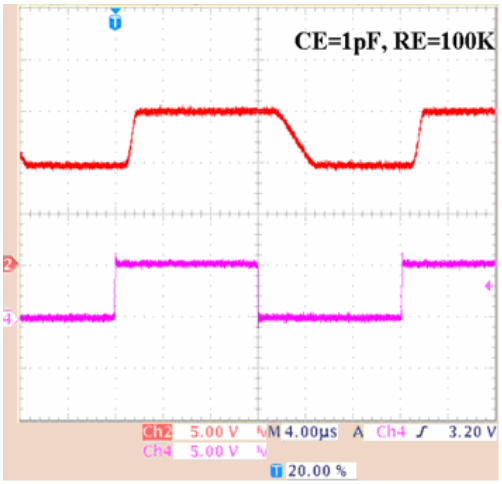


LDO Load Regulation vs I_O

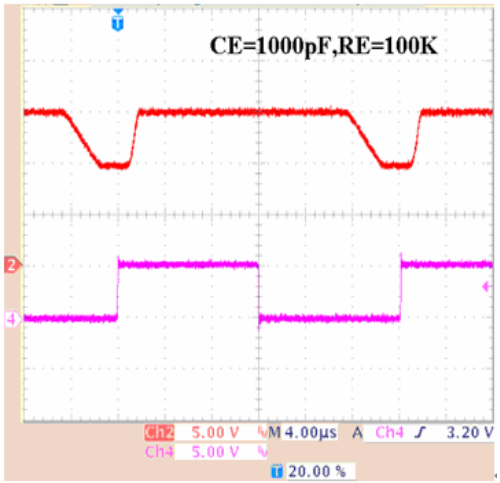


Typical Operating Characteristics (continued)

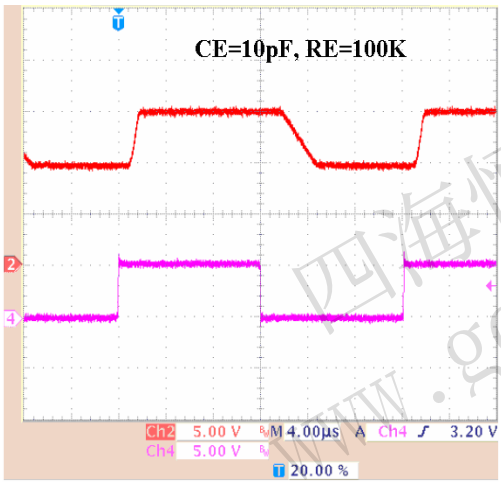
GPM Circuit Waveform



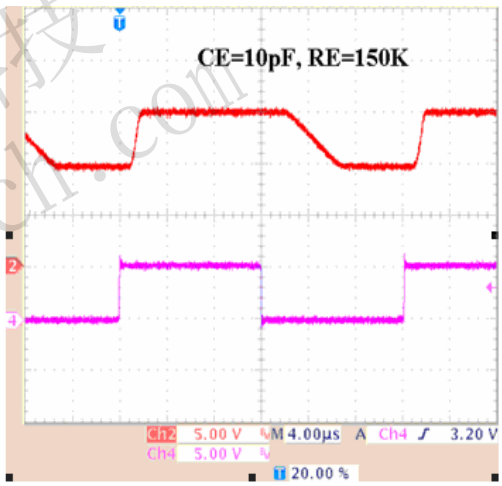
GPM Circuit Waveform



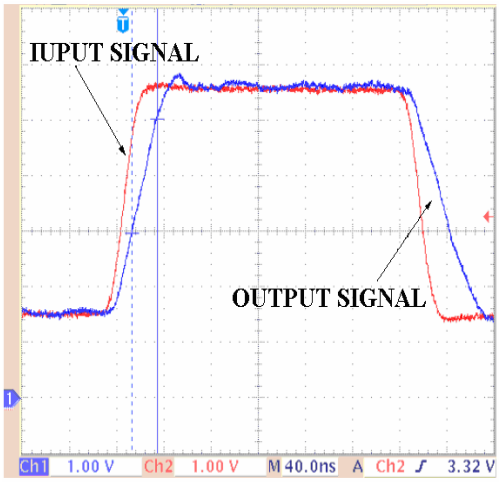
GPM Circuit Waveform



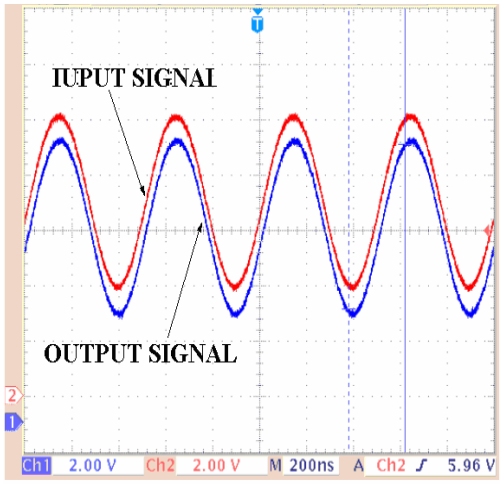
GPM Circuit Waveform



V_{COM} Rsing Slew Rate

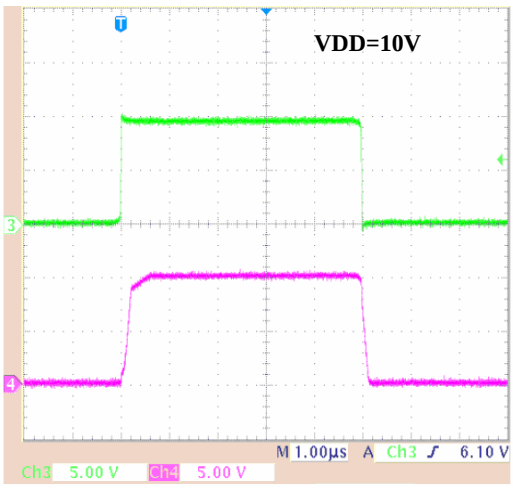


V_{COM} Rail to Rail Input/Output

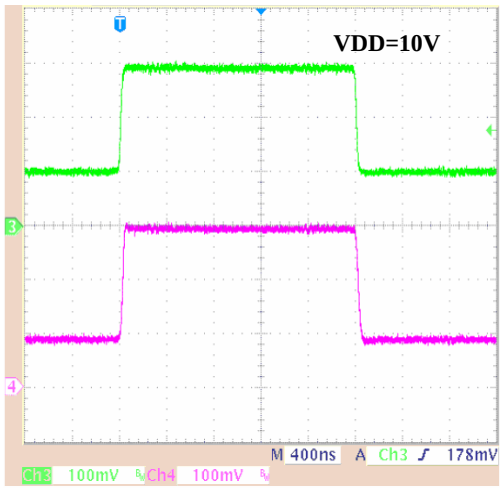


Typical Operating Characteristics (continued)

V_{COM} Large-Signal Response



V_{COM} Small-Signal Response



Application Information

The EUP2644 provides a complete power solution for TFT LCD applications. The system consists of one boost converter to generate A_{VDD} voltage for column drivers, one logic LDO regulator to provide voltage to logic circuit in the LCD panel, one integrated V_{COM} buffer which can provide up to 400mA peak current. This part also integrates Gate Pulse Modulator circuit that can help to optimize the picture quality.

Enable Control

When EN pin is pulling down, the EUP2644 is shut down reducing the supply current to <10µA. When the voltage at EN pin reaches 2.2V, the EUP2644 is on.

Step Up Converter

Frequency Selection

The EUP2644 switching frequency can be user selected to operate at either constant 650kHz or 1.2MHz. Lower switching frequency can save power dissipation, while higher switching frequency can allow smaller external components like inductor and output capacitors, etc. Connecting FSEL pin to ground sets the PWM switching frequency to 650kHz, or connecting FSEL pin to V_{IN} for 1.2MHz.

Soft-Start

The soft-start is provided by an internal 3µA current source to charge the external soft start capacitor. The EUP2644 ramps up current limit from 0A up to full value, as the voltage at SS pin ramps from 0 to 0.6V. Hence the soft-start time is 2ms when the soft-start capacitor is 10nF, 9.42ms for 47nF and 20ms for 100nF.

Operation

The step up converter is a current mode PWM converter operating at either a 650kHz or 1.2MHz. It can operate in both discontinuous conduction mode (DCM) at light load and continuous mode (CCM). In continuous current mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by:

$$\frac{V_{STEP-UP}}{V_{IN}} = \frac{1}{1-D} \qquad \text{(EQ.1)}$$

Where D is the duty cycle of the switching MOSFET.

Figure 2 shows the block diagram of the boost regulator. It uses a error amplifier architecture consisting of gm stages for voltage feedback. A comparator looks at the peak inductor current cycle by cycle and terminates the PWM cycle if the current limit is reached.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. The boost converter output voltage is determined by the following equation:

$$V_{STEP-UP} = \frac{R1+R2}{R2} \times V_{FB} \qquad \text{(EQ. 2)}$$

The current through the MOSFET is limited to 2.9 A_{PEAK}. This restricts the maximum output current (average) based on the following equation:

$$I_{OMAX} = \left(I_{LMT} - \frac{\Delta I_L}{2} \right) \times \frac{V_{IN}}{V_O} \qquad \text{(EQ.3)}$$

Where ΔI_L is peak to peak inductor ripple current, and is set by:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_S} \qquad \text{(EQ.4)}$$

where f_S is the switching frequency (650kHz or 1.2MHz). The Table 1 gives typical values (margins are considered 10%, 3%, 20%, 10% and 15% on V_{IN}, V_O, L, f_S and I_{OMAX}).

Table 1. Maximum Output Current Calculation

V_{IN}(V)	V_O(V)	L(uH)	F_S(MHz)	I_{OMAX}(mA)
3	9	10	0.65	553
3	12	10	0.65	400
3	15	10	0.65	319
5	9	10	0.65	1110
5	12	10	0.65	838
5	15	10	0.65	675
3	9	10	1.2	486
3	12	10	1.2	342
3	15	10	1.2	226
5	9	10	1.2	1066
5	12	10	1.2	779
5	15	10	1.2	610

Capacitor

An input capacitor is used to suppress the voltage ripple injected into the boost converter. The ceramic capacitor with capacitance larger than 10µF is recommended. The voltage rating of input capacitor should be larger than the maximum input voltage.

Inductor

The boost inductor is a critical part which influences the output voltage ripple, transient response, and efficiency. Values of 3.3µH to 10µH are used to match the internal slope compensation. The inductor must be able to handle the following average and peak current:

$$I_{LAVG} = \frac{I_O}{1-D}$$

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2} \qquad \text{(EQ.5)}$$

Rectifier Diode

A high-speed diode is necessary due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The reverse voltage rating of this diode should be higher than the maximum output voltage. The rectifier diode must meet the output current and peak inductor current requirements.

Output Capacitor

The output capacitor supplies the load directly and reduces the ripple voltage at the output. Output ripple voltage consists of two components: the voltage drop due to the inductor ripple current flowing through the ESR of output capacitor, and the charging and discharging of the output capacitor.

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{OUT}} \times \frac{1}{f_S}$$

(EQ.6)

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

Note: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across then increases. COUT in the equation above assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at zero volts.

Compensation

The boost converter of EUP2644 can be compensated by a RC network connected from COMP pin to ground. 4.7nF and 10k RC network is used in the demo board. The larger value resistor and lower value capacitor can lower the transient overshoot, however, at the expense of stability of the loop.

Linear-Regulator (LDO)

The EUP2644 includes a LDO with adjustable output, and it can supply current up to 400mA. The output voltage is adjusted by connection of LFB pin. When LFB pin is connected to ground, the output voltage is set to 3.3V; when LFB pin is floating, the output voltage is set to 2.85V, and when LFB pin is connected to LOUT pin, the output voltage is set to 2.5V.

The efficiency of LDO is depended on the difference between input voltage and output voltage, as well as the output current:

$$\eta(\%) = \frac{V_{LVIN}}{V_{LOUT}} \times 100\% \quad \text{(EQ.7)}$$

The less difference between input and output voltage, the higher efficiency it is. The typical dropout voltage of LDO of EUP2644 is 300mV.

The ceramic capacitors are recommended for the LDO input and output capacitor. Larger capacitors help reduce noise and deviation during transient load change.

Gate Pulse Modulator Circuit

The gate pulse modulator circuit functions as a three way multiplexer, switching VGHM between ground, VGL and VGH. Voltage selection is provided by digital inputs VDPM (enable) and CTRL (control). High to low delay and slew control is provided by external components on pins CE and RE, respectively. A block diagram of the gate pulse modulator circuit is shown in Figure 3. When VDPM is LOW, the block is disabled and VGHM is grounded. When VDPM is HIGH, the output is determined by CTRL. When CTRL goes high, VGHM is pulled to VGH by a 70Ω switch. When CTRL goes low, there is a delay controlled by capacitor CE, following which VGHM is driven to VGL, with a slew rate controlled by resistor RE. Note that VGL is used only as a reference voltage for an amplifier, thus does not have to source or sink a significant DC current.

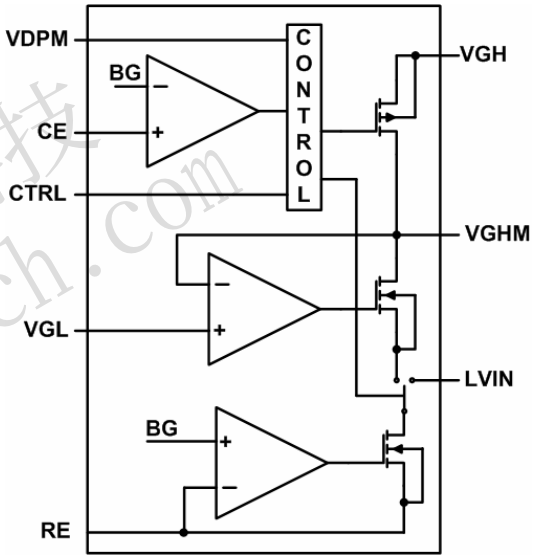


Figure 3. Gate Pulse Modulator Circuit Block Diagram

Low to high transition is determined primarily by the switch resistance and the external capacitive load. High to low transition is more complex. Take the case where the block is already enabled (VDPM is H). When CTRL is H, pin CE is grounded. On the falling edge of CTRL, a current is passed into pin CE, to charge an external capacitor to 1.2V. This creates a delay, equal to CE*4200. At this point, the output begins to pull down from VGH to VGL. The slew current is equal to 300/(RE+5000)*Load Capacitance.

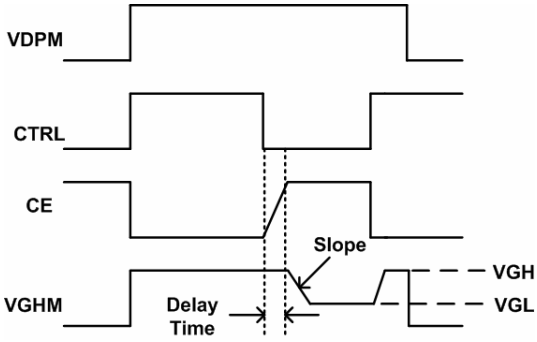


Figure 4. Gate Pulse Modulator Timing Diagram

Start-Up Sequence

Figure 5 shows a detailed start up sequence waveform.

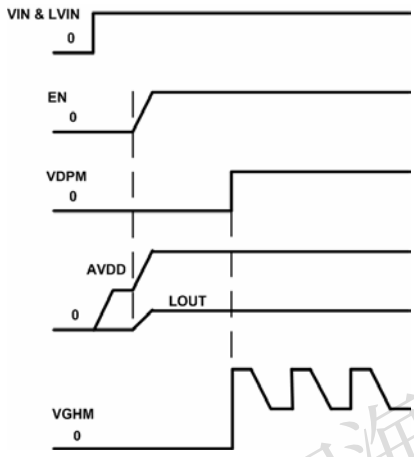


Figure 5. Start-Up Sequence

When V_{IN} exceeds 2.5V and EN reaches the VIH threshold value, step up converter and LDO start up, and gate pulse modulator circuit output holds until VDPM goes to high. Note that there is a DC path in the step up converter from the input to the output through the inductor and diode, hence the input voltage will be seen at output with a forward voltage drop of diode before the part is enabled. If this voltage is not desired, the following circuit can be inserted between input and inductor to disconnect the DC path when the part is disabled.

V_{COM} Amplifier

The V_{COM} amplifier is designed to control the voltage on the back plate of an LCD display. This plate is capacitively coupled to the pixel drive voltage which alternately cycles positive and negative at the line rate for the display. Thus the amplifier must be capable of sourcing and sinking capacitive pulses of current, which can occasionally be quite large (a few 100mA for typical applications). The EUP2644 V_{COM} amplifier's output current is limited to 400mA. This limit level, which is roughly the same for sourcing and sinking, is included to maintain reliable operation of the part. It does not necessarily prevent a large temperature rise if the current is maintained. (In this case the whole chip may be shut down by the thermal trip to protect functionality.) If the display occasionally demands current pulses higher than this limit, the reservoir capacitor will provide the excess and the amplifier will top the reservoir capacitor back up once the pulse has stopped. This will happen on the µs time scale in practical systems and for pulses 2 or 3 times the current limit, the V_{COM} voltage will have settled again before the next line is processed.

Fault Protection

EUP2644 provides the overall fault protections including over current protection and over-temperature protection. An internal temperature sensor continuously monitors the die temperature. In the event that die temperature exceeds the thermal trip point, the device will shut down and disable itself. The upper and lower trip points are typically set to +160°C and +120°C respectively.

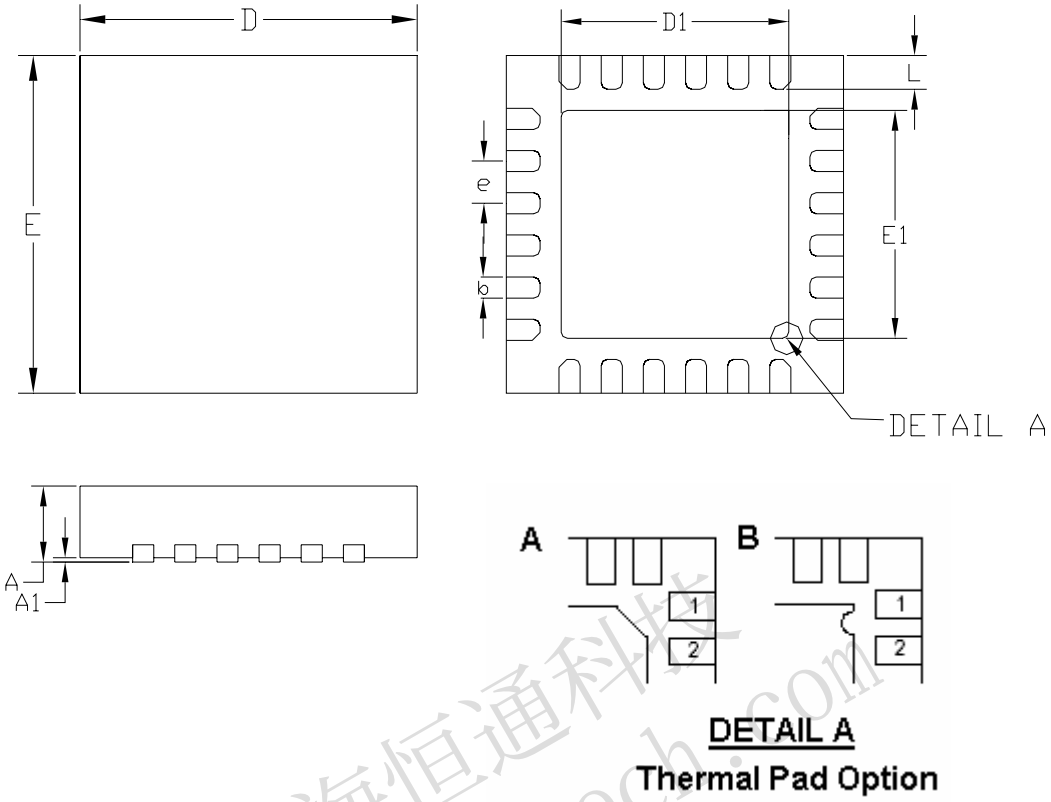
Layout Consideration

The device's performance including efficiency, output noise, transient response and control loop stability is dramatically affected by the PCB layout. PCB layout is critical, especially at high switching frequency.
There are some general guidelines for layout:

1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place VIN and VDD bypass capacitors close to the pins.
3. Reduce the loop area with large AC amplitudes and fast slew rate.
4. The feedback network should sense the output voltage directly from the point of load, and be as far away from LX node as possible.
5. The power ground (PGND) and signal ground (SGND) pins should be connected at only one point.
6. The exposed die plate, on the underneath of the package, should be soldered to an equivalent area of metal on the PCB. This contact area should have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers, if available, to maximize thermal dissipation away from the IC.
7. To minimize the thermal resistance of the package when soldered to a multi-layer PCB, the amount of copper track and ground plane area connected to the exposed die plate should be maximized and spread out as far as possible from the IC. The bottom and top PCB areas especially should be maximized to allow thermal dissipation to the surrounding air.
8. A signal ground plane, separate from the power ground plane and connected to the power ground pins only at the exposed die plate, should be used for ground return connections for control circuit.
9. Minimize feedback input track lengths to avoid switching noise pick-up. A demo board is available to illustrate the proper layout implementation.

Packaging Information

TQFN-24



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.18	0.30	0.007	0.012
E	3.90	4.10	0.154	0.161
D	3.90	4.10	0.154	0.161
D1	2.70		0.106	
E1	2.70		0.106	
e	0.50		0.020	
L	0.30	0.50	0.012	0.020