Dual 1A, 2.25MHz Synchronous Step-Down DC/DC Regulator

DESCRIPTION

The EUP3402 is synchronous dual step-down DC-DC converters optimized for battery powered portable applications. It provides two independent output voltage rails powered by 1-cell Li-Ion or 3-cell NiMH/NiCD batteries. The device is also suitable to operate from a standard 3.3V or 5V voltage rail.

With an input voltage range of 2.7V to 5.5V, the EUP3402 is ideal to power portable applications like smart phones, PDAs and other portable equipment.

The EUP3402 operates at 2.25MHz fixed switching frequency allowing the use of small inductors and capacitors to achieve a small solution size. Each output supports up to 1A load current, typical. The internal synchronous switch increases efficiency and eliminates the need for an external schottky diode.

The EUP3402 has a user selectable mode of forced PWM and PFM/PWM mode. The forced PWM mode operation provides the lowest ripple noise and the PFM mode operation provides high efficiency at light loads.

The EUP3402 has internal soft start and avoids inrush current during startup. When shutdown, internal resistor discharges the output capacitor.

FEATURES

- High Efficiency Up to 95%
- 2.25MHz Constant Switching Frequency
- Dual 1A Available Load Current
- 45μA Typical Quiescent Current
- 2.7V to 5.5V Input Voltage Range
- 2 Channel 180 Degree Out of Phase Operation
- Adjustable Output Voltage as Low as 0.6V
- No Schottky Diode Required
- Short Circuit and Thermal Protection
- Power Good Output
- Internal Soft Start Function
- Available in 3mm×3mm TDFN-10 Package
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

APPLICATIONS

- SSD Module
- Smart Phones
- Tablet PC
- Portable Media Players
- μC/μP, FPGA and DSP Power
- Plug-in DC/DC Modules for Routers and Switchers

Typical Application Circuit

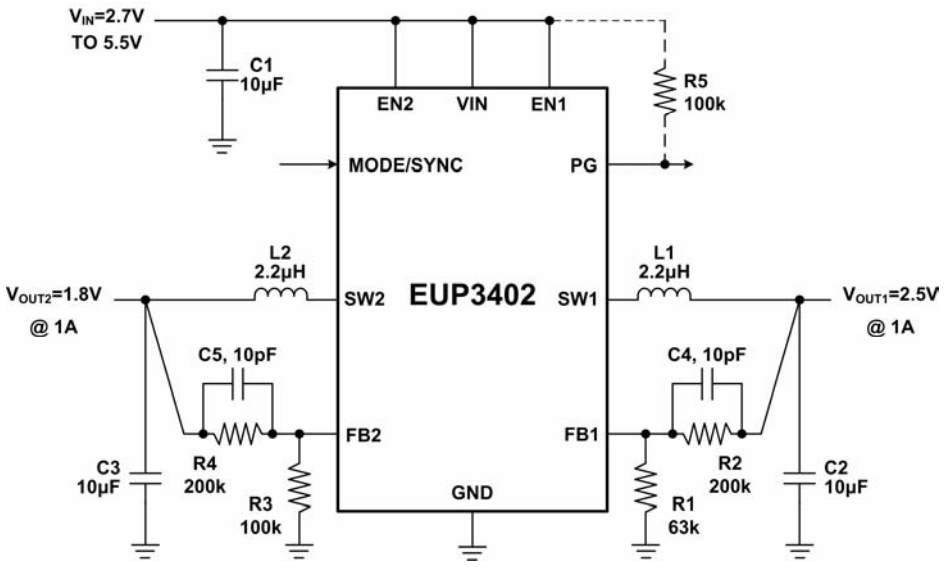
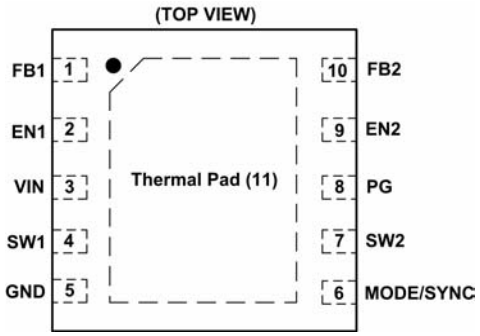


Figure 1.

Pin Configurations

Package Type	Pin Configurations
TDFN-10	

Pin Description

Name	Pin	DESCRIPTION
FB1	1	Output Feedback of Regulator 1. Receives the feedback voltage from the external resistive divider across the output. Nominal voltage for this pin is 0.6V.
EN1	2	Regulator 1 Enable. Forcing this pin to VIN enables regulator 1, while forcing it to GND causes regulator 1 to shut down. Do not leave this pin floating.
VIN	3	Main Power Supply. Must be closely decoupled to GND.
SW1	4	Regulator 1 Switch Node Connection to the Inductor.
GND	5	Main Ground. Connect to the (-) terminal of output capacitor, and (-) terminal of input capacitor.
MODE/SYNC	6	Combination mode selection and oscillator synchronization. When tied to low, forced PWM mode is selected. When tied to high, PFM/PWM mode is selected. Do not leave this pin floating. The switching frequency can be synchronized to an external oscillator applied to this pin and forced PWM mode is automatically selected.
SW2	7	Regulator 2 Switch Node Connection to the Inductor.
PG	8	Power Good Output. When both channels are enabled, this pin is pulled low if any output is not in regulation. If one channel is disabled, then PG only monitors the active channels. There is an internal 1MΩ pull-up resistor.
EN2	9	Regulator 2 Enable. Forcing this pin to VIN enables regulator 2, while forcing it to GND causes regulator 2 to shut down. Do not leave this pin floating.
FB2	10	Output Feedback of Regulator 2. Receives the feedback voltage from the external resistive divider across the output. Nominal voltage for this pin is 0.6V
Thermal Pad (GND)	11	Power Ground. Connect to the (-) terminal of output capacitor, and (-) terminal of input capacitor. Must be soldered well to electrical ground on PCB.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP3402JIR1	TDFN-10	xxxxx P3402 20	-40°C to +85°C

EUP3402 □ □ □ □

Lead Free Code
1: Lead Free, Halogen Free

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
J: TDFN

Block Diagram

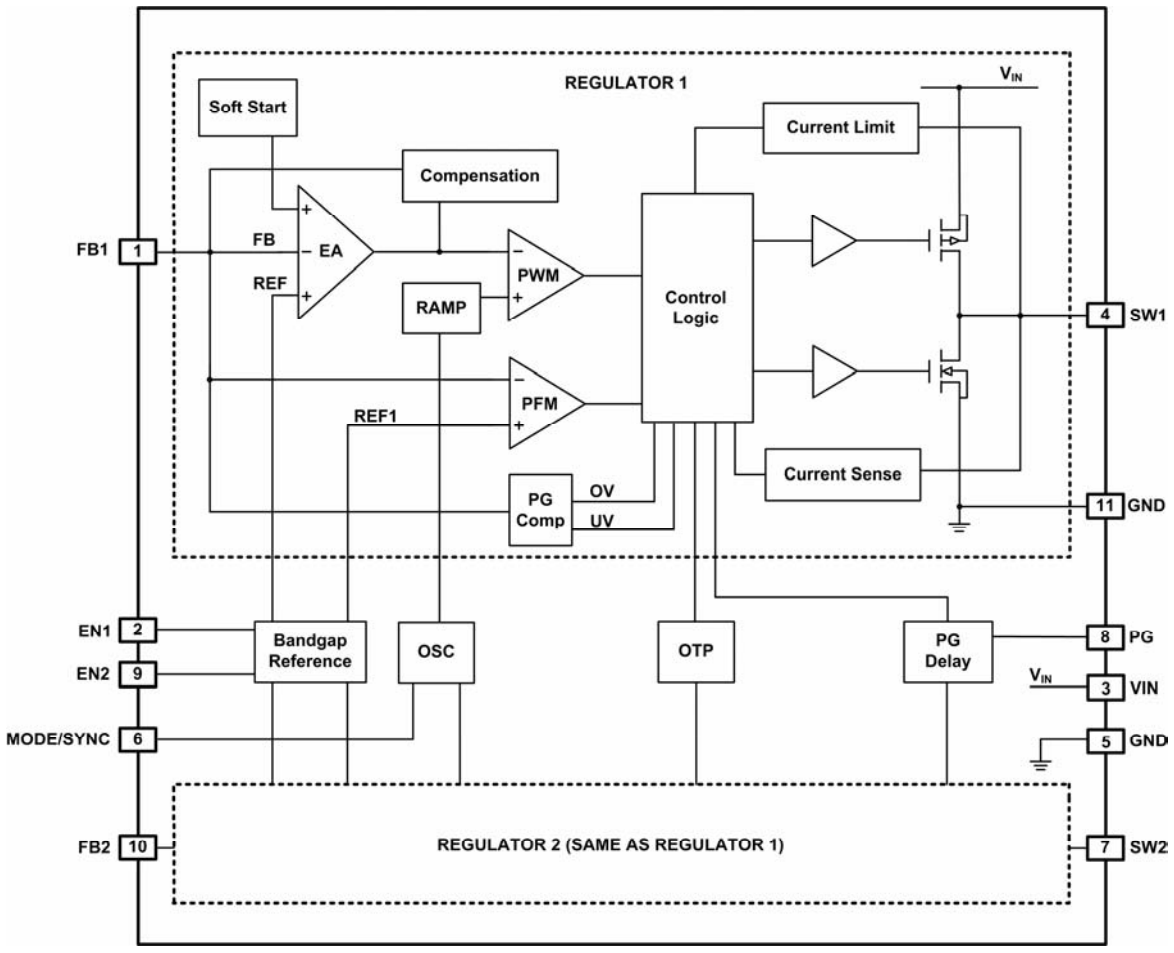


Figure 2.

Absolute Maximum Ratings (1)

- Input Supply Voltage ---------- -0.3V to 6V
- FB1, FB2, SW1, SW2 Voltages ---------- -0.3V to V_{IN} +0.3V
- EN1, EN2, MODE/SYNC, PG Voltages ---------- -0.3V to 6V
- Junction Temperature ---------- 125°C
- Storage Temperature ---------- -65°C to +150°C
- Lead Temp (Soldering, 10sec) ---------- 300°C

Recommended Operating Conditions (2)

- Supply Voltage ---------- 2.7V to 5.5V
- Operating Temperature ---------- -40°C to +85°C

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.

Note (2): The device is not guaranteed to function outside the recommended operating conditions.

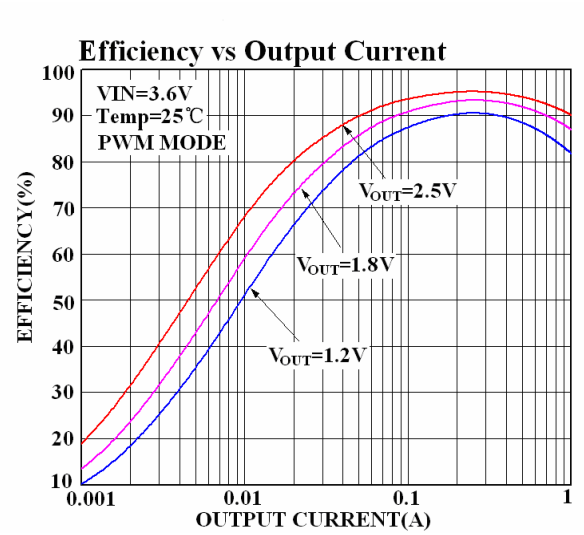
Electrical Characteristics

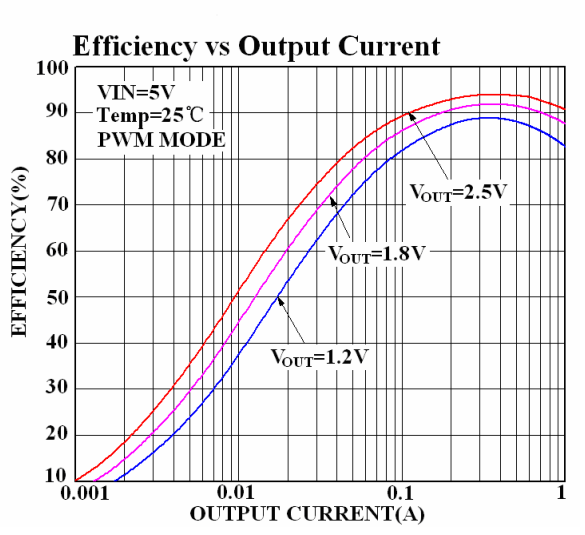
The ● denote the Spec. apply over the full operating temperature range, otherwise Spec. are T_A=+25°C. V_{IN}=3.6V unless otherwise specified.

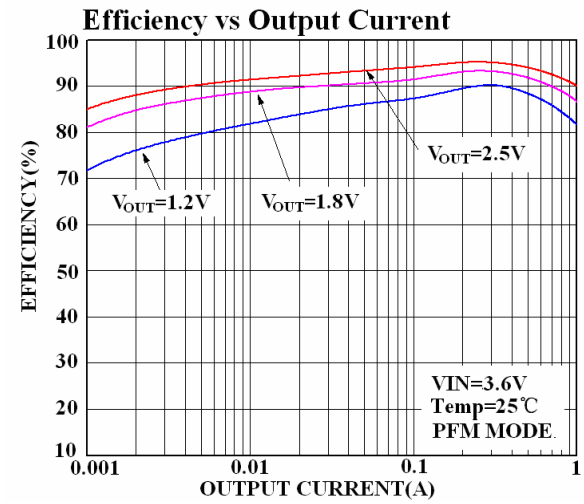
Symbol	Parameter	Conditions		EUP3402			Unit
				Min.	Typ.	Max.	
V_{IN}	Input Voltage Range		●	2.7		5.5	V
UVLO	Input Undervoltage Lockout	Rising			2.5	2.65	V
$UVLO_{\_Hys}$	UVLO Hysterisis				200		mV
I_{FB}	Feedback Current				0		µA
V_{FB}	Regulated Feedback Voltage	T_A=+25°C		0.594	0.6	0.606	V
		-40°C≤ T_A ≤ +85°C	●	0.588	0.6	0.612	V
ΔV_{FB}	Reference Voltage Line Regulation	V_{IN}=2.7V to 5.5V			0.2		%/V
ΔV_{OUT}	Output Voltage Load Regulation	I_{LOAD}=0 to 1A, MODE/SYNC=0V			0.5		%/A
I_Q	Quiescent Current	MODE/SYNC=0V, EN1=EN2=3.6V,(Note 3)			0.9	1.1	mA
		MODE/SYNC=3.6V, EN1=EN2=3.6V,(Note 3)			45	55	µA
I_{SHUT}	Shutdown Current	EN1=EN2=0V, V_{IN}=5V			5.7	10	µA
I_{PK}	Peak Inductor Current				1.6		A
I_{REV}	Reverse Current Limit				1.5		A
f_{OSC}	Oscillator Frequency		●	1.8	2.25	2.7	MHz
f_{SYNC}	Synchronization Frequency			2.7		4	MHz
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SWX}=200mA			170		mΩ
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SWX}=-200mA			160		mΩ
I_{LSW}	SW Leakage Current	EN1=EN2=0V, SWX=0V				1	µA
	Soft Discharge Current	EN1=EN2=0V, SWX=3.6V			21		mA
V_{EN}	EN Threshold Low		●	0		0.3	V
	EN Threshold High		●	2			V
I_{EN}	EN Leakage Current		●			1	µA
V_{MODE}	MODE Threshold Low			0		0.3	V
	MODE Threshold High			V_{IN}-0.5			V
PG	PG Low Rising Threshold	Percentage of nominal voltage			92		%
	Output Low Voltage	Sinking 1mA, FB1=FB2=0.5V			0.165		V
T_{SD}	Thermal Shutdown				150		°C
T_{SD_Hys}	Thermal Shutdown Hysterisis				20		°C

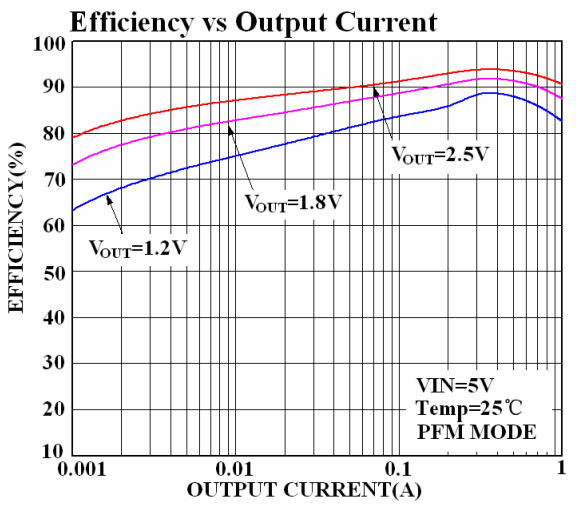
Note (3): Tested in a proprietary test mode.

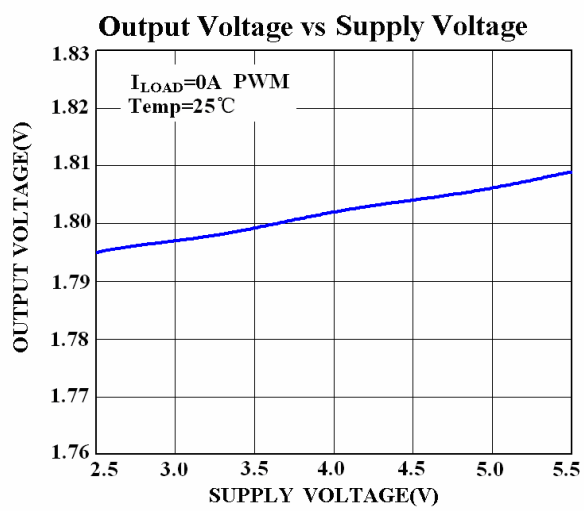
Typical Operating Characteristics

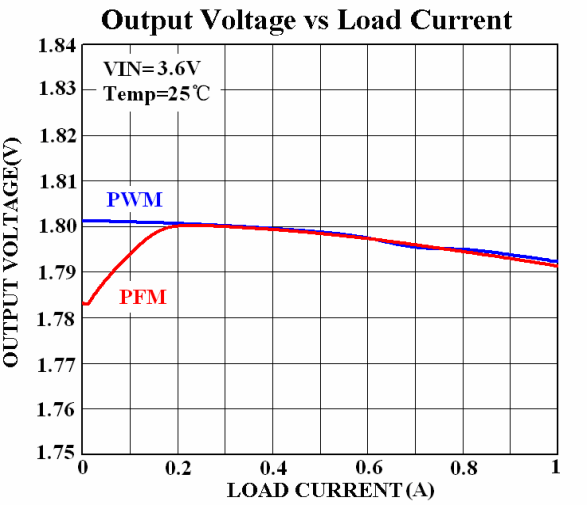




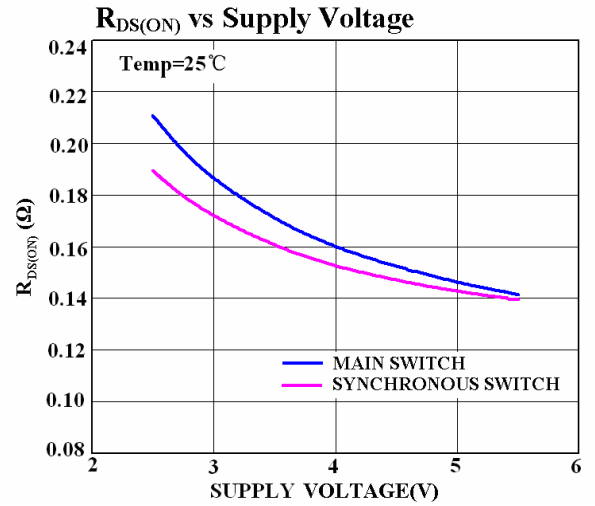


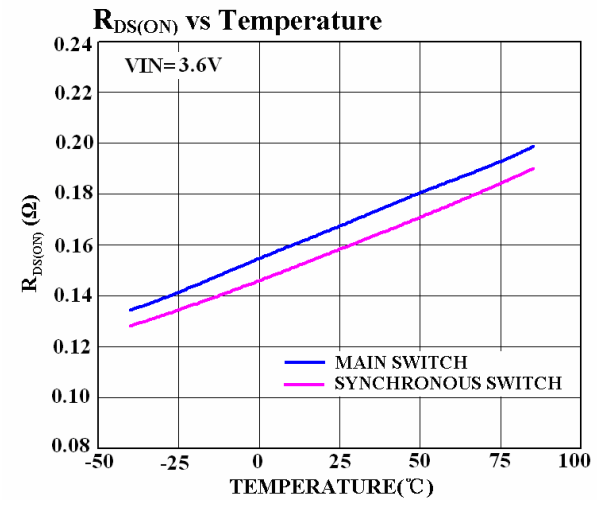


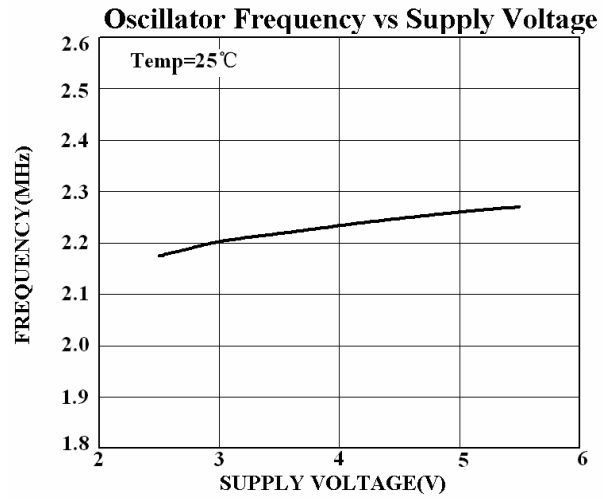


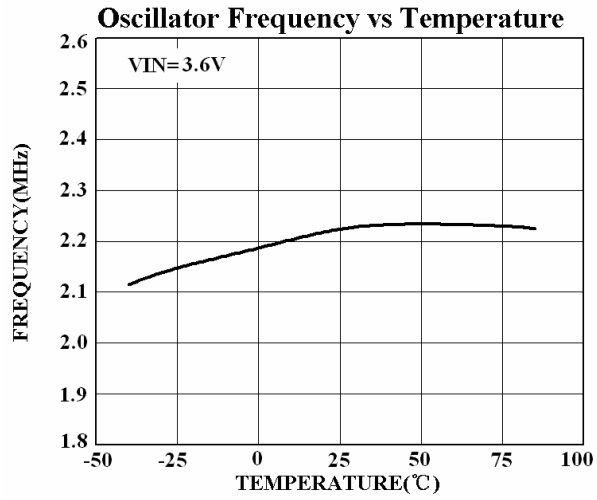


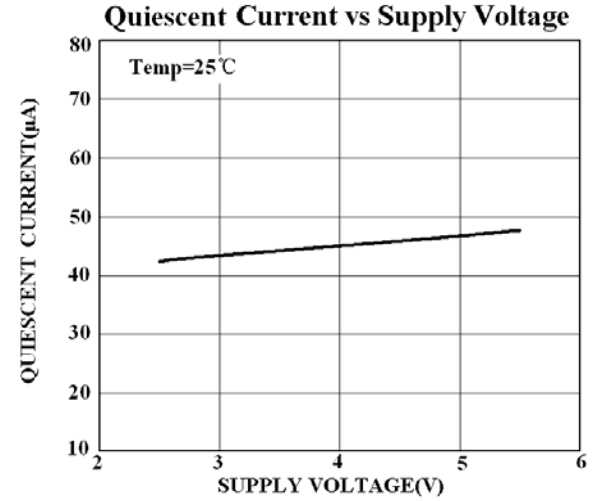
Typical Operating Characteristics (continued)

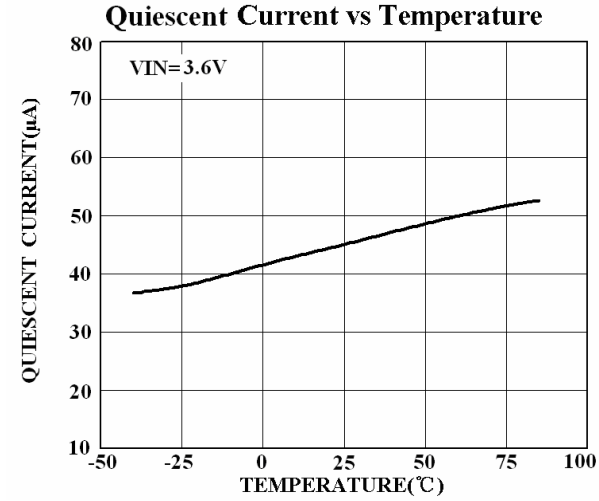






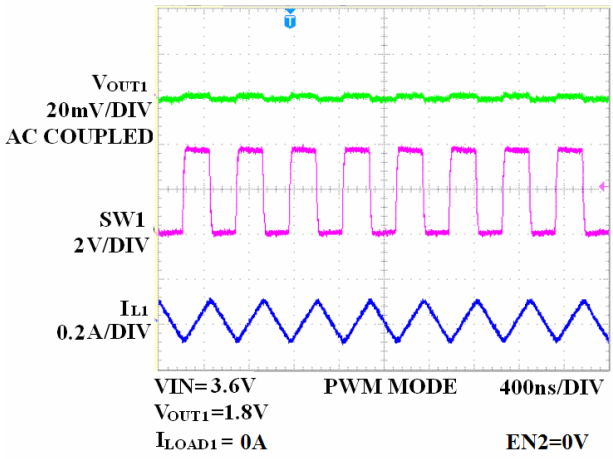




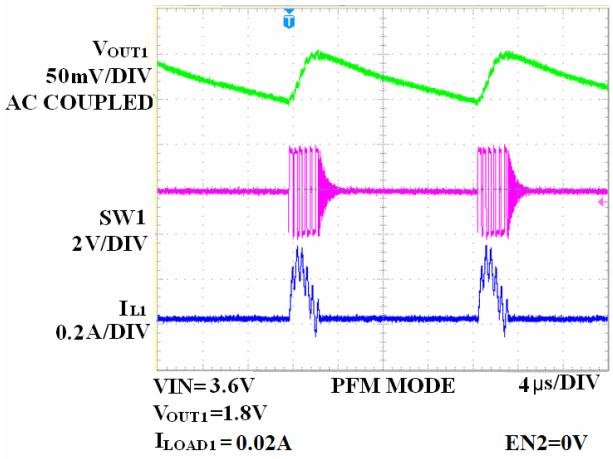


Typical Operating Characteristics (continued)

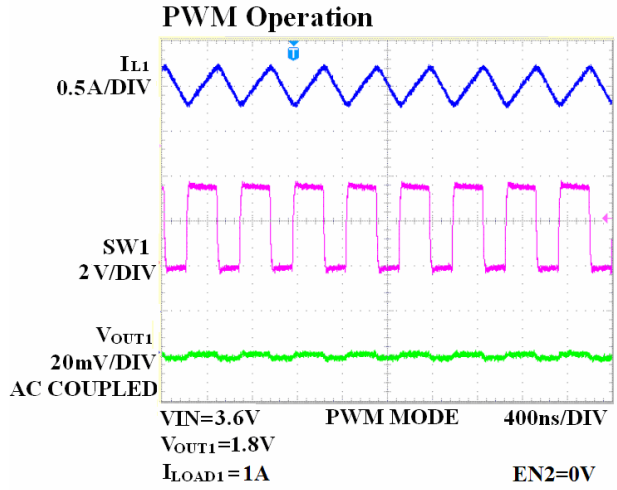
PWM Operation



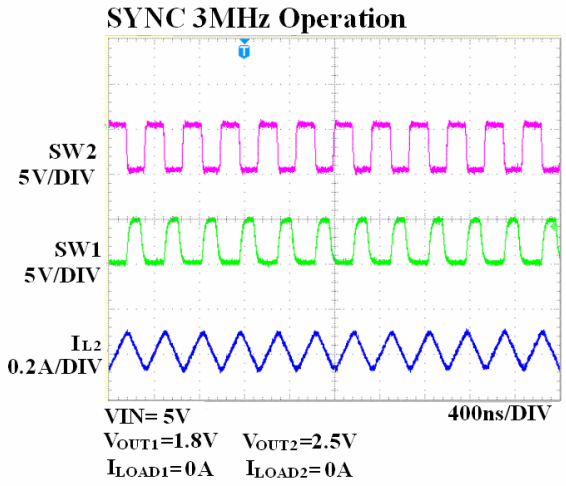
PFM Operation



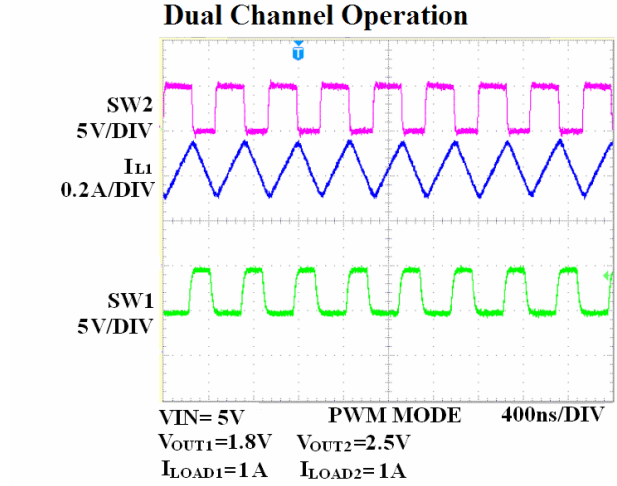
PWM Operation



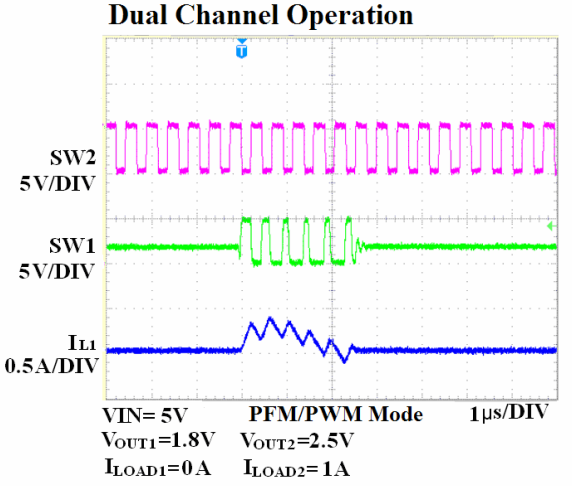
SYNC 3MHz Operation



Dual Channel Operation

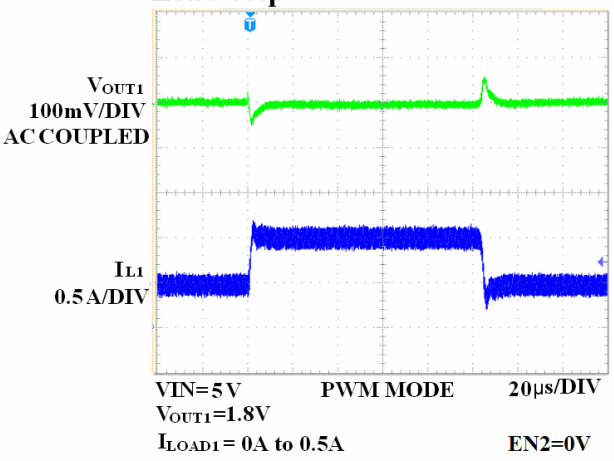


Dual Channel Operation

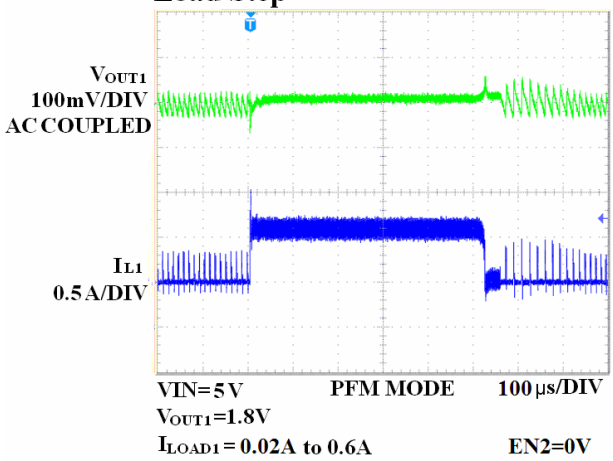


Typical Operating Characteristics (continued)

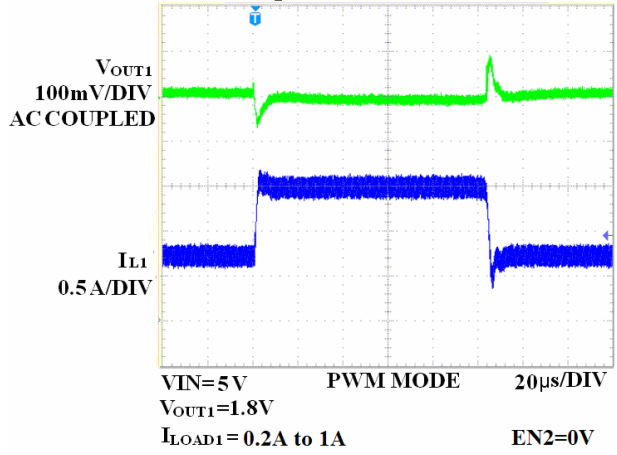
Load Step



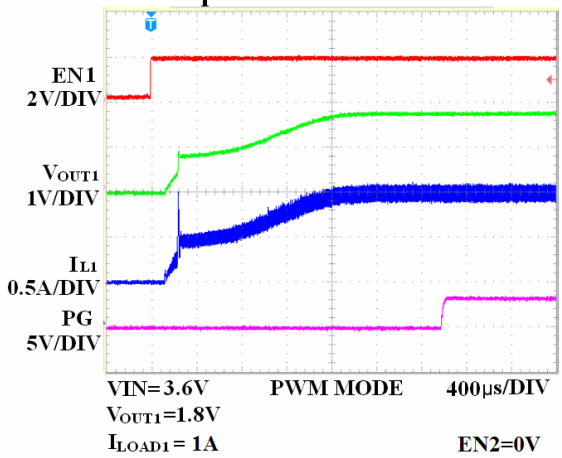
Load Step



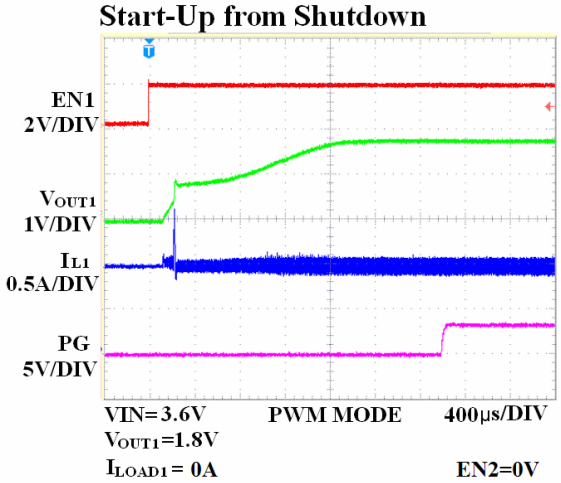
Load Step



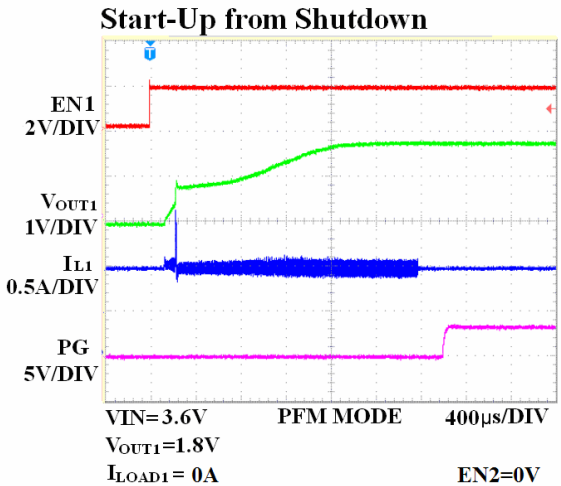
Start-Up from Shutdown



Start-Up from Shutdown

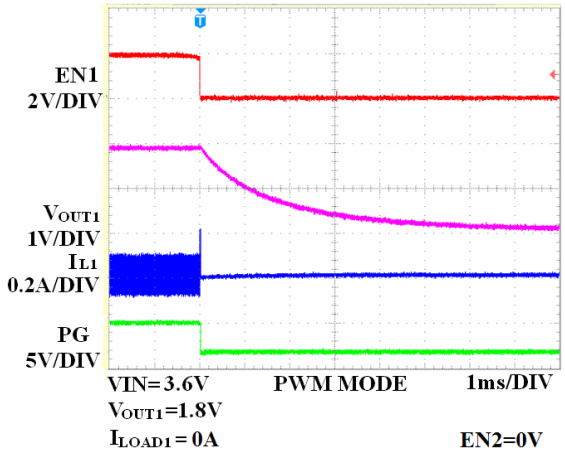


Start-Up from Shutdown

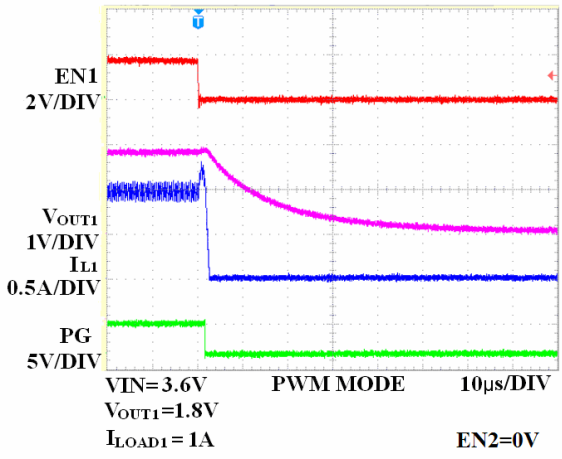


Typical Operating Characteristics (continued)

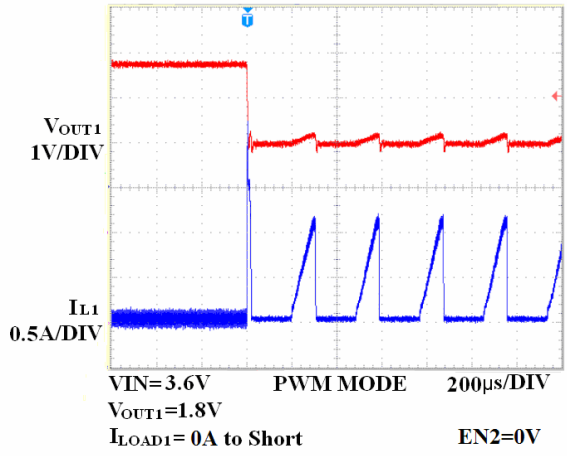
Power Down



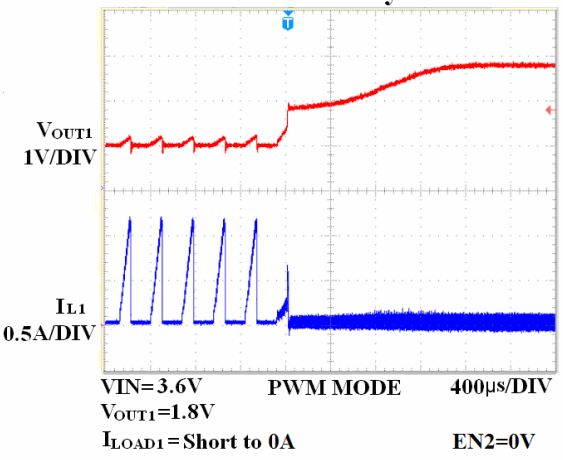
Power Down



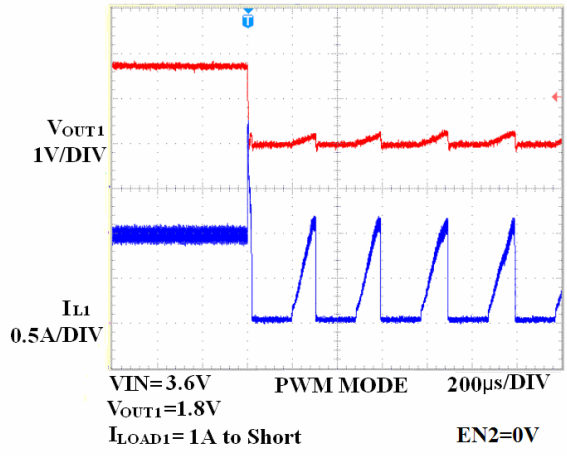
Short Circuit Test



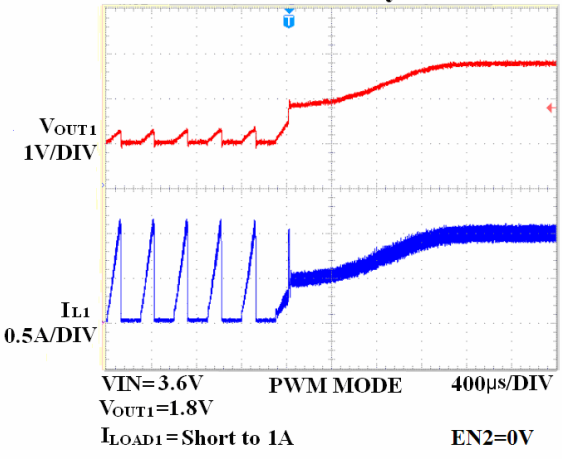
Short Circuit Recovery



Short Circuit Test



Short Circuit Recovery



OPERATION

The EUP3402 uses voltage mode architecture with synchronous rectification. Both the main (P-Channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. The operating frequency is set at 2.25MHz and can be synchronized to an external oscillator. The two channels are 180 degree out of phase operation. The selectable MODE/SYNC pin allows the user to trade-off noise for efficiency.

Forced PWM Operation

Pulling MODE/SYNC pin low selects forced PWM mode. During normal operation, the EUP3402 regulates output voltage by switching at a constant frequency and then modulating the power transferred to the load each cycle using PWM comparator. The duty cycle is controlled by two weighted differential signals: the output of error amplifier and the sawtooth ramp. It modulates output power by adjusting the PFET switch on time during the first half of each cycle. An N-channel, synchronous switch turns on during the second half of each cycle (off time). When the PWM cycle reaches the end of the oscillator period, the synchronous switch turns off. Forced PWM operation provides low ripple noise.

PFM/PWM Operation

Pulling MODE/SYNC high selects auto mode. The converter will automatically switch between PFM state and PWM state based on load demand. At light loads, the device enters PFM mode and operates with reduced switching frequency and quiescent current to maintain high efficiency. During PFM operation, there are two thresholds to control the loop and limit the output ripple as shown in Figure 3. With the increase of load current, the converter changes from PFM to PWM mode with smooth transition.

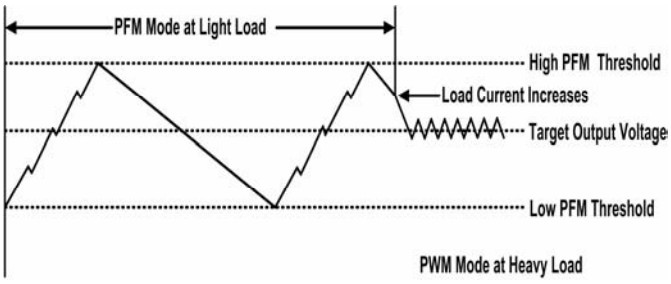


Figure.3 Operation in PFM mode and transfer to PWM mode

Power Good

The PG pin monitors both of the output channels. It is an open-drain output. When both channels are enabled, this pin is pulled low if any output is not in regulation. If one channel is disabled, then PG only monitors the active channels. When powering up, the PG pin holds low for about 1ms after output reaches the preset voltage.

Soft Start and Soft Stop

The EUP3402 has internal soft-start circuit that limits the inrush current and output overshoot during startup. The generated ramp reference limits the rising speed of inductor current and output voltage. When the converter is shutdown, the output is discharged to GND through an internal resistor connected with SW pin.

Input Undervoltage Lockout

The undervoltage lockout circuit prevents device misoperation at low input voltages. It prevents the converter from turning on the main and synchronous switches under undervoltage state.

Frequency Synchronization

The switching frequency can be synchronized by an external signal applied to the MODE/SYNC pin. During synchronization, the mode is set to forced PWM operation.

APPLICATIONS INFORMATION

Inductor Selection

The EUP3402 typically uses a 2.2µH inductor. The output inductor is selected to limit the ripple current to some predetermined value, typically 20%~40% of the full load current at the maximum input voltage. Large value inductors lower ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation.

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. The DC resistance of the inductor directly influences the efficiency of the converter. Therefore for better efficiency, choose a low DC-resistance inductor.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. The primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the EUP3402. A low ESR input capacitor sized for the maximum RMS current must be used. The size required will vary depending on the load, output voltage and input voltage source impedance characteristics. A typically C_{IN} value is around 10µF. If the wire of supply is too long, larger input capacitor should be used.

The input capacitor RMS current varies with the input voltage and the output voltage. The equation for the maximum RMS current in the input capacitor is:

$$I_{RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The output capacitor C_{OUT} has a strong effect on loop stability.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). ESR is a direct function of the volume of the capacitor; that is, physically larger capacitors have lower ESR. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} in PWM mode is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}}\right)$$

In some cases, 0.1µF to 1µF of ceramic capacitors should also be placed closed to EUP3402 in parallel with the main capacitors for high frequency decoupling. When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6V\left(1 + \frac{R2}{R1}\right)$$

The external resistive divider is connected to the output, allowing remote voltage sensing as shown in Figure 4.

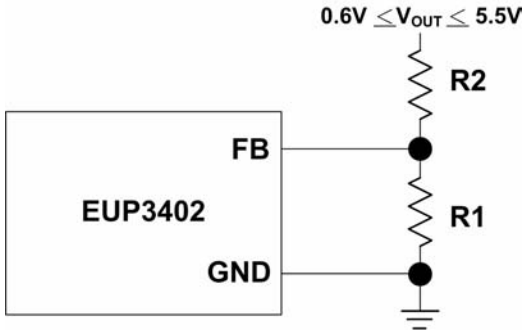


Figure 4. Setting the EUP3402 Output Voltage

Thermal Considerations

To avoid the EUP3402 from exceeding the maximum junction temperature, the user will need to do a thermal analysis. The goal of the thermal analysis is to determine whether the operating conditions exceed the maximum junction temperature of the part. The temperature rise is given by:

$$T_R=(P_D)(\theta_{JA})$$

Where $P_D=I_{LOAD}^2 \times R_{DS(ON)}$ is the power dissipated by the regulator ; θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J=T_A+T_R$$

Where T_A is the ambient temperature.

T_J should be below the maximum junction temperature of 125°C.

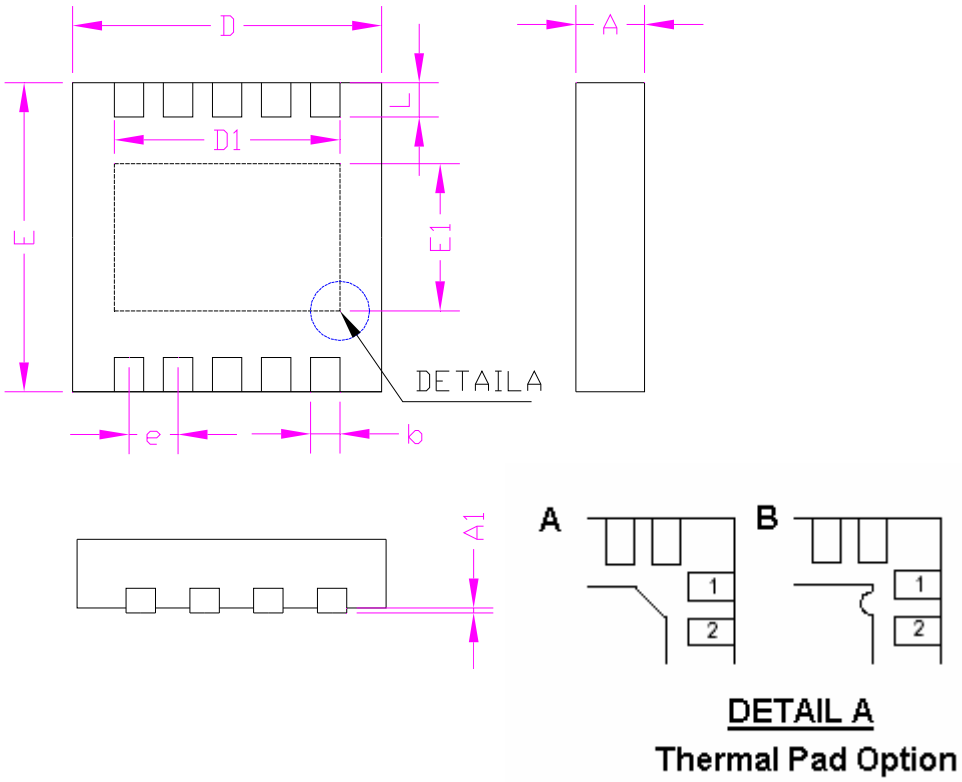
PC Board Layout Checklist

When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the EUP3402.

1. The input capacitor C_{IN} should connect to VIN as closely as possible. This capacitor provides the AC current to the internal power MOSFETs.
2. The power traces, consisting of the GND trace, the SW1, SW2 trace and the VIN trace should be kept short, direct and wide.
3. The FB1 and FB2 pin should connect directly to the feedback resistors. The resistive divider R1/R2 and R3/R4 must be connected between the C_{OUT} and ground.
4. Keep the switching node, SW1 and SW2, away from the sensitive FB1 and FB2 node.
5. For good thermal coupling, PCB vias are required from the Pad for the TDFN paddle to the ground plane.

Packaging Information

TDFN-10



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
D	2.90	3.10	0.114	0.122
E1	1.70		0.067	
E	2.90	3.10	0.114	0.122
L	0.30	0.50	0.012	0.020
b	0.18	0.30	0.007	0.012
e	0.50		0.020	
D1	2.40		0.094	