3.2A, Synchronous Step-Down Converter

DESCRIPTION

The EUP3423 is a 1 MHz fixed frequency synchronous, current-mode, step-down dc-dc converter capable of providing up to 3.2A output current. The EUP3423 operates from an input range of 2.7V to 5.5V and provides a regulated output voltage from 0.8V to 5V. The internal synchronous power switch improves efficiency and eliminates the need for an external Schottky diode. Forced PWM operation provides very low output ripple voltage for noise sensitive applications.

The EUP3423 features short circuit and thermal protection circuits to improve system reliability. Externally adjustable soft-start avoids input inrush current during startup. The EUP3423 is available in SOP-8 (EP) package.

FEATURES

- 2.7V to 5.5V Input Voltage Range
- High Efficiency up to 96%
- 3.2A Available Load Current
- 100/60mΩ Integrated PFET/NFET Switches
- 1MHz Switching Frequency
- 100% Duty Cycle Low Dropout Operation
- Short Circuit and Thermal Protection
- Integrated UVLO
- Excellent Line and Load Transient Response
- Available in SOP-8(EP) Package
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

APPLICATIONS

- High Performance DSPs, FPGAs, ASICs and Microprocessors
- Base Station, Telecom, and Networking Equipment Power Supplies
- ePC and NetPCs

Typical Application Circuit

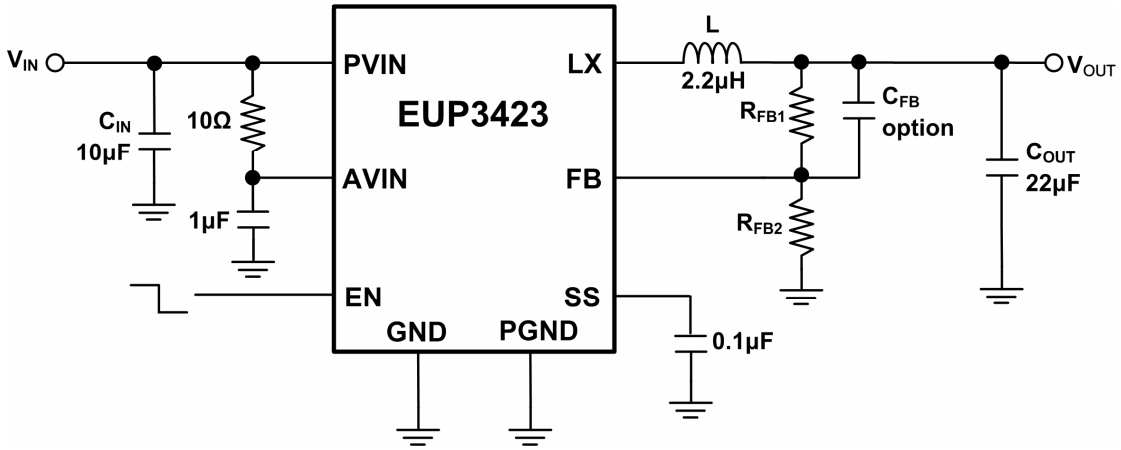
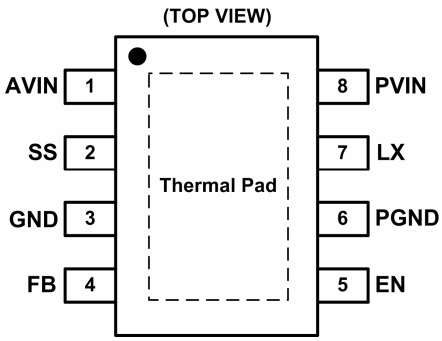


Figure1. Typical Application Circuit

Pin Configurations

Package Type	Pin Configurations
SOP-8 (EP)	

Pin Description

PIN	SOP-8 (EP)	DESCRIPTION
AVIN	1	Analog input supply which is connected to PVIN through a low pass RC filter.
SS	2	Soft-start pin. An internal pull up current source charges an external capacitor to set the soft-start ramp rate.
GND	3	Analog ground.
FB	4	Feedback pin. Connect it to an external resistor divider to set output voltage.
EN	5	Chip enable pin. Forcing this pin above 1.5V enables the part. Forcing this pin below 0.3V shut down the device.
PGND	6	Power ground.
LX	7	Switch node connected to inductor. This pin is connected to the drains of the internal main and synchronous power MOSFET switches.
PVIN	8	Bypass with a 10μF or 22μF ceremic capacitor to ground.
Thermal Pad	-	Ground.(Thermal pad is used as the ground of whole chip.)

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP3423WIR1	SOP-8 (EP)	xxxxx P3423	-40 °C to +85°C

EUP3423 □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen Free
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  W:SOP (EP)

Block Diagram

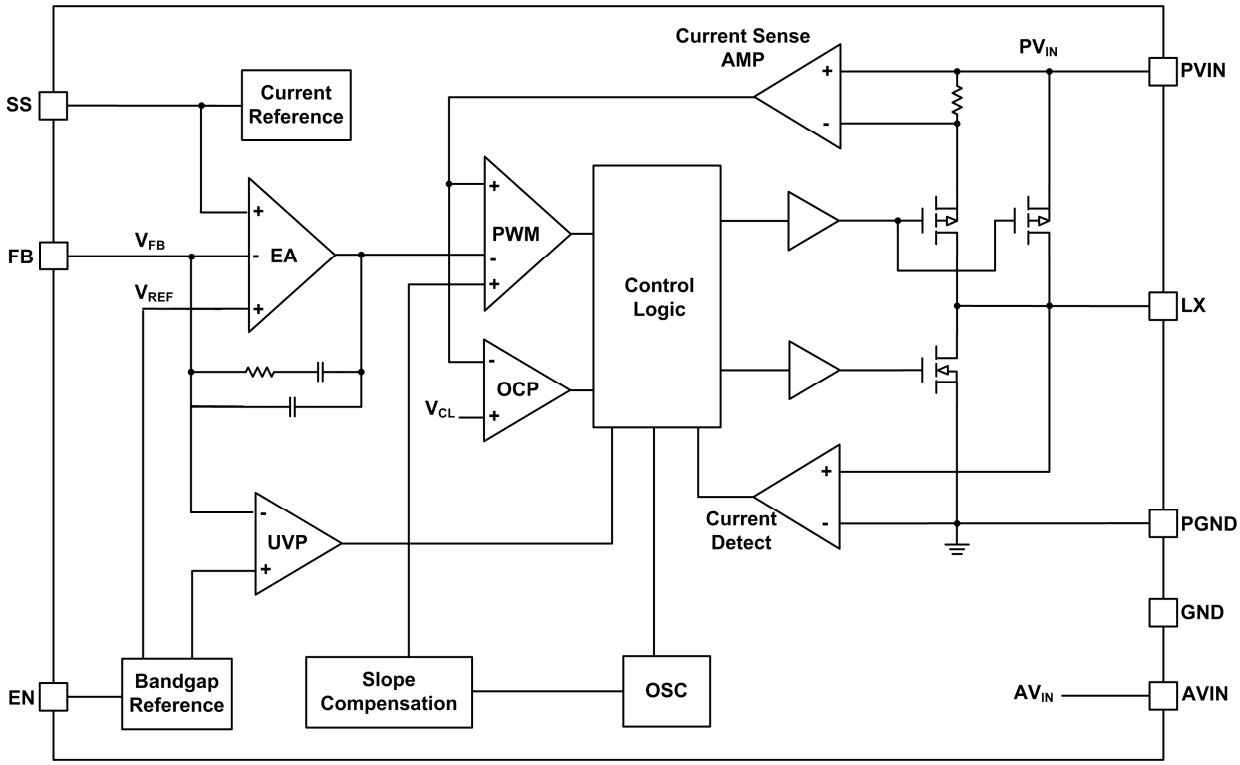


Figure3. Block Diagram

Absolute Maximum Ratings (1)

- Input Supply Voltage(AVIN, PVIN) ---------- -0.3V to 6V
- EN, FB, SS ---------- -0.3V to 6V
- LX Voltage ---------- -0.3V to V_{PVIN}+0.3V
- Junction Temperature ---------- 150°C
- Package Thermal Resistance
  SOP-8(EP) ,θ_{JA} ---------- 60°C/W
- Storage Temperature ---------- -65°C to 150°C
- Lead Temp (Soldering, 10sec) ---------- 260°C
- Minimum ESD Rating ---------- ±2kV

Recommended Operating Conditions (2)

- Supply Voltage ---------- 2.7V to 5.5V
- Operating Temperature Range ---------- -40°C to 85°C

Note(1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.

Note(2): The device is not guaranteed to function outside the recommended operating conditions.

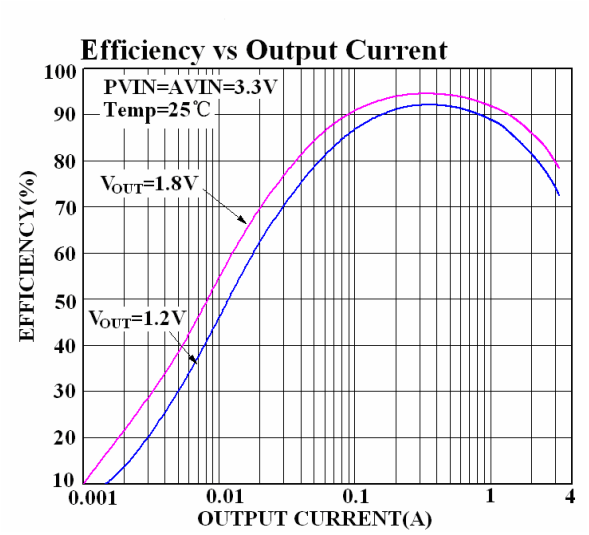
Electrical Characteristics

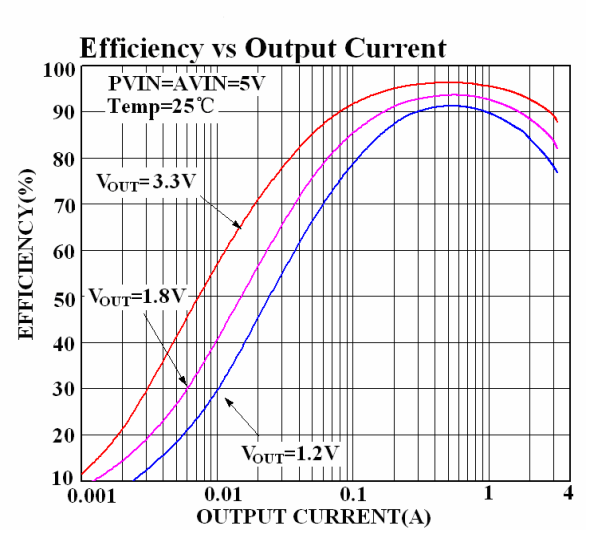
PVIN=AVIN=VEN=5V, T_A=+25°C,unless otherwise specified. The EUP3423 is 100% production tested at 25°C. Typical and temperature specifications are guaranteed by design and statistical characterizations.

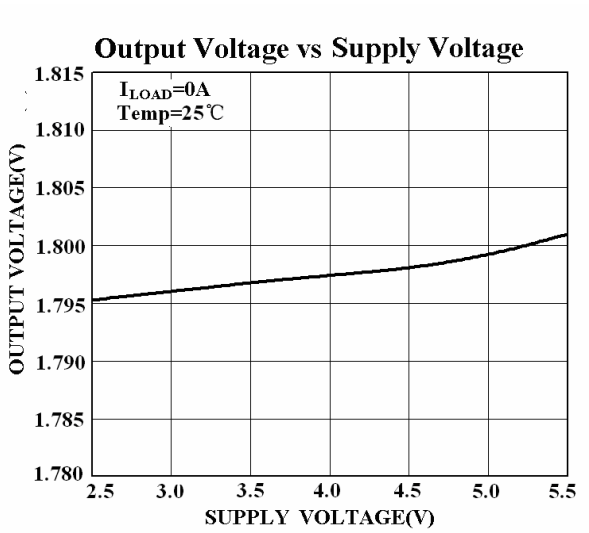
Symbol	Parameter	Conditions	EUP3423			Unit
			Min.	Typ.	Max.	
V_{IN}	Input Voltage Range	-40°C ≤T_A≤+85°C	2.7		5.5	V
UVLO	Input Undervoltage Lockout	Rising	2.1	2.3	2.5	V
UVLO_Hys	UVLO Hysteresis			150		mV
I_{FB}	Feedback Current	V_{FB}=0.8V	-50	0	+50	nA
V_{FB}	Regulated Feedback Voltage	T_A=+25°C	0.792	0.800	0.808	V
		-40°C≤T_A≤+85°C	0.784	0.800	0.816	
UVFB	FB Lockout Threshold			0.43		V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN}=2.7V to 5.5V		0.1		%/V
$V_{LOADREG}$	Output Voltage Load Regulation	I_{LOAD}=0A to 3.2A		0.1		%/A
V_{EN}	EN Threshold	-40°C≤T_A≤+85°C	0.3	1.0	1.5	V
I_Q	Quiescent Current	V_{FB}=0.72V, -40°C≤T_A≤+85°C		0.5	0.6	mA
I_{SHDN}	Shutdown Current	V_{EN}=0V, -40°C≤T_A≤+85°C			1	μA
f_{OSC}	Oscillator Frequency		0.8	1	1.2	MHz
D_{MAX}	Maximum Duty Cycle			100		%
I_{SS}	Soft Start Pull Up Current			20		μA
I_{PEAK}	Hside PCH Switch Peak Current			4		A
I_{NEG}	Lside NCH Negative Current Limit			-1		A
I_{LX}	LX Leakage Current	V_{EN}=0V, V_{LX}=0 or 5V	-5		5	μA
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{LX}=0.2A		100	120	mΩ
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{LX}=0.2A		60	80	mΩ
T_{SD}	Thermal Shutdown			160		°C
T_{SD_Hys}	Thermal Shutdown Hysterisis			20		°C

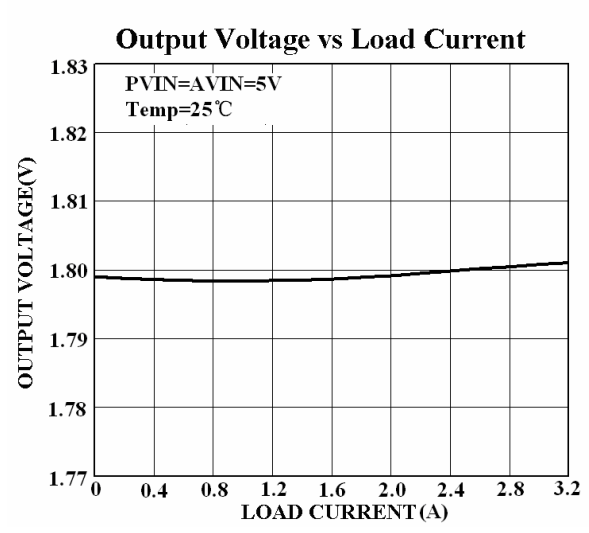
Typical Operating Characteristics

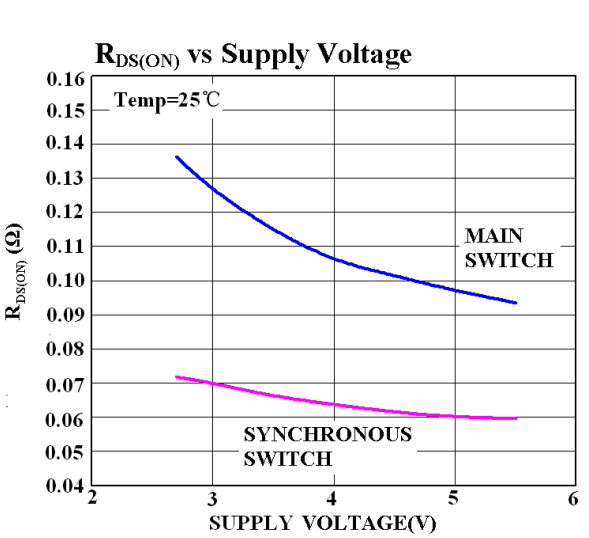
Unless otherwise specified: C_{IN}=10µF, C_{OUT}=22µF, L=2.2µH, T_A=25°C.

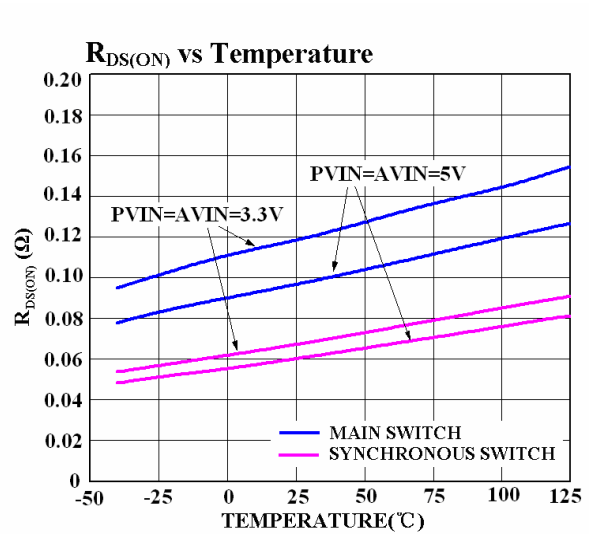




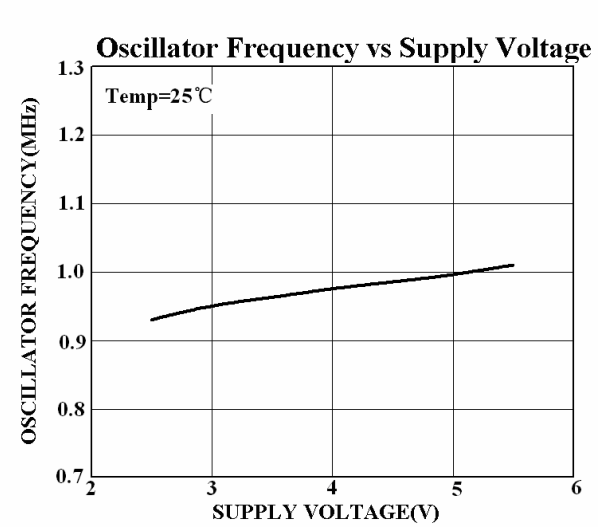


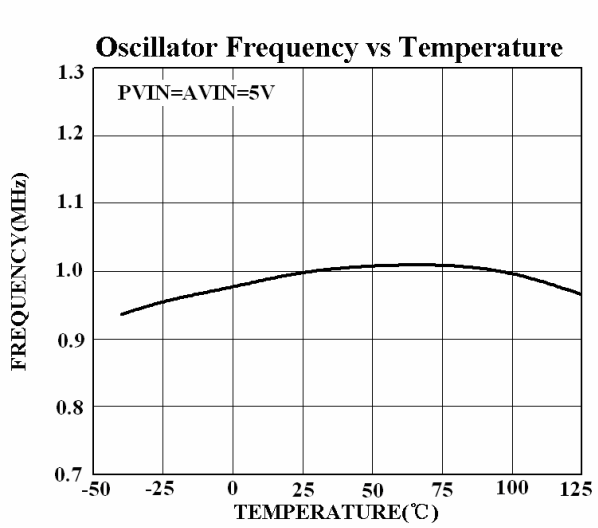


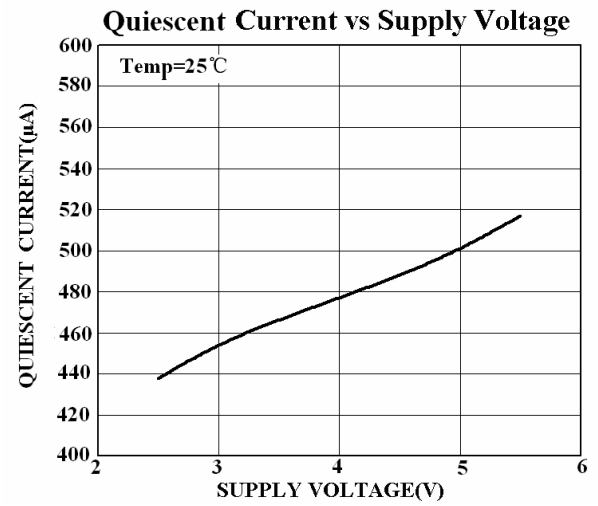


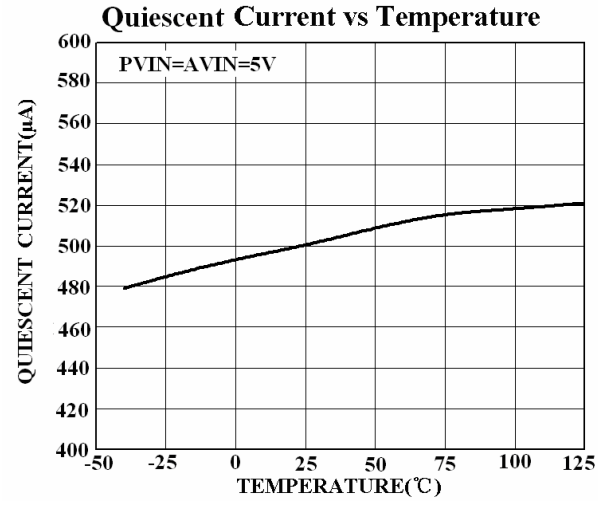


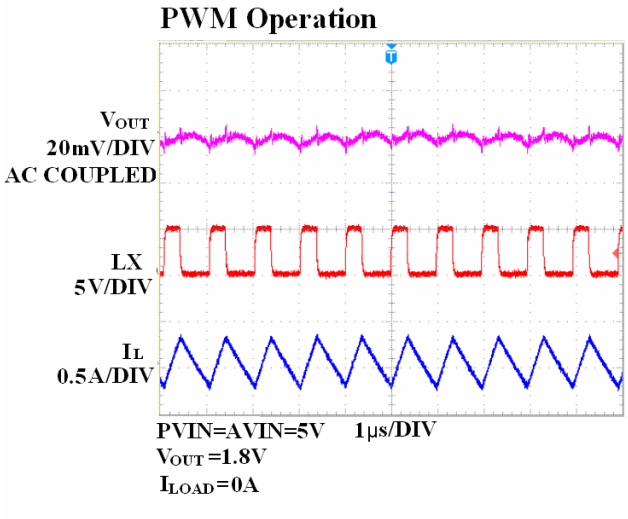
Typical Operating Characteristics (continued)

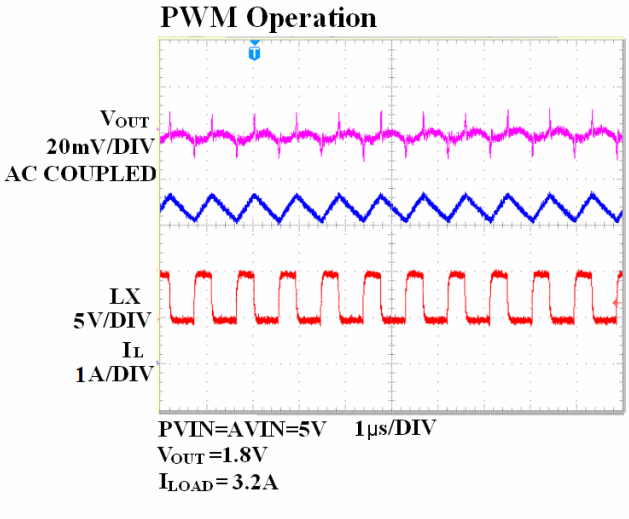






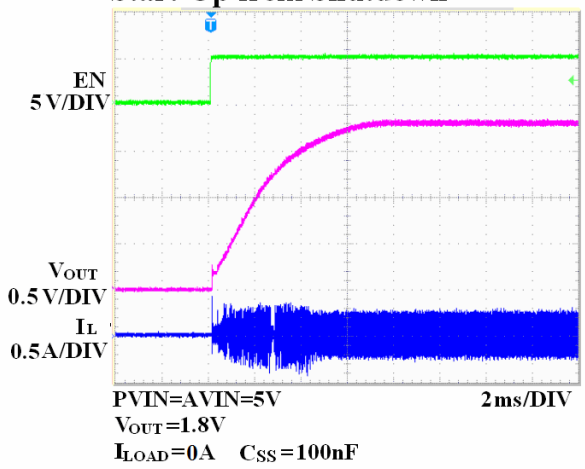




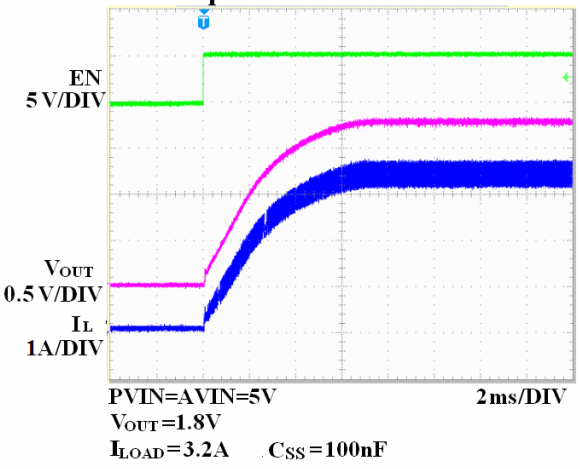


Typical Operating Characteristics (continued)

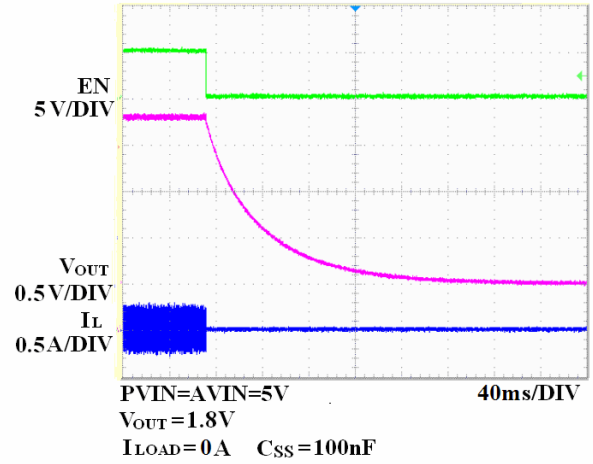
Start-Up from Shutdown



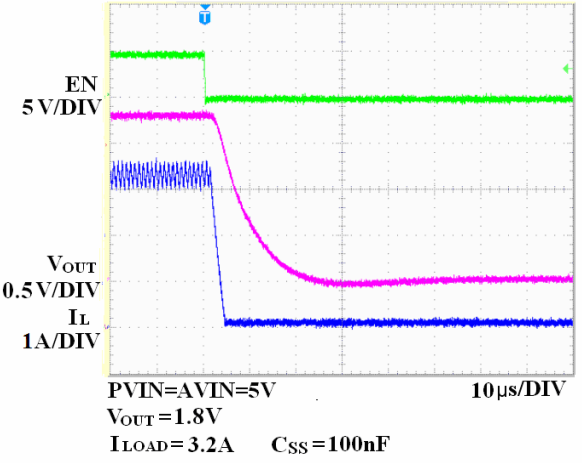
Start-Up from Shutdown



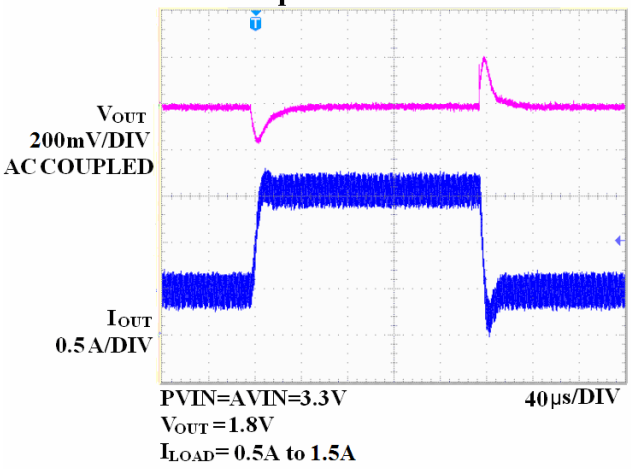
Power Down



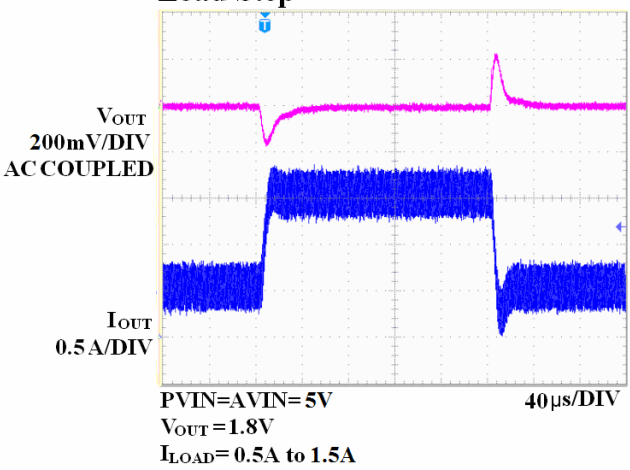
Power Down



Load Step



Load Step



Application Information

The EUP3423 uses a slope-compensated constant frequency, current mode architecture. Both the main (P-Channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. During normal operation, the EUP3423 regulates output voltage by switching at a constant frequency and then modulating the power transferred to the load each cycle using PWM comparator. The duty cycle is controlled by three weighted differential signals: the output of error amplifier, the main switch sense voltage and the slope-compensation ramp. It modulates output power by adjusting the inductor-peak current during the first half of each cycle. An N-channel, synchronous switch turns on during the second half of each cycle.

Soft-Start

The EUP3423 has an SS pin for soft-start that limits the inrush current and output voltage overshoot during startup. The soft-start time can be adjusted by changing the capacitor connected between SS and GND.

Overload Lockout

When startup is finished, if the output is less than 54% of the setting output voltage, EUP3423 would stop switching and operates under lockout state. It protects the IC during overload or short circuit condition. Shutdown the converter by EN pin or remove the supply will reset the lockout condition.

Input Undervoltage Lockout

The undervoltage lockout circuit prevents device misoperation at low input voltages. It prevents the converter from turning on the main and synchronous switches under undervoltage state.

Inductor Selection

The EUP3423 typically uses a 2.2µH output inductor. The output inductor is selected to limit the ripple current to some predetermined value, typically 20%~40% of the full load current at the maximum input voltage. Large value inductors lower ripple currents. Higher V_{IN} or V_{OUT} influence the ripple current as shown in equation.

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation.
The DC-resistance of the inductor directly influences the efficiency of the converter. Therefore for better efficiency, choose a low DC-resistance inductor.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. The primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the EUP3423. A low ESR input capacitor sized for the maximum RMS current must be used. The size required will vary depending on the load, output voltage and input voltage source impedance characteristics. A typical C_{IN} value is around 10µF. If the wire of supply is too long, 22µF input capacitor should be used.
The input capacitor RMS current varies with the input voltage and the output voltage. The equation for the maximum RMS current in the input capacitor is:

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1-\frac{V_{OUT}}{V_{IN}}\right)}$$

The output capacitor C_{OUT} has a strong effect on loop stability.
The selection of C_{OUT} is driven by the required effective series resistance (ESR).
ESR is a direct function of the volume of the capacitor; that is, physically larger capacitors have lower ESR. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L\left(ESR+\frac{1}{8fC_{OUT}}\right)$$

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$R_{FB2} = R_{FB1}\left(\frac{0.8}{V_{OUT}-0.8}\right)$$

The external resistive divider is connected to the output, allowing remote voltage sensing as shown below.

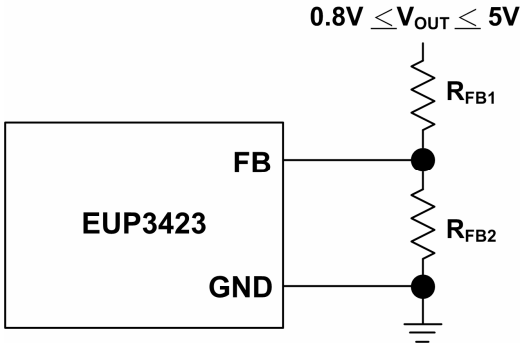


Table1. Recommended Components with PVIN=AVIN=5V

V_{OUT} (V)	C_{IN} (µF)*	C_{OUT} (µF)	L (µH)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	C_{FB} (pF)
3.3	10	22	2.2	200	64	None
1.8	10	22	2.2	200	160	None
1.2	10	22	2.2	200	400	10
1	10	22	2.2	200	800	10

*If the wire of supply is too long, 22µF should be used for C_{IN}.

Thermal Considerations

To avoid the EUP3423 from exceeding the maximum junction temperature, the user will need to do a thermal analysis. The goal of the thermal analysis is to determine whether the operating conditions exceed the maximum junction temperature of the part. The temperature rise is given by:

$$T_R=(P_D)(\theta_{JA})$$

Where $P_D=I_{LOAD}^2 \times R_{DS(ON)}$ is the power dissipated by the regulator ; θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.
The junction temperature, T_J, is given by:

$$T_J=T_A+T_R$$

Where T_A is the ambient temperature.
T_J should be below the maximum junction temperature of 125°C.

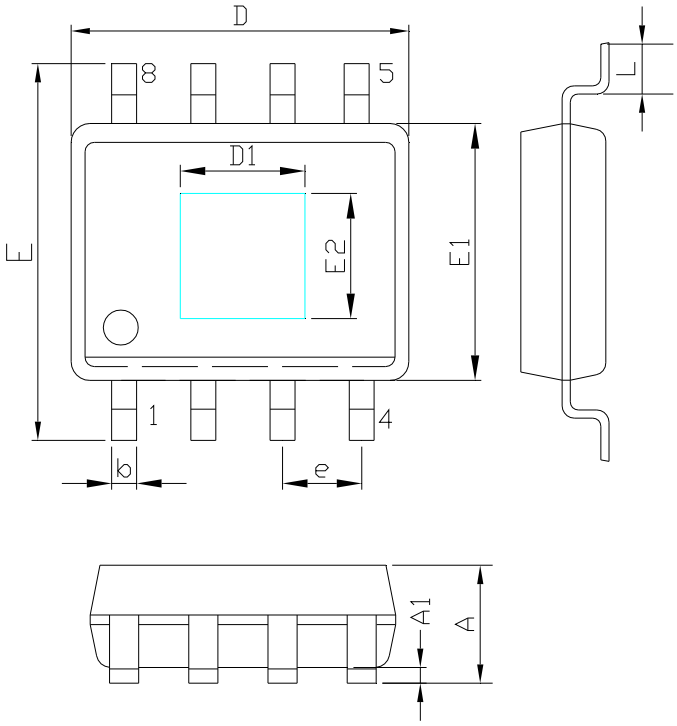
PC Board Layout Checklist

For all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show stability problems as well as EMI problems.
When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the EUP3423.

1. The input capacitor C_{IN} should connect to VIN as closely as possible. This capacitor provides the AC current to the internal power MOSFETs.
2. The power traces, consisting of the GND trace, the LX trace and the VIN trace should be kept short, direct and wide.
3. The FB pin should connect directly to the feedback resistors. The resistive divider R_{FB1}/R_{FB2} must be connected between the C_{OUT} and ground.
4. Keep the switching node, LX, away from the sensitive FB node.

Packaging Information

SOP-8 (EP)



Remark: Exposed pad outline drawing is for reference only.

SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	1.35	-	1.75	0.053	-	0.069
A1	0.00	-	0.25	0.000	-	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	3.70	3.90	4.00	0.146	0.154	0.157
D1	2.67	2.97	3.50	0.105	0.117	0.138
E2	1.78	2.18	2.60	0.070	0.086	0.102
E	5.80	6.00	6.20	0.228	0.236	0.244
L	0.40	-	1.27	0.016	-	0.050
b	0.31	-	0.51	0.012	-	0.020
e	1.27			0.050		