



# 5A, 1MHz Synchronous Step-Down Converter

## DESCRIPTION

The EUP3425 is a 1MHz fixed frequency synchronous, current-mode, step-down dc-dc converter capable of providing up to 5A output current. The EUP3425 operates from an input range of 2.7V to 5.5V and provides a regulated output voltage from 0.8V to 5V. The internal synchronous power switch increases efficiency and eliminates the need for an external Schottky diode. The EUP3425 can be externally set for either forced PWM continuous mode or pulse skipping mode. Forced PWM operation provides very low output ripple voltage for noise sensitive applications while pulse skipping operation improves light load efficiency by reducing switching loss.

The EUP3425 features short circuit and thermal protection circuits to increase system reliability. Externally adjustable soft-start SS pin allows for proper power on sequencing with respect to other power supplies and avoids input inrush current during startup. The EUP3425 is available in a low profile 14pin 3mm×4mm TDFN package .

## FEATURES

- 2.7V to 5.5V Input Voltage Range
- High Efficiency up to 96%
- 5A Available Load Current
- 35mΩ Integrated FET Switches
- 1MHz Switching Frequency
- 100% Duty Cycle Low Dropout Operation
- Short Circuit and Thermal Protection
- Integrated UVLO and Power Good
- Excellent Line and Load Transient Response
- Adjustable Soft-start with An External Capacitor
- Adjustable Output Voltage Down to 0.8V
- Available in 14pin 3mm×4mm TDFN Package
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

## APPLICATIONS

- Distributed 3.3V and 5V Power Supplies
- High Performance DSPs, FPGAs, ASICs and Microprocessors
- Base Station, Telecom, and Networking Equipment Power Supplies
- EPC and NetPCs

## Typical Application Circuit

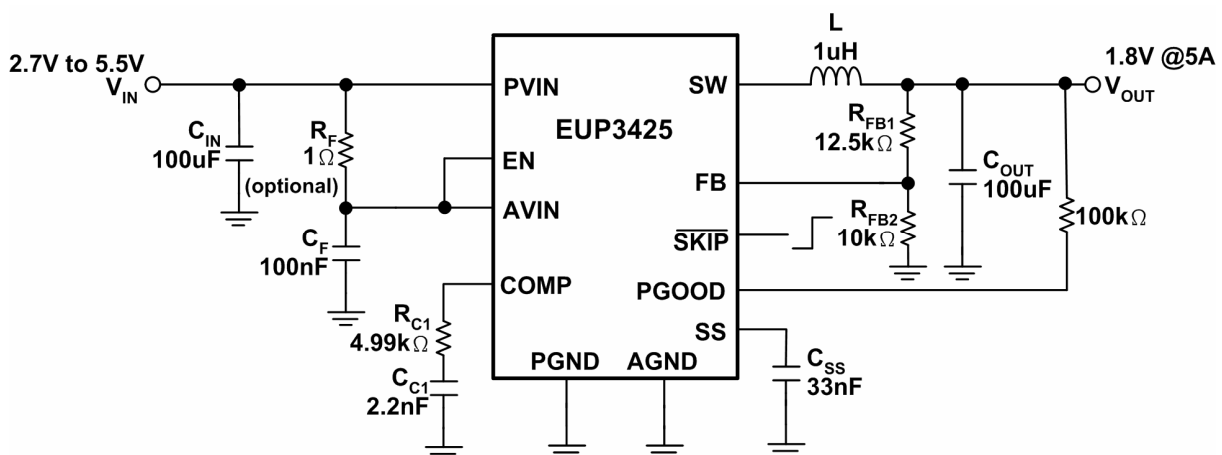


Figure1. Adjustable Output Regulator

Typical Application Circuit (continued)

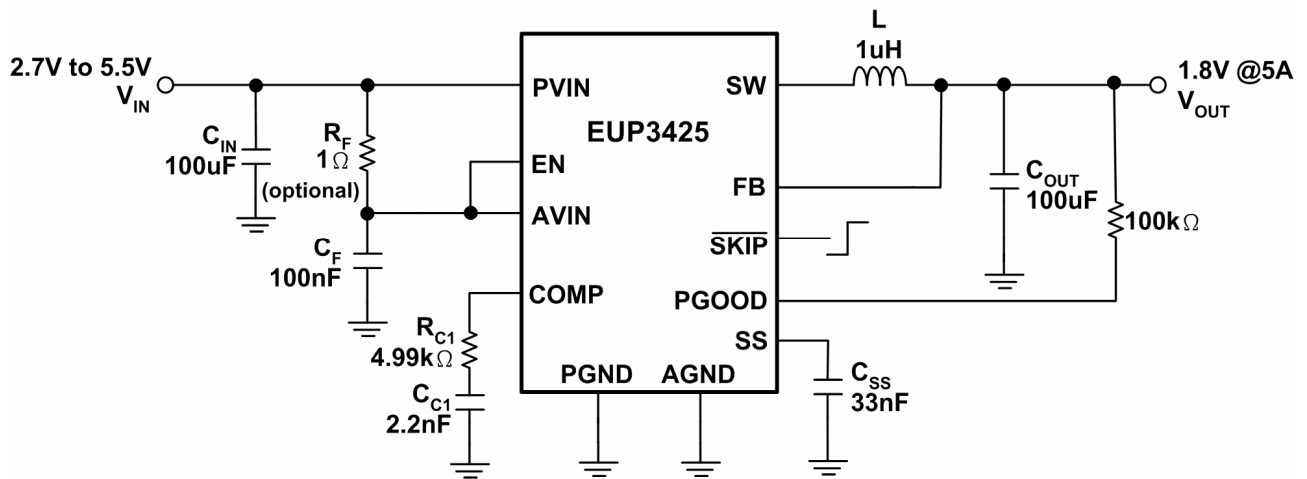


Figure2. Fixed Output Regulator

Block Diagram

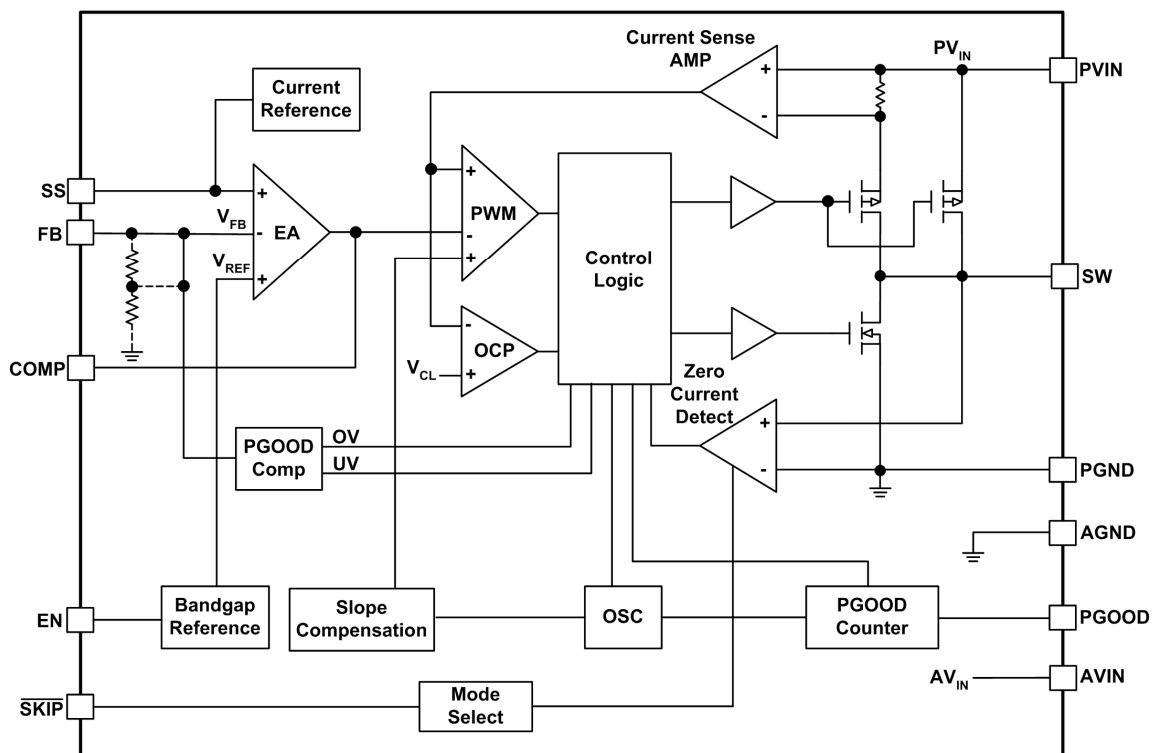


Figure3. Block Diagram

## Pin Configurations

Package Type	Pin Configurations
TDFN-14	<p>(TOP VIEW)</p> <p> SS 1 14 AGND  FB 2 13 AVIN  PGOOD 3 12 <math>\overline{\text{SKIP}}</math>  COMP 4 Thermal Pad 11 EN  PVIN 5 10 PGND  PVIN 6 9 PGND  SW 7 8 SW </p>

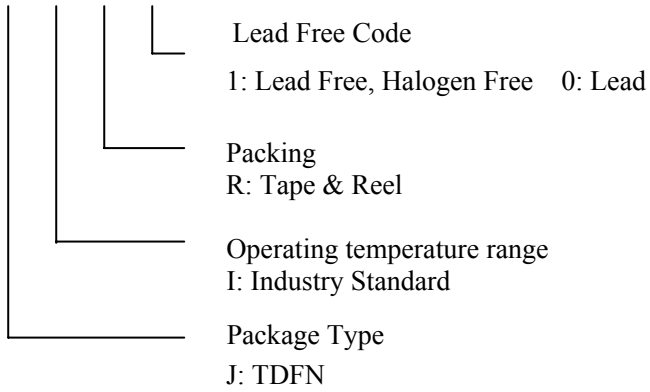
## Pin Description

PIN	TDFN-14	DESCRIPTION
SS	1	Soft-start pin. An internal 5 $\mu$ A pull up current source charges an external capacitor to set the soft-start ramp rate. SS is discharged to GND in shutdown.
FB	2	Feedback pin. Connect it to an external resistor divider for adjustable output version; and connect it directly to the output for fixed output version.
PGOOD	3	Power good output signal. Logic high when regulator output is within $\pm 10\%$ of target output voltage.
COMP	4	Loop compensation pin.
PVIN	5	Input voltage to the power switches.
SW	7, 8	Switch node connection to inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
PGND	9, 10	Power ground.
EN	11	Chip enable pin. Forcing this pin above 1.5V enables the part. Forcing this pin below 0.3V shuts down the device. Do not leave EN floating.
$\overline{\text{SKIP}}$	12	Operation Mode Select Input. Logic Low selects pulse skipping mode, and logic high chooses forced PWM mode. If the pin floats, an internal 5 $\mu$ A current source pull it down to GND.
AVIN	13	Analog input supply which is connected to PVIN through a low pass RC filter.
AGND	14	Analog ground.
Thermal Pad	-	The Thermal Pad is PGND, and it is connected to the PCB ground plane for electrical connection and heat dissipation.

**Ordering Information**

Order Number	Package Type	Marking	Operating Temperature Range
EUP3425JIR1	TDFN-14	XXXXX P3425	-40 °C to +85°C

EUP3425



## Absolute Maximum Ratings (1)

- Input Supply Voltage(AVIN, PVIN) ----- -0.3V to 6V
- EN, FB, SS, SKIP, COMP, PGOOD ----- -0.3V to 6V
- SW Voltages ----- -0.3V to  $V_{PVIN}+0.3V$
- Junction Temperature ----- 150°C
- Package Thermal Resistance  
TDFN-14,  $J_A$  ----- 65°C/W
- Storage Temperature ----- -65°C to 150°C
- Lead Temp (Soldering, 10sec) ----- 260°C
- Minimum ESD Rating -----  $\pm 2kV$

## Recommended Operating Conditions (2)

- Supply Voltage ----- 2.7V to 5.5V
- Operating Temperature Range ----- -40°C to 85°C

Note(1): Stress beyond those listed under “Absolute Maximum Ratings” may damage the device.

Note(2): The device is not guaranteed to function outside the recommended operating conditions.

## Electrical Characteristics

PVIN=AVIN=VEN=5V,  $T_A=+25^\circ C$ , unless otherwise specified. The ● indicates specifications which apply over the full operating range -40°C to +85°C. The EUP3425 is 100% production tested at 25°C. Typical and temperature specifications are guaranteed by design and statistical characterizations.

Symbol	Parameter	Conditions	EUP3425			Unit
			Min.	Typ.	Max.	
$V_{IN}$	Input Voltage Range	$-40^\circ C \leq T_A \leq +85^\circ C$	● 2.7		5.5	V
UVLO	Input Undervoltage Lockout	Rising $-40^\circ C \leq T_A \leq +85^\circ C$	2.25	2.45	2.65	V
UVLO_Hys	UVLO Hysteresis			200		mV
$I_{FB}$	Feedback Current	For adjustable output, $V_{FB}=0.8V$	-50	0	+50	nA
$V_{FB}$	Regulated Feedback Voltage	$T_A=+25^\circ C$	0.792	0.800	0.808	V
		$-40^\circ C \leq T_A \leq +85^\circ C$	● 0.784	0.800	0.816	
$\Delta V_{OUT}$	Output Voltage Line Regulation	$V_{IN}=3V$ to 5.5V		0.1		%/V
$V_{LOADREG}$	Output Voltage Load Regulation	$I_{LOAD}=100mA$ to 5A		0.1		%/A
$V_{PGH}$	Power Good High Trip Threshold	With Respect To $V_{FB}$	+7	+10	+13	%
$V_{PGL}$	Power Good Low Trip Threshold	With Respect To $V_{FB}$	-13	-10	-7	%
$T_{PG}$	Power Good Deglitch Time			16		Cycles
$V_{LPG}$	Power Good Low Voltage	$I_{SINK}=1mA$		0.1	0.3	V
$I_{PG}$	Power Good Leakage Current	High Impedance, Focre VPGOOD=5V			1	$\mu A$
$V_{EN}$	EN Threshold	$-40^\circ C \leq T_A \leq +85^\circ C$	● 0.3	1.0	1.5	V
$I_{EN}$	EN Input Bias Current		-1		+1	$\mu A$
$I_Q$	Quiescent Current	$V_{FB}=0.75V$ or $V_{OUT}=90\%$ , $V_{SKIP}=5V$ , $-40^\circ C \leq T_A \leq +85^\circ C$	●	0.5	0.6	mA
		$V_{FB}=0.75V$ or $V_{OUT}=90\%$ , $V_{SKIP}=0V$ , $-40^\circ C \leq T_A \leq +85^\circ C$	●	0.5	0.6	mA
$I_{SHDN}$	Shutdown Current	$V_{EN}=0V$			5	$\mu A$
$V_{SKIP}$	SKIP Threshold	$-40^\circ C \leq T_A \leq +85^\circ C$	● 0.3	1.0	1.5	V
$I_{SKIP}$	SKIP Pull Down Current		2	5	8	$\mu A$
$I_{SS}$	Soft Start Pull Up Current	$V_{SS}=0V$	3	5	7	$\mu A$

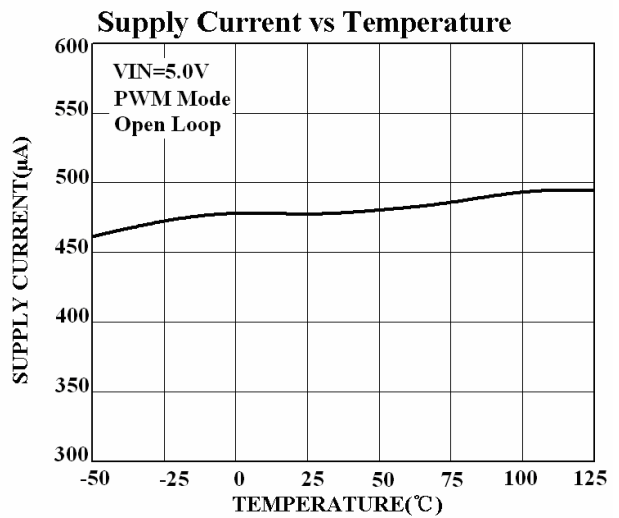
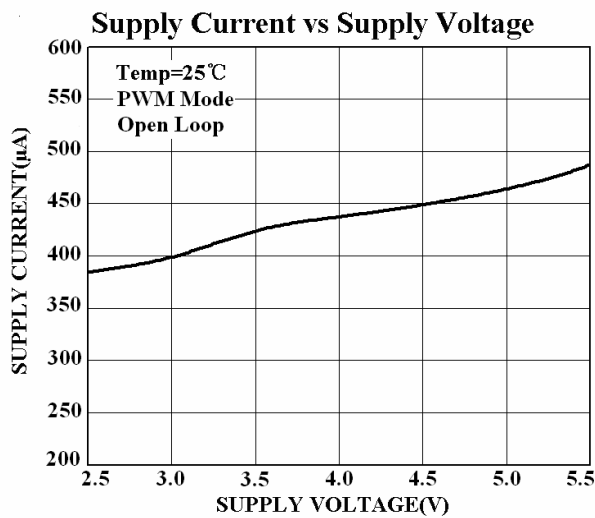
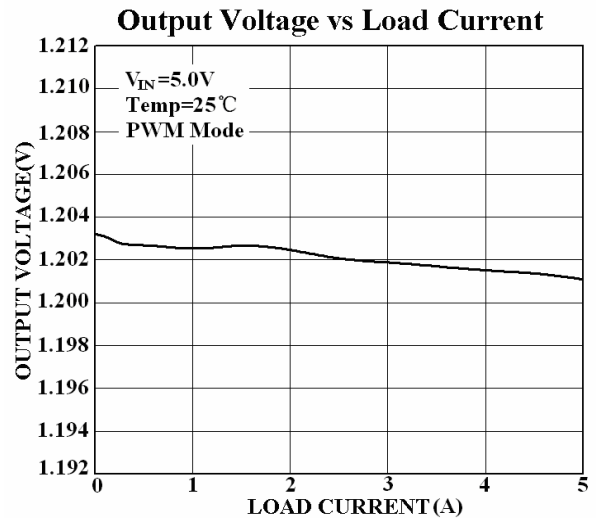
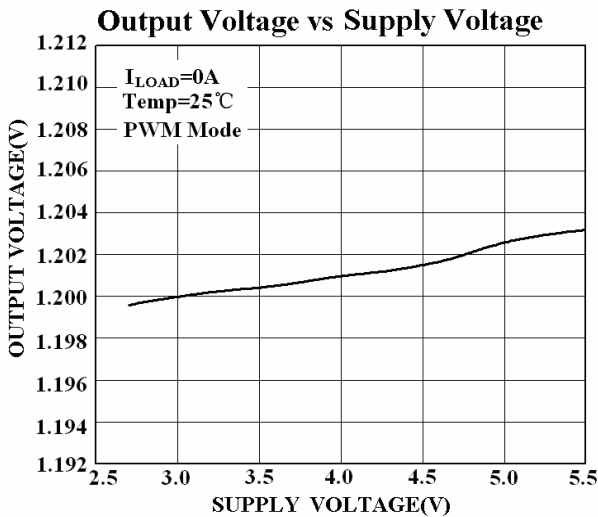
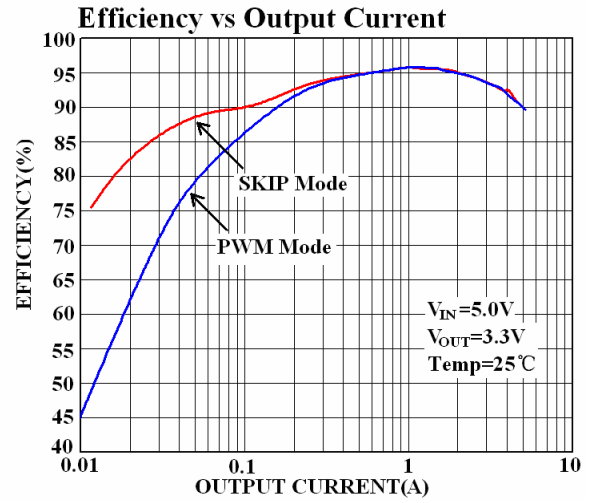
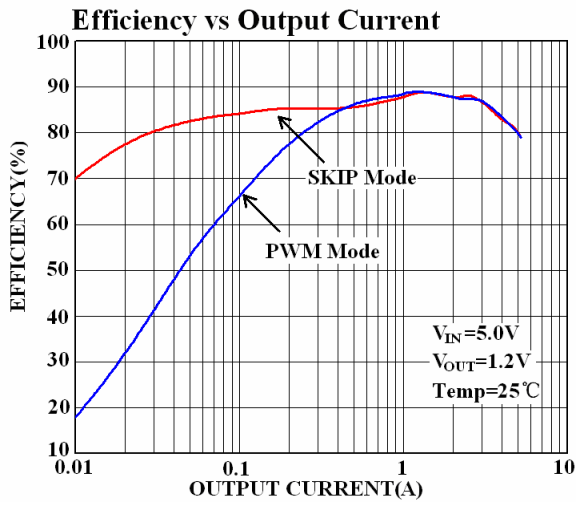
**Electrical Characteristics (continued)**

PVIN=AVIN=VEN=5V, T<sub>A</sub>=+25°C, unless otherwise specified. The ● indicates specifications which apply over the full operating range -40°C to +85°C. The EUP3425 is 100% production tested at 25°C. Typical and temperature specifications are guaranteed by design and statistical characterizations.

Symbol	Parameter	Conditions	EUP3425			Unit	
			Min.	Typ.	Max.		
V <sub>SSC</sub>	SS to FB Clamp Voltage	V <sub>SS</sub> -V <sub>FB</sub> , FB=0V		70		mV	
f <sub>OSC</sub>	Oscillator Frequency	SKIP=0V, V <sub>FB</sub> =0.75V or V <sub>OUT</sub> =90% -40°C≤T <sub>A</sub> ≤+85°C	●	0.8	1	1.2	MHz
D <sub>MAX</sub>	Maximum Duty Cycle			100		%	
T <sub>ONMIN</sub>	Minimum On Time			100		ns	
I <sub>PEAK</sub>	Hside PCH Switch Peak Current	V <sub>FB</sub> =0.75V or V <sub>OUT</sub> =90%		6	8	A	
I <sub>NEG</sub>	Lside NCH Negative Current Limit	SKIP=AVIN, PWM Mode			-2	A	
I <sub>ZX</sub>	Lside NCH Reverse Current Limit	SKIP=0V, Pulse Skipping Mode			0.2	A	
I <sub>LSW</sub>	SW Leakage Current	V <sub>EN</sub> =0V, V <sub>SW</sub> =0 or 5V		-5		+5	μA
R <sub>PFET</sub>	R <sub>DS(ON)</sub> of P-Channel FET	I <sub>SW</sub> =3A			46	60	mΩ
R <sub>NFET</sub>	R <sub>DS(ON)</sub> of N-Channel FET	I <sub>SW</sub> =3A			35	50	mΩ
G <sub>EA</sub>	Error Amplifier Transconductance	I <sub>COMP</sub> = ±50uA			600		μA/V
A <sub>EA</sub>	Error Amplifier Voltage Gain				2000		V/V
I <sub>COMP_SRC</sub>	COMP Maximum Source Current	V <sub>FB</sub> =0.6V, V <sub>COMP</sub> =1V		80	100		μA
I <sub>COMP_SNK</sub>	COMP Maximum Sink Current	V <sub>FB</sub> =1.0V, V <sub>COMP</sub> =1V		80	100		μA
T <sub>SD</sub>	Thermal Shutdown				160		°C
T <sub>SD-Hys</sub>	Thermal Shutdown Hysteresis				20		°C

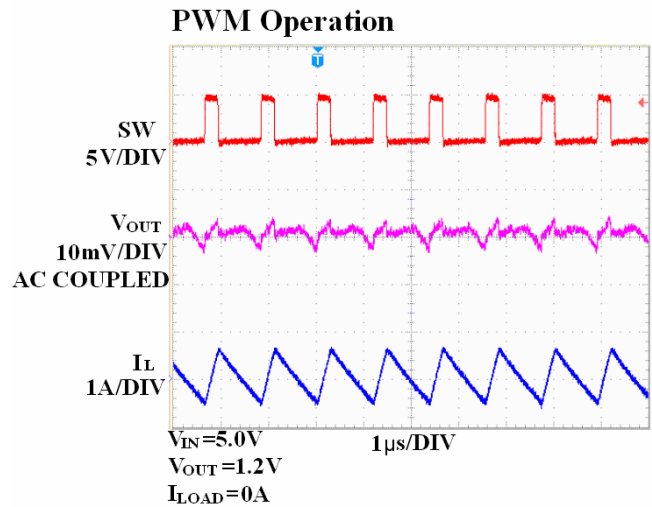
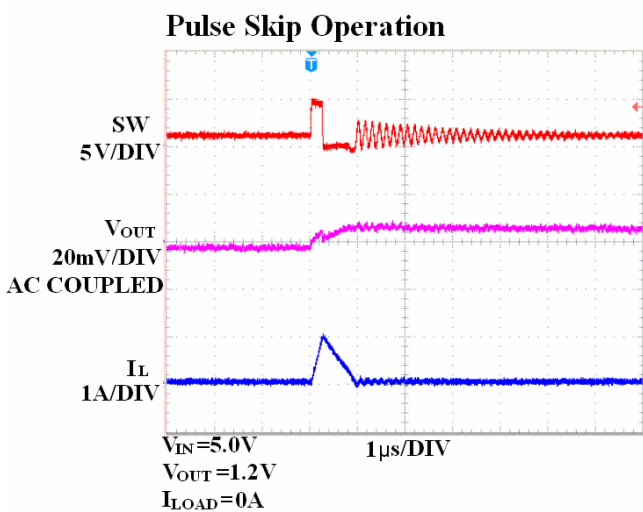
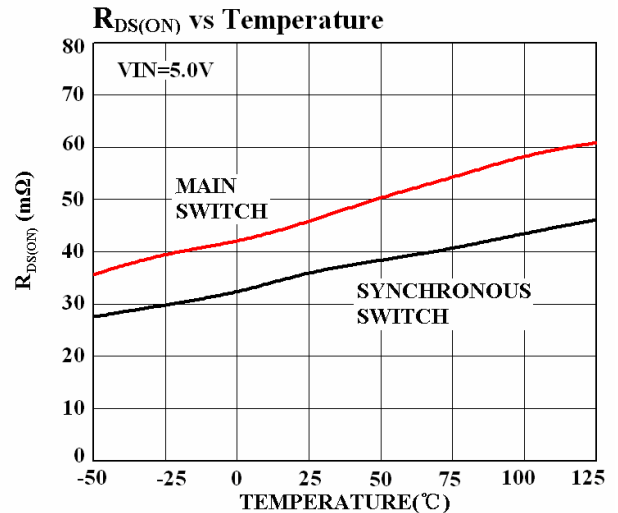
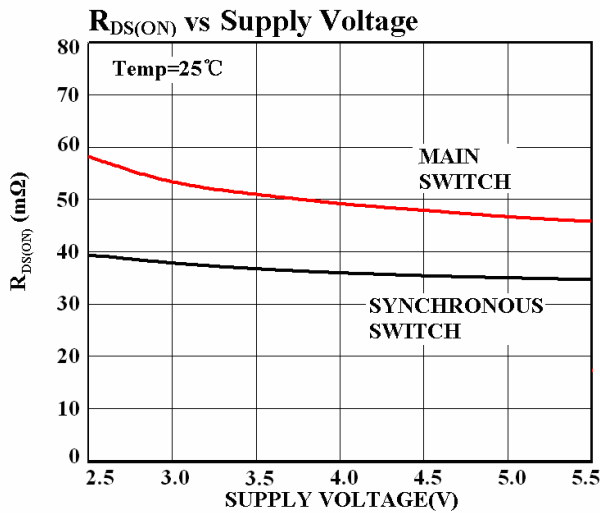
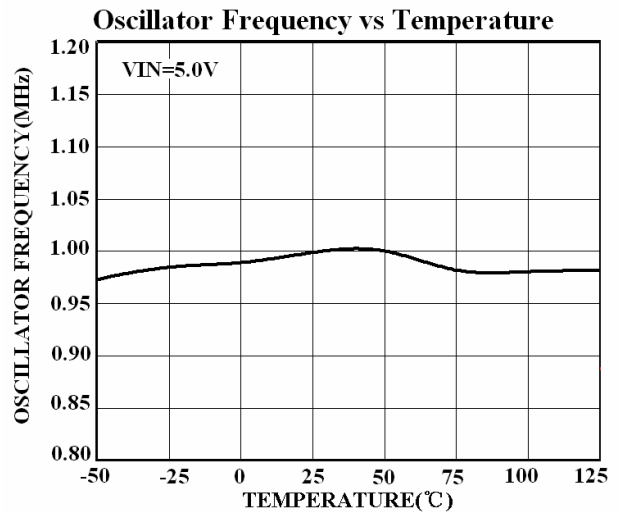
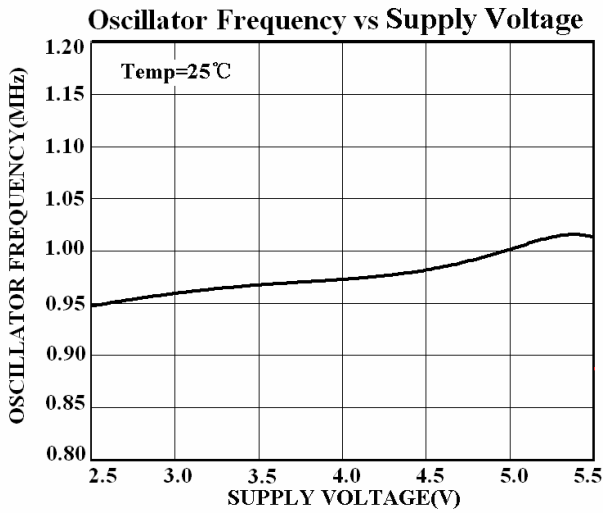
**Typical Operating Characteristics**

Unless otherwise specified:  $C_{IN}=C_{OUT}=100\mu F$ ,  $L=1\mu H$ ,  $V_{IN}=5V$ ,  $V_{OUT}=1.2V$ ,  $T_A=25^\circ C$ .



**Typical Operating Characteristics (continued)**

Unless otherwise specified:  $C_{IN}=C_{OUT}=100\mu F$ ,  $L=1\mu H$ ,  $V_{IN}=5V$ ,  $V_{OUT}=1.2V$ ,  $T_A=25^\circ C$ .

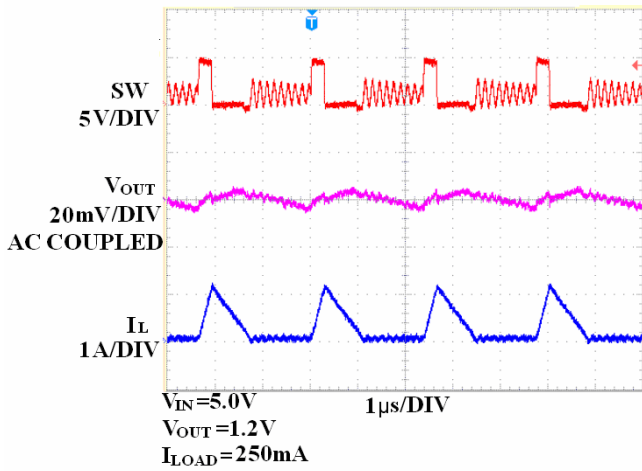




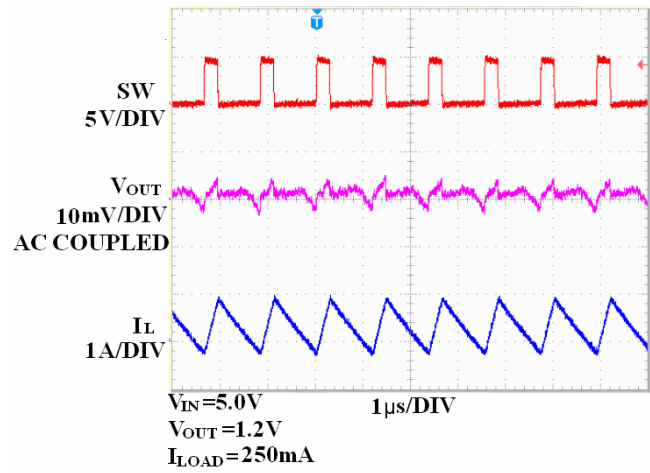
**Typical Operating Characteristics (continued)**

Unless otherwise specified:  $C_{IN}=C_{OUT}=100\mu F$ ,  $L=1\mu H$ ,  $V_{IN}=5V$ ,  $V_{OUT}=1.2V$ ,  $T_A=25^\circ C$ .

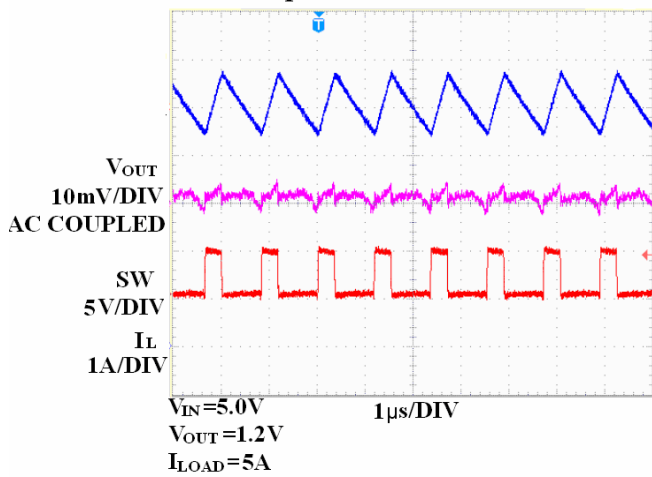
**Pulse Skip Operation**



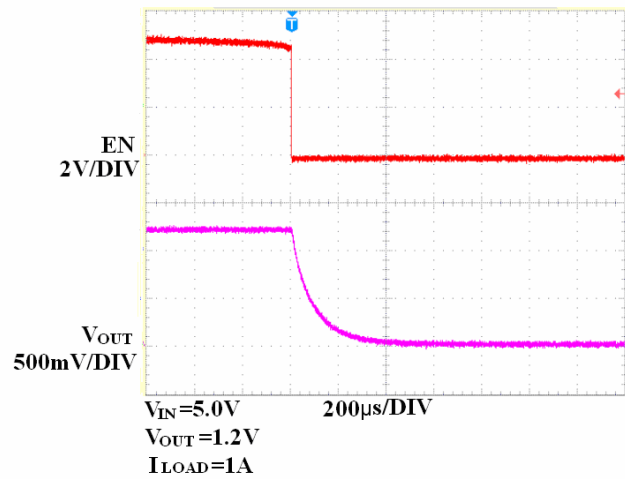
**PWM Operation**



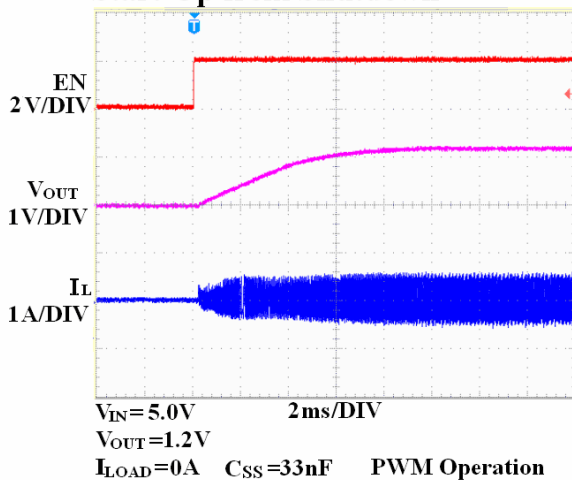
**PWM Operation**



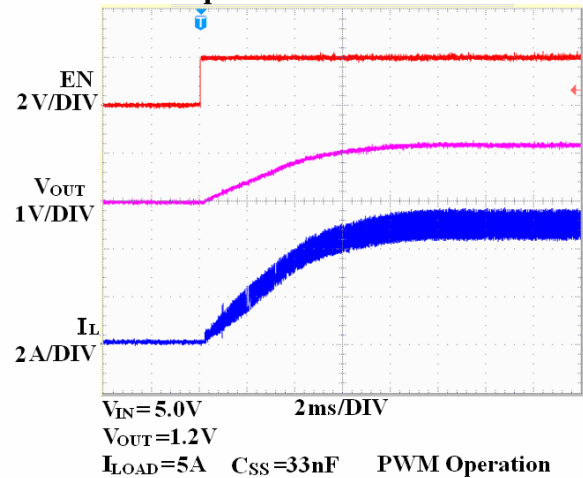
**Power Down**



**Start-Up from Shutdown**



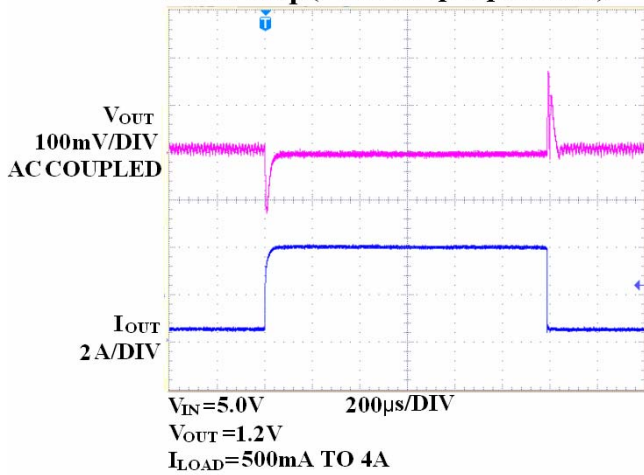
**Start-Up from Shutdown**



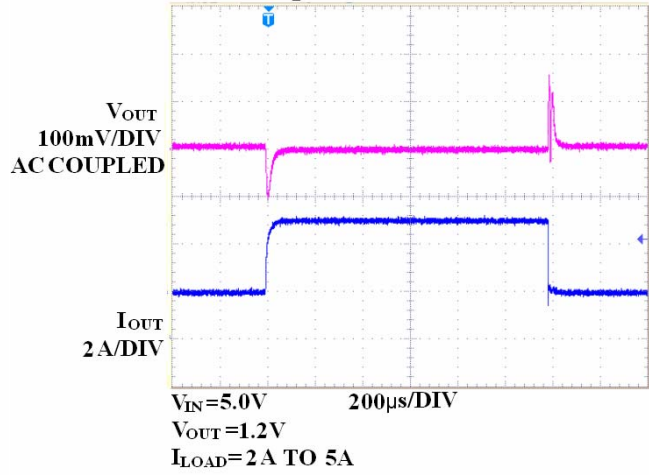
**Typical Operating Characteristics (continued)**

Unless otherwise specified:  $C_{IN}=C_{OUT}=100\mu\text{F}$ ,  $L=1\mu\text{H}$ ,  $V_{IN}=5\text{V}$ ,  $V_{OUT}=1.2\text{V}$ ,  $T_A=25^\circ\text{C}$ .

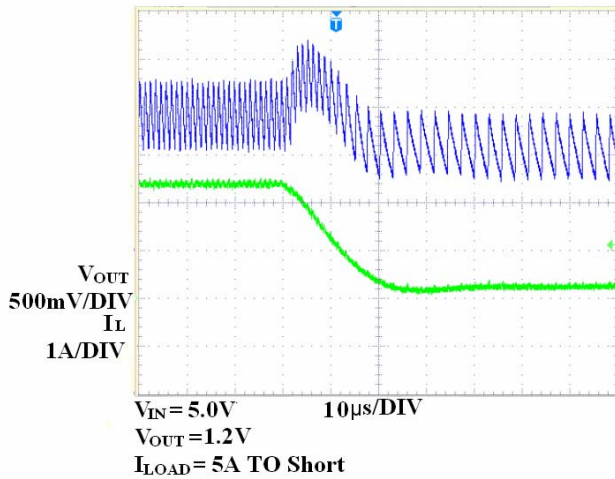
**Load Step(Pulse Skip Operation)**



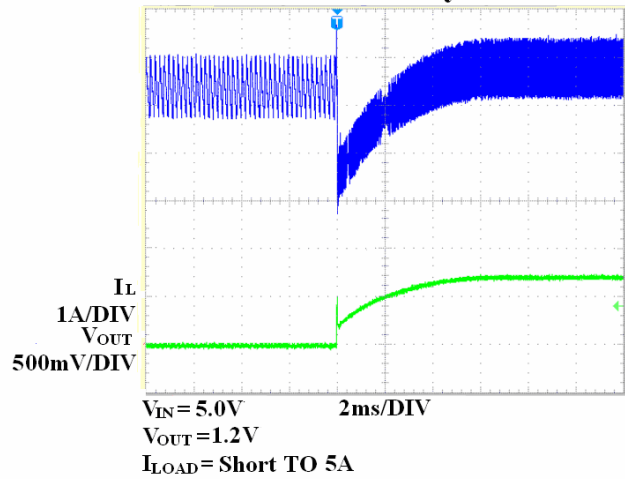
**Load Step**



**Short Circuit Test**



**Short Circuit Recovery**



## Application Information

The EUP3425 uses a slope-compensated constant frequency, current mode architecture. Both the main (P-Channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. During normal operation, the EUP3425 regulates output voltage by switching at a constant frequency and then modulating the power transferred to the load each cycle using PWM comparator. The duty cycle is controlled by three weighted differential signals: the output of error amplifier, the main switch sense voltage and the slope-compensation ramp. It modulates output power by adjusting the inductor-peak current during the first half of each cycle. An N-channel, synchronous switch turns on during the second half of each cycle (off time). When the inductor current starts to reverse in pulse skipping mode operation or when the PWM reaches the end of the oscillator period in forced PWM operation, the synchronous switch turns off.

### Soft-Start

The EUP3425 has an SS pin for soft-start that limits the inrush current and output voltage overshoot during startup. The soft-start time can be adjusted by changing the capacitor connected between SS and AGND.

### Short-Circuit Protection

As soon as the output voltage drops below 50% of the nominal output voltage, the converter switching frequency as well as the current limit is reduced.

### Output Overvoltage Protection

The output voltage is monitored by a comparator through FB pin. It guards against transient overshoots >10% by turning the main switch off.

### Input Undervoltage Lockout

The undervoltage lockout circuit prevents device misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET with undefined conditions.

### Inductor Selection

The EUP3425 typically uses a 1μH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions.

The output inductor is selected to limit the ripple current to some predetermined value, typically 20%~40% of the full load current at the maximum input voltage. Large value inductors lower ripple currents. Higher  $V_{IN}$  or  $V_{OUT}$  also increases the ripple current as shown in equation.

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation.

The DC-resistance of the inductor directly influences the efficiency of the converter. Therefore for better efficiency, choose a low DC-resistance inductor.

### $C_{IN}$ and $C_{OUT}$ Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle  $V_{OUT}/V_{IN}$ . The primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the EUP3425. A low ESR input capacitor sized for the maximum RMS current must be used. The size required will vary depending on the load, output voltage and input voltage source impedance characteristics. A typical value is around 100μF.

The input capacitor RMS current varies with the input voltage and the output voltage. The equation for the maximum RMS current in the input capacitor is:

$$I_{RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}} \times \left( 1 - \frac{V_O}{V_{IN}} \right)}$$

The output capacitor  $C_{OUT}$  has a strong effect on loop stability.

The selection of  $C_{OUT}$  is driven by the required effective series resistance (ESR).

ESR is a direct function of the volume of the capacitor; that is, physically larger capacitors have lower ESR. Once the ESR requirement for  $C_{OUT}$  has been met, the RMS current rating generally far exceeds the  $I_{RIPPLE(P-P)}$  requirement. The output ripple  $\Delta V_{OUT}$  is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left( ESR + \frac{1}{8fC_{OUT}} \right)$$

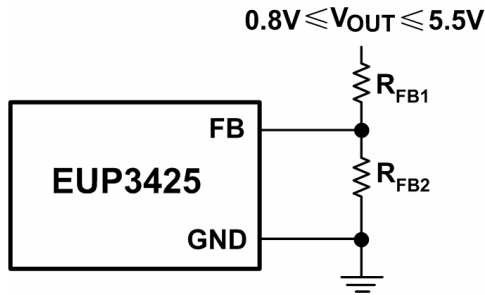
When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

### Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} \cong 0.8 \left( 1 + \frac{R_{FB1}}{R_{FB2}} \right)$$

For adjustable voltage package, the external resistive divider is connected to the output, allowing remote voltage sensing as shown below.



### Thermal Considerations

To avoid the EUP3425 from exceeding the maximum junction temperature, the user will need to do a thermal analysis. The goal of the thermal analysis is to determine whether the operating conditions exceed the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = (P_D)(\theta_{JA})$$

Where  $P_D = I_{LOAD}^2 \times R_{DS(ON)}$  is the power dissipated by the regulator ;  $\theta_{JA}$  is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature,  $T_J$ , is given by:

$$T_J = T_A + T_R$$

Where  $T_A$  is the ambient temperature.

$T_J$  should be below the maximum junction temperature of 125°C.

### PC Board Layout Checklist

For all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show stability problems as well as EMI problems.

When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the EUP3425.

1. The input capacitor  $C_{IN}$  should connect to  $V_{IN}$  as closely as possible. This capacitor provides the AC current to the internal power MOSFETs.
2. The power traces, consisting of the GND trace, the SW trace and the  $V_{IN}$  trace should be kept short, direct and wide.
3. The FB pin should connect directly to the feedback resistors. The resistive divider  $R_{FB1}/R_{FB2}$  must be connected between the  $C_{OUT}$  and ground.
4. Keep the switching node, SW, away from the sensitive FB node.

### Bill of Materials( $V_{IN}=5V, V_{OUT}=1.2V, I_{OUTMAX}=5A$ )

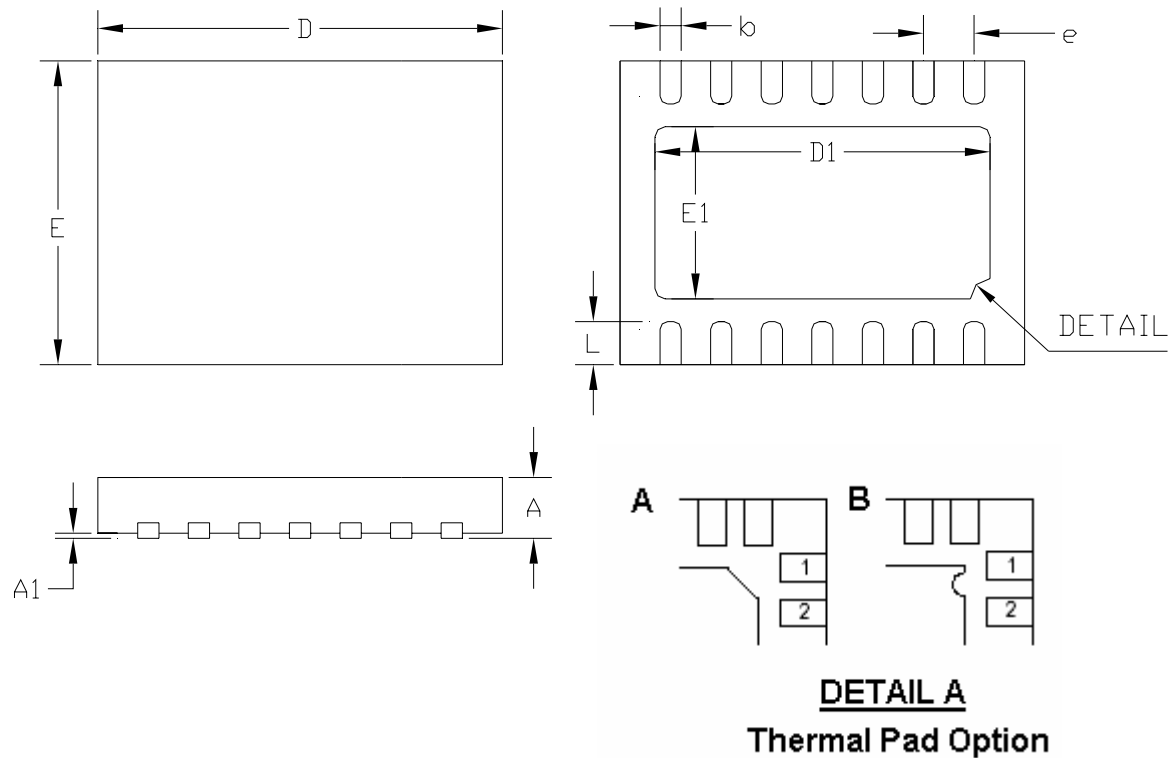
Designator	Description
$C_{IN}$	100 $\mu$ F, 1210, X5R, 6.3V
$C_{OUT}$	100 $\mu$ F, 1210, X5R, 6.3V
L	1 $\mu$ H, 6m $\Omega$
$R_F$	1 $\Omega$ , 0603
$C_F$	100nF, 0603, X7R, 16V
$R_{C1}$	4.99k $\Omega$ , 0603
$C_{C1}$	2.2nF, 0603, X7R, 25V
$C_{SS}$	33nF, 0603, X7R, 25V
$R_{FB1}$	4.99k $\Omega$ , 0603
$R_{FB2}$	10k $\Omega$ , 0603

### Bill of Materials( $V_{IN}=5V, V_{OUT}=3.3V, I_{OUTMAX}=5A$ )

Designator	Description
$C_{IN}$	100 $\mu$ F, 1210, X5R, 6.3V
$C_{OUT}$	100 $\mu$ F, 1210, X5R, 6.3V
L	1.8 $\mu$ H
$R_F$	1 $\Omega$ , 0603
$C_F$	100nF, 0603, X7R, 16V
$R_{C1}$	10k $\Omega$ , 0603
$C_{C1}$	1.8nF, 0603, X7R, 25V
$C_{SS}$	33nF, 0603, X7R, 25V
$R_{FB1}$	31.6k $\Omega$ , 0603
$R_{FB2}$	10.2k $\Omega$ , 0603

## Packaging Information

## TDFN-14



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.20	0.35	0.008	0.014
E	2.90	3.10	0.114	0.122
D	3.90	4.10	0.153	0.161
D1	3.25		0.128	
E1	1.65		0.065	
e	0.50		0.020	
L	0.30	0.50	0.012	0.020