Dual, Low-Noise, High-PSRR, 300mA LDO without Bypass Capacitor

DESCRIPTION

The EUP7230 is a dual-channel low noise, low dropout. High PSRR, high accuracy CMOS voltage regulator. Performance features include low output noise, high ripple rejection ratio, low dropout and very fast turn-on times.

The EUP7230 is also fully compatible with low ESR ceramic capacitors, reducing cost and improving output stability. This high level of output stability is maintained even during frequent load fluctuations, due to the excellent transient response performance and high PSRR achieved across a broad range of frequencies.

The EN function allows the output of each regulator to be turned off independently, resulting in greatly reduced power consumption. The EUP7230 is available in small 1.6mm×1.6mm TDFN-6 and TSOT23-6 packages.

FEATURES

- 300mA Output Current (Per LDO)
- 30μV_{RMS} Low Noise Output
- 70dB PSRR at 1KHz
- Low 50uA Quiescent Current (Both LDOs active)
- 2.5V to 5.5V Input Voltage Range
- 380mV Dropout at 300mA Load
- Dual Shutdown pins Control Each Output
- Current Limiting and Thermal Protection
- Short Circuit Protection
- Available in TDFN-6 1.6mm×1.6mm and TSOT23-6 Packages
- RoHS Compliant and 100% Lead (Pb)-Free Halogen-Free

APPLICATIONS

- Cellular Phones
- Camera, Video Recordes
- PDAs
- Hand-held Equipment

Typical Application Circuit

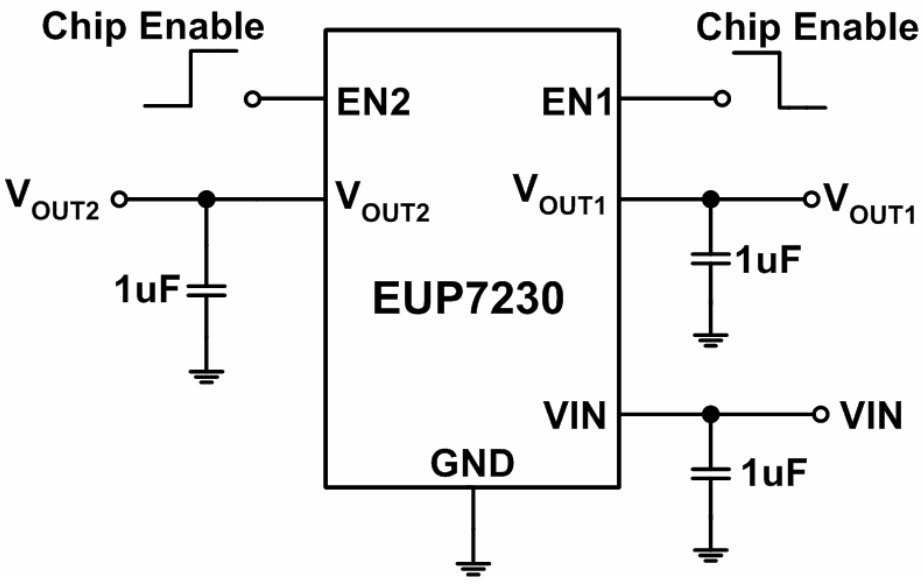


Figure 1.

Block Diagram

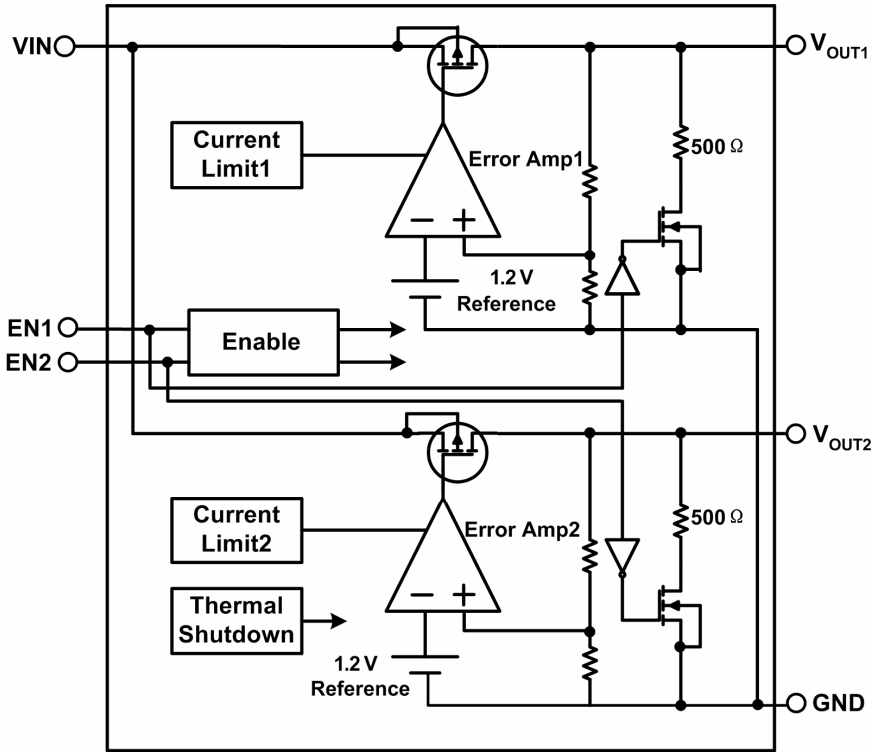
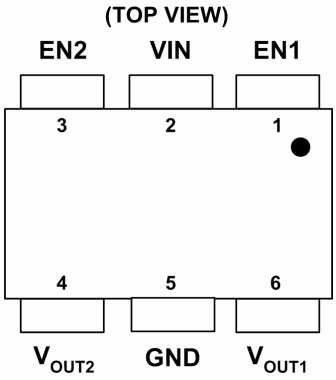
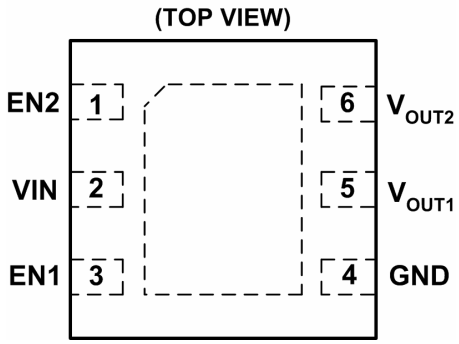


Figure 2.

Pin Configurations

Package Type	Pin Configurations	Package Type	Pin Configurations
TSOT23-6		TDFN-6	

Pin Description

PIN	TSOT23-6	TDFN-6	DESCRIPTION
EN1	1	3	Enable Input(Channel1). Active High Input. Logic High=On; Logic Low=Off; Do not leave floating.
VIN	2	2	Supply Input.
EN2	3	1	Enable Input(Channel2). Active High Input. Logic High=On; Logic Low=Off; Do not leave floating.
V_{OUT2}	4	6	Channel 2 Output Voltage.
GND	5	4	Ground.
V_{OUT1}	6	5	Channel 1 Output Voltage.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP7230-1.3/2.8OIR1	TSOT23-6	xxxxx ASBP	-40 °C to +85°C
EUP7230-1.5/2.8OIR1	TSOT23-6	xxxxx AS2C	-40 °C to +85°C
EUP7230-1.8/2.8OIR1	TSOT23-6	xxxxx AS2A	-40 °C to +85°C
EUP7230-1.8/3.3OIR1	TSOT23-6	xxxxx AS2H	-40 °C to +85°C
EUP7230-2.8/1.2OIR1	TSOT23-6	xxxxx AS2P	-40 °C to +85°C
EUP7230-2.8/3.3OIR1	TSOT23-6	xxxxx AS2L	-40 °C to +85°C
EUP7230-3.0/3.0OIR1	TSOT23-6	xxxxx AS2N	-40 °C to +85°C
EUP7230-3.0/3.3OIR1	TSOT23-6	xxxxx AS2T	-40 °C to +85°C
EUP7230-3.3/3.3OIR1	TSOT23-6	xxxxx AS2J	-40 °C to +85°C
EUP7230-1.8/2.8JIR1	TDFN-6	xxx E2A	-40 °C to +85°C
EUP7230-2.8/1.2JIR1	TDFN-6	xxx E2P	-40 °C to +85°C
EUP7230-3.3/3.3JIR1	TDFN-6	xxx E2J	-40 °C to +85°C

EUP7230-□□/□□ □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen Free 0: Lead
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  O: TSOT
  J: TDFN
- Output Voltage Option
  * EUP7230-VOUT1/VOUT2 OIRI

Absolute Maximum Ratings (1)

- Supply Input Voltage ---------- 6V
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- -65°C to +150°C
- Lead Temperature ---------- 260°C
- Thermal Resistance θ_{JA} (TSOT23-6) ---------- 200°C/W
- Thermal Resistance θ_{JA} (TDFN-6) ---------- 76°C/W
- ESD Rating
  Human Body Model ---------- ±2kV

Recommend Operating Conditions (2)

- V_{IN} ---------- 2.5V to 5.5V
- Enable Input Voltage ---------- 0V to 5.5V
- Operating Temperature Range ---------- -40°C to +85°C

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.
Note (2): The device is not guaranteed to function outside the recommended operating conditions.

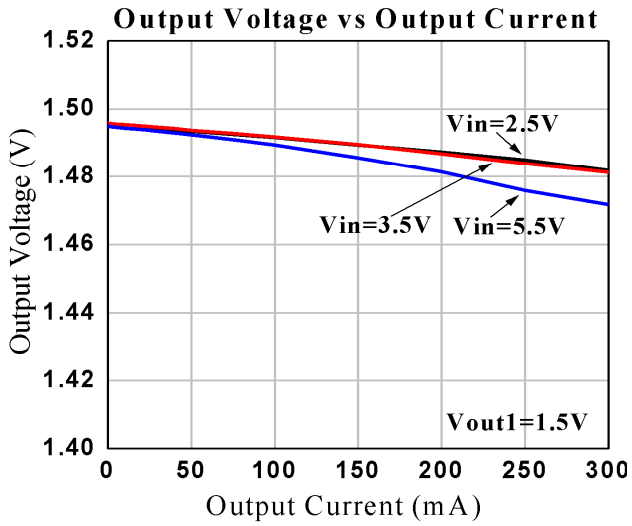
Electrical Characteristics

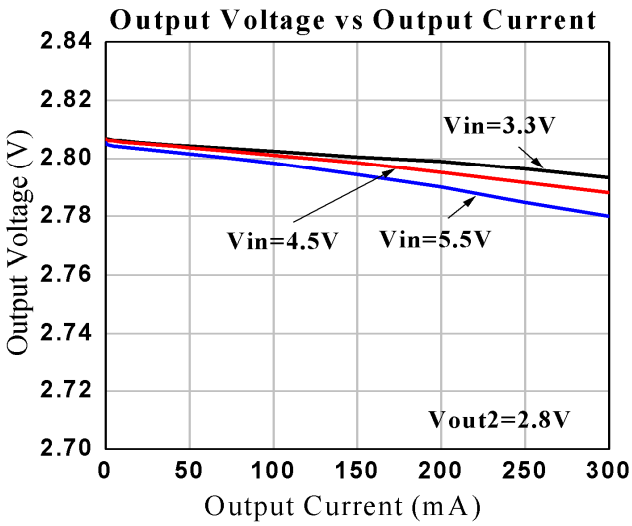
V_{IN}=(V_{OUT}+1V) or V_{IN}=2.5V whichever is greater, C_{IN}=C_{OUT}=1μF, EN1=EN2=V_{IN}, T_A=25°C. Unless otherwise noted.

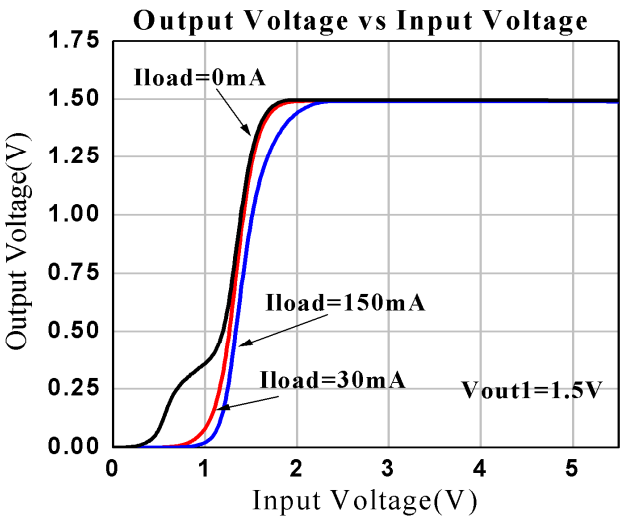
Symbol	Parameter	Conditions	EUP7230			Unit
			Min.	Typ.	Max.	
	Input Voltage		2.5		5.5	V
V_{OUT}	Output Voltage	I_{OUT}=1mA to 30mA, T_A=25°C	-2		2	%
		I_{OUT}=1mA to 30mA,T_A=-40°C～85°C	-3		3	
I_{MAX}	Maximum Output Current	Continuous,T_A=-40℃～85°C	300	550		mA
I_{LIM}	Current Limit	V_{OUT}=V_{OUT}(nom)×90%	350	600		
I_G	Quiescent Current	No Load (two channels)		50		μA
V_{DROP}	Dropout Voltage (Note 3)	I_{OUT}=300mA		380		mV
ΔV_{OUT}	Load Regulation	1mA<I_{OUT}<300mA		15	30	
ΔV_{LINE}	Line Regulation	V_{IN}=V_{OUT}+0.5V to 5.5V I_{OUT}=10mA		0.02	0.15	%/V
V_{IH}	EN Input High Threshold	V_{IN}=2.5V to 5.5V, T_A=-40°C～85°C	1.5			V
V_{IL}	EN Input Low Threshold	V_{IN}=2.5V to 5.5V, T_A=-40°C～85°C			0.4	
I_{SD}	EN Input Bias Current	EN=GND or V_{IN}			0.1	μA
I_{GSD}	Shutdown Supply Current	EN1=EN2=GND		0.1	1	
PSRR	Ripple Rejection Rate	V_{IN}=V_{OUT}+1V, I_{OUT}=10mA, f=1kHz		70		dB
		V_{IN}=V_{OUT}+1V, I_{OUT}=10mA, f=10kHz		55		
V(rms)	Output Noise Voltage (RMS)	F=10Hz~100kHz, V_{OUT}=1.5V, No Load		30		μV
TSD	Thermal Shutdown Temperature			165		°C
ΔTSD	Thermal Shutdown Hysteresis			15		

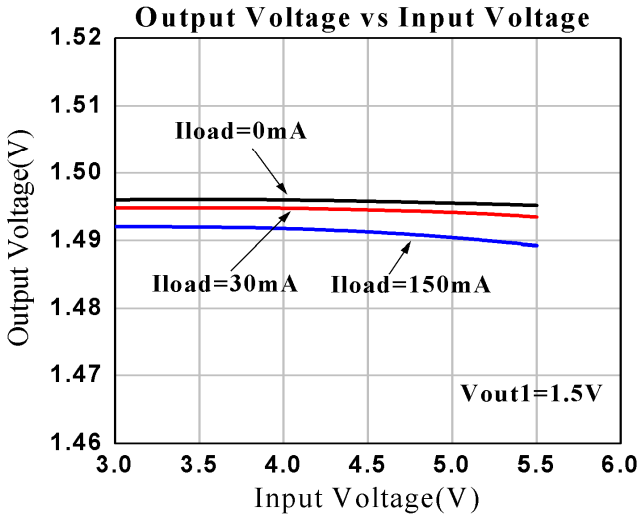
Note (3):Dropout is defined as V_{IN}-V_{OUT} when V_{OUT} is 100mV below the value of V_{OUT}.

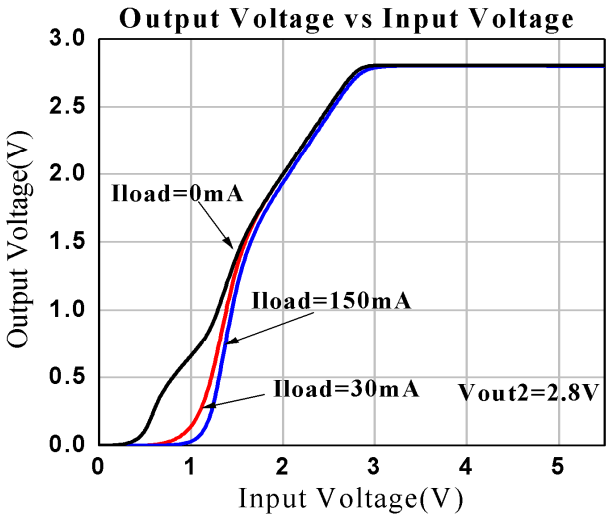
Typical Operating Characteristics

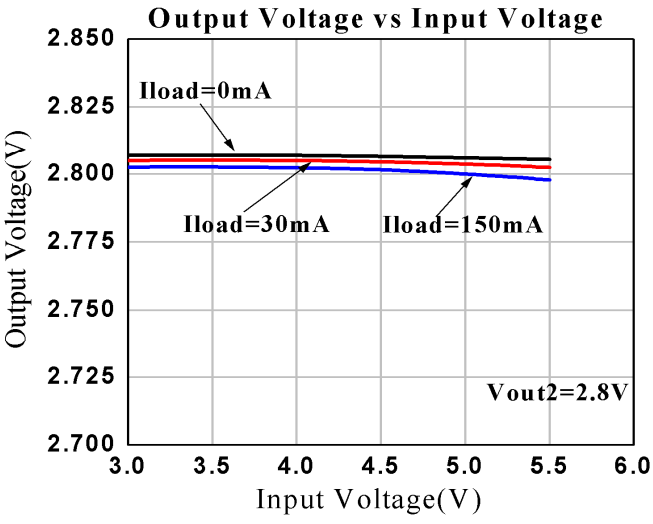




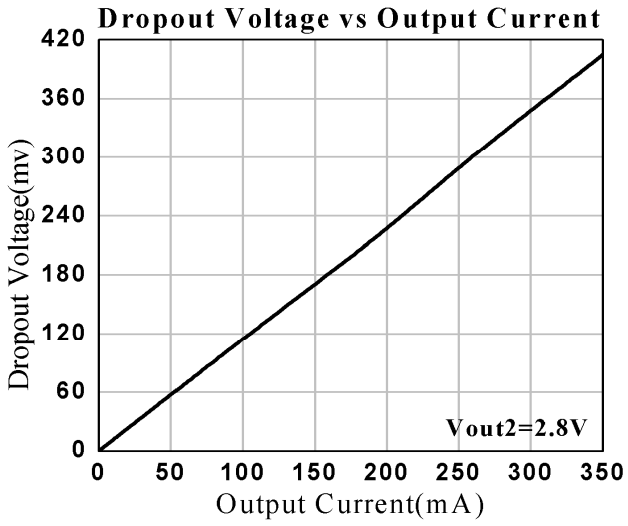


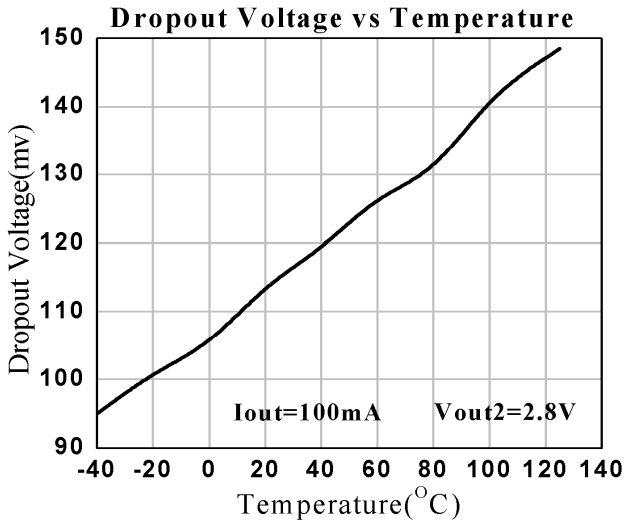


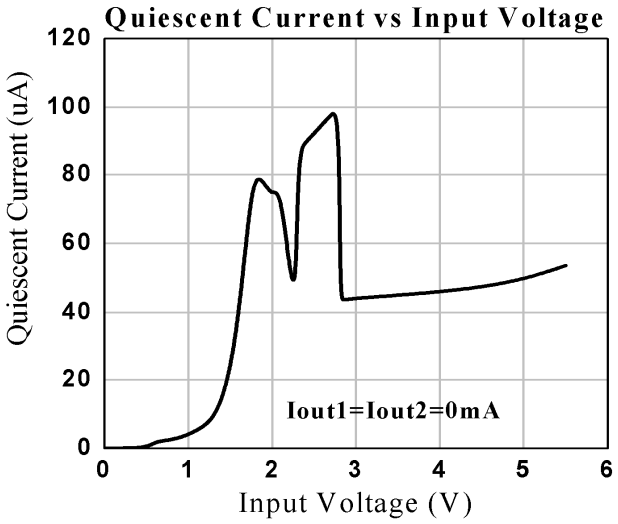


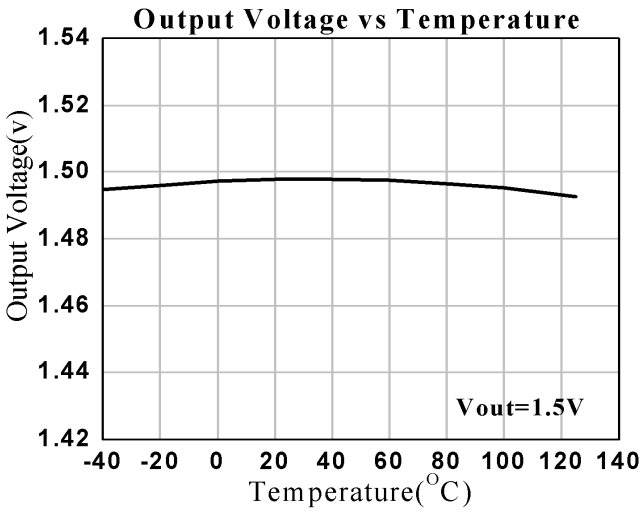


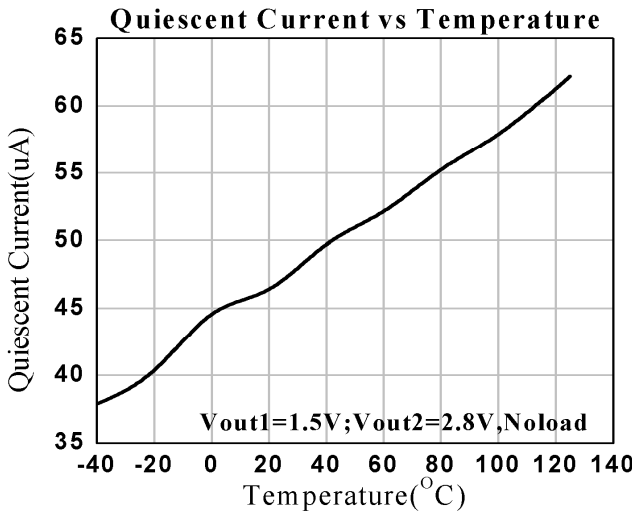
Typical Operating Characteristics (continued)

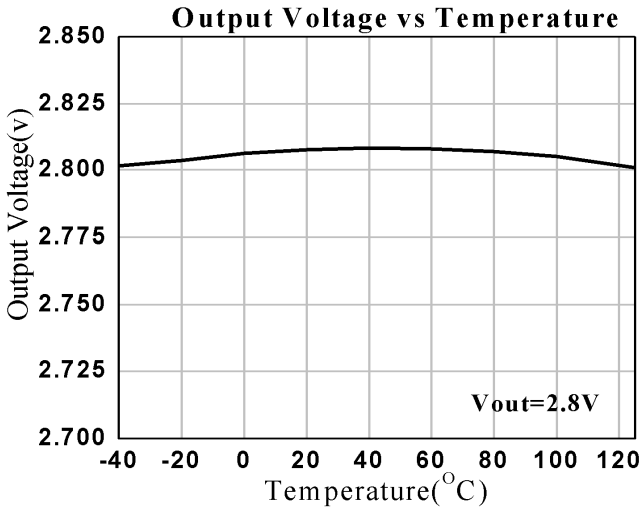






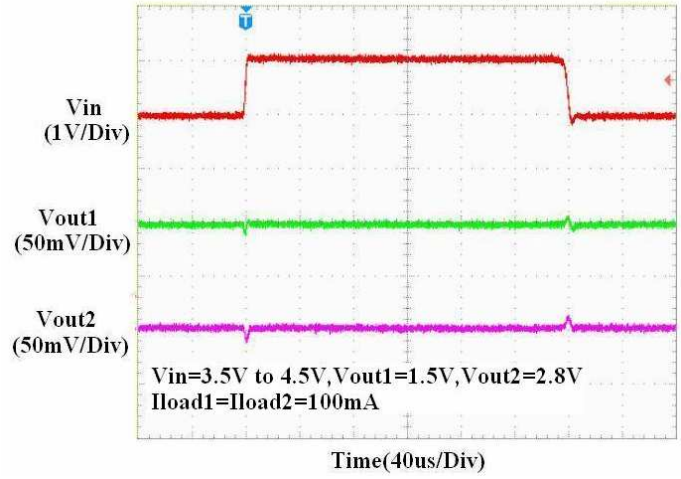




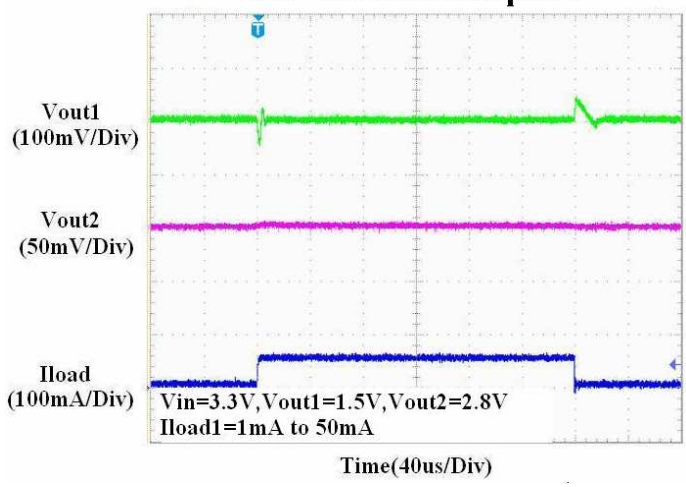


Typical Operating Characteristics (continued)

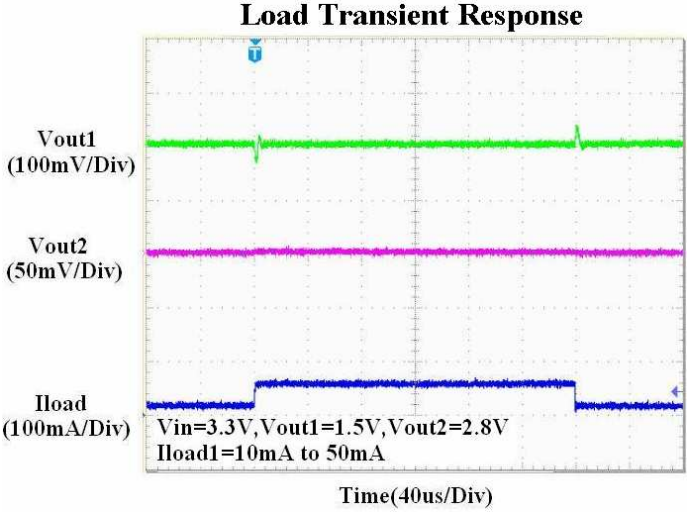
Line Transient Response



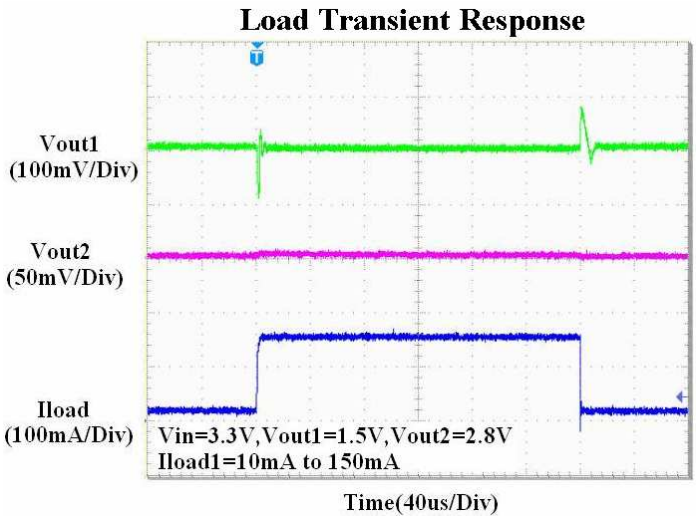
Load Transient Response



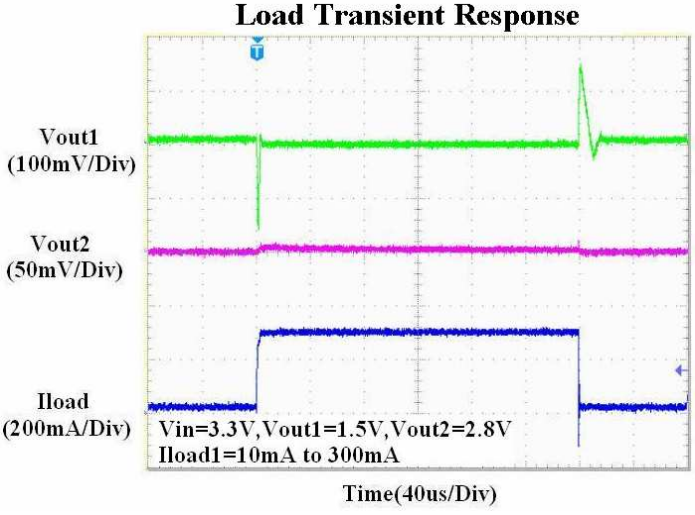
Load Transient Response



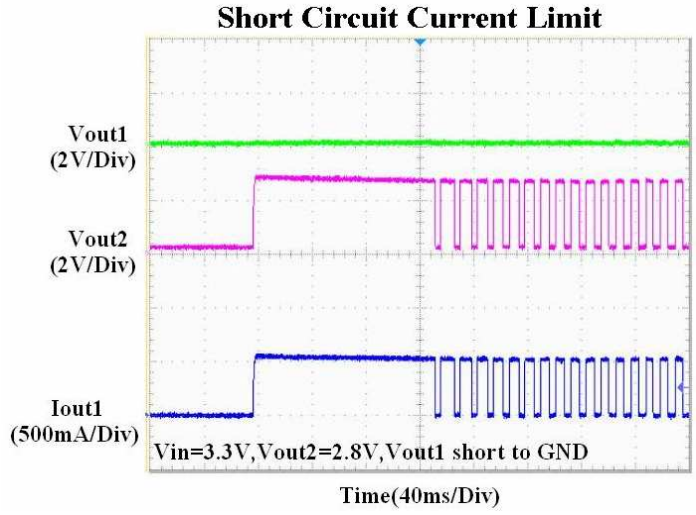
Load Transient Response



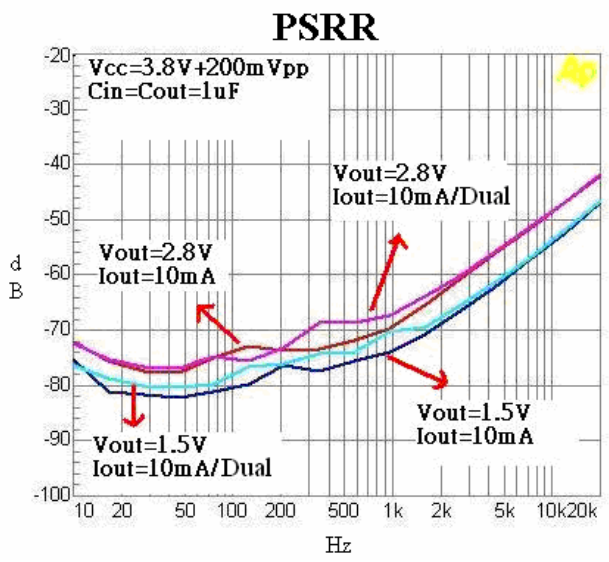
Load Transient Response



Short Circuit Current Limit



Typical Operating Characteristics (continued)



Application Note

External Capacitors

Like any low-dropout regulator, the EUP7230 requires external capacitors for regulator stability. The EUP7230 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

Input Capacitor

An input capacitance of 1μF or higher is required between the EUP7230 input pin and ground (the amout of the capacitance may be increased without limit).This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input. If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be 1μF over the entire operating temperature range.

Output Capacitor

The EUP7230 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (temperature characteristics X7R or X5R) in 1μF to 10μF range with 5mΩ to 500mΩ ESR range is suitable in the EUP7230 application circuit.The output capacitor must meet the requirement for minimum amount of capacitance to maintain good loop stability and phase margin.

No-Load Stability

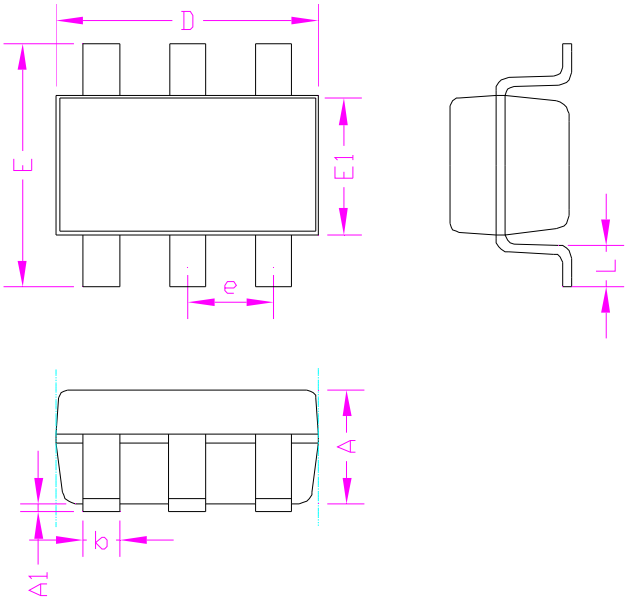
The EUP7230 is stable without any external load. This is specially important for CMOS RAM keep-alive applications.

On/Off Input Operation

The EUP7230 is turned off by pulling the EN pin low, and turned on by pulling it high. If this pin is floating, the regulator is uncertainty. To assure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics. When EN is logic low, output is internally discharged to GND through a 500Ω resistor.

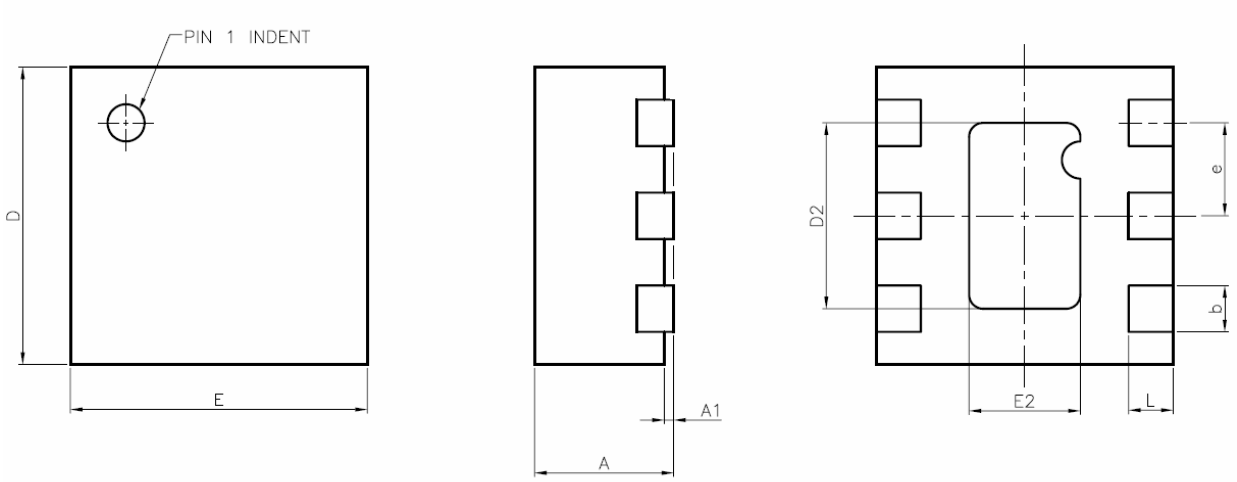
Packaging Information

TSOT23-6



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.00	-	0.039
A1	0.00	0.15	0.000	0.006
b	0.30	0.50	0.012	0.020
D	2.90		0.114	
E1	1.60		0.063	
e	0.95		0.037	
E	2.60	3.00	0.102	0.118
L	0.3	0.60	0.012	0.024

TDFN-6



SYMBOLS	MILLIMETERS			INCHES		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.50	1.60	1.70	0.059	0.629	0.067
D2	1.00 REF			0.039 REF		
E	1.50	1.60	1.70	0.059	0.063	0.067
E2	0.60 REF			0.024 REF		
e	-	0.50	-	-	0.020	-
L	0.19	0.24	0.29	0.007	0.009	0.011