EV10AQ190

Low power QUAD 10-bit 1.25 Gsps ADC operating up to 5 Gsps

Datasheet - *Preliminary*

Main Features

- Quad ADC with 10-bit resolution using true e2v single core technology
  - 1.25 Gsps Sampling Rate in 4-channel mode
  - 2.5 Gsps Sampling Rate in 2-channel mode
  - 5 Gsps Sampling Rate in 1-channel mode
  - Built-in four-by-four Cross Point Switch
- Single 2.5 GHz Differential Symmetrical Input Clock
- 500 mVpp Analog Input (Differential AC or DC Coupled)
- ADC Master Reset (LVDS)
- Double Data Rate Output Protocol
- LVDS Output format
- Digital Interface (SPI) with Reset Signal:
  - Channel Mode Selection
  - Selectable bandwidth (2 available settings)
  - Gain, Offset, Phase Control
  - Standby Mode (full or partial)
  - Binary or Gray Coding Selection
  - Test Modes (ramp, flashing “1”)
- Power Supplies: single 3.3V (1.8V Outputs)
- Reduced clock induced transients on power supply pins due to BiCMOS Silicon technology
- Power Dissipation: 1.4W per channel
- EBGA380 Package (RoHS, 1.27 mm Pitch)

Performance

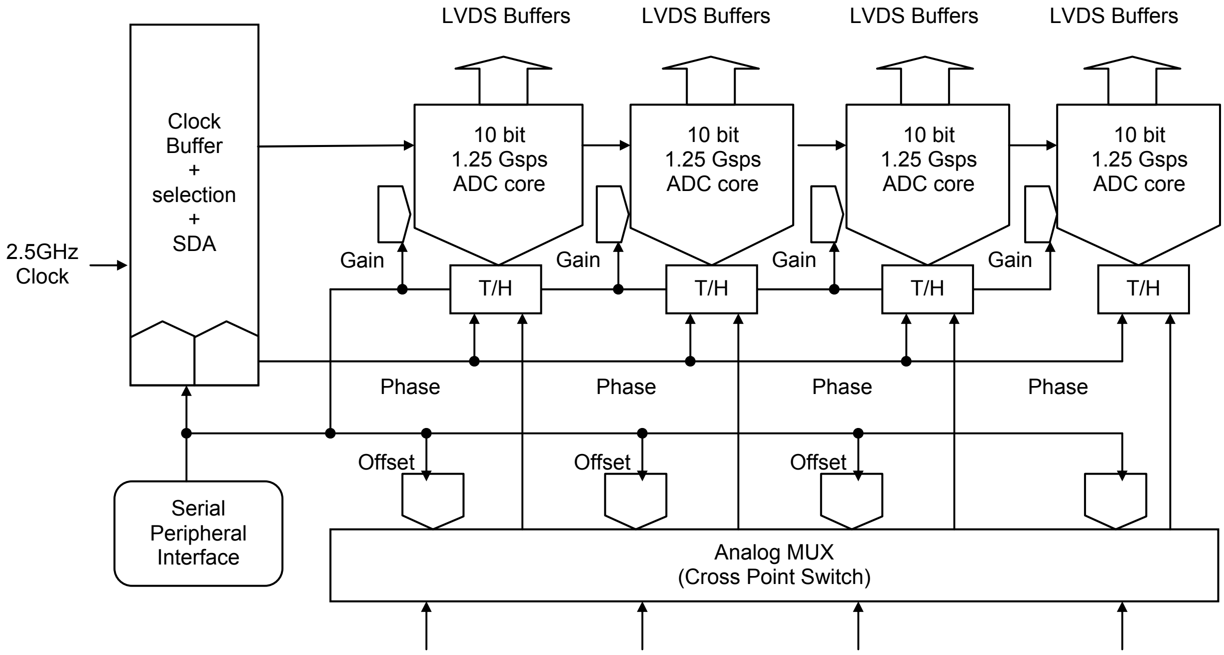
- Selectable Full Power Input Bandwidth (-3 dB) up to 3 GHz (4-2-1 channel mode)
- Band flatness: ± 0.5 dB from DC to 30% of full Power Input bandwidth
- Channel-To-Channel Isolation: > 60 dB
- 4-channel mode (Fsampling = 1.25 Gsps, -1 dBFS)
  - ENOB = 8.8 bit, SFDR = 65 dBc, SNR = 56 dB, DNL = ±0.3 LSB, INL = ±1.5 LSB (Fin= 100 MHz)
  - ENOB = 8.5 bit, SFDR = 63 dBc, SNR = 54 dB (Fin= 620 MHz)
  - ENOB = 7.8 bit, SFDR = 57 dBc, SNR = 50 dB (Fin= 1.2 GHz)
- 2-channel mode or 1-channel mode (Fsampling = 2.5 Gsps and 5 Gsps respectively)
  - ENOB = 8.7 bit, SFDR = 63 dBc, SNR = 56 dB, DNL = ±0.3 LSB, INL = ±1.5 LSB (Fin= 100 MHz)
  - ENOB = 8.4 bit, SFDR = 61 dBc, SNR = 54 dB (Fin= 620 MHz)
  - ENOB = 7.7 bit, SFDR = 55 dBc, SNR = 50 dB (Fin= 1.2 GHz)
- BER: 10^{-16} at Full speed
- Band flatness: ± 0.5 dB from DC to 30% of full Power Input bandwidth
- Low pipe line delay: 4-channel: 9 cycles, 2-channel:9-10 cycles, -channel: 8.5-10 cycles

Applications

- Direct RF Down conversion
- Ultra Wideband Satellite Digital Receiver
- 16 Gbps pt-pt microwave receivers
- High energy Physics
- Automatic Test Equipment
- High Speed Test Instrumentation

1 Block Diagram

Figure 1 Simplified Block Diagram



2 Description

The Quad ADC is made up of four 10-bit ADC cores which can be considered independently (4-channel mode) or grouped by 2 x 2 cores (2-channel mode with the ADCs interleaved two by two) or 1-channel mode (where all four ADCs are all interleaved together).

All four ADCs are clocked by the same external input clock signal and controlled via an industry standard SPI (Serial Peripheral Interface). An analog multiplexer (Cross point Switch) is used to select the analog inputs depending on the mode the Quad ADC is used in.

The **Clock Circuit** is common to all four ADCs. This block receives an external 2.5 GHz clock (maximum frequency) and preferably a low jitter sinewave signal. In this block, the external clock signal is then divided by two in order to generate the internal sampling clocks:

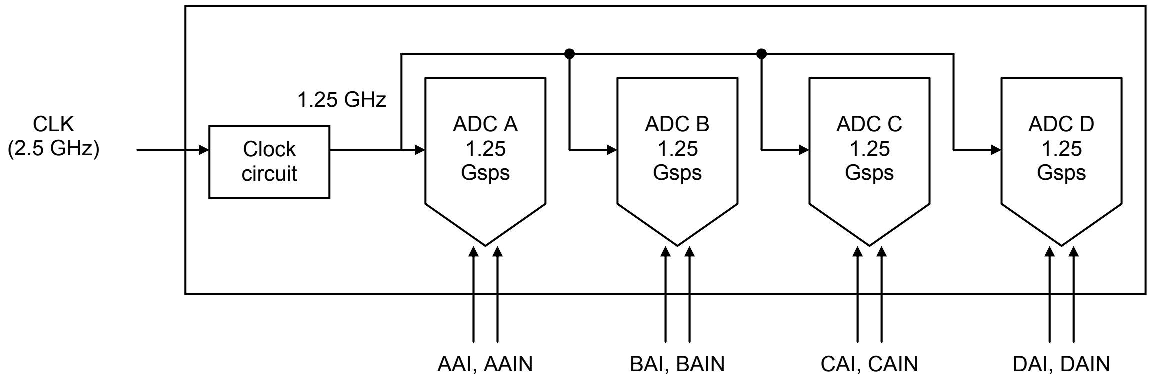
- in 4-channel mode, the same 1.25 GHz clock is directed to all four ADC cores and T/H;
- in 2-channel mode, the in-phase 1.25 GHz clock is sent to ADC A or C and the inverted 1.25 GHz clock is sent to ADC B or D, while the analog input is sent to both ADCs, resulting in an interleaved mode with an equivalent sampling frequency of 2.5 Gsps;
- in 1-channel mode, the in-phase 1.25 GHz clock is sent to ADC A while the inverted 1.25 GHz clock is sent to ADC B, the in-phase 1.25 GHz clock is delayed by 90° to generate the clock for ADC C and the inverted 1.25 GHz clock is delayed by 90° to generate the clock for ADC D, resulting in an interleaved mode with an equivalent sampling frequency of 5 Gsps.

Several adjustments for the sampling delay and the phase are included in this clock circuit to ensure a proper phase relation between the different clocks generated internally from the 2.5 GHz clock.

The **Cross point switch** (Analog MUX) is common to all ADCs. It allows to select which analog input has been chosen by the user:

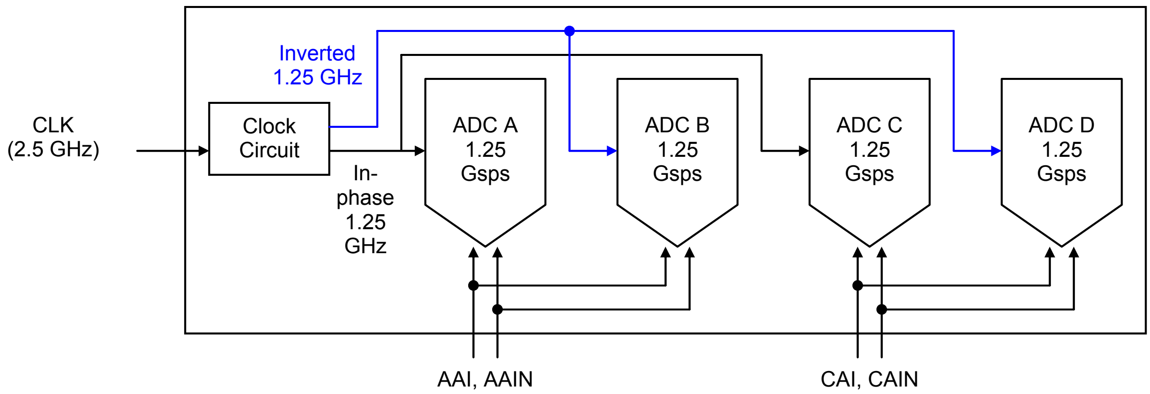
- in 4-channel mode, each analog input is sent to the corresponding ADC (AAI to ADC A, BAI to ADC B, CAI to ADC C and DAI to ADC D);
- in 2-channel mode, one can consider that there 2 two independent ADCs composed of ADC A and B for the first one and of ADC C and D for the second one; the two analog inputs can be applied on AAI or on BAI for the first ADC (in which case, the signal is redirected internally to the second ADC of the pair – ie. B or A respectively) and on CAI or DAI (in which case, the signal is redirected internally to the second ADC of the pair – ie. D or C respectively);
- in 1-channel mode, one analog input is chosen among AAI, BAI, CAI and DAI and then sent to all four ADCs.

Figure 2 4-channel mode configuration



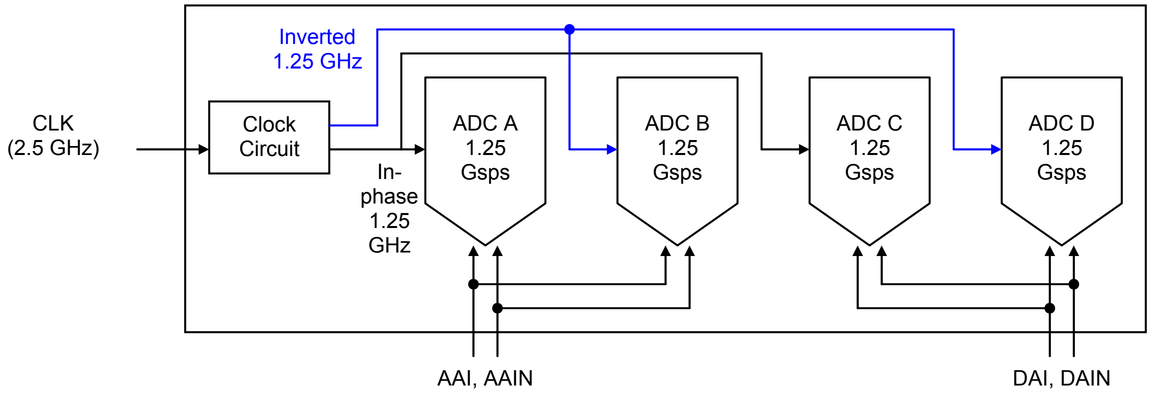
Note: Refer to Figure 8 ADC Timing in 4-Channel mode

Figure 3 2-channel mode configuration (Analog input A and Analog input C)



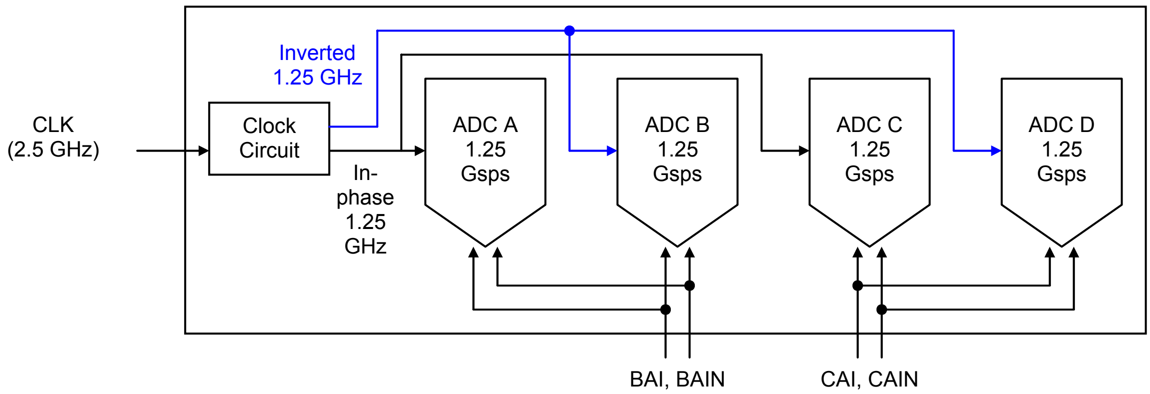
Note: refer to Figure 9 ADC Timing in 2-Channel mode

Figure 4 2-channel mode configuration (Analog input A and Analog input D)



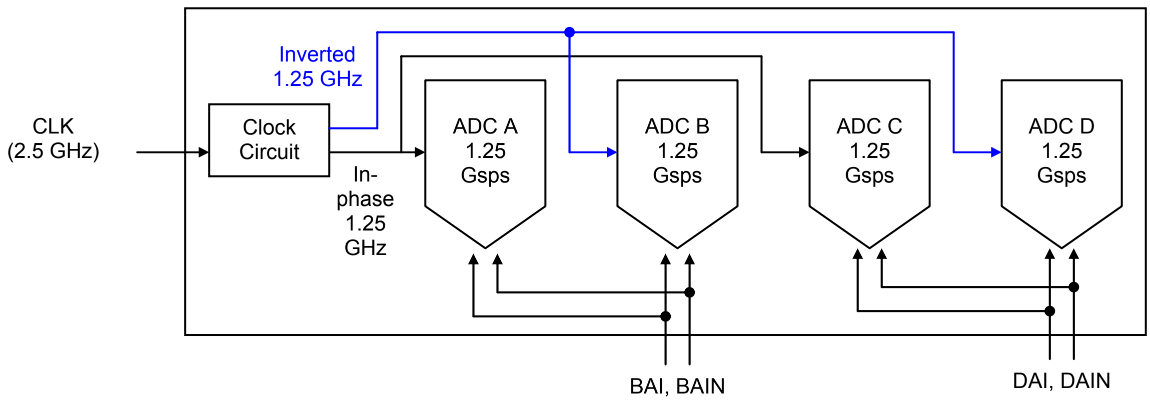
Note: refer to Figure 9 ADC Timing in 2-Channel mode

Figure 5 2-channel mode configuration (Analog input B and Analog input C)



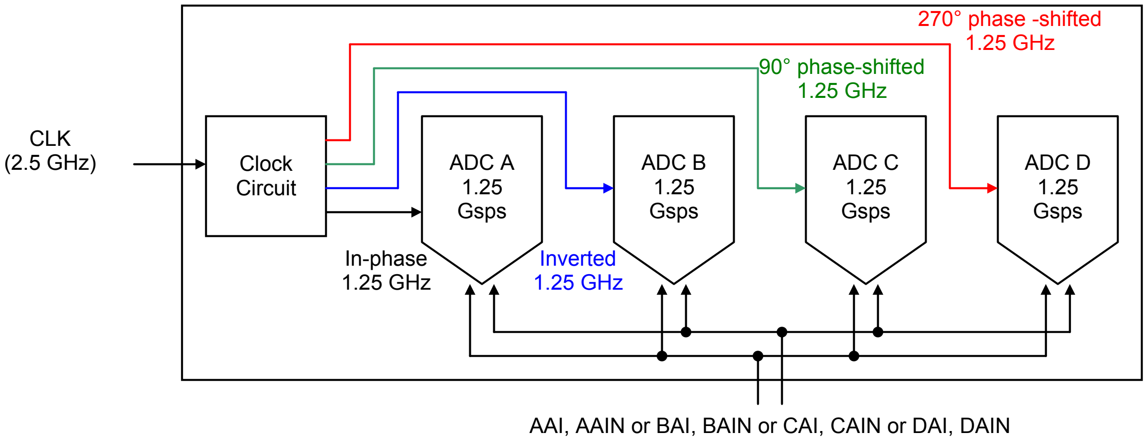
Note: refer to Figure 9 ADC Timing in 2-Channel mode

Figure 6 2-channel mode configuration (Analog input B and Analog input D)



Note: Refer to Figure 9 ADC Timing in 2-Channel mode

Figure 7 1-channel mode configuration



Notes: 1. Refer to Figure 10 ADC Timing in 1-Channel mode

2. For simplification purpose of the timer circuit, the temporary order of ports for sampling is A C B D, therefore sampling order at output port is as follows:

A: N, N + 4, N + 8, N + 12…
C: N + 1, N + 5, N + 9…
B: N + 2, N + 6, N + 10…
D: N + 3, N + 7, N + 11…

The **T/H** (Track and Hold) is located after the Cross Point Switch and before the ADC cores. This block is used to track the data when the internal sampling clock is low and to hold the data when the internal sampling clock is high. This stage has a gain of 2.

The **ADC cores** are all the same for the four ADCs. They include a quantifier block as well as a fast logic block composed of regenerating latches and the Binary/Gray decoding block.

The **SPI block** provides the digital interface for the digital controls of the ADCs. All the functions of the ADC are contained in the SPI registers and controlled via this SPI (channel selection, standby mode, Binary or Gray coding, Offset Gain and Phase adjust..).

The **Output buffers** are LVDS compatible. They should be terminated using a 100Ω external termination resistor.

The **ADC SYNC buffer** is also LVDS compatible. When active, the SYNC signal makes the output clock signals go low. The output data are undetermined during the reset and until the output clock restarts.
When the SYNC signal is released, the output clock signals restart after TDR + pipeline delay + a certain number of input clock cycles which is programmed via the SPI in the SYNC register (from min delay to min delay + 15 x 2 input clock cycles).

A **Diode** for the die junction temperature monitoring is implemented using a diode-mounted transistor but not connected to the die: both cathode and anode are accessible externally.

Eight **DACs for the gain and the offset controls** are included in the design and are addressed through the SPI:

- Offset DACs come into play close to the cross point switch;
- Gain DACs come into play on the biasing of the reference ladders of each ADC core.

These DACs have a resolution of 10-bit and will allow the control via the SPI of the offset and gain of the ADCs:

- Gain adjustment on 1024 steps, ±10% range;
- Offset adjustment on 1024 steps, ±40 mV range (1 step is about 80µV or 0,16 LSB)

Four **DACs for fine phase control** are included in the design and are addressed through the SPI, they have an 10-bit resolution, and a tuning range of ±15 ps (1 step is about 30 fs).

3 Specifications

3.1. Absolute Maximum Ratings

Table 1. Absolute Maximum ratings

Parameter	Symbol	Value	Unit
Positive supply voltage (analog core + SPI pads)	V_{CC}	4	V
Positive Digital supply voltage	V_{CCD}	2.5	V
Positive Digital supply voltage	V_{CCO}	2.5	V
Maximum difference between V_{CC} and V_{CCO}	V_{CC} to V_{CCO}	1.6	V
Maximum difference between V_{CCD} and V_{CCO}	V_{CCD} to V_{CCO}	0.3	V
Analog input voltages	V_{IN} or V_{INN}	TBD	V
Maximum difference between V_{IN} and V_{INN}	V_{IN} - V_{INN}	TBD	V
Clock input voltage	V_{CLK} or V_{CLKN}	TBD	V
Maximum difference between V_{CLK} and V_{CLKN}	V_{CLK} - V_{CLKN}	TBD	Vpp
Junction Temperature	T_J	125	°C
Storage Temperature	Tstg	-55 to 150	°C

Note: Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

3.2. Recommended Conditions Of Use

Table 2. Recommended Conditions of Use

Parameter	Symbol	Comments	Recommended Value	Unit
Positive supply voltage	V_{CC}	Includes SPI pads	3.3	V
Positive digital supply voltage	V_{CCD}	Digital parts	1.8	V
Positive Output supply voltage	V_{CCO}	Output buffers	1.8	V
Differential analog input voltage (Full Scale)	V_{IN}, V_{INN} V_{IN} -V_{INN}		±250 500	mV mVpp
Clock input power level	P_{CLK} P_{CLKN}		0	dBm
Digital CMOS input	V_D	V_{IL} V_{IH}	0 Vcc	V
Clock frequency	Fc	For operation at 1.25 Gsps in 4-channel mode or 2.5 Gsps in 2-channel mode or 5 Gsps in 1-channel mode	≤ 2.5	GHz
Operating Temperature Range	Ta	Commercial "C" grade Industrial « V » grade	0°C < T_A < 70°C -40°C < T_A < 85°C	°C

3.3. Electrical Characteristics for supplies, Inputs and Outputs

Unless otherwise specified:
V_{CC} = 3.3V, V_{CCD} = 1.8V, V_{CCO} = 1.8V
-1 dBFS Analog input (Full Scale Input: V_{IN} - V_{INN} = 500 mVpp)
Clock input differentially driven; analog input differentially driven.
Default mode: 4-channel mode ON, Binary output data format, Standby mode OFF, Full bandwidth

Table 3. Electrical characteristics for Supplies, Inputs and Outputs

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
POWER REQUIREMENTS						
Power Supply voltage - Analog (and SPI pads) - Digital - Output		 V_{CC} V_{CCD} V_{CCO}		 3.3 1.8 1.8		 V V V
Power Supply current - Analog (and SPI pads) - Digital - Output		 I_{CC} I_{CCD} I_{CCO}		 1.6 3 200		 A mA mA
Power Supply current (full standby mode) - Analog (and SPI pads) - Digital - Output		 I_{CC} I_{CCD} I_{CCO}		 890 3 110		 mA mA mA
Power Supply current (partial standby mode) - Analog (and SPI pads) - Digital - Output		 I_{CC} I_{CCD} I_{CCO}		 190 3 20		A
Power dissipation Default mode Full Standby mode Partial Standby mode (2 channels)		P_D		 5.65 0.6 3.15		 W W W
DATA INPUTS						
Input Common Mode		V_{ICM}		1.6V		V
Full Scale Input Voltage range (differential mode)		V_{IN} V_{INN}		250 250		mVpp mVpp
Input swing		V_{INN} -V_{IN}		500		mVpp
Analog input capacitance (die)		C_{IN}		0.5		pF
Input Resistance (differential)		R_{IN}		100		Ω
CLOCK INPUTS						
Source Type		Differential Sinewave				
Clock input common mode voltage		V_{CM}		1.8		V
Clock input power level (low phase noise sinewave input) 100Ω differential, AC coupled signal		P_{CLK}	-9	0	2	dBm
Clock input swing (differential voltage) – on each clock input		$V_{CLK,}$ V_{CLKN}	150 150	450 450	565 565	mVpp mVpp
Clock input capacitance (die only)		C_{CLK}		0.5		pF
Clock input resistance (differential)		R_{CLK}		100		Ω
Clock Jitter (max. allowed on clock source) For 1 GHz sinewave analog input		Jitter			150	fs
Clock Duty Cycle requirement in 1-channel mode for performance		Duty Cycle	48	50	52	%
Clock Duty Cycle requirement in 2-channel mode for performance		Duty Cycle	40	50	60	%
Clock Duty Cycle requirement in 4-channel mode for performance		Duty Cycle	40	50	60	%
SYNCP, SYNCN Signal						
Logic Compatibility		LVDS				
Differential input voltage Offset voltage		V_{IH}- V_{IL} V_{ICM}	100 0.25	350 1.25	 2.25	mV V

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
SYNCP, SYNCN input capacitance (die only)		CSYNC		0.5		pF
SYNCP, SYNCN input resistance		RSYNC		100		Ω
SPI						
Logic compatibility			3.3V CMOS			
CMOS low level input voltage		V_{IL}	0		$0.25*V_{CC}$	V
CMOS high level input voltage		V_{IH}	$0.75*V_{CC}$		V_{CC}	V
CMOS low level output voltage (Iolc =2 or 3 mA)		V_{OL}			0.4	V
CMOS high level output voltage (Iohc =2 or 3 mA)		V_{OH}	$0.8*V_{CC}$			V
CMOS low level input current (Vinc=0 V)		I_{IL}			0.7	nA
CMOS high level input current (Vinc=V_{CC})		I_{IH}			165	nA
DIGITAL DATA and DATA READY OUTPUTS (see Note)						
Logic Compatibility			LVDS (over 100 ohm differential load)			
Differential output voltage Offset voltage		V_{OD} V_{OS}	250 1.125		450 1.375	mV V

Note: Differential output buffers impedance = 100Ω differential.

3.4. Converter Characteristics

Unless otherwise specified:
V_{CC} = 3.3V, V_{CCD} = 1.8V, V_{CCO} = 1.8V
-1 dBFS Analog input (Full Scale Input: V_{IN} - V_{INN} = 500 mVpp)
Clock input differentially driven; analog input differentially driven.
Default mode: 4-channel mode ON, Binary output data format, 1:2 DMUX ON, Standby mode OFF, full bandwidth

Table 4. DC Converter Characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
DC ACCURACY						
Gain central value				TBD		
Gain error drift				TBD		ppm/°C
Input offset voltage				TBD		mV
4-Channel Mode (Fsampling = 1.25 Gsps, Fin = 95 KHz, -1 dBFS), for each channel						
DNLrms		DNLrms		TBD		LSB
Differential non linearity		DNL+		0.3		LSB
Differential non linearity		DNL-		-0.3		LSB
Integral non linearity		INL-		1.5		LSB
Integral non linearity		INL+		-1.5		LSB
2-Channel Mode (Fsampling = 2.5 Gsps, Fin = 95 KHz, -1 dBFS), for each channel						
DNLrms		DNLrms		TBD		LSB
Differential non linearity		DNL+		0.3		LSB
Differential non linearity		DNL-		-0.3		LSB
Integral non linearity		INL-		1.5		LSB
Integral non linearity		INL+		-1.5		LSB
1-Channel Mode (Fsampling = 5 Gsps, Fin = 95 KHz, -1 dBFS)						
DNLrms		DNLrms		TBD		LSB
Differential non linearity		DNL+		0.3		LSB
Differential non linearity		DNL-		-0.3		LSB
Integral non linearity		INL-		1.5		LSB
Integral non linearity		INL+		-1.5		LSB

Table 5. Dynamic Converter Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
AC ANALOG INPUTS (differentially driven)						
Full Power Input Bandwidth in Full mode (BW = "1" in 0x01 register) Full Power Input Bandwidth in Nominal mode (default mode – BW = "0" in 0x01 register)	FPBW		3 1		GHz GHz	1, 2
Gain Flatness (over any 500 MHz band in full band mode setting BW = "1" in 0x01 register)	GF			TBD	dB	
Input Voltage Standing Wave Ratio up to 3 GHz	VSWR		TBD			3
Crosstalk (Fin = 620 MHz)		60			dB	
Dynamic Performance – 4-Channel Mode (Fsampling = 1.25 Gsps, -1 dBFS) for each channel						

Parameter	Symbol	Min	Typ	Max	Unit	Note
Effective Number Of Bits Fs = 1.25 Gsps Fin = 100 MHz Fs = 1.25 Gsps Fin = 620 MHz Fs = 1.25 Gsps Fin = 1200 MHz	ENOB		8.8 8.5 7.8		Bit	4
Signal to Noise Ratio Fs = 1.25 Gsps Fin = 100 MHz Fs = 1.25 Gsps Fin = 620 MHz Fs = 1.25 Gsps Fin = 1200 MHz	SNR		56 54 50		dB	4
Total Harmonic Distortion (25 Harmonics) Fs = 1.25 Gsps Fin = 100 MHz Fs = 1.25 Gsps Fin = 620 MHz Fs = 1.25 Gsps Fin = 1200 MHz	|THD|		63 61 56		dB	4
Spurious Free Dynamic Range Fs = 1.25 Gsps Fin = 100 MHz Fs = 1.25 Gsps Fin = 620 MHz Fs = 1.25 Gsps Fin = 1200 MHz	|SFDR|		65 63 57		dBc	4
Two tone third order intermodulation distortion Fs = 1.25 Gsps Fin1 = 490 MHz ; Fin2 = 495 MHz [- 7dBFS]	|IMD3|		60		dBFS	4
Dynamic Performance – 2-and 1-Channel Mode (Fsampling = 2.5 Gsps and 5 Gsps respectively, -1 dBFS) for each channel						
Effective Number Of Bits Fin = 100 MHz Fin = 620 MHz Fin = 1200 MHz	ENOB		8.7 8.4 7.7		Bit	4
Signal to Noise Ratio Fin = 100 MHz Fin = 620 MHz Fin = 1200 MHz	SNR		56 54 50		dB	4
Total Harmonic Distortion (25 Harmonics) Fin = 100 MHz Fin = 620 MHz Fin = 1200 MHz	|THD|		61 59 54		dB	4
Spurious Free Dynamic Range Fin = 100 MHz Fin = 620 MHz Fin = 1200 MHz	|SFDR|		63 61 55		dBc	4
Two tone third order intermodulation distortion Fin1 = 490 MHz ; Fin2 = 495 MHz [- 7dBFS]	|IMD3|		60		dBFS	4

Notes:
1. It is recommended to use the ADC in reduced bandwidth mode in order to minimize the noise in the ADC when allowed by the application.
2. These figures apply in all 4-/2- and 1-channel modes (interleaved and non interleaved modes)
3. Specified from DC up to 2.5 GHz input signal. Input VSWR is measured on a soldered device. It assumes an external 50Ω ± 2Ω controlled impedance line, and a 50Ω driving source impedance (S_{11} < - 30 dB).
4. All the figures provided at Fin = 100 MHz and at Fin = 620 MHz are obtained using the ADC in nominal band mode. The one provided at Fin = 1.2 GHz is obtained using the ADC in full band mode.

3.5. Transient and Switching Characteristics

Table 6. Transient and Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
TRANSIENT PERFORMANCE						
Bit Error Rate	BER			10^{-16}	Error/ sample	1
ADC settling time (V_{IN}-V_{INN} = 400 mVpp) in Full BW mode	TS		TBD		ns	
Overvoltage recovery time	ORT		TBD		ps	
ADC step response Rise/fall time (10/90%)			TBD		ps	
Overshoot			TBD		%	
Ringback			TBD		%	

Note 1. Output error amplitude < ± 6 lsb. Fs = 1.25 Gsps T_J = 110 °C

Table 7. Transient and Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
SWITCHING PERFORMANCE AND CHARACTERISTICS						
Clock frequency	F_{CLK}	400		2500	MHz	1, 2
Maximum sampling frequency (for each channel) 4-channel mode 2-channel mode 1-channel mode	F_S	200 400 800		1250 2500 5000	Msps Msps Msps	
Minimum clock pulse width (high)	TC1			200	ps	
Minimum clock pulse width (low)	TC2			200	ps	
Aperture Delay	TA		300		ps	1
ADC Aperture uncertainty	Jitter		TBD		fs rms	1
Output rise time for DATA (20%-80%)	TR		90		ps	3
Output fall time for DATA (20%-80%)	TF		100		ps	
Output rise time for DATA READY (20%-80%)	TR		90		ps	3
Output fall time for DATA READY (20%-80%)	TF		80		ps	
Data output delay	TOD		3		ns	4
Data Ready output delay	TDR		3		ns	4
	|TOD-TDR|			50	ps	4
Output Data to Data Ready Propagation Delay	TD1		420		ps	5
Data Ready to Output Data Propagation Delay	TD2		380		ps	5
Data Ready pipeline delay 4-channel mode 2-channel mode 1-channel mode	TPD		TBD		Clock Cycles	

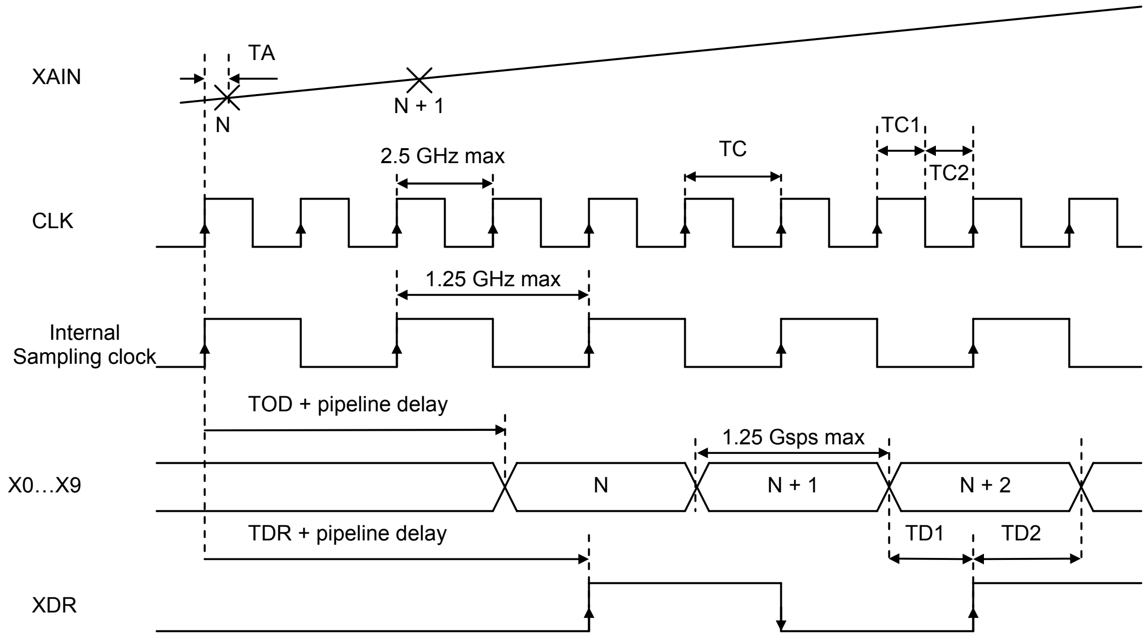
Parameter	Symbol	Min	Typ	Max	Unit	Note
Output Data pipeline delay 4-channel mode Ports A, B, C, D 2-channel mode Ports A, C Ports B, D 1-channel mode Port A Port B Port C Port D	TPD		TBD		Clock Cycles	
Data Ready Reset delay	TRDR		2.5		ns	
Minimum SYNC pulse width	TSYNC	2 x Tclock			ns	6
SYNC setup time			TBD			
SYNC hold time			TBD			

Notes
1. See Definition Of Terms.
2. The clock frequency lower limit is due to the gain.
3. 50Ω // C_{LOAD} = 2pF termination (for each single-ended output). Termination load parasitic capacitance derating value: 50ps/pF (ECL).
4. TOD and TDR propagation times are defined at package input/outputs. They are given for reference only.
5. Values for TD1 and TD2 are given for a 2.5 GHz external clock frequency (50% duty cycle). For different sampling rates, apply the following formula: TD1 = T/2 +(|TOD-TDR|) and TD2 = T/2 +(|TOD-TDR|), where T=clock period.
This places the rising edge (True-False) of the differential Data Ready signal in the middle of the Output Data valid window. This gives maximum setup and hold times for external data acquisition.
6. Tclock = external clock period. SYNC cannot change less than 40 ps before CLK has a rising edge. SYNC can change 0 ps after CLK has a rising edge. SYNC must be high for 2 CLK (external clock) rising edges.

3.6. Timing Diagrams

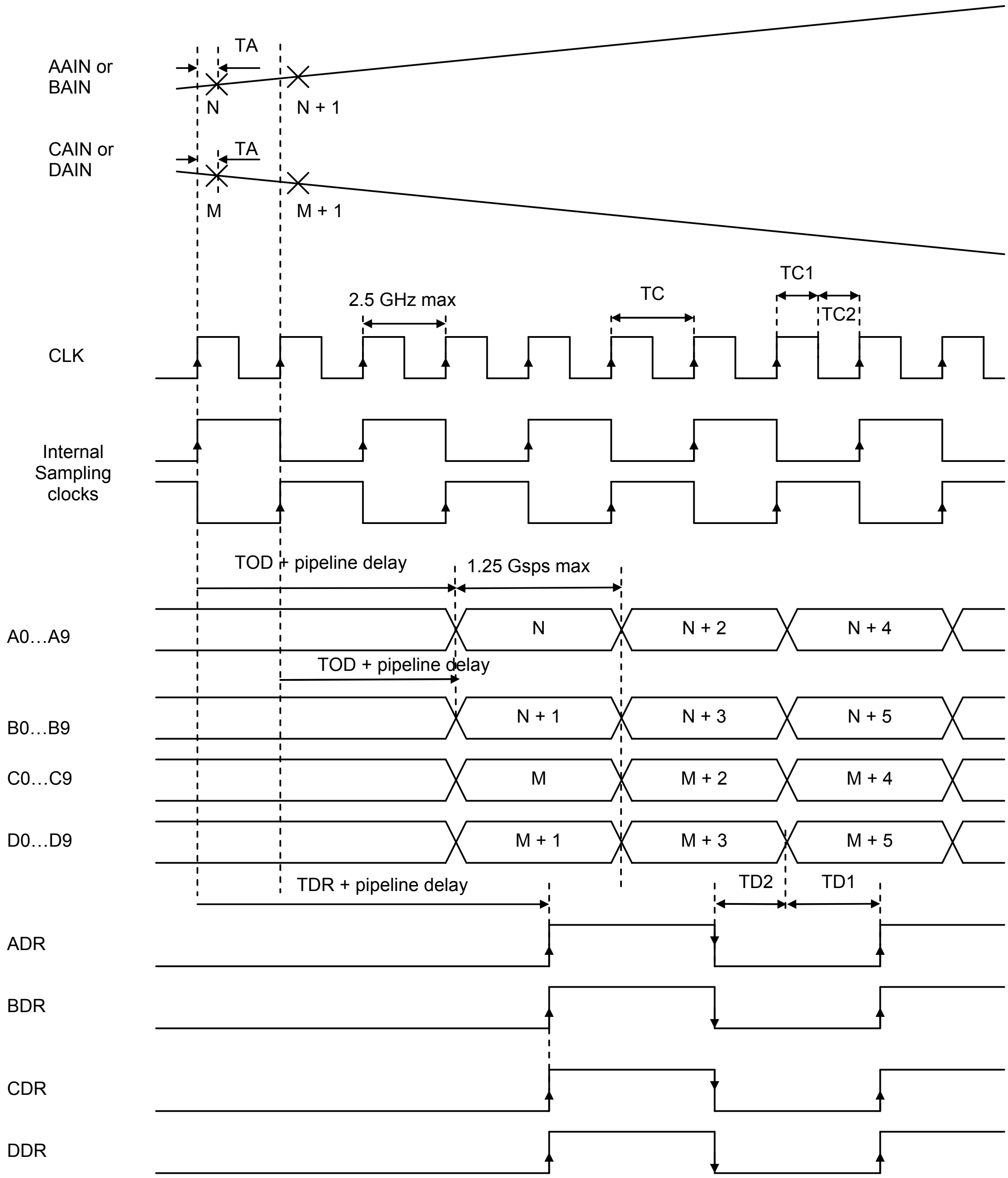
For the information on the reset sequence (using SYNCP, SYNCN signals, please refer to section 8.1).

Figure 8 ADC Timing in 4-Channel mode



Note: X refers to A, B, C and D.

Figure 9 ADC Timing in 2-Channel mode

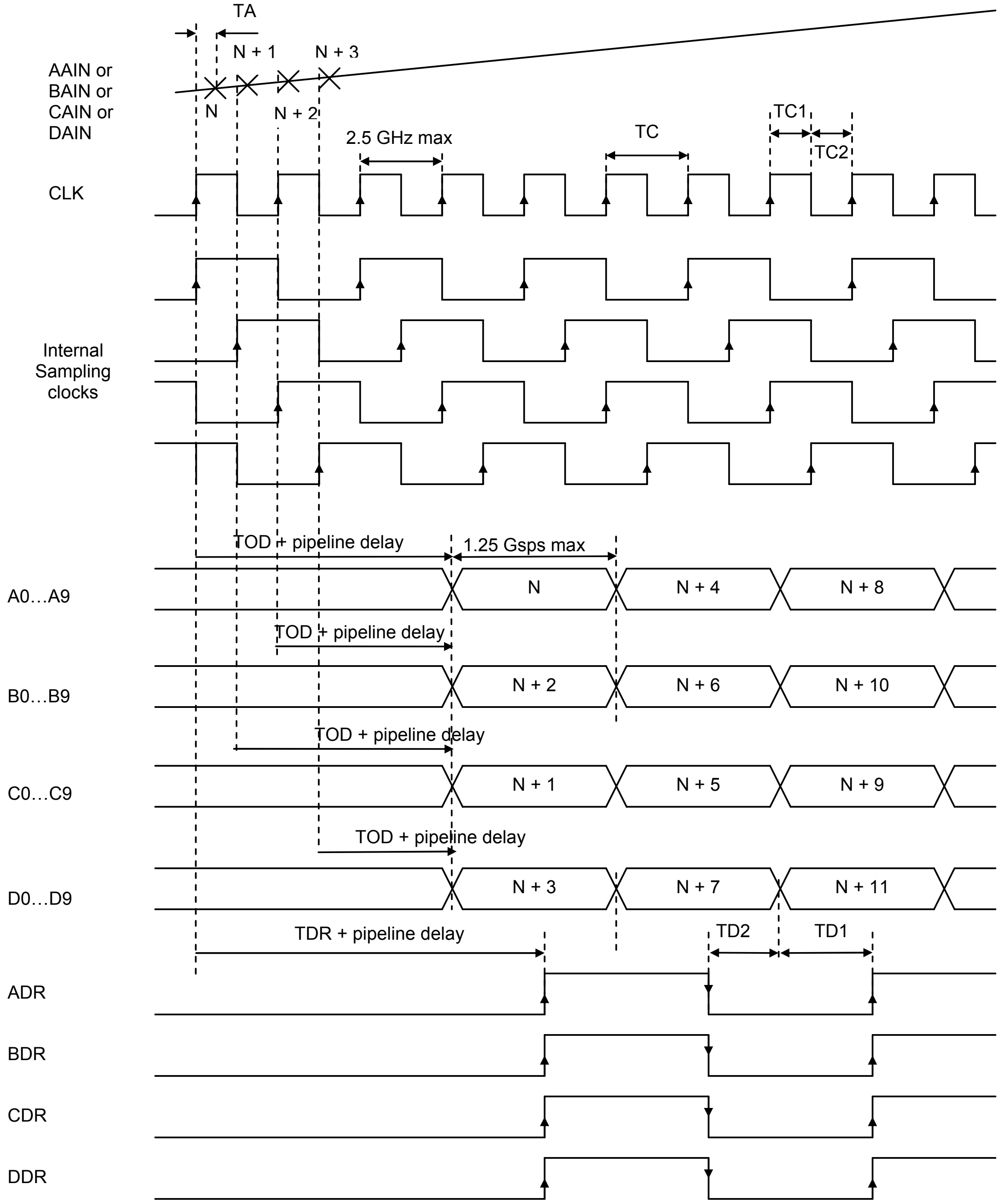


Note: In 2-channel mode, the two analog inputs can be applied on

- (AAI, AAIN) and (CAI, CAIN), in which case, the outputs corresponding to (AAI, AAIN) will be on A0…A9 and B0…B9 and the ones corresponding to (CAI, CAIN) on C0…C9 and D0…D9;
- or (AAI, AAIN) and (DAI, DAIN), in which case, the outputs corresponding to (AAI, AAIN) will be on A0…A9 and B0…B9 and the ones corresponding to (DAI, DAIN) on C0…C9 and D0…D9;

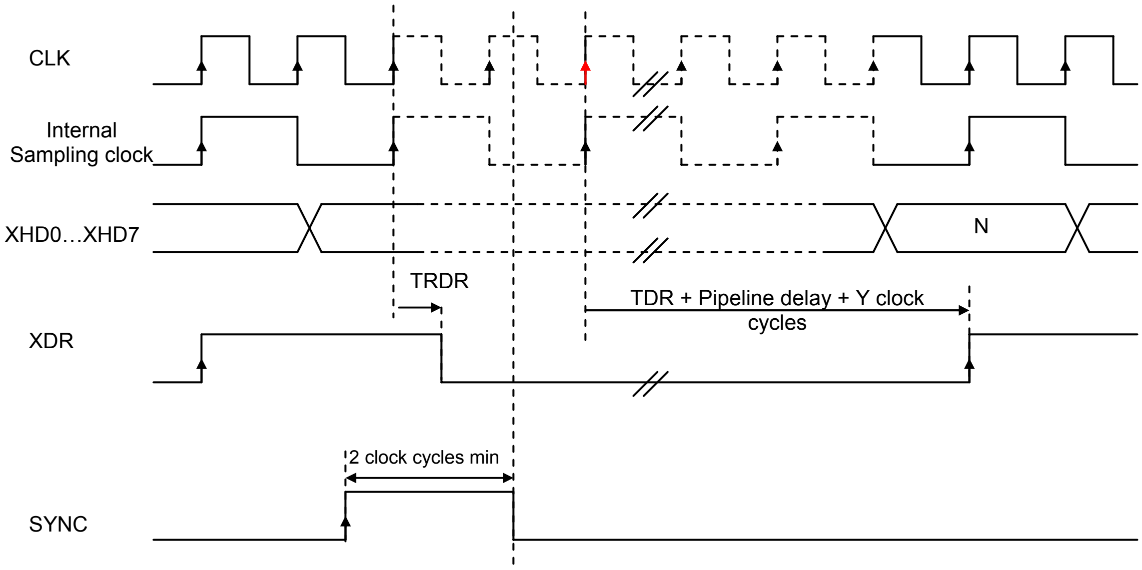
- or (BAI, BAIN) and (CAI, CAIN), in which case, the outputs corresponding to (BAI, BAIN) will be on A0…A9 and B0…B9 and the ones corresponding to (CAI, CAIN) on C0…C9 and D0…D9;
- or (BAI, BAIN) and (DAIN, DAIN), in which case, the outputs corresponding to (BAI, BAIN) will be on A0…A9 and B0…B9 and the ones corresponding to (DAI, DAIN) on C0…C9 and D0…D9.

Figure 10 ADC Timing in 1-Channel mode



Note: In 1-Channel mode, the analog input can be applied on (AAI,AAIN), (BAI, BAIN), (CAI, CAIN) or (DAI, DAIN). The choice is made via the SPI in the control register.

Figure 11 ADC SYNC Timing in 4-Channel mode



Note: X refers to A, B, C and D.

3.7. Digital Output Coding

Table 8. ADC Digital output coding table

Differential analog input	Voltage level	Digital output: Binary MSB (bit 9)………LSB(bit 0)	Out-of-Range	Digital output: GRAY MSB (bit 9)……LSB (bit 0)	Out-of-Range
> + 250.25 mV	>Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1 1 1	1	1 0 0 0 0 0 0 0 0 0	1
+ 250.25 mV + 249.75 mV	Top end of full scale + ½ LSB Top end of full scale - ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	0 0	1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1	0 0
+ 124.75 mV + 124.25 mV	$^{3}/_{4}$ full scale + ½ LSB $^{3}/_{4}$ full scale - ½ LSB	1 1 0 0 0 0 0 0 0 0 1 0 1 1 1 1 1 1 1 1	0 0	1 0 1 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0	0 0
+ 0.25 mV - 0.25 mV	Mid scale + ½ LSB Mid scale - ½ LSB	1 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1	0 0	1 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	0 0
- 124.25 mV - 124.75 mV	$^{1}/_{4}$ full scale + ½ LSB $^{1}/_{4}$ full scale - ½ LSB	0 1 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1	0 0	0 1 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0	0 0
- 249.75 mV - 250.25 mV	Bottom end of full scale + ½ LSB Bottom end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	0 0
< - 250.25 mV	< Bottom end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 0	1	0 0 0 0 0 0 0 0 0 0	1

3.8. Definition of Terms

Abbreviation	Term	Definition
(Fs max)	*Maximum Sampling Frequency*	Sampling frequency for which ENOB < 6bits
(Fs min)	*Minimum Sampling frequency*	Sampling frequency for which the ADC Gain has fallen by 0.5dB with respect to the gain reference value. Performances are not guaranteed below this frequency.
(BER)	*Bit Error Rate*	Probability to exceed a specified error threshold for a sample at maximum specified sampling rate. An error code is a code that differs by more than +/- 4 LSB from the correct code.
(FPBW)	*Full power input bandwidth*	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale –1 dB (- 1 dBFS).
(SSBW)	*Small Signal Input bandwidth*	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale –10 dB (- 10 dBFS).
(SINAD)	*Signal to noise and distortion ratio*	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below Full Scale (- 1 dBFS), to the RMS sum of all other spectral components, including the harmonics except DC.
(SNR)	*Signal to noise ratio*	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below Full Scale, to the RMS sum of all other spectral components excluding the nine first harmonics.
(THD)	*Total harmonic distortion*	Ratio expressed in dB of the RMS sum of the first nine harmonic components, to the RMS input signal amplitude, set at 1 dB below full scale. It may be reported in dB (i.e, related to converter –1 dB Full Scale), or in dBc (i.e, related to input signal level).
(SFDR)	*Spurious free dynamic range*	Ratio expressed in dB of the RMS signal amplitude, set at 1dB below Full Scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dB (i.e., related to converter –1 dB Full Scale), or in dBc (i.e, related to input signal level).

(ENOB)	*Effective Number Of Bits*	$ENOB = \dfrac{SINAD - 1.76 + 20 \log (A / FS/2)}{6.02}$	Where A is the actual input amplitude and FS is the full scale range of the ADC under test
(DNL)	*Differential non linearity*	The Differential Non Linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.	
(INL)	*Integral non linearity*	The Integral Non Linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.	
(TA)	*Aperture delay*	Delay between the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point), and the time at which (XAI, XAIN where X = A, B C or D) is sampled.	
(JITTER)	*Aperture uncertainty*	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.	
(TS)	*Settling time*	Time delay to achieve 0.2 % accuracy at the converter output when a 80% Full Scale step function is applied to the differential analog input.	
(ORT)	*Overvoltage recovery time*	Time to recover 0.2 % accuracy at the output, after a 150 % full scale step applied on the input is reduced to midscale.	
(TOD)	*Digital data Output delay*	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.	
(TDR)	*Data ready output delay*	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.	
(TD1)	*Time delay from Data transition to Data Ready*	General expression is TD1 = TC1 + TDR – TOD with TC = TC1 + TC2 = 1 encoding clock period.	
(TD2)	*Time delay from Data Ready to Data*	General expression is TD2 = TC2 + TDR – TOD with TC = TC1 + TC2 = 1 encoding clock period.	
(TC)	*Encoding clock period*	TC1 = Minimum clock pulse width (high) TC = TC1 + TC2 TC2 = Minimum clock pulse width (low)	
(TPD)	*Pipeline Delay*	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD).	
(TRDR)	*Data Ready reset delay*	Delay between the first rising edge of the external clock after reset (SYNCP, SYNCN) and the reset to digital zero transition of the Data Ready output signal (XDR, where X = A, B, C or D).	
(TR)	*Rise time*	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.	
(TF)	*Fall time*	Time delay for the output DATA signals to fall from 20% to 80% of delta between low level and high level.	
(PSRR)	*Power supply rejection ratio*	Ratio of input offset variation to a change in power supply voltage.	
(NRZ)	*Non return to zero*	When the input signal is larger than the upper bound of the ADC input range, the output code is identical to the maximum code and the Out of Range bit is set to logic one. When the input signal is smaller than the lower bound of the ADC input range, the output code is identical to the minimum code, and the Out of range bit is set to logic one. (It is assumed that the input signal amplitude remains within the absolute maximum ratings).	
(IMD)	*InterModulation Distortion*	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products.	
(NPR)	*Noise Power Ratio*	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the	

		input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
(VSWR)	*Voltage Standing Wave Ratio*	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20dB return loss (ie. 99% power transmitted and 1% reflected).

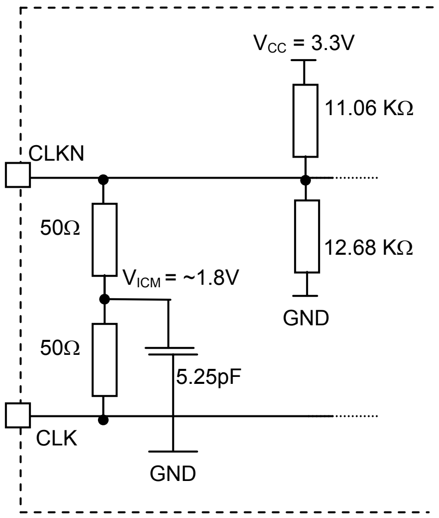
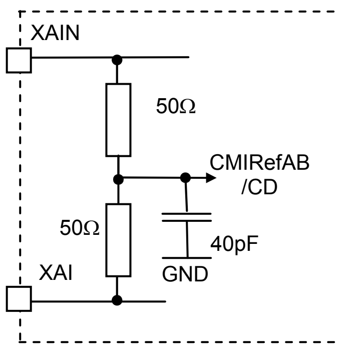
4 Pin Description

4.1. Pinout View (Bottom view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
AD	GND	VCC	B8	B9	BOR	GND	DiodA	NC	GND	NC	SYNCP	CLK	CLKN	scan0	scan2	sclk	mosi	Res50	GND	COR	C9	C8	VCC	GND	AD
AC	GND	VCC	B8N	B9N	BORN	GND	DiodC	GND	VCC	NC	SYNCN	GND	GND	scan1	rstn	csn	miso	Res62	GND	CORN	C9N	C8N	VCC	GND	AC
AB	NC	NC	VCC	GND	VCC	GND	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	GND	VCC	GND	VCC	NC	NC	AB
AA	NC	NC	VCC	GND	VCCO	VCC	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	VCC	VCCO	GND	VCC	NC	NC	AA
Y	NC	NC	VCCO	GND	GND	VCCO	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	VCCO	GND	GND	VCCO	NC	NC	Y
W	NC	NC	VCCO	GND	GND															GND	GND	VCCO	NC	NC	W
V	NC	NC	NC	NC	GND															GND	NC	NC	NC	NC	V
U	B7	B7N	NC	NC	VCCO															VCCO	NC	NC	C7N	C7	U
T	B5	B5N	B6	B6N	GND															GND	C6N	C6	C5N	C5	T
R	B3	B3N	B4	B4N	VCC															VCC	C4N	C4	C3N	C3	R
P	B1	B1N	B2	B2N	GND															GND	C2N	C2	C1N	C1	P
N	BDR	BDRN	B0	B0N	VCC															VCC	C0N	C0	CDRN	CDR	N
M	ADR	ADRN	A0	A0N	VCC															VCC	D0N	D0	DDRN	DDR	M
L	A1	A1N	A2	A2N	GND															GND	D2N	D2	D1N	D1	L
K	A3	A3N	A4	A4N	VCC															VCC	D4N	D4	D3N	D3	K
J	A5	A5N	A6	A6N	GND															GND	D6N	D6	D5N	D5	J
H	A7	A7N	NC	NC	VCCO															VCCO	NC	NC	D7N	D7	H
G	NC	NC	NC	NC	GND															GND	NC	NC	NC	NC	G
F	NC	NC	VCCO	GND	GND															GND	GND	VCCO	NC	NC	F
E	NC	NC	VCCO	GND	GND	VCCO	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCCO	GND	GND	VCCO	NC	NC	E
D	NC	NC	VCC	GND	VCCO	VCC	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCC	VCCO	GND	VCC	NC	NC	D
C	NC	NC	VCC	GND	VCC	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCC	GND	VCC	NC	NC	C
B	GND	VCC	A8N	A9N	AORN	GND	GND	GND	GND	GND	GND	MIRefA	MIRefC	GND	GND	GND	GND	GND	GND	DORN	D9N	D8N	VCC	GND	B
A	GND	VCC	A8	A9	AOR	GND	AAI	AAIN	GND	BAI	BAIN	GND	GND	CAI	CAIN	GND	DAI	DAIN	GND	DOR	D9	D8	VCC	GND	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	

4.2. Pinout Table

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Power supplies				
GND	A1, A6, A9, A12, A13, A16, A19 A24, B1, B6, B7, B8, B9, B10, B11, B14, B15, B16, B17, B18, B19, B24, C4, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C21, D4, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D21, E8, E9, E10, E11, E12, E13, E14, E15, E16, E17, J5, J20, L5, L20, P5, P20, T5, T20, Y8, Y9, Y12, Y13, Y16, Y17, AA4, AA8, AA9, AA12, AA13, AA16, AA17, AA21, AB4, AB6, AB8, AB9, AB12, AB13, AB16, AB17, AB19, AB21, AC1, AC6, AC12, AC13, AC19, AC24, AD1, AD6, AD19, AD24 E4, E5, E20, E21, F4, F5, F20, F21, G5, G20, V5, V20, W4, W5, W20, W21, Y4, Y5, Y20, Y21, AC8, AD9	Ground All ground pin must be connect to a one solid ground plane on evaluation board Common ground (analog + digital)		
VCC	A2, A23, B2, B23, C3, C5, C6, C19, C20, C22, D3, D6, D7, D18, D19, D22, E7, E18, K5, K20, M5, M20, N5, N20, R5, R20, Y7, Y10, Y15, Y18, AA3, AA6, AA7, AA10, AA15, AA18, AA19, AA22, AB3, AB5, AB7, AB10, AB15, AB18, AB20, AB22, AC2, AC23, AD2, AD23 AA14, AB14, Y14 AC9	Analog + SPI pads power supply (3.3V)		
VCCD	Y11, AB11, AA11	Digital power supply (1.8V)		
VCCO	D5, D20, E3, E6, E19, E22, F3, F22, H5, H20, U5, U20, W3, W22, Y3, Y6, Y19, Y22, AA5, AA20	Output power supply (1.8V)		

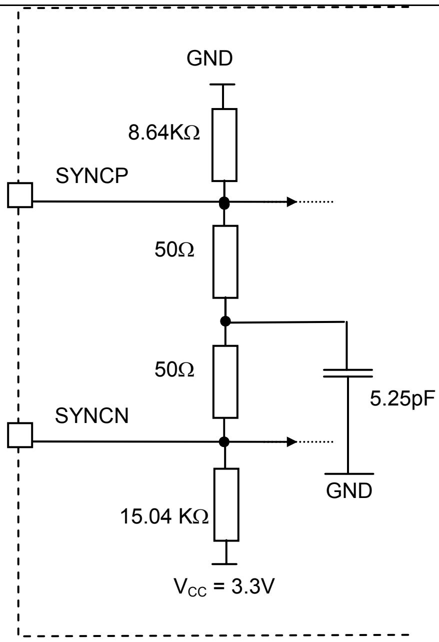
Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Clock signal				
CLK CLKN	AD12, AD13	In phase input clock signal and Out of phase input clock signal Master input clock (Sampling clock). This is a differential clock with internal common mode at 1.8V It should be driven in AC coupling Equivalent internal differential 100Ω input resistor	I	
Analog input signals				
AAI AAIN	A7 A8	In phase analog input channel A Out of phase analog input channel A	I	
BAI BAIN	A10 A11	In phase analog input channel B Out of phase analog input channel B	I	
CAI CAIN	A14 A15	In phase analog input channel C Out of phase analog input channel C	I	
DAI DAIN	A17 A18	In phase analog input channel D Out of phase analog input channel D	I	
XAI XAIN		In phase analog input channel X (X = A, B, C or D) Out of phase analog input channel X Analog input (differential) with internal common mode at 1.6V (CMIRefAB/CD signal) It should be driven in AC coupling or DC coupling with CMIREFAB/CD output signal XAI input is sampled and converted (10 bit) on each positive transition on the CLK Input Equivalent internal differential 100Ω input resistor	I	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Digital Output signals				
A0, A0N A1, A1N A2, A2N A3, A3N A4, A4N A5, A5N A6, A6N A7, A7N A8, A8N A9, A9N	M3, M4 L1, L2 L3, L4 K1, K2 K3, K4 J1, J2 J3, J4 H1, H2 A3, B3 A4, B4	Channel A in phase output data* A0 is the LSB, A9 is the MSB Channel A out of phase output data A0N is the LSB, A9N is the MSB This differential digital output data is transmitted at CLK/2 clock rate (1.25Gbps max). Each of these outputs should always be terminated by 100Ω differential resistor placed as close as possible to differential receiver Differential LVDS signal	O	
AOR AORN	A5 B5	Channel A output Out of range bit This differential output is asserted logic high while the over or under range condition exist for the channel A Each of these outputs should always be terminated by 100Ω differential resistor placed as close as possible to differential receiver Differential LVDS signal	O	
ADR ADRN	M1 M2	Channel A Output clock (Data Ready clock in DDR mode) This differential output clock is used to latch the output data on rising and falling edge. This differential digital output clock is at CLK/4 clock frequency (625MHz max). should always be terminated by 100Ω differential resistor placed as close as possible to differential receiver Differential LVDS signal	O	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
B0, B0N B1, B1N B2, B2N B3, B3N- B4, B4N B5, B5N B6, B6N B7, B7N B8, B8N B9, B9N	N3, N4 P1, P2 P3, P4 R1, R2 R3, R4 T1, T2 T3, T4 U1, U2 AD3, AC3 AD4 AC4	Channel B in phase output data B0 is the LSB, B9 is the MSB B0N is the LSB, B9N is the MSB This differential digital output data is transmitted at CLK/2 clock rate (1.25Gbps max). Each of these outputs should always be terminated by 100Ω differential resistor place as close as possible to differential receiver Differential LVDS signal	O	
BOR BORN	AD5 AC5	Channel B output Out of range bit This differential output is asserted logic high while the over or under range condition exist for the channel B Each of these outputs should always be terminated by 100Ω differential resistor placed as close as possible to differential receiver Differential LVDS signal	O	
BDR BDRN	N1 N2	Channel B Output clock This differential output clock is used to latch the output data on rising and falling edge. This differential digital output clock is at CLK/4 clock frequency (625MHz max). should always be terminated by 100Ω differential resistor placed as close as possible to differential receiver Differential LVDS signal	O	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
C0, C0N C1, C1N C2, C2N C3, C3N C4, C4N C5, C5N C6, C6N C7, C7N C8, C8N C9, C9N	N22, N21 P24, P23 P22, P21 R24, R23 R22, R21 T24, T23 T22, T21 U24, U23 AD22, AC22 AD21, AC21	Channel C in phase output data C0 is the LSB, C9 is the MSB C0N is the LSB, C9N is the MSB This differential digital output data is transmitted at CLK/2 clock rate (1.25Gbps max). Each of these outputs should always be terminated by 100Ω differential resistor placed as close as possible to differential receiver Differential LVDS signal	O	
COR CORN	AD20 AC20	Channel C output Out of range bit This differential output is asserted logic high while the over or under range condition exist for the channel C Each of these outputs should always be terminated by 100Ω differential resistor placed as close as possible to differential receiver Differential LVDS signal	O	
CDR CDRN	N24 N23	Channel C Output clock This differential output clock is used to latch the output data on rising and falling edge. This differential digital output clock is at CLK/4 clock frequency (625MHz max). should always be terminated by 100Ω differential resistor placed as close as possible to differential receiver Differential LVDS signal	O	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
D0, D0N D1, D1N D2, D2N D3, D3N D4, D4N D5, D5N D6, D6N D7, D7N D8, D8N D9, D9N	M22, M21 L24, L23 L22, L21 K24, K23 K22, K21 J24, J23 J22, J21 H24, H23 A22, B22 A21, B21	Channel D in phase output data D0 is the LSB, D9 is the MSB D0N is the LSB, D9N is the MSB This differential digital output data is transmitted at CLK/2 clock rate (1.25Gbps max). Each of these outputs should always be terminated by 100Ω differential resistor placed as close as possible to differential receiver Differential LVDS signal	O	
DOR DORN	A20 B20	Channel D output Out of range bit This differential output is asserted logic high while the over or under range condition exist for the channel D Each of these outputs should always be terminated by 100Ω differential resistor placed as close as possible to differential receiver Differential LVDS signal	O	
DDR DDRN	M24 M23	Channel D Output clock This differential output clock is used to latch the output data on rising and falling edge. This differential digital output clock is at CLK/4 clock frequency (625MHz max). should always be terminated by 100Ω differential resistor placed as close as possible to differential receiver Differential LVDS signal	O	
SPI signals				
csn	AC16	SPI signal (3.3V CMOS) Input Chip Select signal (Active low) When this signal is active low, sclk is used to clock data present on MOSI or MISO signal Refer to section 5.5 for more information	I	

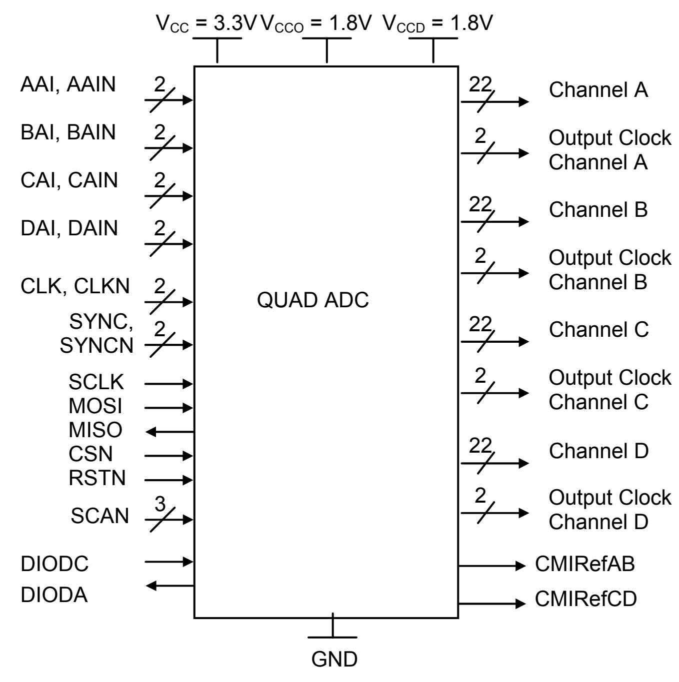
Pin Label	Pin number	Description	Direction	Simplified electrical schematics
sclk	AD16	SPI signal (3.3V CMOS) Input SPI serial Clock Serial data is shifted into and out SPI synchronously to this signal on positive transition of sclk Refer to section 5.5 for more information	I	
mosi	AD17	SPI signal (3.3V CMOS) Data SPI Input signal (Master Out Slave In) Serial data input is shifted into SPI while sldn is active low Refer to section 5.5 for more information	I	
miso	AC17	SPI signal (3.3V CMOS) Data output SPI signal (Master In Slave Out) Serial data output is shifted out SPI while sldn is active low Refer to section 5.5 for more information	O	
rstn	AC15	SPI signal (3.3V CMOS) Input Digital asynchronous SPI reset (Active low) This signal allows to reset the internal value of SPI to their default value Refer to section 5.5 for more information	I	
Other signals				
scan0 scan1 scan2	AD14 AC14 AD15	Scan mode signals (Used for internal purpose) Pull up to V_{CC}		
SYNCN SYNCP	AC11 AD11	Differential Input Synchronization signal (LVDS) Active high signal This signal is used to synchronies external ADC, Refer to section 8.5 for more information Equivalent internal differential 100Ω input resistor	I	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Res50 Res62	AD18 AC18	50Ω and 62Ω reference resistor input Refer to section 5.4 for more information		
CMIRefAB CMIRefCD	B12 B13	Output voltage reference for Channel A-B and C-D Input Common mode In AC coupling operation this output could be left floating (not used) In DC coupling operation, this pins provides an output voltage witch is the common mode voltage for the analog input signal and should be used to set the common mode voltage of the input driving buffer. CMIRefAB for A and B channel CMIRefCD for C and D channel	O	
DiodA DiodC	AD7 AC7	Input Temperature diode Anode Input Temperature diode Cathode Refer to section 5.3 for more information	I O	
NC	C1, C2, C23, C24, D1, D2, D23, D24, E1, E2, E23, E24, F1, F2, F23, F24, G1, G2, G3, G4, G21, G22, G23, G24, H3, H4, H21, H22, U3, U4, U21, U22, V1, V2, V3, V4, V21, V22, V23, V24, W1, W2, W23, W24, Y1, Y2, Y23, Y24, AA1, AA2, AA23, AA24, AB1, AB2, AB23, AB24, AD10, AD8, AC10	Reserved pins DO NOT CONNECT		

5 Theory Of Operation

5.1. Overview

Table 9. Functional Description



Name	Function		
V_{CC}	3.3V Power Supply (analog core + SPI Pads)		
V_{CCO}	1.8V Output Power Supply		
V_{CCD}	1.8V Digital Power Supply		
GND	Ground		
AAI, AAIN	Channel A Differential Analog Input		
BAI, BAIN	Channel B Differential Analog Input		
CAI, CAIN	Channel C Differential Analog Input		
DAI, DAIN	Channel D Differential Analog Input		
CLK,CLKN	Differential Clock Input		
[A0:A9] [A0N:A9N]	Channel A Differential Output Data		
[B0:B9] [B0N:B9N]	Channel B Differential Output Data		
[C0:C9] [C0N:C9N]	Channel C Differential Output Data		
[D0:D9] [D0N:D9N]	Channel D Differential Output Data		
AOR, AORN	Channel A Differential Output Out of Range Data		
BOR, BORN	Channel B Out of Range Data Differential Output	CSN	Chip Select Input (Active Low)
COR, CORN	Channel C Out of Range Data Differential Output	RSTN	SPI Asynchronous Reset Input (Active Low)
DOR, DORN	Channel D Out of Range Data Differential Output	SCAN[2:0]	Digital Scan Mode Signals
ADR, ADRN	Channel A Data Ready Differential Output Clock	DIOD1A	Diode Anode Input for die junction temperature monitoring
BDR, BDRN	Channel B Data Ready Differential Output Clock	DIOD1C	Diode Cathode Input for die junction temperature monitoring
CDR, CDRN	Channel C Data Ready Differential Output Clock	Res50	50Ω reference input resistor
DDR, DDRN	Channel D Data Ready Differential Output Clock	Res62	62Ω reference input resistor
SYNCP, SYNCN	Synchronization of Data Ready (LVDS input)	CMIRefAB	Output voltage Reference for Input common Mode reference Channels A and B
SCLK	SPI Input Clock	CMIRefCD	Output voltage Reference for Input common Mode reference Channels C and D
MISO	SPI Output Data (Master In Slave Out)		
MOSI	SPI input Data (Master Out Slave In)		

5.2. ADC Synchronization Signal (SYNCP, SYNCN)

The SYNCP, SYNCN signal has LVDS electrical characteristics. It is active high and should last at least 2 clock cycles to work properly.

Once asserted, it has an effect on the output clock signals which are then forced to LVDS low level as described in. During reset, the output data are not refreshed.

Once de-asserted, the output clock signals restart toggling after (TDR + pipeline delay) + Y clock cycles, where Y can be selected via the SPI at address 0x06 (from 0 to 15). This SYNC signal can be used to ensure the synchronization of multiple ADCs.

The SYNCN, SYNCP signal is mandatory whenever the following ADC modes are changed: Standby, DMUX mode, Test mode (see note 1), Channel mode.
For all other ADC modes there is no need to perform a SYNCN, SYNCP.
Examples:

The SYNCN, SYNCP signal is mandatory after power up or power configuration: when switching the ADC from standby (full or partial) to normal mode

The SYNCN, SYNCP signal is mandatory after channel mode configuration: when switching the ADC from 4-channel mode to 1-channel mode

The SYNCN, SYNCP signal is mandatory after test sequence: when switching the ADC from normal running mode to ramp or flashing mode but it is no needed when the ADC is switched from test mode (ramp or flashing) to normal running mode.

Notes: 1. SYNC is not needed from Test mode to normal mode

2. Refer to Figure 11

5.3. Digital Scan Mode (SCAN[2:0])

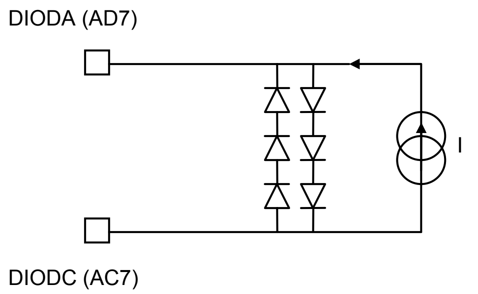
These signals allow to perform a scan of the digital part of the ADC.
FOR e2v USE ONLY.
Pull up to V_{CC}.

5.4. Die Junction Temperature Monitoring Diode

DIODA, DIODC: two pins are provided so that the diode can be probed using standard temperature sensors from the market.

It is recommended to protect the diode using 2 x 3 head-to-tail diodes as illustrated in Figure 12 (note that if a standard temperature sensor is used, the protection diodes are not necessary).

Figure 12 Protection diodes for the junction temperature monitoring diode



Note: If the diode function is not used, DIODA and DIODC can be left unconnected (open).

5.5. Res50 and Res62

The Res50 and Res62 correspond to the input of internal 50 Ω and 62 Ω reference resistors that are used to check the process deviation.
The idea is to inject a current into pin Res50, measure the voltage across Res50 and nearest ground pin (AD19), same process should be used for Res62.
You then have 2 equations with 2 unknown parameters:
Res50 = k x 50 + e1
Res62 = k x 62 + e2
- where k is due to the process
- where e1 and e2 are due to the measurement errors.

Assuming that e1 = e2 since the same process is used to measure both Res50 and Res62 in the same conditions, you can obtain the k factor by working out this equation, which helps you determine if you need to compensate for the process by increasing or decreasing the resistors value (TRIMMER register at address 0x13) of the input resistors (there are two 50 Ω resistors per analog input channel).

Note: If the Res50, Res62 function is not used, Res50 and Res62 can be left unconnected (open).

5.6. QUAD ADC Digital Interface (SPI)

The digital interface will be a standard SPI (3.3V CMOS pads, 1.8V core) with:
- 8 bits for the address A[7] to A[0] including a R/W bit (A[7] = R/W and is the MSB);
- 16 bits of data D[15] to D[0] with D[15] the MSB.

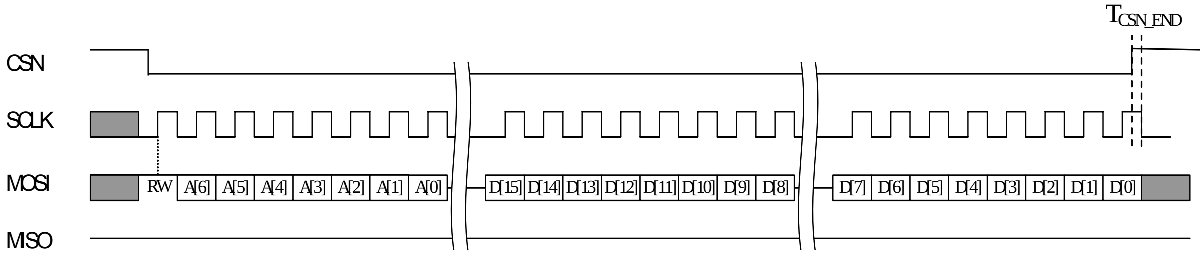
5 signals are required:
- RSTN for the SPI reset;
- SCLK for the SPI clock;
- CSN for the Chip Select;
- MISO for the Master In Slave Our SPI Output;
- MOSI for the Master Out Slave In SPI Input.

The MOSI sequence should start with one R/W bit:

- R/W = 0 is a read procedure
- R/W = 1 is a write procedure

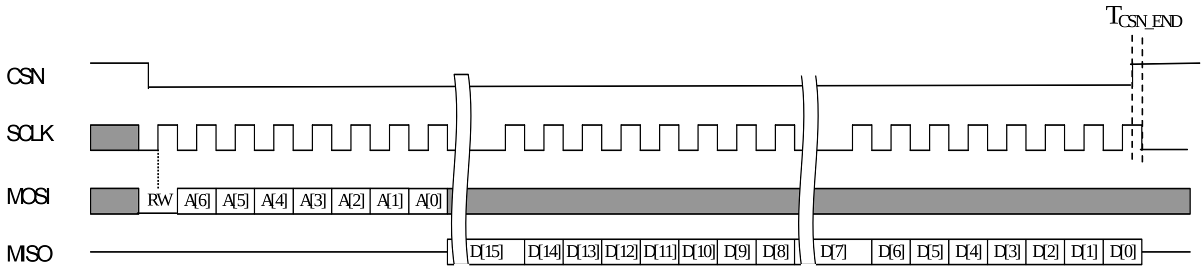
5.6.1. TIMINGS

Register Write to a 16-bit register:



Note: Last falling edge of sclk should occur only once csn is back to high level at the end of the write procedure.

Register Read from a 16-bit register:



$T_{CSN\_END} = T_{SCLK}/4 = 12.5$ ns (see note 3)

Table 10. Timing characteristics

Pin	Max Frequency	Setup (see note 1)	Hold (see note 1)
SCLK	20 MHz		
CSN (to SCLK) (see note 2)		0.5 ns/1 ns	0.5 ns/1 ns
MOSI (to SCLK)		0.5 ns/1.2 ns	0.5 ns/1.0 ns
MISO (to SCLK)		1.5 ns/4 ns	1.7 ns/3.5 ns

Notes:
1. 1st value is in Min Conditions, 2nd value is in Max Conditions.
2. Setup/Hold to both SCLK edges.
3. Last falling edge of sclk should occur once csn is set to 1, due to an internal operation.

5.6.2. Digital Reset (RSTN)

This is a global Reset for the SPI.
It is active Low.

There are 2 ways to reset the Quad 10-bit 1.25 Gsps ADC:

- by asserting low the RSTN primary pad (hardware reset)
- by writing a '1' in the bit SWRESET of the SWRESET register through the SPI (software reset)

Both ways will clear ALL configuration registers to their reset values.

5.6.3. Registers description

Table 11. Registers Mapping

Address	Label	Description	R/W	Default Setting
Common Registers				
0x00	Chip ID	Chip ID and version	Read Only	0x0414 0x0418 (latest)
0x01	Control Register	ADC mode (channel mode) Standby Binary/gray Test Mode ON/OFF Bandwidth Selection	R/W	4-channel mode (1.25 Gsps) No standby Binary coding Test mode OFF Nominal bandwidth
0x02	STATUS	Status register	Read Only	
0x04	SWRESET	Software SPI reset	R/W	No reset
0x05	TEST	Test Mode	R/W	Test Pattern = ramp
0x06	SYNC	Programmable delay on ADC Data ready after Reset XDR, XDRN (4 bits), with X = A, B, C, D	R/W	0 extra clock cycle
0x0F	Channel Select	Channel X Selection	R/W	0x0000
Per Channel Registers (X=A/B/C/D)				
0x10	Cal Ctrl X	Calibration control register of Channel X	R/W	
0x11	Cal Ctrl X Mlbx	Status/Busy of current Calibration of Channel X	Read Only (poll)	
0x12	Status X	Global Status of Channel X	Read Only	
0x13	Trimmer X	Impedance Trimmer of Channel X	R/W	0x07
0x20	Ext Offset X	External Offset Adjustment of Channel X	R/W	0 LSB
0x21	Offset X	Offset Adjustment of Channel X	Read Only	0 LSB
0x22	Ext Gain X	External Gain Adjustment of Channel X	R/W	0 dB
0x23	Gain X	Gain Adjustment of Channel X	Read Only	0 dB
0x24	Ext Phase X	External Phase Adjustment of Channel X	R/W	0 ps
0x25	Phase X	Phase Adjustment of Channel X	Read Only	0 ps

Notes 1. ALL registers are 16-bits long.
2. The “external” gain/offset/phase adjustment registers correspond to the registers where one can write the external values to calibrate the gain/offset/phase parameters of the ADCs. The Gain/offset/phase adjustment registers are read only registers. They provide you with the internal settings for the gain/offset/phase parameters. The “external” and read only adjustment registers should give the same results two by two once any calibration has been performed.

5.6.4. Chip ID Register (Read Only)

Table 12. Chip ID Register Mapping: address 0x00

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TYPE								BRANCH<3:0>				VERSION<3:0>			

Table 13. Chip ID Register Description

Bit label	Value	Description	Default Setting
VERSION <3:0>	0100	Version Number	See Note
BRANCH<3:0>	0001	Branch Number	
TYPE<7:0>	00001000	Chip Type	

Note: 0x0414 = alpha Silicon, 0x0418 = beta Silicon

5.6.5. Control Register

Table 14. Control Register Mapping: address 0x01

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused<1:0>		0	TEST	0	Unused	Unused	BDW	B/G	Unused	STDBY <1:0>		ADCMODE <3:0>			

Table 15. Control Register Description

Bit label	Value	Description	Default Setting
ADCMODE <3:0>	00XX	4 Channels mode (1.25 Gsps per channel)	0000 4-channels Mode
	0100	2 Channels mode (channel A and channel C, 2.5 Gsps per channel)	
	0101	2 Channels mode (channel B and channel C, 2.5 Gsps per channel)	
	0110	2 Channels mode (channel A and channel D, 2.5 Gsps per channel)	
	0111	2 Channels mode (channel B and channel D, 2.5 Gsps per channel)	
	1000	1 Channel mode (channel A, 5 Gsps)	
	1001	1 Channel mode (channel B, 5 Gsps)	
	1010	1 Channel mode (channel C, 5 Gsps)	
	1011	1 Channel mode (channel D, 5 Gsps)	
	1100	Common input mode, simultaneous sampling (channel A)	
	1101	Common input mode, simultaneous sampling (channel B)	
	1110	Common input mode, simultaneous sampling (channel C)	
	1111	Common input mode, simultaneous sampling (channel D)	
STDBY <1:0>	00	Full Active Mode	00 **Full Active Mode**
	01	Standby channel A/channel B: • if 4-channels mode selected → standby of channel A and B • if 2-channel mode selected → standby of channel A or B • if 1-channel mode selected → full standby • if Common input mode selected → full standby	
	10	Standby channel C/channel D ▪ if 4-channels mode selected → standby of channel C and D ▪ if 2-channels mode selected → standby of channel C or D ▪ if 1-channel mode selected → full standby ▪ if Common input mode selected → full standby	
	11	Full Standby	
B/G	0	Binary	0 Binary Coding
	1	Gray	
BDW	0	Nominal bandwidth (1 GHz typical)	0 Nominal bandwidth
	1	Full bandwidth	
TEST	0	No Test Mode	0 No Test Mode
	1	Test Mode Activated, Refer to the Test register	

Table 16. Control Register Settings (address 0x01): Bit7 to Bit0

Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Label	**B/G**	**Unused**	**STDBY <1:0>**		**ADCMODE <3:0>**			
4-channels mode 1.25 Gsps max per channel	X	X	X	X	**0**	**0**	**X**	**X**

Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Label	**B/G**	**Unused**	**STDBY <1:0>**		**ADCMODE <3:0>**			
2-channels mode (channel A and channel C) 2.5 Gsps max per channel	X	X	X	X	**0**	**1**	**0**	**0**
2-channels mode (channel B and channel C) 2.5 Gsps max per channel	X	X	X	X	**0**	**1**	**0**	**1**
2-channels mode (channel A and channel D) 2.5 Gsps max per channel	X	X	X	X	**0**	**1**	**1**	**0**
2-channels mode (channel B and channel D) 2.5 Gsps max per channel	X	X	X	X	**0**	**1**	**1**	**1**
1-channel mode (Channel A, 5 Gsps max)	X	X	X	X	**1**	**0**	**0**	**0**
1-channel mode (Channel B, 5 Gsps)	X	X	X	X	**1**	**0**	**0**	**1**
1-channel mode (Channel C, 5 Gsps)	X	X	X	X	**1**	**0**	**1**	**0**
1-channel mode (Channel D, 5 Gsps)	X	X	X	X	**1**	**0**	**1**	**1**
Common input mode, simultaneous sampling 1.25Gsps max (channel A)	X	X	X	X	**1**	**1**	**0**	**0**
Common input mode, simultaneous sampling 1.25Gsps max (channel B)	X	X	X	X	**1**	**1**	**0**	**1**
Common input mode, simultaneous sampling 1.25Gsps max (channel C)	X	X	X	X	**1**	**1**	**1**	**0**
Common input mode, simultaneous sampling 1.25Gsps max (channel D)	X	X	X	X	**1**	**1**	**1**	**1**
No standby	X	X	**0**	**0**	X	X	X	X
Standby channel A, channel B	X	X	**0**	**1**	X	X	X	X
Standby channel C, channel D	X	X	**1**	**0**	X	X	X	X
Full Standby	X	X	**1**	**1**	X	X	X	X
Binary Coding	**0**	X	X	X	X	X	X	X
Gray Coding	**1**	X	X	X	X	X	X	X

Table 17. Control Register Settings (address 0x01): Bit15 to Bit8

Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Label	**Unused<1:0>**		**Reserved**	**TEST**	**Reserved**	**Unused**	**Unused**	**BDW**
Nominal bandwidth	X	X	**0**	X	**0**	X	X	**0**
Full bandwidth	X	X	**0**	X	**0**	X	X	**1**
Test Mode OFF	X	X	**0**	0	**0**	X	X	X
Test Mode ON	X	X	**0**	**1**	**0**	X	X	X

Note: 1. It is mandatory to apply a SYNCP, SYNCN signal to the ADC when the Test Mode is activated.

Table 18. ADCMODE and STBY allowed combinations

Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Label	**B/G**	**Unused**	**STDBY <1:0>**		**ADCMODE <3:0>**			
4-channels mode, 1.25Gsps max No standby	X	X	**0**	**0**	**0**	**0**	X	X
4-channels mode,1.25Gsps max Standby channel A, channel B	X	X	**0**	**1**	**0**	**0**	X	X
4-channels mode, 1.25Gsps max Standby channel C, channel D	X	X	**1**	**0**	**0**	**0**	X	X
4-channels mode (1.25Gsps max) Full Standby	X	X	**1**	**1**	**0**	**0**	X	X
2-channels mode, 2.5Gsps max (Channels A and C) No Standby	X	X	**0**	**0**	**0**	**1**	**0**	**0**

Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Label	**B/G**	**Unused**	**STDBY <1:0>**		**ADCMODE <3:0>**			
2-channels mode, 2.5Gsps max (Channels A and C) Standby channel A	X	X	**0**	**1**	**0**	**1**	**0**	**0**
2-channels mode, 2.5Gsps max (Channels A and C) Standby Channel C	X	X	**1**	**0**	**0**	**1**	**0**	**0**
2-channels mode, 2.5Gsps max (Channels A and C) Full Standby	X	X	**1**	**1**	**0**	**1**	**0**	**0**
2-channels mode, 2.5Gsps max (Channels B and C) No Standby	X	X	**0**	**0**	**0**	**1**	**0**	**1**
2-channels mode, 2.5Gsps max (Channels B and C) Standby Channel B	X	X	**0**	**1**	**0**	**1**	**0**	**1**
2-channels mode, 2.5Gsps max (Channels B and C) Standby Channel C	X	X	**1**	**0**	**0**	**1**	**0**	**1**
2-channels mode, 2.5Gsps max (Channels B and C) Full Standby	X	X	**1**	**1**	**0**	**1**	**0**	**1**
2-channels mode, 2.5Gsps max (Channel A and D) No Standby	X	X	**0**	**0**	**0**	**1**	**1**	**0**
2-channels mode, 2.5Gsps max (Channels A and D) Standby Channel A	X	X	**0**	**1**	**0**	**1**	**1**	**0**
2-channels mode, 2.5Gsps max (Channels A and D) Standby Channel D	X	X	**1**	**0**	**0**	**1**	**1**	**0**
2-channels mode, 2.5Gsps max (Channels A and D) Full Standby	X	X	**1**	**1**	**0**	**1**	**1**	**0**
2-channels mode, 2.5Gsps max (Channels B and D) No Standby	X	X	**0**	**0**	**0**	**1**	**1**	**1**
2-channels mode, 2.5Gsps max (Channels B and D) Standby Channel B	X	X	**0**	**1**	**0**	**1**	**1**	**1**
2-channels mode, 2.5Gsps max (channels B and D) Standby Channel D	X	X	**1**	**0**	**0**	**1**	**1**	**1**
2-channels mode, 2.5Gsps max (channels B and D) Full Standby	X	X	**1**	**1**	**0**	**1**	**1**	**1**
1-channel mode (Channel A, 5 Gsps max) No Standby	X	X	**0**	**0**	**1**	**0**	**0**	**0**
1-channel mode (Channel B, 5 Gsps max) No Standby	X	X	**0**	**0**	**1**	**0**	**0**	**1**
1-channel mode (Channel C, 5 Gsps max) No Standby	X	X	**0**	**0**	**1**	**0**	**1**	**0**
1-channel mode (Channel D, 5 Gsps) No Standby	X	X	**0**	**0**	**1**	**0**	**1**	**1**
1-channel mode (Channel A, 5 Gsps) Full Standby	X	X	**01 or 10 or 11**		**1**	**0**	**0**	**0**
1-channel mode (Channel B, 5 Gsps) Full Standby	X	X	**01 or 10 or 11**		**1**	**0**	**0**	**1**
1-channel mode (Channel C, 5 Gsps) Full Standby	X	X	**01 or 10 or 11**		**1**	**0**	**1**	**0**
1-channel mode (Channel D, 5 Gsps) Full Standby	X	X	**01 or 10 or 11**		**1**	**0**	**1**	**1**
Common input mode (Channel A, 1.25Gsps) No Standby	X	X	**0**	**0**	**1**	**1**	**0**	**0**
Common input mode (Channel B, 1.25Gsps) No Standby	X	X	**0**	**0**	**1**	**1**	**0**	**1**
Common input mode (Channel C, 1.25Gsps) No Standby	X	X	**0**	**0**	**1**	**1**	**1**	**0**
Common input mode (Channel D, 1.25Gsps) No Standby	X	X	**0**	**0**	**1**	**1**	**1**	**1**
Common input mode (Channel A , 1.25Gsps) Full standby	X	X	01 or 10 or 11		**1**	**1**	**0**	**0**
Common input mode (Channel B , 1.25Gsps) Full standby	X	X	01 or 10 or 11		**1**	**1**	**0**	**1**
Common input mode (Channel C , 1.25Gsps) Full standby	X	X	01 or 10 or 11		**1**	**1**	**1**	**0**
Common input mode (Channel D , 1.25Gsps) Full standby	X	X	01 or 10 or 11		**1**	**1**	**1**	**1**

5.6.6. STATUS Register (Read Only)

Table 19. STATUS Register Mapping: address 0x02

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused												**ADCXUP<3:0>**			

Table 20. STATUS Register Description

Bit label	Value	Description	Default Setting
ADCXUP<3:0>	XXX0	ADC A standby	1111
	XXX1	ADC A active	
	XX0X	ADC B standby	
	XX1X	ADC B active	
	X0XX	ADC C standby	
	X1XX	ADC C active	
	0XXX	ADC D standby	
	1XXX	ADC D active	

5.6.7. SWRESET Register

Table 21. SWRESET Register Mapping: address 0x04

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused															**SWRESET**

Table 22. SWRESET Register Description

Bit label	Value	Description	Default Setting
SWRESET	0	No Software Reset	0 No software reset
	1	Unconditional Software Reset (see Note)	

Note: Global Software Reset will reset ALL design registers (configuration registers as well as any flip-flop in the digital part of the design). This bit is automatically reset to 0 after some ns. There is no need to clear it by an external access.

5.6.8. TEST Register

Table 23. TEST Register Mapping: address 0x05

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused									**Unused**		**"00"**		**FlashM**		**TEST M**

Table 24. TEST Register Description (Chip ID 0x414)

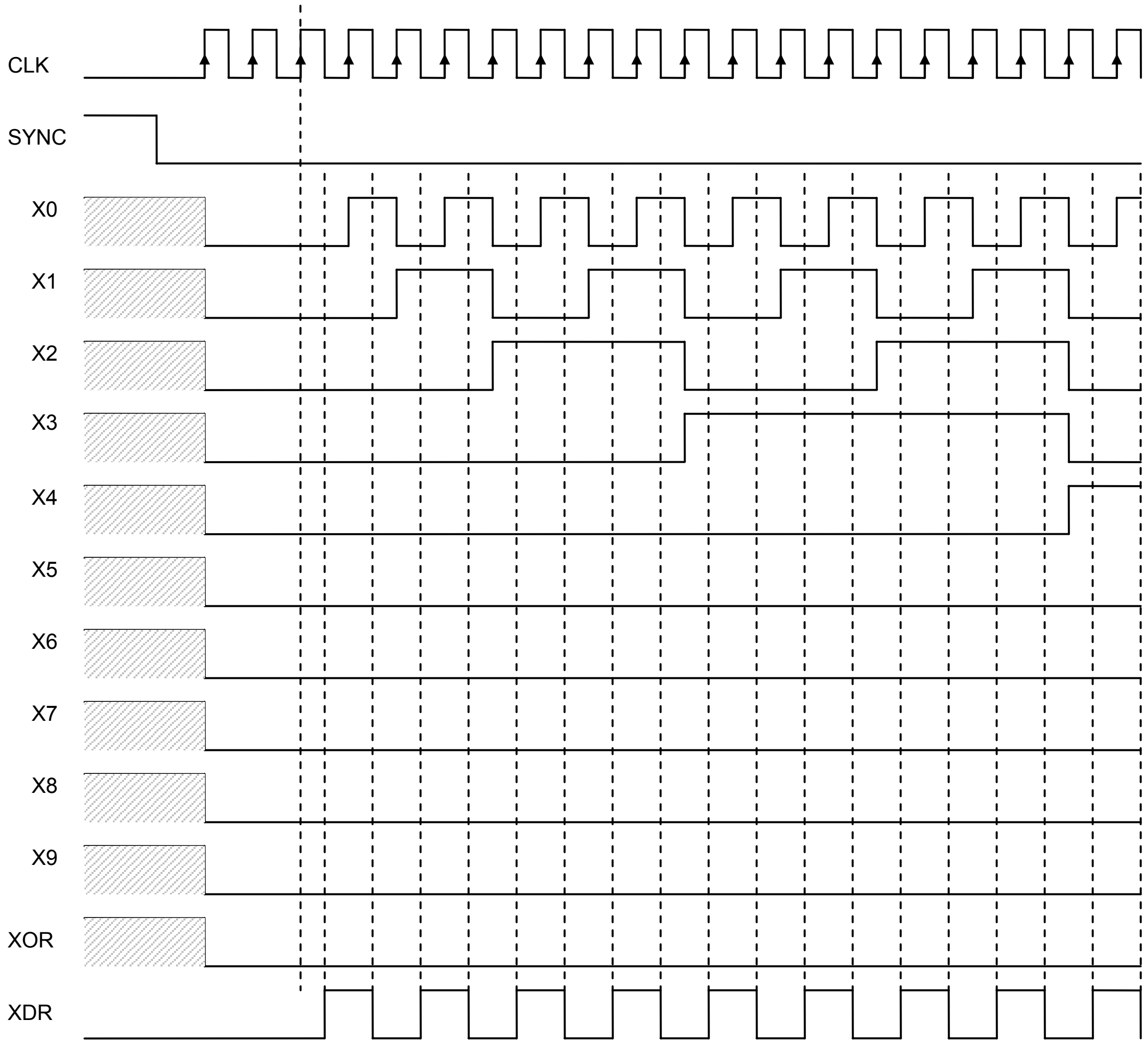
Bit label	Value	Description	Default Setting
TESTM	0	Increasing (simultaneous) ramp	0 Increasing ramp
	1	Flashing 1 (7 FF pattern every ten 00 patterns) on each ADC	

Table 25. TEST Register Description (Chip ID 0x418)

Bit label	Value	Description	Default Setting
TESTM	0	Increasing (simultaneous) ramp 11bit (0 up to 2047) see note 5	0 Increasing ramp
	1	Flashing mode (refer to Bit 1 and Bit 2 to select the flashing 1 period)	
FlashM	00	Flashing “11” mode = 1 (7 FF pattern every **ten** 00 patterns) on each ADC	00 Flashing “11” mode
	01	Flashing “12” mode = 1 (7 FF pattern every **eleven** 00 patterns) on each ADC	
	10	Flashing “16” mode = 1 (7 FF pattern every **fifteen** 00 patterns) on each ADC	

Notes 1: TESTM is taken into account only if bit12 (TEST) of Control register (address 0x01) is at 1.
2. It is mandatory to apply a SYNCP, SYNCN signal to the ADC when the Test Mode is activated.
3. When Bit 0 is set to 1, it is necessary to choose the flashing “1” period (11, 12 or 16) using Bit 1 and Bit 2. The default flashing mode is the one with 11 period.
4. Flashing mode 7FF pattern on 11bit (Out of rage bit + data 10bit)
5. Ramp mode: 11 bit (Out of range bit + data 10bit)

Figure 13 Ramp mode



Notes: 1. X = A, B, C or D

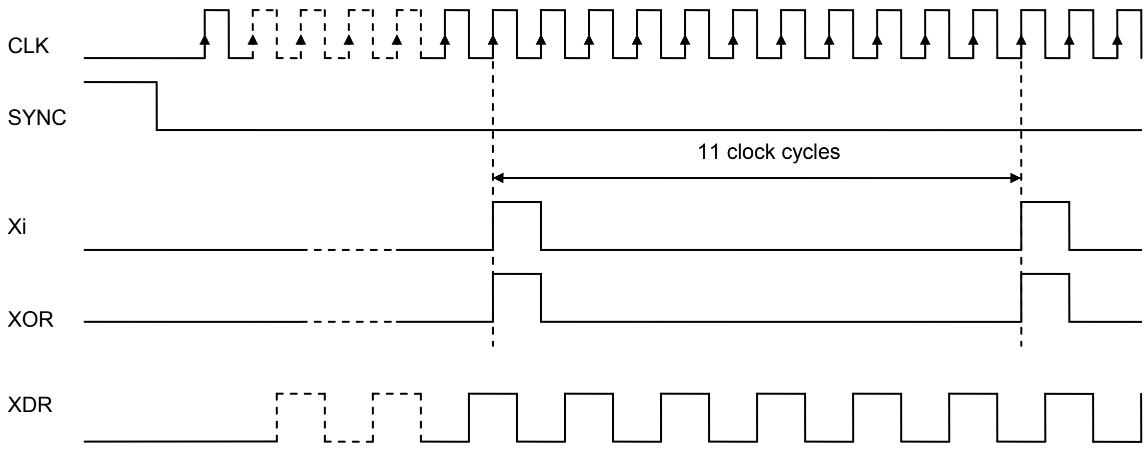
2. When the ramp Test mode is activated and during reset, the outputs stay at the value before reset. After reset, the ramp starts either with code “0” or code “256” depending on the clock frequency. After reset, the first 3 to 4 clock pulses may not be correct depending on the clock frequency.

Table 26. Ramp mode coding (binary counting)

XOR	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	1	0	1
…										
1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0	0	0

Note: X = A, B, C or D

Figure 14 Flashing mode (“11” mode)



Notes: 1. X = A, B, C or D
2. i = 0, 1, 2 …, 8, 9
3. In flashing “12” and “16” modes, 11 clock cycles becomes 12 and 16 respectively.

Table 27. Flashing mode coding (“11” mode))

Cycle	XOR	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
N	1	1	1	1	1	1	1	1	1	1	1
N+1	0	0	0	0	0	0	0	0	0	0	0
N+2	0	0	0	0	0	0	0	0	0	0	0
N+3	0	0	0	0	0	0	0	0	0	0	0
N+4	0	0	0	0	0	0	0	0	0	0	0
N+5	0	0	0	0	0	0	0	0	0	0	0
N+6	0	0	0	0	0	0	0	0	0	0	0
N+7	0	0	0	0	0	0	0	0	0	0	0
N+8	0	0	0	0	0	0	0	0	0	0	0
N+9	0	0	0	0	0	0	0	0	0	0	0
N+10	0	0	0	0	0	0	0	0	0	0	0
N+11	1	1	1	1	1	1	1	1	1	1	1
N+12	0	0	0	0	0	0	0	0	0	0	0

Note: X = A, B, C or D

5.6.9. SYNC Register Mapping

Table 28. SYNC Register Mapping: address 0x06

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused												**SYNC<3:0>**			

Table 29. SYNC Register Description

Bit label	Value	Description	Default Setting
SYNC<3:0>	0000	0 extra clock cycle before starting up	0000 0 Clock Cycle
	0001	1 extra clock cycle before starting up	
	…	…	
	1111	15 extra clock cycles before starting up	

5.6.10. CHANNEL SELECTOR Register

Table 30. CHANNEL SELECTOR Register Mapping: address 0x0F

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused													**Channel Selector <2:0>**		

Table 31. CHANNEL SELECTOR Register Description

Bit label	Value	Description	Default Setting
Channel Selector <2:0>	000	No channel selected (only common registers are accessible)	000 No channel selected
	001	Channel A selected to access to “per-channel” registers	
	010	Channel B selected to access to “per-channel” registers	
	011	Channel C selected to access to “per-channel” registers	
	100	Channel D selected to access to “per-channel” registers	
	Any others	No channel selected (only common registers are accessible)	

Note : The CHANNEL SELECTOR register has to be set before any access to “per-channel” registers in order to determine which channel is targeted.

5.6.11. CAL Control Registers

Applies to CAL Control registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 32. CAL Control Register Mapping: address 0x10

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused								**PCALCTRL X <1:0>**		**GCALCTRL X <1:0>**		**OCALCTRL X <1:0>**		**“00”**	

Table 33. CAL Control Register Description

Bit label	Value	Description	Default Setting
OCALCTRL X <1:0>	00	Idle mode for selected channel	00
	01	Idle mode for selected channel	
	10	External Offset adjust for selected channel (transfer of Ext Offset register content into current Offset register)	

Bit label	Value	Description	Default Setting
	11	Idle mode for selected channel	
GCALCTRL X <1:0>	00	Idle mode for selected channel	00
	01	Idle mode for selected channel	
	10	External Gain adjust for selected channel (transfer of Ext Gain register content into current Gain register)	
	11	Idle mode for selected channel	
PCALCTRL X <1:0>	00	Idle mode for selected channel	00
	01	Idle mode for selected channel	
	10	External Phase adjust for selected channel (transfer of Ext Phase register content into current Phase register)	
	11	Idle mode for selected channel	

Notes 1: Writing to the register will start the corresponding operation(s). In that case, the Status/Busy bit of the mailbox (see below) is asserted until the operation is over. (At the end of a calibration/tuning process, CAL Control register relevant bit slice is NOT reset to default value.)

2. If different calibrations are ordered, they are performed successively following the priority order defined hereafter.

- Gain has priority over Offset, and Phase
- Offset has priority over Phase.

Indeed, the transfer function of the ADC is given by the following formula transfer function result = offset + (input*gain).

5.6.12. CAL Control Registers Mailbox (Read Only)

Applies to CAL Control Registers Mailbox A, B, C and D according to CHANNEL SELECTOR register contents.

Table 34. CAL Control Registers Mailbox Register Mapping: address 0x11

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused<12:0>															STATUS/ BUSY X

5.6.13. GLOBAL STATUS Register (Read Only)

Applies to GLOBAL STATUS registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 35. GLOBAL STATUS Register Mapping: address 0x12

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused															STBY X

Table 36. GLOBAL STATUS Register Description

Bit label	Value	Description	Default Setting
STBY X	0	Selected Channel is in standby	0
	1	Selected Channel is active	

5.6.14. TRIMMER Register

Applies to TRIMMER registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 37. TRIMMER Register Mapping: address 0x13

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused												**TRIMMER X <3:0>**			

Table 38. TRIMMER Register Description

Bit label	Value	Description	Default Setting
TRIMMER X <3:0>	0000	+10.00 Ω	0111 50Ω
	0001	+8.34 Ω	
	0010	+6.77 Ω	
	0011	+5.29 Ω	
	0100	+3.89 Ω	
	0101	+2.57 Ω	
	0110	+1.31 Ω	
	0111	+0.11 Ω	
	1000	-1.03 Ω	
	1001	-2.12 Ω	
	1010	-3.15 Ω	
	1011	-4.14 Ω	
	1100	-5.09 Ω	
	1101	-5.99 Ω	
	1110	-6.86 Ω	
	1111	-7.69 Ω	

Note: R = 3 + (114 / [2 + 0.06 x (8 x bit3 + 4 x bit2 + 2 x bit1 + 1 x bit0)]) – the practical results (simulated) are not exactly the ones given above.

Refer to section 5.5 for more information.

5.6.15. External Offset Registers

Apply to External Offset Registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 39. External Offset Control Register Mapping: address 0x20

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						**EXTERNAL OFFSET X <9:0>** (See Notes)									

Table 40. External Offset Control Register Description

Bit label	Value	Description	Default Setting
EXTERNAL OFFSET X<9:0>	0x000	Maximum positive offset applied	0x200 0 LSB Offset
	0x1FF	Minimum positive offset applied	
	0x200	Minimum negative offset applied	
	0x3FF	Maximum negative offset applied	

Notes 1: Offset variation range: ~+/- 40 mV, 1024 steps (1 step ~0.08 mV ~0.15 LSB).
2: Current offset of the selected channel is controlled by the External Offset Control Register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.
3: The transfer function of the ADC is given by the following formula transfer function result = offset + (input*gain).

5.6.16. Offset Registers (Read Only)

Apply to Offset Registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 41. Offset Control Register Mapping: address 0x21

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						**OFFSET X <9:0>** (See Notes)									

Table 42. Offset Control Register Description

Bit label	Value	Description	Default Setting
OFFSET X <9:0>	0x000	Maximum positive offset applied	0x200 0 LSB Offset
	0x1FF	Minimum positive offset applied	
	0x200	Minimum negative offset applied	
	0x3FF	Maximum negative offset applied	

Notes 1: Offset variation range: ~+/- 40 mV, 1024 steps (1 step ~0.08 mV ~0.15 LSB).
2: Current offset of the selected channel is controlled by the External Offset Control Register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.
3: The transfer function of the ADC is given by the following formula transfer function result = offset + (input*gain).

5.6.17. External Gain Control Registers

Apply to External Gain Control registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 43. External Gain Control Register Mapping: address 0x22

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						**EXTERNAL GAIN X <9:0>** (See Notes)									

Table 44. External Gain Control Register Description

Bit label	Value	Description	Default Setting
EXTERNAL GAIN X <9:0>	0x000	Gain shrunk to min accessible value	0x200 0 dB gain
	0x200	Gain at Default value (no correction, actual gain follow process scattering)	
	…..		
	0x3FF	Gain Increased to max accessible value	

Notes 1: Gain variation range: ~+/-10%, 1024 steps (1 step ~0.02%).
2: Current gain of the selected channel is controlled by the External Gain Control Register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.
3: The transfer function of the ADC is given by the following formula transfer function result = offset + (input*gain).

5.6.18. Gain Control Registers (Read Only)

Apply to Gain Control registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 45. Gain Control Register Mapping: address 0x23

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						**GAIN X <9:0>** (See Notes)									

Table 46. Gain Control Register Description

Bit label	Value	Description	Default Setting
GAIN X <9:0>	0x000	Gain shrunk to min accessible value	0x200 0 dB gain
	0x200	Gain at Default value (no correction, actual gain follow process scattering)	
	…..		
	0x3FF	Gain Increased to max accessible value	

Notes 1: Gain variation range: ~+/-10%, 1024 steps (1 step ~0.02%).
2: Current gain of the selected channel is controlled by the External Gain Control Register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.
3: The transfer function of the ADC is given by the following formula transfer function result = offset + (input*gain).

5.6.19. External Phase Registers

Apply to Phase Registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 47. External Phase Register Mapping: address 0x24

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						**EXTERNAL PHASE X <9:0>** (See Notes)									

Table 48. External Phase Control Register Description

Bit label	Value	Description	Default Setting

EXTERNAL PHASE X <9:0>	0x000	~ -15ps correction on selected channel aperture Delay	0x200 0ps correction on ADC X aperture Delay
	…..		
	0x3FF	~ +15ps correction on selected channel aperture Delay	

Notes 1: Delay control range for edges of internal sampling clocks: ~+/-15 ps (1 step ~30 fs).
2: Actual Aperture Delay of the selected channel is controlled by the External Phase Control Register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.

5.6.20. Phase Registers (Read Only)

Apply to Phase Registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 49. Phase Register Mapping: address 0x25

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						**PHASE X <9:0>** (See Notes)									

Table 50. Phase Control Register Description

Bit label	Value	Description	Default Setting
PHASE X <9:0>	0x000	~ -15ps correction on selected channel aperture Delay	0x200 0ps correction on ADC X aperture Delay
	…..		
	0x3FF	~ +15ps correction on selected channel aperture Delay	

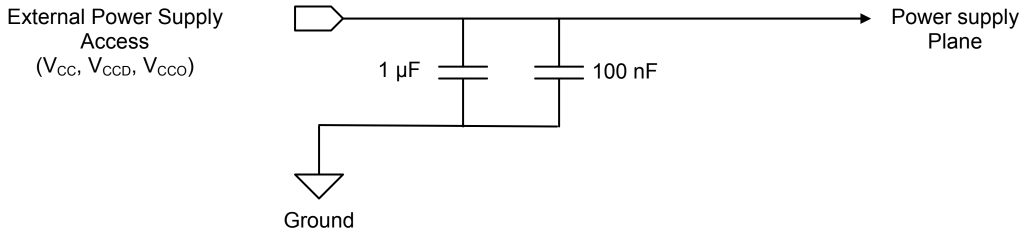
Notes 1: Delay control range for edges of internal sampling clocks: ~+/-15 ps (1 step ~30 fs).
2: Actual Aperture Delay of the selected channel is controlled by the External Phase Control Register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.

6 Application Information

6.1. Bypassing, decoupling and grounding

All power supplies have to be decoupled to ground as close as possible to the signal accesses to the board by 1 µF in parallel to 100 nF.

Figure 15 EV10AQ190 Power supplies Decoupling and grounding Scheme

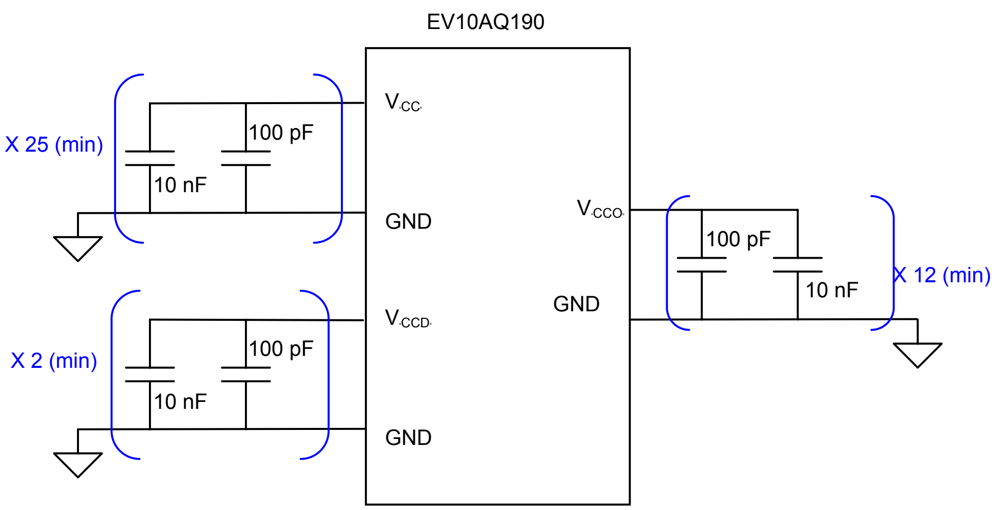


Note: V_{CCD} and V_{CCO} planes should be separated but the two power supplies can be reunited by a strap on the board.

Each group of neighboring power supply pins attributed to the same value should be bypassed with at least one pair of 100 pF in parallel to 10 nF capacitors. These capacitors should be placed as close as possible to the power supply package pins.
The minimum required number of pairs of capacitors by power supply type is:

25 for V_{CC}
2 for V_{CCD}
12 for V_{CCO}

Figure 16 EV10AQ190 Power Supplies Bypassing Scheme



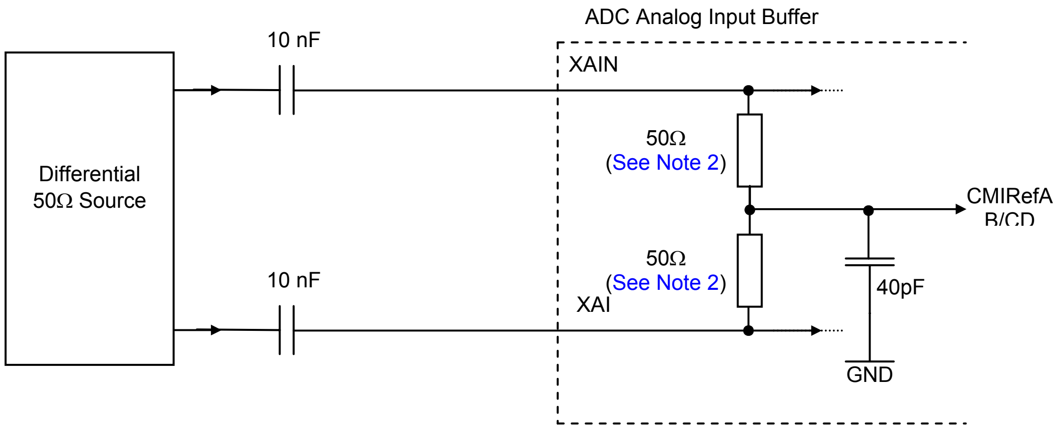
Each power supply has to be bypassed as close as possible to its source or access by 100 nF in parallel to 1µF capacitors.

6.2. Analog Inputs (VIN/VINN)

6.2.1. Differential analog input

The analog input can be either DC or AC coupled as described in Figure 17 and Figure 18.

Figure 17 Differential analog input implementation (AC coupled)

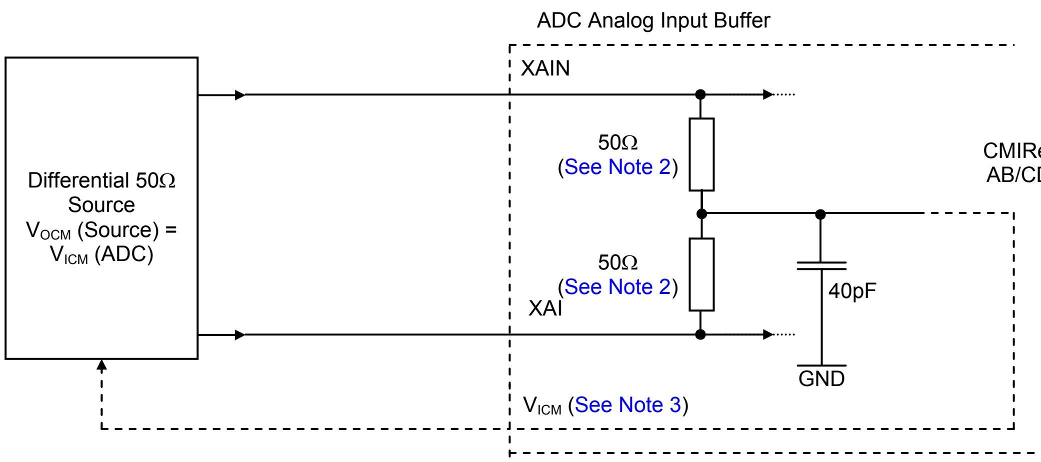


Notes: 1. X = A, B, C or D

2. The 50Ω terminations are on chip.

3. CMIRefAB/CD = 1.6V.

Figure 18 Differential analog input implementation (DC coupled)



Notes: 1. X = A, B, C or D

2. The 50Ω terminations are implemented on-chip and can be fine tuned (TRIMMER register at address 0x13)

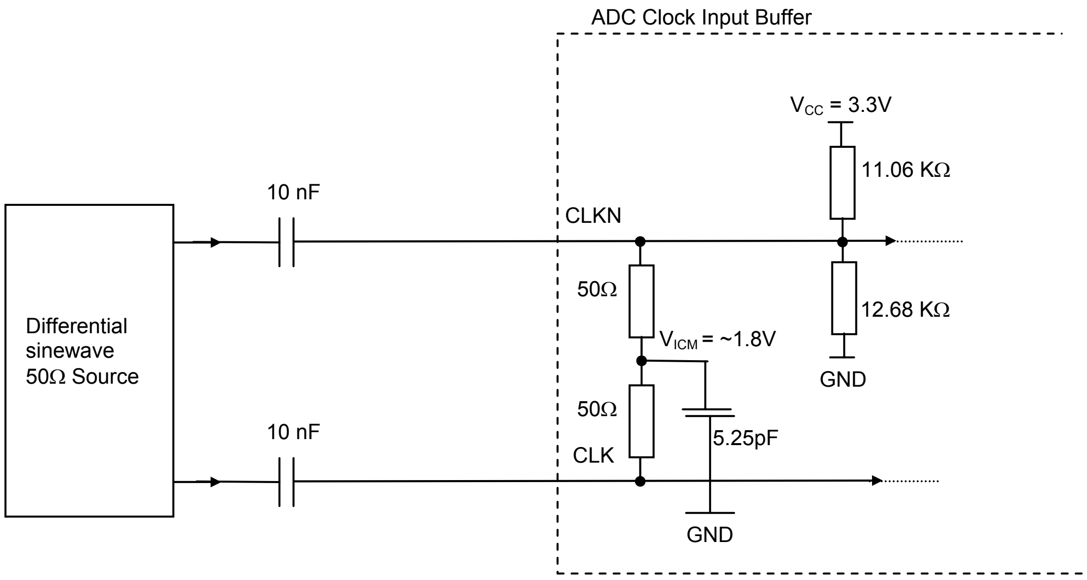
3. CMIRefAB/CD = 1.6V. The Common mode is output on signal CMIRefAB for A and B channels and CMIRefCD for C and D channels.

Note: If some Analog inputs are not used, they can be left unconnected (open).
Example: ADC in 1 channel mode with analog input signal on A channel.
➔ Analog inputs B, C and D can be left unconnected

6.3. Clock Inputs (CLK/CLKN)

It is recommended to enter the clock input signal differential mode. Since the clock input common mode is around 1.8V, we recommend to AC couple the input clock as described in Figure 19.

Figure 19 Differential clock input implementation (AC coupled)

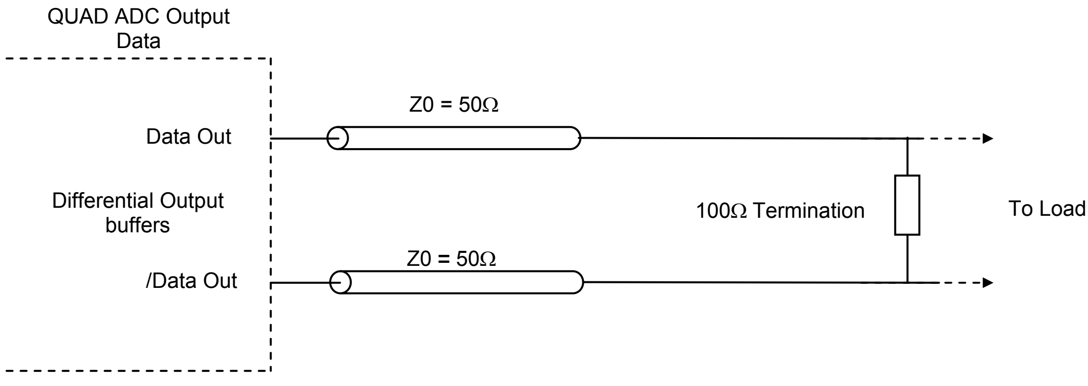


Differential mode is the recommended input scheme.
Single ended input is not recommended due to performance limitations.

6.4. Digital Outputs

The digital outputs are LVDS compatible. They have to be 100Ω differentially terminated.

Figure 20 Differential digital outputs Terminations (100Ω LVDS)

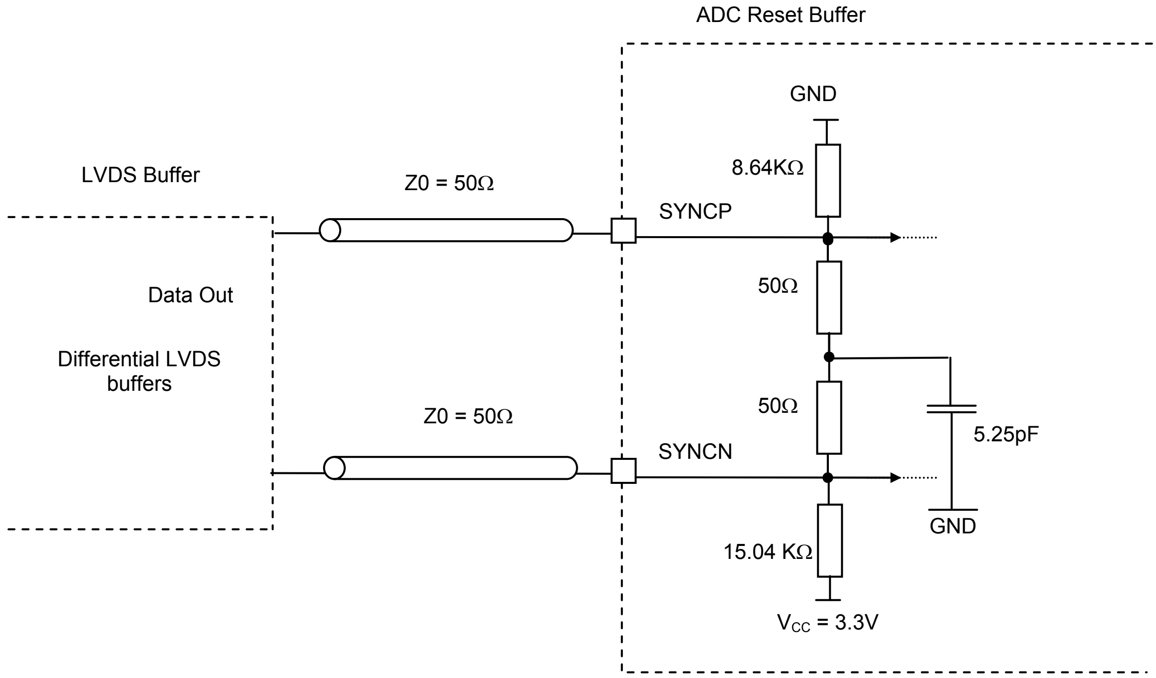


Note: If not used, leave the pins of the differential pair open

6.5. Reset Buffer (SYNCP, SYNCN)

The SYNCP, SYNCN signal has LVDS electrical characteristics. It is active high and should last at least 2 clock cycles to work properly

Figure 21 Reset Buffer (SYNCP, SYNCN)



Note: If not used, leave the pins of the differential pair open

7 Package Information

7.1. Package outline

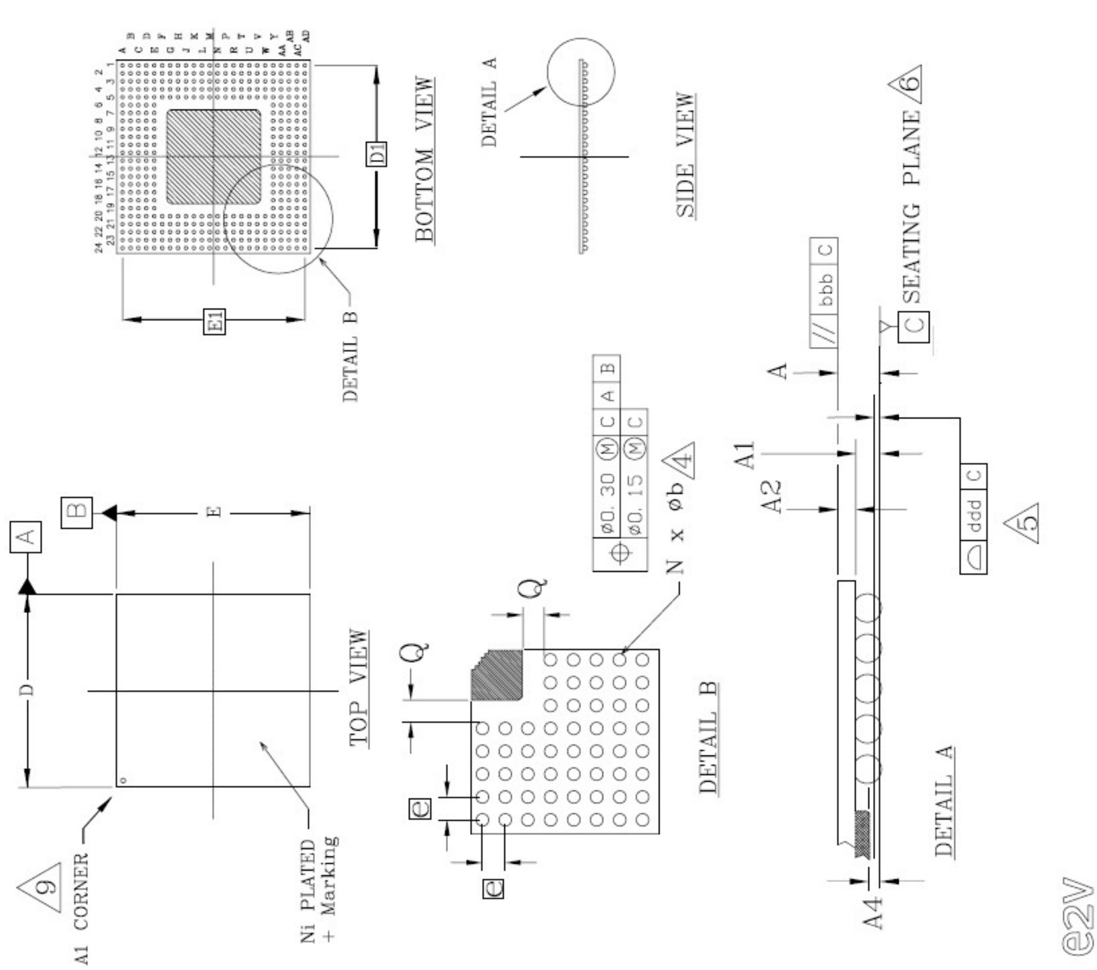
REF.	MIN.	NOM.	MAX.
A	1.25	1.45	1.60
A1	0.50	0.60	0.70
D	30.80	31.00	31.20
D1		29.21 (BSC.)	
E	30.80	31.00	31.20
E1		29.21 (BSC.)	
b	0.70	0.80	0.90
A2	0.75	0.85	0.95
M		24	
N		380	
bbb			0.25
ddd			0.20
e		1.27 TYP.	
A4	0.15		
Q	1.1		

DIMENSIONAL REFERENCES

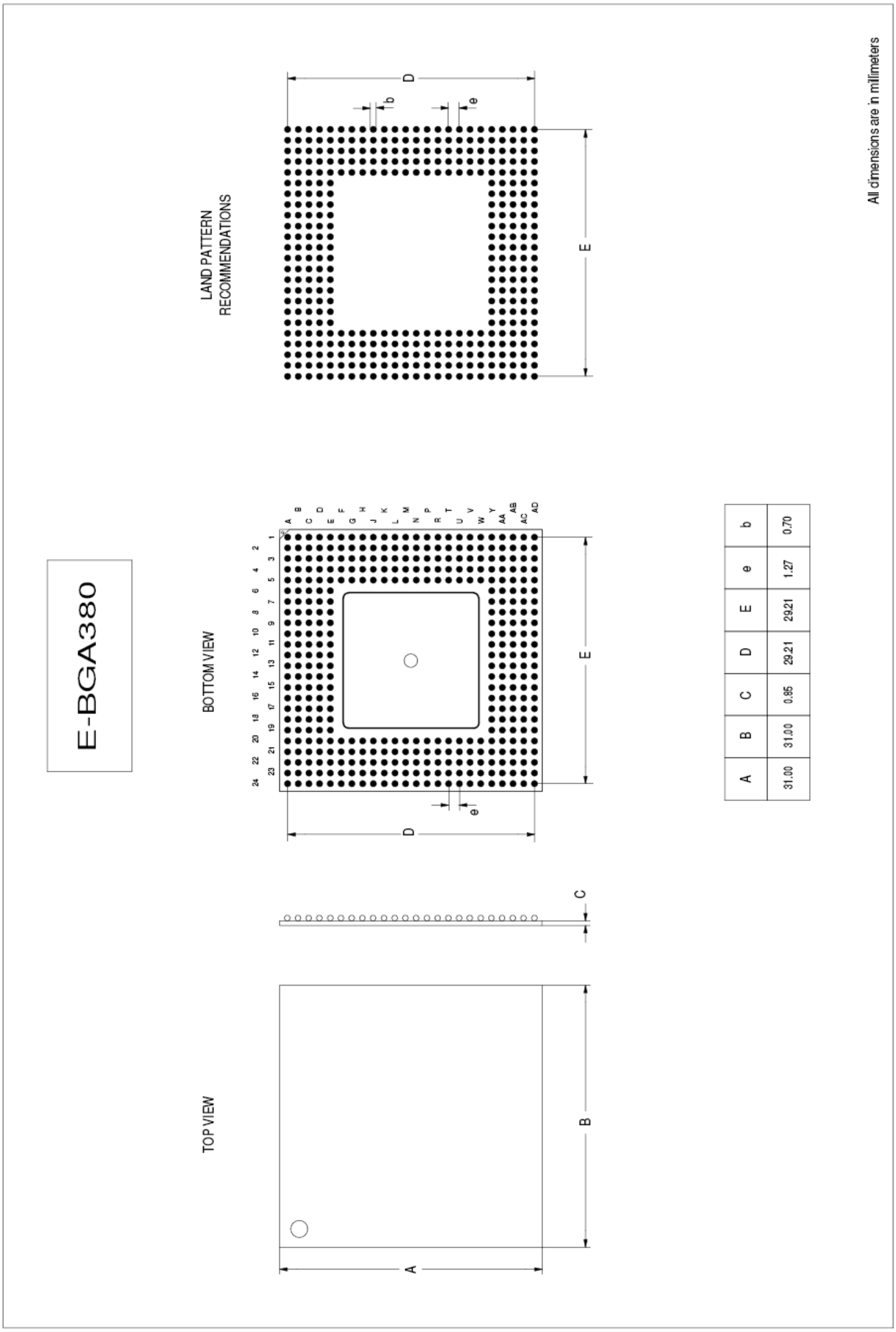
REF: JEDEC MS-034B VARIATION BAK-1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE, AND SYMBOL "N" IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING.
4. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM [C].
5. DIMENSION "ddd" IS MEASURED PARALLEL TO PRIMARY DATUM [C].
6. PRIMARY DATUM [C] AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE Ni PLATED.
8. ENCAPSULANT SIZE MAY VARY WITH DIE SIZE.
9. SMALL ROUND DEPRESSION FOR PIN 1 IDENTIFICATION.
10. "A4" IS MEASURED AT THE EDGE OF ENCAPSULANT TO THE INNER EDGE OF BALL PAD.
11. DIMENSIONING AND TOLERANCING PER ASME Y14.5 1994
12. THIS DRAWING IS FOR QUALIFICATION PURPOSE ONLY.



7.2. EBGA380 Land Pattern Recommendations



A	B	C	D	E	e	b
31.00	31.00	0.85	29.21	29.21	1.27	0.70

7.3. Thermal Characteristics

Assumptions:

- No air
- Pure conduction
- No radiation

7.3.1. Thermal Characteristics

- Rth Junction -bottom of Balls = TBD °C/W
- Rth Junction - board = TBD °C/W
- Rth Junction -top of case = TBD °C/W
- Rth Junction - top of case with 50 µm thermal grease = TBD °C/W
- Rth Junction - ambient (JEDEC standard, 49 x 49 mm² board size) = TBD °C/W
- Rth Junction - ambient (180 x 170 mm² evaluation board size) = TBD °C/W

7.3.2. Thermal Management Recommendations

In still air and 25°C ambient temperature conditions, the maximum temperature for the device soldered on the evaluation board is TBD °C. In this environment, extra cooling is necessary.
In the case of the need of an external thermal management, it is recommended to have an external heatsink on top of the EBGA380 with a thermal resistance of 5°C/W max.

7.4. Moisture Characteristics

This device is sensitive to the moisture (MSL3 according to JEDEC standard).
Shelf life in sealed bag : 12 months at <40°C and <90% relative humidity (RH).
After this bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temp. 220°C) must be :

- mounted within 168 hours at factory conditions of ≤30°C/60% RH, or
- stored at ≤20% RH

Devices require baking, before mounting, if Humidity Indicator is >20% when read at 23°C ± 5°C.
If baking is required, devices may be baked for :

- 192 hours at 40°C + 5°C/-0°C and <5% RH for low temperature device containers, or
- 24 hours at 125°C ± 5°C for high-temperature device containers.

8 Ordering Information

Table 51. Ordering information

Part Number	Package	Temperature Range	Screening Level	Comments
EVX10AQ190TPY	EBGA380 RoHS	Ambient	Prototype	
EV10AQ190TPY-EB	EBGA380 RoHS	Ambient	Prototype	Evaluation board
EV10AQ190CTPY	EBGA380 RoHS	Commercial 0°C < Ta < 70°C	Standard	Contact e2v Sales Office for availability
EV10AQ190VTPY	EBGA380 RoHS	Commercial -40°C < Ta < 85°C	Standard	Contact e2v Sales Office for availability

Table of contents

September version : chip Id 0x0418 added + trimmer updated + info on ramp mode + land pattern recommendation