EV12AQ600 / EV12AQ605
Quad 12-bit 1.6 GSps ADC with embedded cross-point switch, Digitizing up to 6.4 GSps

OVERVIEW

EV12AQ60x is a quad channel 12-bit 1.6 GSps ADC. The built-in Cross-Point-Switch (CPS) allows multi-mode operation with the capability to interleave the four independent cores in order to reach higher sampling rates. In 4-channel operating mode, the four cores can sample, in phase, four independent inputs at 1.6 GSps. In 2-channel operating mode, the cores are interleaved by 2 in order to reach 3.2 GSps sampling rate on each of the two inputs. In 1-channel operating mode, a single input is propagated to each of the four cores which are interleaved by 4 in order to reach a sampling rate of 6.4 GSps. This high flexibility enables digitization of IF and RF signals with up to 3.2 GHz of instantaneous bandwidth.
With an extended input bandwidth above 6 GHz (EFPBW) the EV12AQ60x allows the sampling of signals directly in the C-band (4-8 GHz) without the need to translate the signal to baseband through a down-conversion stage.
The ADC includes a multiple ADC chained synchronization feature to enable design of multi-channel systems.
The device is built in a non-hermetic flip-chip package using HiTCE glass ceramic material in order to reach optimized RF performance and higher pin density.
This circuit is designed, manufactured and will be qualified to be compliant with ESCC (European Space Components Coordination) and QML-Y space requirements.

APPLICATIONS

- Earth Observation SAR payload
- Telecommunication MIMO satellite payload
- High-Speed Data Acquisition & Test Instrumentation
- Automatic Test Equipment
- Software Defined Radio/Microwave
- Ultra Wideband Satellite Digital Receivers
- Point-to-Point Microwave Receivers
- Machine Condition Monitoring Systems
- Time of Flight Mass-Spectrometry
- LiDAR (Light Detection and Ranging)
- High Energy Physics

FEATURES & MAIN CHARACTERISTICS

- 1 Vpp 100 Ω differential DC/AC coupled input voltage
- 100 Ω Differential input AC coupled clock
- Cross-point switch enabling 1, 2 or 4 channel mode at 6.4 GSps / 3.2 GSps / 1.6 GSps
- 4.5 / 6.5 GHz selectable analog input bandwidth (-3dB)
- Low Latency ESIstream serial link at 12.8 Gbps
- Clock and SYNC chaining

PERFORMANCE

- **Single core performance**

4-channel mode at 1.6 GSps:

Output Level	Fin (MHz)	ENOB (bit)	SNR (dB_{FS})	SFDR (dB_{FS})
-1 dB_{FS} (NFPBW)	100 (NZ1)	8.7/(9.6)*	54.6/(59.9)*	73.3
	780 (NZ1)	8.7/(9.5)*	54.3/(59.4)*	73.4
	1580 (NZ2)	8.4/(9.1)*	53.4/(58.4)*	64.3
	2380 (NZ3)	8.1/(8.8)*	51.3/(56.3)*	63.6
-8 dB_{FS} (EFPBW)	3180 (NZ4)	8.4/(9.2)*	52.5/(57.7)*	66.6
	3980 (NZ5)	8.3/(9.2)*	52.2/(57.3)*	70.6
	4780 (NZ6)	8.2/(8.9)*	51.7/(56.8)*	61.8
	5580 (NZ7)	8.1/(8.7)*	51.3/(56.3)*	67.1

(*) Averaged simultaneous sampling by averaging the samples of the 4 cores when they are in phase.

SFDR at -8 dB_{FS} is better than 60 dB_{FS} up to the 6th Nyquist zone and ENOB is better than 8.0 bit.

SFDR at -8 dB_{FS}, without H2 and H3 harmonics, is better than 74 dB_{FS} up to the 8th Nyquist zone.

- **Interleaved cores performance**

1-channel mode at 6.4 GSps:

Output level	Fin (MHz)	ENOB (bit)	SFDR (dB_{FS})
-1 dB_{FS}	100 (NZ1)	8.6	66.2
	2380 (NZ1)	8.0	64.7
-8 dB_{FS}	3980 (NZ2)	7.9	53.2

- **Broadband performance at -12 dB loading factor:**

4-channel mode at 1.6 GSps over 760 MHz bandwidth
- NPR = 44 dB in 1st Nyquist (NFPBW) (at LF = -12 dB_{FS})
- NPR = 43 dB in 2nd Nyquist (NFPBW)
- NPR = 42 dB in 3rd Nyquist (EFPBW)
- NPR = 42 dB in 4th Nyquist (EFPBW)

1-channel mode at 6.4 GSps over 2560 MHz bandwidth
- NPR = 44 dB in 1st Nyquist (NFPBW)

- **Gain Flatness:**

0.5 dB Gain Flatness in extended bandwidth is typically 4 GHz.

- Power supply: 3.3 V (analog), 2.5 V (I/O), 1.2 V (digital), 2.5V or 3.3 V (SPI output)
- Power consumption: 6.6 W
- SPI digital interface
- Manufacturing calibration sets for interleaving
- ADC Gain, Offset, Sampling delay adjustment
- Package: CBGA323 (HiTCE) 16x16 mm pitch 0.80 mm
- Extended temperature range: Tc -55 °C / Tj +125 °C

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1 INTRODUCTION

This document is the Datasheet of 12-bit 4x1.6 GSps ADC with embedded Cross Point Switch (P/N EV12AQ60x)

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2 DESCRIPTION

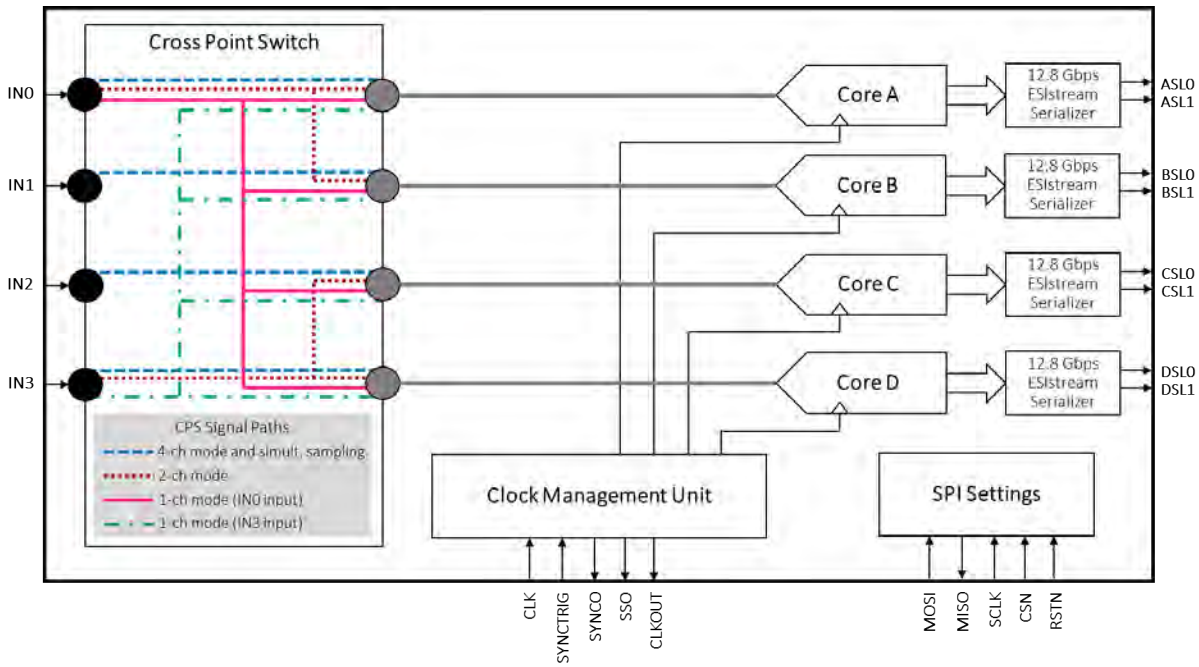


Figure 1: Quad 12-bit ADC with 12.8 Gbps serial link

EV12AQ60x is a quad 12-bit 1.6 GSps ADC featuring a built-in cross-point switch (controlled through the SPI) allowing 1, 2 or 4 channel digitizing at respectively 6.4 GSps, 3.2 GSps or 1.6 GSps sampling rate.

The four ADC cores can operate in phase or interleaved (option controlled though the SPI). External clock must be provided at four times the individual sampling rate.
The architecture uses four high sampling rate single cores (up to 1.6 GSps) without interleaving thus providing high level of spectral purity.

Data is output on a short latency serial link at up to 12.8 Gbps, using ESIstream protocol.

ADC synchronization is possible through SYNCTRIG pin and multiple ADC synchronization is simplified thanks to the ability of SYNC chaining through SYNCO.

Digital SPI CMOS input levels can be in 2.5 V or 3.3 V logic compatibility.
Digital SPI CMOS output levels can be configured in 2.5 V or 3.3 V logic compatibility by V_{CC_SPI} and V_{SPI_SEL} (see Table 16).

Tuning and functionalities are controlled through a Serial Peripheral Interface (SPI):

Functionalities controlled through the SPI are:

- Test mode activation and selection (ramp, PRBS, …)
- Clocking modes: 4 ADCs cores sampling simultaneously, 2 ADCs cores sampling simultaneously in opposition with 2 others, 4 ADCs cores interleaved.
- Clocking features: enabled/disabled CLKOUT, SSO and SYNCO outputs (in order to save power if these features are not needed).
- Inputs selection: 4 ADCs cores interleaved (1-channel mode) and driven by the same input IN0 (or IN3), 2 ADCs cores interleaved (2-channel mode) driven simultaneously by IN0 (and IN3), 4 ADCs cores (4-ch annel mode) driven simultaneously by IN0, IN1, IN2 and IN3.
- Analog input bandwidth: 4.5 GHz (nominal) or 6.5 GHz (extended).
- Sampling Delay Adjust enabled (for fine tuning of aperture delay) or disabled (recommended for clock Jitter Reduction)
- Factory calibration sets (Offset, Phase, Gain) selection for performance optimization (1-channel and 2-channel mode). 2 sets available for AQ605 and 4 sets for AQ600.
- Customization of calibration (Offset, Phase, Gain)
- Sync/Trigger mode (in Trigger mode the input on SYNCTRIG is propagated with the same delay as the Analog input, in Sync mode the input on SYNCTRIG is used to reinitialize internal clock dividers of the ADC, SYNCO is a synchronized copy of SYNCTRIG, PRBS are reset by a SYNC pulse).

- Input signal dynamic in-range detection
- Serial output frame configuration (12-bit data parity information, 12-bit data MSB/LSB first, frame order identification with PRBS sequence)
- Swing Adjust: Output swing of both serial links and timer CML or LVDS buffers is reduced by 30% for power dissipation reduction purpose.
- Output buffer impedance adjust (trim by a range of 20%) to improve transmission.
- 12.8 Gbps Serial link polarity can be inverted.

The ADC features internal DACs controlled though the SPI for tuning:

- Sampling Delay Adjust 12-bit with 150 ps tuning range :
  - 2 bit for coarse step (~ 37 ps/step)
  - 10 bit for fine step (~ 37 fs/step)
- Gain Adjust: 4096 steps (12-bit DAC), 456 LSB full scale variation, step of 0.11 LSB.
- Offset Adjust: 512 steps (9-bit DAC), ± 75 LSB offset variation, step of 0.29 LSB.
- Phase Adjust: 512 steps (9-bit DAC), ± 4.5 ps phase variation, step of 17 fs.
- Analog Input impedance termination trimming (5 bit DAC, 1.7 Ω step) common to all analog inputs.
- Input common mode trimming (5-bit DAC) common to all analog inputs, step of 5 mV.
- CML output impedance termination trimming (2-bit DAC) by lane, 14 Ω step.

3 SPECIFICATIONS

3.1 Absolute Maximum Ratings

Absolute maximum ratings are limiting values (referenced to GND = 0 V), to be applied individually, while other parameters are within specified operating conditions.
Exposure above those conditions may cause permanent damage. Long exposure to maximum ratings may affect device reliability

Table 1. Absolute Maximum ratings

Parameter	Symbol	Value		Unit
		Min	Max	
Analog supply voltage 3.3V	V_{CCA}	AGND – 0.3	4	V
Output supply voltage 2.5V	V_{CCO}	GNDO – 0.3	3.1	V
Digital supply voltage 1.2V	V_{CCD}	DGND – 0.3	1.5	V
SPI output supply voltage 2.5V or 3.3V	V_{CC_SPI}	DGND – 0.3	4	V
V_{SPI_SEL} supply voltage	V_{SPI_SEL}	DGND – 0.3	4	V
Analog input swing (mode ON)	| INxP – InxN | (x=0,1, 2 or 3)		4.8	Vppdiff
Analog input swing (mode OFF)	| INxP – InxN | (x=0,1, 2 or 3)		Note (1)	Vppdiff
Analog input peak voltage	INxN or INxP (x=0,1, 2 or 3)	AGND – 0.3	V_{CCA} + 0.3	V
Clock input swing (mode ON)	$\|V_{CLKP} - V_{CLKN}\|$		4	Vppdiff
Clock input swing (mode OFF)	$\|V_{CLKP} - V_{CLKN}\|$		Note (1)	Vppdiff
Clock input voltage	V_{CLKP} or V_{CLKN}	AGND – 0.3	V_{CCA}+ 0.3	V
SYNC input swing (mode ON)	$\|V_{SYNCP} - V_{SYNCN}\|$		4	Vppdiff
SYNC input swing (mode OFF)	$\|V_{SYNCP} - V_{SYNCN}\|$		Note (1)	Vppdiff
SYNC input peak voltage	V_{SYNCP} or V_{SYNCN}	AGND – 0.3	V_{CCA}+ 0.3	V
SPI input voltage	CSN, SCLK, RSTN, MOSI	DGND - 0.3	V_{CC0} + 0.3	V
Max Junction Temperature	T_{JMAX}		150	°C
Storage Temperature	T_{stg}	-65	150	°C
VDIODEA input voltage to prevent leakage (VDIODEC=GND)	$VDIODE_A$	-0.3	0.30	V
Maximum input current on DIODE	$IDIODE_A$		1	mA

Note (1): For cold sparing application, see application note AN 60S 217359
All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.
Input buffers and associated ESD protection have been designed to allow “cold sparing”.

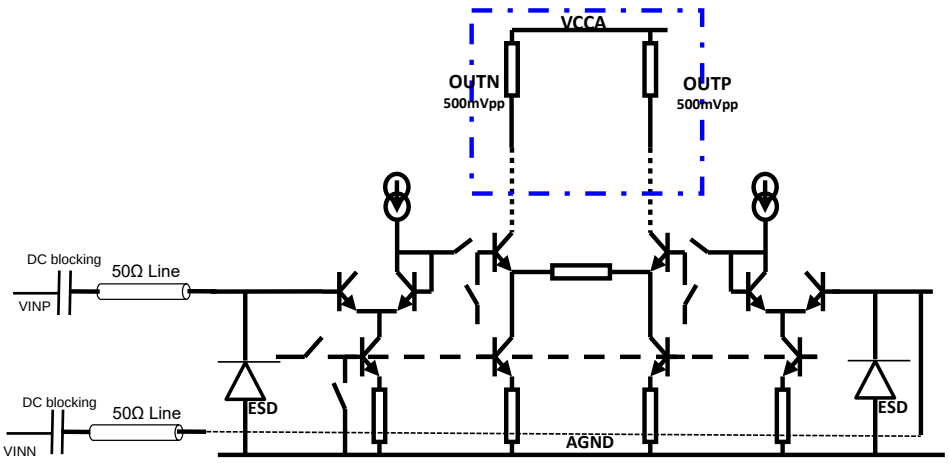


Figure 2: Analog input scheme regarding max ratings

3.2 Qualification requirements

This circuit is designed and manufactured and will be qualified to be compliant with space requirement (ESCC9000 and QML-Y specifications).

Table 2. Qualification information

Parameter	Symbol	Value	Unit
Die operating life at Tj = +125 °C	HTOL	10	Years
Die operating life at Tj = +110 °C	HTOL	17	Years
ESD protection (HBM)	HBM	2000	V
Latch up (JEDEC 78A)	LU	+/- 100	mA

Note 1: Tj refers to the hot spot junction temperature on the die.

3.3 Recommended conditions of use

Table 3. Recommended conditions of use

Parameter	Symbol	Comments	Recommended Value	Unit
Analog supply voltage	V_{CCA}	Analog Part	3.3 V	V
Output supply voltage	V_{CCO}	Output buffers	2.5 V	V
Digital supply voltage	V_{CCD}	Digital buffers	1.2 V	V
SPI output supply voltage	V_{CC_SPI}		2.5 V(1) 3.3 V(1)	V
Maximum differential input voltage (Full Scale)	V_{IN} -V_{INN}		1(3) 1	Vpp dBm
Clock input power level	P_{CLK} P_{CLKN}		6	dBm
Digital CMOS input	V_D	V_{IL} V_{IH}	0 2.5 or 3.3(2)	V
External Clock frequency	Fc		≤ 6.4	GHz
Operating Temperature Range	T_C; T_J		-55 °C <T_C ; T_J< 125 °C	°C

Note 1: Depending on SPI output buffer logic compatibility (refer to §7.1)
Note 2: Buffer compatible with both logic levels (refer to §7.1)
Note 3: Above this value the ADC will saturate. It is recommended to provide a signal below -1 dBFS to avoid this saturation.

3.4 Explanation of test levels

Table 4. Explanation of test levels

Test level	Comment
1A	100% tested over specified temperature range and specified power supply range, Fclock = 6 GHz
1B	100% tested over specified temperature range at typical power supplies, Fclock = 6 GHz
1C	100% tested at room temperature over specified supply range, Fclock = 6 GHz
1D	100% tested at room temperature at typical power supplies, Fclock = 6 GHz
2	100% production tested in 25 °C environment and samples tested at specified temperatures.
3	Samples tested only at specified temperature.
4	Parameter value is guaranteed by characterization testing (thermal steady-state conditions at specified temperature), Fclock = 6.4 GHz unless specified otherwise
5	Parameter value is only guaranteed by design

Only Min and Max values are guaranteed.
Interleaving performance (1-channel and 2-channel mode) are given for IN0 only. For IN3, interleaving calibration must be done to achieve those performance.

3.5 Electrical Characteristics for supplies, Inputs and Outputs

Unless otherwise specified:
Typical values are given for typical supplies V_{CCA} = 3.3 V, V_{CCD} = 1.2 V, V_{CCO} = 2.5 V at room temperature with Fclk = 6GHz and with nominal mode of the SPI (SDA, CLKOUT and SYNCO disabled).
Minimum and Maximum values are given over temperature and power supplies.

Table 5. Electrical characteristics for Supplies, Inputs and Outputs

Parameter	Test Level AQ600/AQ605	Symbol	Min	Typ	Max	Unit	Note
RESOLUTION			12			bit	
POWER REQUIREMENTS							
Power Supply voltage							
Analog		V_{CCA}	3.20	3.3	3.40	V	(1)
Output		V_{CCO}	2.35	2.5	2.65		
Digital		V_{CCD}	1.1	1.2	1.3		
SPI output		V_{CC_SPI}	2.35 3.20	2.5 3.3	2.65 3.4		
Power Supply current							
Analog	1A/1C	I_{CCA}	1400	1675	2035	mA	(2)
Output							
Full swing	1A/1C	I_{CCO}		365			
Reduced swing	1A/1C	I_{CCO}	300	330	410		
Digital	1A/1C	I_{CCD}	150	195	300		
SPI output	1A/1C	I_{CC_SPI}	0	0.2	2.5		
Power Supply current standby mode							
Analog	1A/1C	I_{CCA}		510		mA	
Output	1A/1C	I_{CCO}		20			
Digital	1A/1C	I_{CCD}		20			
SPI output	1A/1C	I_{CC_SPI}		0.2			
Power dissipation - Full power mode							
Full swing		PD		6.76		W	(2)
Reduced swing	1A/1C		5.5	6.65	7.95		
Stand-by mode	1A/1C			1.77			
Maximum number of power-up		NbPWRup	1E6				(3)
ANALOG INPUTS							
Common mode compatibility for analog inputs		AC or DC					(4)
Input Common Mode (default register value)	1A/1C	VICM	1.48	1.63	1.78	V	
Full Scale Input Voltage range on each differential input		VIN-pp		1000		mVpp Diff	
Analog Input power Level (in 100Ω differential termination)		PIN		+1		dBm	
Input leakage current for V_{INN} = V_{INP} = Common Mode + 75mV	1D	IIN	40	130	220	µA	
Input Resistance (differential)							
Before digital trimming through SPI	4	RIN	80	100	120	Ω	(5)
After digital trimming through SPI at given temperature			98	100	102	Ω	
Cross-talk between inputs @ Fin=2.4 GHz	4			70		dB	

Parameter	Test Level AQ600/AQ605	Symbol	Min	Typ	Max	Unit	Note
CLOCK INPUTS (CLKIN)							
Source Type		Low Phase noise Differential Sinewave					
Clock input common mode voltage	1A/1C	V_{CM}	2.4	2.6	2.8	V	
Clock input power level in 100 Ω	4	$P_{CLK, CLKN}$	-4	6	+10	dBm	
Clock input voltage on each single ended input	4	V_{CLK} or V_{CLKN}	±140	±450	±700	mV	
Clock input voltage into 100 Ω differential clock input	4	$\lvert V_{CLK} - V_{CLKN} \rvert$	0.56	1.8	2.8	Vpp	
Clock input minimum slew rate (square or sinewave clock)	5	SR_{CLK}	8	12		GV/s	
Clock input capacitance (die + package)	5	C_{CLK}		1		pF	
Clock input resistance (differential)	1B/1D	R_{CLK}	90	105	115	Ω	(5)
Clock Jitter (max. allowed on clock source) For 6.4 GHz sinewave analog input	4	Jitter		70		fs_{rms}	(6)
Clock Duty Cycle	4	Duty Cycle	45	50	55	%	
CLOCK output (CLKOUT)							
Logic Compatibility		CML					
50 Ω transmission lines,100 Ω (2 x50 Ω differential termination)							
Output levels : swing adjust off = full swing							
Logic low	1A/1C	V_{OL}		V_{CCA} – 0.31	V_{CCA} – 0.26	V	
Logic high	1A/1C	V_{OH}	V_{CCA} – 0.20	V_{CCA} - 0.14		V	
Differential output	1A/1C	V_{OH}- V_{OL}	140	175	220	mVp	
Common mode	1A/1C	V_{OCM}	V_{CCA} – 0.29	V_{CCA} - 0.22	V_{CCA} – 0.19	V	
Output levels : swing adjust on = reduced swing							
Logic low	1A/1C	V_{OL}		V_{CCA} – 0.17	V_{CCA} – 0.12	V	
Logic high	1A/1C	V_{OH}	V_{CCA} – 0.15	V_{CCA} - 0.09		V	
Differential output	1A/1C	V_{OH}- V_{OL}	70	90	110	mVp	
Common mode	1A/1C	V_{OCM}	V_{CCA} – 0.2	V_{CCA} - 0.13	V_{CCA} – 0.1	V	
SYNC, SYNCN Signal							
Input Voltages to be applied Swing	1A/1C	V_{IH}- V_{IL}	100	350	450	mV	
Common Mode	1A/1C	V_{ICM}	1.125	1.25	1.375	V	
SYNCTRIGP, SYNCTRIGN input capacitance		C_{SYNC}		1		pF	
SYNCTRIGP, SYNCTRIGN input resistance	1B/1D	R_{SYNC}	98	118	134	Ω	

Parameter	Test Level AQ600/AQ605	Symbol	Min	Typ	Max	Unit	Note
Digital CMOS signals (CSN, SCLK, RSTN, MOSI, MISO)							
Low level threshold of Schmitt Trigger	1A/1C	Vil			0.7	V	
High level threshold of Schmitt Trigger	1A/1C	Vih	1.70			V	
CMOS Schmitt Trigger hysteresis		Vhystc	0.10 * V_{CCO}			V	
CMOS low level input current (Vinc=0 V)		Iilc			300	nA	(7)
CMOS high level input current (Vinc=VCCD max)		Iihc			1000	nA	
CMOS low level output voltage (Iolc = 3 mA)	1A/1C	Volc			0.20 * V_{CC_SPI}	V	
CMOS high level output voltage (Iohc = 3 mA)	1A/1C	Vohc	0.8 * V_{CC-SPI}			V	
LVDS OUTPUTS (SSO, SYNCO)							
Logic Compatibility			LVDS				
50 Ω transmission lines, 100 Ω (2 x 50 Ω) differential termination							
Output levels : swing adjust off = full swing							
Logic low	1A/1C	V_{OL}			1. 460	V	
Logic high	1A/1C	V_{OH}	1. 16			V	
Differential output	1A/1C	V_{OH}- V_{OL}	200	310	375	mV	
Common mode	1A/1C	V_{OCM}	1.05	1.30	1.55	V	
Output levels : swing adjust on = reduced swing							
Differential output	1A/1C	V_{OH}- V_{OL}	80	210	275	mV	
Common mode	1A/1C	V_{OCM}	1.1		1.6	V	
SERIAL LINK OUTPUTS (ASLx,BSLx,CSLx,DSLx) with x=0 or 1							
Logic Compatibility			CML				
50 Ω transmission lines, 100 Ω (2 x 50 Ω) differential termination							
Output levels : swing adjust off = full swing							
Logic low	1A/4	V_{OL}		V_{CCO} – 0.65	Vcco – 0.55	V	
Logic high	1A/ 4	V_{OH}	V_{CCO} – 0.42	V_{CCO} – 0.324		V	
Differential output	1A/ 4	V_{OH}- V_{OL}	260	325	400	mVp	
Common mode	1A/ 4	V_{OCM}	V_{CCO} – 0.6	V_{CCO} - 0.45	V_{CCO} – 0.4	V	
Output levels : swing adjust on = reduced swing							
Logic low	1A/ 4	V_{OL}		V_{CCO} – 0.45	V_{CCO} – 0.35	V	
Logic high	1A/ 4	V_{OH}	V_{CCO} – 0.32	V_{CCO} - 0.22		V	
Differential output	1A/ 4	V_{OH}- V_{OL}	170	215	280	mVp	
Common mode	1A/ 4	V_{OCM}	V_{CCO} – 0.45	V_{CCO} - 0.35	V_{CCO} – 0.25	V	

Notes:

1. V_{CC_SPI} supply value is defined according to the chosen SPI input signals level. Refer to §7.1.
2. Enabling either SDA or other features (CLKOUT, SSO, SYNCO) increases power consumption by 170 mW (51 mA on V_{CCA}). Maximum power consumption is estimated at Tj = 125 °C, maximum supplies value and all features enabled.
3. Maximum number of power-up is limited by the maximum number of OTP memory cells reading.
4. The DC analog common mode voltage is provided by the ADC.

5. For optimal performance in term of VSWR, characteristic impedance of input traces on the PCB must be differential 100 Ω ± 5% and analog input impedance must be digitally trimmed to cope with process deviation (see chapter 8.5.6).
6. Jitter calculation integrated up to 6.4 GHz.
7. Vil & Vih being referenced to Vcco (see simplified electrical schematics Table 14) the following equations apply: Vih_min = 0.65*Vcco_max & Vil_max = 0.3* Vcco_min

3.6 Converter Characteristics

Unless otherwise specified:

- Typical values are given for typical supplies VCCA = 3.3 V, VCCD = 1.2 V, VCCO = 2.5 V at room temperature with Fclk = 6.4 GHz and with nominal mode of the SPI (SDA, CLKOUT and SYNCO disabled).
- Minimum and Maximum values are given over temperature and power supplies with Fclk = 6 GHz.
- ADC output level -1 dBFS.
- Clock input differentially driven @ +7 dBm at ADC input.
- Input common mode is trimmed using 2 different register values (see Table 29): 0x1B for 1st, 2nd and 3rd Nyquist and default value for higher frequencies.
- Nominal bandwidth is selected for 1st and 2nd Nyquist and extended one is applied for other frequencies.

Table 6. Low frequency characteristics

Parameter	Test Level AQ600/AQ605	Symbol	Min	Typ	Max	Unit	Note
DC ACCURACY							
Analog Input frequency = 100 MHz, -1 dBFS							
Part to part Gain deviation	4	G	-0.5	0	0.5	dB	
Gain variation versus temperature	4	G(T)	-0.4		+0.1	dB	
DC offset before trimming through SPI	4	OFFSET	2011		2092	LSB	
DC offset mismatch	4	OFFSET M		+45/-35		LSB	
DC offset after trimming through SPI	4	OFFSET	2043	2047	2051	LSB	
Analog Input frequency = 100 MHz, -1 dBFS, 1-Channel mode							
DNLrms	1A/1D	DNLrms		0.15	0.28	LSB	
Differential non linearity	1A/1D	DNL	-0.85	-0.5/+0.5	1.2	LSB	
INLrms	1A/1D	INLrms		0.6	1.4	LSB	
Integral non linearity	1A/1D	INL	-4.5	-1.75/+1.75	4.5	LSB	
Analog Input frequency = 100 MHz, -1 dBFS, 2-Channel mode							
DNLrms	4	DNLrms		0.2		LSB	
Differential non linearity	4	DNL	-0.7		0.9	LSB	
INLrms	4	INLrms		0.65		LSB	
Integral non linearity	4	INL	-2.5		2.5	LSB	
Analog Input frequency = 100 MHz, -1 dBFS, 4-Channel mode							
DNLrms	4	DNLrms		0.2		LSB	
Differential non linearity	4	DNL	-0.7		0.9	LSB	
INLrms	4	INLrms		0.65		LSB	
Integral non linearity	4	INL	-2.5		2.5	LSB	

3.7 AC Analog Inputs

Table 7. Dynamic Characteristics

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ	Max	Note
Full Power Input Bandwidth						
Nominal Full Power Bandwidth (selected by SPI)	4	GHz		4.3		
Extended Full Band Power Bandwidth (selected by SPI)		GHz		6.5		
Gain Flatness (+/- 0.5 dB) (1)						
Nominal Gain Flatness bandwidth (selected by SPI)	4	GHz		1		
Extended Gain Flatness bandwidth (selected by SPI)		GHz		3.8		
Input Voltage Standing Wave Ratio						
up to 2.4 GHz	4	VSWR			< 1.3:1	
up to 6 GHz					< 2:1	

Gain flatness is the bandwidth over which the difference between the gain and the DC gain is lower than 0.5 dB

3.8 Dynamic Performance - 4-channel mode – 1.6 GSps

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ Nominal	Typ Without H2 – H3	Max	Note
SFDR - Spurious Free Dynamic Range - Single tone - 4-channel mode – 1.6 GSps							
At -1 dBFS output level							
Fin = 98 MHz	4	SFDR dBFS		73.3	73.5		(1)(2)(3)(4)
Fin = 778 MHz	4			73.4	75.2		
Fin = 1578 MHz	4			64.3	66.8		
Fin = 2230 MHz	1A/1D		55	66.8			
Fin = 2378 MHz	4			63.6	69.7		
Fin = 3178 MHz	4			55.9	69.0		
Fin = 3978 MHz	4			49.3	65.1		
Fin = 4778 MHz	4			45.3	74.2		
Fin = 5578 MHz	4			48.2	73.1		
At -3 dBFS output level							
Fin = 98 MHz	4	SFDR dBFS		67.3	69.2		(1)(2)(3)(4)
Fin = 778 MHz	4			71.1	72.8		
Fin = 1578 MHz	4			68.5	68.5		
Fin = 2230 MHz	4			69.2			
Fin = 2378 MHz	4			69.6	71.0		
Fin = 3178 MHz	4			64.4	74.9		
Fin = 3978 MHz	4			56.6	70.9		
Fin = 4778 MHz	4			50.5	73.2		
Fin = 5578 MHz	4			52.3	73.1		
At -8 dBFS output level							
Fin = 98 MHz	4	SFDR dBFS		75.0	76.2		(1)(2)(3)(4)
Fin = 778 MHz	4			72.3	76.2		
Fin = 1578 MHz	4			72.2	76.5		
Fin = 2230 MHz	4			74.6			
Fin = 2378 MHz	4			73.4	75.8		
Fin = 3178 MHz	4			66.6	75.9		
Fin = 3978 MHz	4			70.6	75.4		
Fin = 4778 MHz	4			61.8	74.1		
Fin = 5578 MHz	4			67.1	75.7		
At -12 dBFS output level							
Fin = 98 MHz	4	SFDR dBFS		75.0	75.0		(1)(2)(3)(4)
Fin = 778 MHz	4			74.6	75.0		
Fin = 1578 MHz	4			74.3	74.6		
Fin = 2230 MHz	4			75			
Fin = 2378 MHz	4			73.8	74.4		
Fin = 3178 MHz	4			73.7	74.5		
Fin = 3978 MHz	4			73.6	75.0		
Fin = 4778 MHz	4			71.2	74.6		
Fin = 5578 MHz	4			73.1	74.7		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ	Max	Note
IMD3 - InterModulation Distortion (third order) – Dual tone - 4-channel mode – 1.6 GSps						
At -7 dBFS output level - Δ FIN = 10 MHz						
Fin = 100 MHz	4	IMD3 dBFS		61		(1)
Fin = 700 MHz	4			62		
Fin = 1500 MHz	4			62		
Fin = 2300 MHz	4			61		
Fin = 3100 MHz	4			57		
Fin = 3900 MHz	4			52		
Fin = 4700 MHz	4			45		
Fin = 5500 MHz	4			38		
Fin = 5900 MHz	4			34		
At -9 dBFS output level - Δ FIN = 10 MHz						
Fin = 100 MHz	4	IMD3 dBFS		64		(1)
Fin = 700 MHz	4			63		
Fin = 1500 MHz	4			64		
Fin = 2300 MHz	4			64		
Fin = 3100 MHz	4			61		
Fin = 3900 MHz	4			58		
Fin = 4700 MHz	4			52		
Fin = 5500 MHz	4			46		
Fin = 5900 MHz	4			42		
At -14 dBFS output level - Δ FIN = 10 MHz						
Fin = 100 MHz	4	IMD3 dBFS		67		(1)
Fin = 700 MHz	4			66		
Fin = 1500 MHz	4			67		
Fin = 2300 MHz	4			70		
Fin = 3100 MHz	4			68		
Fin = 3900 MHz	4			69		
Fin = 4700 MHz	4			65		
Fin = 5500 MHz	4			61		
Fin = 5900 MHz	4			58		
At -18 dBFS output level - Δ FIN = 10 MHz						
Fin = 100 MHz	4	IMD3 dBFS		73		(1)
Fin = 700 MHz	4			72		
Fin = 1500 MHz	4			72		
Fin = 2300 MHz	4			75		
Fin = 3100 MHz	4			72		
Fin = 3900 MHz	4			77		
Fin = 4700 MHz	4			74		
Fin = 5500 MHz	4			70		
Fin = 5900 MHz	4			69		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ		Max	Note
				Nominal	Without H2 – H3		
THD - Total harmonic distortion - 4-channel mode – 1.6 GSps							
At -1 dBFS output level							
Fin = 98 MHz	4	THD dBFS		-67.2	-68.1		(1)
Fin = 778 MHz	4			-67.1	-68.9		
Fin = 1578 MHz	4			-60.9	-64.5		
Fin = 2230 MHz	1A/1D			-62.2		-52	
Fin = 2378 MHz	4			-60.4	-65.6		
Fin = 3178 MHz	4			-55.0	-65.6		
Fin = 3978 MHz	4			-48.8	-62.7		
Fin = 4778 MHz	4			-45.1	-67.7		
Fin = 5578 MHz	4			-47.0	-67.0		
At -3 dBFS output level							
Fin = 98 MHz	4	THD dBFS		-63.7	-66.4		(1)
Fin = 778 MHz	4			-66.3	-68.4		
Fin = 1578 MHz	4			-64.9	-66.0		
Fin = 2230 MHz	4			-65.0			
Fin = 2378 MHz	4			-64.8	-66.7		
Fin = 3178 MHz	4			-62.0	-68.7		
Fin = 3978 MHz	4			-55.6	-66.8		
Fin = 4778 MHz	4			-50.3	-68.3		
Fin = 5578 MHz	4			-51.1	-68.2		
At -8 dBFS output level							
Fin = 98 MHz	4	THD dBFS		-68.4	-69.7		(1)
Fin = 778 MHz	4			-67.2	-69.6		
Fin = 1578 MHz	4			-67.2	-69.7		
Fin = 2230 MHz	4			-67.4			
Fin = 2378 MHz	4			-67.3	-69.2		
Fin = 3178 MHz	4			-64.3	-69.2		
Fin = 3978 MHz	4			-66.2	-69.2		
Fin = 4778 MHz	4			-60.5	-68.3		
Fin = 5578 MHz	4			-63.7	-69.3		
At -12 dBFS output level							
Fin = 98 MHz	4	THD dBFS		-68.6	-69.5		(1)
Fin = 778 MHz	4			-68.3	-69.4		
Fin = 1578 MHz	4			-68.1	-68.9		
Fin = 2230 MHz	4			-68.2			
Fin = 2378 MHz	4			-67.5	-68.7		
Fin = 3178 MHz	4			-67.3	-68.8		
Fin = 3978 MHz	4			-67.6	-68.9		
Fin = 4778 MHz	4			-66.2	-68.9		
Fin = 5578 MHz	4			-67.3	-69.0		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ		Max	Note
				Nominal mode	Averaged Simul. Sampling (*)		
SNR - Signal to noise ratio - 4-channel mode – 1.6 GSps							
At -1 dBFS output level							
Fin = 98 MHz	4	SNR dBFS		54.6	59.9		(1)
Fin = 778 MHz	4			54.3	59.4		
Fin = 1578 MHz	4			53.5	58.4		
Fin = 2230 MHz	1A/1D		49	51.1			
Fin = 2378 MHz	4			51.3	56.3		
Fin = 3178 MHz	4			50.3	54.9		
Fin = 3978 MHz	4			49.3	54.0		
Fin = 4778 MHz	4			48.4	52.9		
Fin = 5578 MHz	4			47.4	51.8		
At -3 dBFS output level							
Fin = 98 MHz	4	SNR dBFS		54.7	59.9		(1)
Fin = 778 MHz	4			54.4	59.7		
Fin = 1578 MHz	4			53.9	58.9		
Fin = 2230 MHz	4			51.7			
Fin = 2378 MHz	4			51.9	57.0		
Fin = 3178 MHz	4			51.1	55.9		
Fin = 3978 MHz	4			50.4	55.1		
Fin = 4778 MHz	4			49.6	54.2		
Fin = 5578 MHz	4			48.7	53.2		
At -8 dBFS output level							
Fin = 98 MHz	4	SNR dBFS		54.8	60.2		(1)
Fin = 778 MHz	4			54.8	60.1		
Fin = 1578 MHz	4			54.6	59.8		
Fin = 2230 MHz	4			52.7			
Fin = 2378 MHz	4			52.9	58.0		
Fin = 3178 MHz	4			52.6	57.7		
Fin = 3978 MHz	4			52.2	57.3		
Fin = 4778 MHz	4			51.8	56.8		
Fin = 5578 MHz	4			51.4	56.3		
At -12 dBFS output level							
Fin = 98 MHz	4	SNR dBFS		55.1	60.4		(1)
Fin = 778 MHz	4			55.0	60.3		
Fin = 1578 MHz	4			54.8	60.1		
Fin = 2230 MHz	4			53.1			
Fin = 2378 MHz	4			53.2	58.5		
Fin = 3178 MHz	4			53.1	58.3		
Fin = 3978 MHz	4			52.9	58.1		
Fin = 4778 MHz	4			52.8	57.9		
Fin = 5578 MHz	4			52.6	57.7		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ			Max	Note
				Nominal mode	Without H2 – H3	Averaged Simul. Sampling(*)		
SINAD - Signal to noise and distortion ratio - 4 Channels mode – 1.6 GSps								
At -1 dBFS output level								
Fin = 98 MHz	4	SINAD dBFS		54.2	54.2	59.3		(1)
Fin = 778 MHz	4			53.8	53.9	59.0		
Fin = 1578 MHz	4			52.5	52.8	56.5		
Fin = 2230 MHz	1A/1D		48	50.8				
Fin = 2378 MHz	4			50.5	50.9	54.7		
Fin = 3178 MHz	4			48.7	49.8	52.5		
Fin = 3978 MHz	4			45.8	48.7	47.8		
Fin = 4778 MHz	4			43.2	47.8	44.0		
Fin = 5578 MHz	4			43.9	46.9			
At -3 dBFS output level								
Fin = 98 MHz	4	SINAD dBFS		54.0	54.2	58.4		(1)
Fin = 778 MHz	4			54.0	54.1	58.9		
Fin = 1578 MHz	4			53.3	53.4	57.8		
Fin = 2230 MHz	4			51.5				
Fin = 2378 MHz	4			51.5	51.5	56.3		
Fin = 3178 MHz	4			50.5	50.8	55.2		
Fin = 3978 MHz	4			49.0	49.9	52.4		
Fin = 4778 MHz	4			46.7	49.1	48.4		
Fin = 5578 MHz	4			46.5	48.3			
At -8 dBFS output level								
Fin = 98 MHz	4	SINAD dBFS		54.5	54.6	59.8		(1)
Fin = 778 MHz	4			54.4	54.5	59.7		
Fin = 1578 MHz	4			54.2	54.3	59.4		
Fin = 2230 MHz	4			52.5				
Fin = 2378 MHz	4			52.5	52.6	57.7		
Fin = 3178 MHz	4			52.1	52.3	57.1		
Fin = 3978 MHz	4			51.8	51.8	56.8		
Fin = 4778 MHz	4			51.0	51.4	55.3		
Fin = 5578 MHz	4			50.8	51.0			
At -12 dBFS output level								
Fin = 98 MHz	4	SINAD dBFS		54.7	54.7	60.1		(1)
Fin = 778 MHz	4			54.7	54.7	60.1		
Fin = 1578 MHz	4			54.6	54.6	59.9		
Fin = 2230 MHz	4			52.9				
Fin = 2378 MHz	4			53.0	53.0	58.3		
Fin = 3178 MHz	4			52.8	52.9	58.1		
Fin = 3978 MHz	4			52.7	52.7	58.0		
Fin = 4778 MHz	4			52.4	52.5	57.5		
Fin = 5578 MHz	4			52.2	52.2			

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ			Max	Note
				Nominal	Without H2 – H3	Averaged Simul. Sampling(*)		
ENOB - Effective Number Of Bits - 4-channel mode – 1.6 GSps								
At -1 dBFS output level								
Fin = 98 MHz	4			8.7	8.7	9.6		
Fin = 778 MHz	4			8.7	8.7	9.5		
Fin = 1578 MHz	4			8.4	8.5	9.1		
Fin = 2230 MHz	1A/1D	ENOB	7.7	8.1				(1)
Fin = 2378 MHz	4	Bit_FS		8.1	8.2	8.8		
Fin = 3178 MHz	4			7.8	8.0	8.4		
Fin = 3978 MHz	4			7.3	7.8	7.6		
Fin = 4778 MHz	4			6.9	7.6	7.0		
Fin = 5578 MHz	4			7.0	7.5			
At -3 dBFS output level								
Fin = 98 MHz	4			8.7	8.7	9.4		
Fin = 778 MHz	4			8.7	8.7	9.5		
Fin = 1578 MHz	4			8.6	8.6	9.3		
Fin = 2230 MHz	4	ENOB		8.3				(1)
Fin = 2378 MHz	4	Bit_FS		8.3	8.3	9.1		
Fin = 3178 MHz	4			8.1	8.1	8.9		
Fin = 3978 MHz	4			7.8	8.0	8.4		
Fin = 4778 MHz	4			7.5	7.9	7.7		
Fin = 5578 MHz	4			7.4	7.7			
At -8 dBFS output level								
Fin = 98 MHz	4			8.8	8.8	9.6		
Fin = 778 MHz	4			8.7	8.8	9.6		
Fin = 1578 MHz	4			8.7	8.7	9.6		
Fin = 2230 MHz	4	ENOB		8.4				(1)
Fin = 2378 MHz	4	Bit_FS		8.4	8.4	9.3		
Fin = 3178 MHz	4			8.4	8.4	9.2		
Fin = 3978 MHz	4			8.3	8.3	9.2		
Fin = 4778 MHz	4			8.2	8.2	8.9		
Fin = 5578 MHz	4			8.1	8.2	8.7		
At -12 dBFS output level								
Fin = 98 MHz	4			8.8	8.8	9.7		
Fin = 778 MHz	4			8.8	8.8	9.7		
Fin = 1578 MHz	4			8.8	8.8	9.7		
Fin = 2230 MHz	4	ENOB		8.5				(1)
Fin = 2378 MHz	4	Bit_FS		8.5	8.5	9.4		
Fin = 3178 MHz	4			8.5	8.5	9.4		
Fin = 3978 MHz	4			8.5	8.5	9.3		
Fin = 4778 MHz	4			8.4	8.4	9.3		
Fin = 5578 MHz	4			8.4	8.4	9.2		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ	Max	Note
NSD - Noise Spectral Density - 4-channel mode – 1.6 GSps						
At -1 dBFS output level						
1st Nyquist (NFPBW)		NSD dBm/Hz		-143		(1)
2nd Nyquist (EFPBW)				-140		
At -8 dBFS output level						
1st Nyquist (NFPBW)		NSD dBm/Hz		-144		(1)
2nd Nyquist (EFPBW)				-142		
NPR - Noise Power Ratio - 4-channel mode – 1.6 GSps						
At loading factor = -12 dBFS - 640 MHz noise pattern width - 5 MHz notch centered at Fs/4						
1st Nyquist (NFPBW)		NPR dB		44		(1)
At loading factor = -12 dBFS - 640 MHz noise pattern width - 5 MHz notch centered at 3Fs/4						
2nd Nyquist (NFPBW)		NPR dB		43		
At loading factor = -12 dBFS - 640 MHz noise pattern width - 5 MHz notch centered at 5 Fs/4						
3rd Nyquist (EFPBW)		NPR dB		42		
At loading factor = -12 dBFS - 640 MHz noise pattern width - 5 MHz notch centered at 7Fs/4						
4th Nyquist (EFPBW)		NPR dB		42		

(*) Averaged Simul. Sampling:
Simultaneous sampling is obtained by setting the 4 cores in phase (CLK_MODE_SEL = 0b11, see §6.3 Register map).
Average simultaneous sampling is obtained by averaging the samples of the 4 cores when they are in phase.

Notes:

1. Optimal bandwidth selection depends on signal characteristic. The bandwidth selection allows optimizing noise and linearity trade-off. For signals below 1.6 GHz, the bandwidth selection must be set to Nominal. For signals beyond this frequency, the bandwidth must be set to Extended. The extended bandwidth degrades noise floor up to 1 dB, compensated at high frequency by inputing signals with lower signal attenuation.
2. Linearity of high frequencies is dominated by H3 and H2, stepping back 3 or 6 dB on input signals involving signifiant improvement on SFDR figures. For narrow band operation (10 MHz or 50 MHz), a carefuly chosen frequency plan allows rejection of these folded harmonics up to H8 beyond the band of interest.
3. SFDR without H3 harmonic is better than 60 dB_{FS} at -1 dB_{FS}. Removing H2 and H3 allows an SFDR performance higher than 68 dB_{FS} up to 5580 MHz. H3 dominates up to 5300 MHz, then H2 dominates above 5300 MHz.
4. Adjustment of input common mode can also be used to optimize ADC linearity.

3.9 Dynamic Performance - 2-channel mode – 3.2 GSps

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ Nominal	Typ ILG recal at Fin (**)	Max	Note
SFDR - Spurious Free Dynamic Range - Single tone - 2-channel mode – 3.2 GSps							
At -1 dBFS output level							
Fin = 98 MHz	4	SFDR dBFS		71.8	71.8		(1)(2)(3)(4)(5)(6)
Fin = 778 MHz	4			68.3	68.3		
Fin = 1578 MHz	4			61.8	67.2		
Fin = 2230 MHz	4			63.2	69.5		
Fin = 2378 MHz	4			61.5			
Fin = 3178 MHz	4			56.0	61.5		
Fin = 3978 MHz	4			47.9	48.6		
Fin = 4778 MHz	4			42.5	45.0		
Fin = 5578 MHz	4			38.0	64.3		
At -3 dBFS output level							
Fin = 98 MHz	4	SFDR dBFS		68.1	68.3		(1)(2)(3)(4)(5)(6)
Fin = 778 MHz	4			66.2	73.3		
Fin = 1578 MHz	4			65.5	68.0		
Fin = 2230 MHz	4			64.8			
Fin = 2378 MHz	4			64.0	74.4		
Fin = 3178 MHz	4			59.2	68.3		
Fin = 3978 MHz	4			50.3	55.8		
Fin = 4778 MHz	4			44.3	50.1		
Fin = 5578 MHz	4			40.2	58.1		
At -8 dBFS output level							
Fin = 98 MHz	4	SFDR dBFS		76.7	71.7		(1)(2)(3)(4)(5)(6)
Fin = 778 MHz	4			70.9	69.6		
Fin = 1578 MHz	4			69.8	70.2		
Fin = 2230 MHz	4			71.3			
Fin = 2378 MHz	4			68.3	70.4		
Fin = 3178 MHz	4			64.1	67.8		
Fin = 3978 MHz	4			55.7	70.1		
Fin = 4778 MHz	4			49.4	61.5		
Fin = 5578 MHz	4			45.4	65.4		
At -12 dBFS output level							
Fin = 98 MHz	4	SFDR dBFS		76.3	75.7		(1)(2)(3)(4)(5)(6)
Fin = 778 MHz	4			74.0	73.5		
Fin = 1578 MHz	4			72.2	76.4		
Fin = 2230 MHz	4			73.9			
Fin = 2378 MHz	4			72.1	76.7		
Fin = 3178 MHz	4			70.6	69.7		
Fin = 3978 MHz	4			59.7	75.3		
Fin = 4778 MHz	4			53.7	71.0		
Fin = 5578 MHz	4			49.6	68.1		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ	Max	Note
IMD3 - InterModulation Distortion (third order) – Dual tone -2 channel mode – 3.2 GSps						
At -7 dBFS output level - Δ FIN = 10 MHz						
Fin = 100 MHz	4	IMD3 dBFS		62		(1)
Fin = 700 MHz	4			62		
Fin = 1500 MHz	4			63		
Fin = 2300 MHz	4			61		
Fin = 3100 MHz	4			58		
Fin = 3900 MHz	4			53		
Fin = 4700 MHz	4			46		
Fin = 5500 MHz	4			38		
Fin = 5900 MHz	4			35		
At -9 dBFS output level - Δ FIN = 10 MHz						
Fin = 100 MHz	4	IMD3 dBFS		64		(1)
Fin = 700 MHz	4			63		
Fin = 1500 MHz	4			64		
Fin = 2300 MHz	4			64		
Fin = 3100 MHz	4			62		
Fin = 3900 MHz	4			59		
Fin = 4700 MHz	4			53		
Fin = 5500 MHz	4			47		
Fin = 5900 MHz	4			43		
At -14 dBFS output level - Δ FIN = 10 MHz						
Fin = 100 MHz	4	IMD3 dBFS		68		(1)
Fin = 700 MHz	4			67		
Fin = 1500 MHz	4			67		
Fin = 2300 MHz	4			69		
Fin = 3100 MHz	4			68		
Fin = 3900 MHz	4			69		
Fin = 4700 MHz	4			65		
Fin = 5500 MHz	4			62		
Fin = 5900 MHz	4			59		
At -18 dBFS output level - Δ FIN = 10 MHz						
Fin = 100 MHz	4	IMD3 dBFS		74		(1)
Fin = 700 MHz	4			72		
Fin = 1500 MHz	4			72		
Fin = 2300 MHz	4			75		
Fin = 3100 MHz	4			73		
Fin = 3900 MHz	4			76		
Fin = 4700 MHz	4			74		
Fin = 5500 MHz	4			70		
Fin = 5900 MHz	4			70		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ		Max	Note
				Nominal	Without H2 – H3		
THD - Total harmonic distortion - Single tone - 2-channel mode – 3.2 GSps							
At -1 dBFS output level							
Fin = 98 MHz	4	THD dBFS		-70.0	-70.7		
Fin = 778 MHz	4			-70.7	-72.3		
Fin = 1578 MHz	4			-62.3	-65.7		
Fin = 2230 MHz	4			-63.7			
Fin = 2378 MHz	4			-62.5	-66.9		
Fin = 3178 MHz	4			-56.5	-67.5		
Fin = 3978 MHz	4			-51.0	-63.3		
Fin = 4778 MHz	4			-47.8	-70.1		
Fin = 5578 MHz	4			-48.0	-69.5		
At -3 dBFS output level							
Fin = 98 MHz	4	THD dBFS		-64.8	-67.3		
Fin = 778 MHz	4			-68.3	-70.5		
Fin = 1578 MHz	4			-66.5	-66.9		
Fin = 2230 MHz	4			-66.3			
Fin = 2378 MHz	4			-67.0	-68.2		
Fin = 3178 MHz	4			-63.8	-70.9		
Fin = 3978 MHz	4			-58.5	-68.3		
Fin = 4778 MHz	4			-52.9	-71.0		
Fin = 5578 MHz	4			-52.1	-71.2		
At -8 dBFS output level							
Fin = 98 MHz	4	THD dBFS		-70.5	-71.9		
Fin = 778 MHz	4			-69.1	-71.8		
Fin = 1578 MHz	4			-68.3	-71.5		
Fin = 2230 MHz	4			-70.0			
Fin = 2378 MHz	4			-68.7	-71.1		
Fin = 3178 MHz	4			-65.0	-70.7		
Fin = 3978 MHz	4			-68.9	-71.4		
Fin = 4778 MHz	4			-62.5	-70.4		
Fin = 5578 MHz	4			-64.1	-71.9		
At -12 dBFS output level							
Fin = 98 MHz	4	THD dBFS		-70.7	-70.8		
Fin = 778 MHz	4			-70.0	-70.6		
Fin = 1578 MHz	4			-70.6	-70.0		
Fin = 2230 MHz	4			-70.8			
Fin = 2378 MHz	4			-69.9	-69.9		
Fin = 3178 MHz	4			-69.0	-69.8		
Fin = 3978 MHz	4			-69.6	-69.9		
Fin = 4778 MHz	4			-67.9	-69.6		
Fin = 5578 MHz	4			-69.7	-69.9		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ		Max	Note
				Nominal	ILG recal at Fin (**)		
TILD - Total InterLeaving Distortion - Single tone - 2-channel mode – 3.2 GSps							
At -1 dBFS output level							
Fin = 98 MHz	4	TILD dBFS		-68.7	-69.4		(1) (4) (5)
Fin = 778 MHz	4			-63.5	-67.0		
Fin = 1578 MHz	4			-62.2	-70.3		
Fin = 2230 MHz	1A/1C			-65.4			
Fin = 2378 MHz	4			-63.5	-72.3		
Fin = 3178 MHz	4			-58.4	-67.9		
Fin = 3978 MHz	4			-49.0	-65.3		
Fin = 4778 MHz	4			-43.3	-63.1		
Fin = 5578 MHz	4			-38.8	-63.5		
At -3 dBFS output level							
Fin = 98 MHz	4	TILD dBFS		-69.3	-73.1		(1) (4) (5)
Fin = 778 MHz	4			-65.6	-72.8		
Fin = 1578 MHz	4			-64.1	-68.1		
Fin = 2230 MHz	4			-65.6			
Fin = 2378 MHz	4			-65.2	-72.9		
Fin = 3178 MHz	4			-59.9	-69.8		
Fin = 3978 MHz	4			-51.0	-67.9		
Fin = 4778 MHz	4			-45.1	-68.7		
Fin = 5578 MHz	4			-40.9	-65.9		
At -8 dBFS output level							
Fin = 98 MHz	4	TILD dBFS		-75.5	-72.2		(1) (4) (5)
Fin = 778 MHz	4			-61.3	-75.5		
Fin = 1578 MHz	4			-69.3	-78.9		
Fin = 2230 MHz	4			-70.5			
Fin = 2378 MHz	4			-70.3	-77.6		
Fin = 3178 MHz	4			-66.5	-79.1		
Fin = 3978 MHz	4			-56.2	-77.4		
Fin = 4778 MHz	4			-50.1	-76.0		
Fin = 5578 MHz	4			-46.0	-65.1		
At -12 dBFS output level							
Fin = 98 MHz	4	TILD dBFS		-78.2	-78.3		(1) (4) (5)
Fin = 778 MHz	4			-73.5	-74.3		
Fin = 1578 MHz	4			-73.2	-80.1		
Fin = 2230 MHz	4			-76.1			
Fin = 2378 MHz	4			-75.7	-78.7		
Fin = 3178 MHz	4			-70.4	-78.7		
Fin = 3978 MHz	4			-59.8	-80.3		
Fin = 4778 MHz	4			-54.0	-77.4		
Fin = 5578 MHz	4			-50.0	-68.1		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ		Max	Note
				Nominal	Averaged Simult. Sampling		
SNR - Signal to noise ratio - Single tone - 2-channel mode – 3.2 GSps							
At -1 dBFS output level							
Fin = 98 MHz	4	SNR dBFS		54.3	57.1		
Fin = 778 MHz	4			53.9	56.7		
Fin = 1578 MHz	4			53.1	55.9		
Fin = 2230 MHz	4			51.0			
Fin = 2378 MHz	4			51.0	53.7		
Fin = 3178 MHz	4			50.0	52.7		
Fin = 3978 MHz	4			49.0	51.6		
Fin = 4778 MHz	4			48.0	50.6		
Fin = 5578 MHz	4			47.1	49.5		
At -3 dBFS output level							
Fin = 98 MHz	4	SNR dBFS		54.4	57.1		
Fin = 778 MHz	4			54.1	56.9		
Fin = 1578 MHz	4			53.6	56.3		
Fin = 2230 MHz	4			51.7			
Fin = 2378 MHz	4			51.7	54.3		
Fin = 3178 MHz	4			50.9	53.5		
Fin = 3978 MHz	4			50.1	52.7		
Fin = 4778 MHz	4			49.3	51.9		
Fin = 5578 MHz	4			48.6	51.0		
At -8 dBFS output level							
Fin = 98 MHz	4	SNR dBFS		54.6	57.4		
Fin = 778 MHz	4			54.6	57.3		
Fin = 1578 MHz	4			54.3	57.1		
Fin = 2230 MHz	4			52.6			
Fin = 2378 MHz	4			52.6	55.4		
Fin = 3178 MHz	4			52.3	55.1		
Fin = 3978 MHz	4			51.9	54.7		
Fin = 4778 MHz	4			51.6	54.2		
Fin = 5578 MHz	4			51.1	53.8		
At -12 dBFS output level							
Fin = 98 MHz	4	SNR dBFS		54.8	57.6		
Fin = 778 MHz	4			54.7	57.6		
Fin = 1578 MHz	4			54.6	57.4		
Fin = 2230 MHz	4			53.0			
Fin = 2378 MHz	4			53.0	55.8		
Fin = 3178 MHz	4			52.9	55.7		
Fin = 3978 MHz	4			52.7	55.5		
Fin = 4778 MHz	4			52.5	55.3		
Fin = 5578 MHz	4			52.3	55.1		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typical			Max	Note
				Nominal	Averaged Simult. Sampling(*)	ILG recal at Fin (**)		
SINAD - Signal to noise and distortion ratio - Single tone - 2-channel mode – 3.2 GSps								
At -1 dBFS output level								
Fin = 98 MHz	4	SINAD dBFS		53.9	56.9	54.1		(1)(4)(5)
Fin = 778 MHz	4			53.2	56.5	53.6		
Fin = 1578 MHz	4			52.0	54.8	52.7		
Fin = 2230 MHz	4			50.5				
Fin = 2378 MHz	4			50.4	52.8	50.9		
Fin = 3178 MHz	4			48.5	50.4	49.5		
Fin = 3978 MHz	4			44.8	46.0	45.6		
Fin = 4778 MHz	4			41.0	43.5	43.1		
Fin = 5578 MHz	4			37.8	44.5	46.8		
At -3 dBFS output level								
Fin = 98 MHz	4	SINAD dBFS		53.8	56.4	54.0		(1) (4) (5)
Fin = 778 MHz	4			53.4	56.5	54.0		
Fin = 1578 MHz	4			52.9	55.9	53.2		
Fin = 2230 MHz	4			51.3				
Fin = 2378 MHz	4			51.2	54.0	51.6		
Fin = 3178 MHz	4			50.1	52.9	50.7		
Fin = 3978 MHz	4			47.1	50.2	48.9		
Fin = 4778 MHz	4			43.2	47.3	46.4		
Fin = 5578 MHz	4			39.9	47.3	47.8		
At -8 dBFS output level								
Fin = 98 MHz	4	SINAD dBFS		54.4	57.3	54.4		(1) (4) (5)
Fin = 778 MHz	4			54.3	57.0	54.3		
Fin = 1578 MHz	4			54.0	56.8	54.1		
Fin = 2230 MHz	4			52.4				
Fin = 2378 MHz	4			52.4	55.2	52.5		
Fin = 3178 MHz	4			51.8	54.6	52.1		
Fin = 3978 MHz	4			50.4	54.3	51.8		
Fin = 4778 MHz	4			47.5	53.0	51.0		
Fin = 5578 MHz	4			44.6	52.8	50.8		
At -12 dBFS output level								
Fin = 98 MHz	4	SINAD dBFS		54.6	57.4	54.7		(1) (4) (5)
Fin = 778 MHz	4			54.5	57.4	54.6		
Fin = 1578 MHz	4			54.4	57.2	54.5		
Fin = 2230 MHz	4			52.9				
Fin = 2378 MHz	4			52.9	55.6	53.0		
Fin = 3178 MHz	4			52.7	55.5	52.7		
Fin = 3978 MHz	4			51.9	55.3	52.6		
Fin = 4778 MHz	4			50.1	54.9	52.4		
Fin = 5578 MHz	4			47.9	54.8	52.2		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ			Max	Note
				Nominal	Averaged Simult. Sampling(*)	ILG recal at Fin(**)		
ENOB - Effective Number Of Bits - Single tone - 2-channel mode – 3.2 GSps								
At -1 dBFS output level								
Fin = 98 MHz	4	ENOB Bit_FS		8.7	9.2	8.7		(1) (4) (5)
Fin = 778 MHz	4			8.6	9.1	8.6		
Fin = 1578 MHz	4			8.4	8.8	8.5		
Fin = 2230 MHz	4			8.1				
Fin = 2378 MHz	4			8.1	8.5	8.2		
Fin = 3178 MHz	4			7.7	8.1	7.9		
Fin = 3978 MHz	4			7.1	7.3	7.3		
Fin = 4778 MHz	4			6.5	6.9	6.9		
Fin = 5578 MHz	4			6.0	7.1	7.5		
At -3 dBFS output level								
Fin = 98 MHz	4	ENOB Bit_FS		8.7	9.1	8.7		(1) (4) (5)
Fin = 778 MHz	4			8.6	9.1	8.7		
Fin = 1578 MHz	4			8.5	9.0	8.5		
Fin = 2230 MHz	4			8.2				
Fin = 2378 MHz	4			8.2	8.7	8.3		
Fin = 3178 MHz	4			8.0	8.5	8.1		
Fin = 3978 MHz	4			7.5	8.0	7.8		
Fin = 4778 MHz	4			6.9	7.6	7.4		
Fin = 5578 MHz	4			6.3	7.6	7.7		
At -8 dBFS output level								
Fin = 98 MHz	4	ENOB Bit_FS		8.7	9.2	8.7		(1) (4) (5)
Fin = 778 MHz	4			8.7	9.2	8.7		
Fin = 1578 MHz	4			8.7	9.1	8.7		
Fin = 2230 MHz	4			8.4				
Fin = 2378 MHz	4			8.4	8.9	8.4		
Fin = 3178 MHz	4			8.3	8.8	8.4		
Fin = 3978 MHz	4			8.1	8.7	8.3		
Fin = 4778 MHz	4			7.6	8.5	8.2		
Fin = 5578 MHz	4			7.1	8.5	8.2		
At -12 dBFS output level								
Fin = 98 MHz	4	ENOB Bit_FS		8.8	9.2	8.8		(1) (4) (5)
Fin = 778 MHz	4			8.8	9.2	8.8		
Fin = 1578 MHz	4			8.8	9.2	8.8		
Fin = 2230 MHz	4			8.5				
Fin = 2378 MHz	4			8.5	9.0	8.5		
Fin = 3178 MHz	4			8.5	8.9	8.5		
Fin = 3978 MHz	4			8.3	8.9	8.5		
Fin = 4778 MHz	4			8.0	8.8	8.4		
Fin = 5578 MHz	4			7.6	8.8	8.4		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ	Max	Note
NSD - Noise Spectral Density - 2-channel mode – 3.2 GSps						
At -1 dBFS output level						
1st Nyquist (NFPBW)		NSD dBm/Hz		-146		(1)
2nd Nyquist (EFPBW)				-143		
At -8 dBFS output level						
1st Nyquist (NFPBW)		NSD dBm/Hz		-147		(1)
2nd Nyquist (EFPBW)				-145		
NPR - Noise Power Ratio - 2-channel mode – 3.2 GSps						
At loading factor = -12 dBFS - 1280 MHz noise pattern width - 5 MHz notch centered at Fs/4						
1st Nyquist (NFPBW)		NPR dB		43		(1)
At loading factor = -12 dBFS - 1280 MHz noise pattern width - 5 MHz notch centered at 3Fs/4						
2nd Nyquist (EFPBW)		NPR dB		39		

(*) Averaged Simul.Sampling :
Simultaneous sampling is obtained by setting the 4 cores in phase (CLK_MODE_SEL = 0b11, see §6.3 Register map).
Average simultaneous sampling is obtained by averaging the samples of the 4 cores when they are in phase.

(**) **ILG recal at Fin:**
Performance after recalibration at measurement frequency

Notes:

1. Optimal bandwidth selection depends on signal characteristics. The bandwidth selection allows optimizing noise and linearity trade-off. For signals below 1.5 GHz, the bandwidth selection must be set to Nominal. For signals beyond this frequency, the bandwidth select must be set to Extended. The extended bandwidth degrades noise floor up to 1dB, compensated at high frequency by inputing signals with lower signal attenuation.
2. Linearity of high frequencies is dominated by H3 and H2, stepping back 3 or 6 dB on input signals involving signifiant improvement on SFDR figures. For narrow band operation (10 MHz or 50 MHz), a carefuly chosen frequency plan allows rejection of these folded harmonics up to H8 beyond the band of interest.
3. SFDR without H3 harmonic is better than 60 dBFS at -1 dBFS. Removing H2 and H3 allows an SFDR performance higher than 68 dBFS up to 5580 MHz. H3 dominates up to 5300 MHz, then H2 dominates above 5300 MHz.
4. For input frequencies < 800 MHz, the SFDR is given with the interleaving calibration set CALSET2. For input frequencies > 800 MHz, the SFDR is given with CALSET0.
5. Interleaving performance (1-channel and 2-channel mode) are given for IN0 only. For IN3, interleaving calibration must be done to achieve those performance.
6. Adjustment of input common mode can also be used to optimize ADC linearity.

3.10 Dynamic Performance - 1-channel mode – 6.4 GSps

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ		Max	Note
				Nominal	ILG recal at Fin(**)		
SFDR - Spurious Free Dynamic Range - Single tone - 1-channel mode – 6.4 GSps							
At -1 dBFS output level							
Fin = 98 MHz	4	SFDR dBFS		66.2	70.4		(1)(2)(3) (4)(5)(6)
Fin = 778 MHz	4			63.1	73.4		
Fin = 1578 MHz	4			56.2	64.5		
Fin = 2230 MHz	1A/1D		53(*)	64.7			
Fin = 2378 MHz	4			62.4	64.0		
Fin = 3178 MHz	4			52.3	55.3		
Fin = 3978 MHz	4			46.3	48.3		
Fin = 4778 MHz	4			42.5	44.7		
Fin = 5578 MHz	4			39.8	46.7		
At -3 dBFS output level							
Fin = 98 MHz	4	SFDR dBFS		66.7	67.4		(1)(2)(3) (4) (5)(6)
Fin = 778 MHz	4			64.5	72.2		
Fin = 1578 MHz	4			58.8	68.9		
Fin = 2230 MHz	4			67.2			
Fin = 2378 MHz	4			63.8	69.0		
Fin = 3178 MHz	4			54.5	63.5		
Fin = 3978 MHz	4			48.1	55.5		
Fin = 4778 MHz	4			44.4	49.8		
Fin = 5578 MHz	4			41.8	51.7		
At -8 dBFS output level							
Fin = 98 MHz	4	SFDR dBFS		67.8	73.1		(1)(2)(3) (4) (5)(6)
Fin = 778 MHz	4			67.3	70.4		
Fin = 1578 MHz	4			63.6	70.9		
Fin = 2230 MHz	4			69.1			
Fin = 2378 MHz	4			68.1	72.9		
Fin = 3178 MHz	4			59.3	66.0		
Fin = 3978 MHz	4			53.2	69.7		
Fin = 4778 MHz	4			49.4	61.4		
Fin = 5578 MHz	4			46.8	62.9		
At -12 dBFS output level							
Fin = 98 MHz	4	SFDR dBFS		67.0	74.0		(1)(2)(3) (4) (5)(6)
Fin = 778 MHz	4			68.0	74.7		
Fin = 1578 MHz	4			66.1	75.2		
Fin = 2230 MHz	4			67.5			
Fin = 2378 MHz	4			69.4	74.0		
Fin = 3178 MHz	4			63.7	75.0		
Fin = 3978 MHz	4			57.4	74.1		
Fin = 4778 MHz	4			53.5	70.0		
Fin = 5578 MHz	4			50.9	67.3		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ	Max	Note
IMD3 - InterModulation Distortion (third order) – Dual tone -1 channel mode – 6.4 GSps						
At -7 dBFS output level - Δ FIN = 10 MHz						
Fin = 100 MHz	4	IMD3 dBFS		62		(1)
Fin = 700 MHz	4			63		
Fin = 1500 MHz	4			63		
Fin = 2300 MHz	4			61		
Fin = 3100 MHz	4			58		
Fin = 3900 MHz	4			54		
Fin = 4700 MHz	4			46		
Fin = 5500 MHz	4			39		
Fin = 5900 MHz	4			36		
At -9 dBFS output level - Δ FIN = 10 MHz						
Fin = 100 MHz	4	IMD3 dBFS		64		(1)
Fin = 700 MHz	4			64		
Fin = 1500 MHz	4			65		
Fin = 2300 MHz	4			64		
Fin = 3100 MHz	4			63		
Fin = 3900 MHz	4			59		
Fin = 4700 MHz	4			53		
Fin = 5500 MHz	4			47		
Fin = 5900 MHz	4			44		
At -14 dBFS output level - Δ FIN = 10 MHz						
Fin = 100 MHz	4	IMD3 dBFS		68		(1)
Fin = 700 MHz	4			67		
Fin = 1500 MHz	4			67		
Fin = 2300 MHz	4			69		
Fin = 3100 MHz	4			68		
Fin = 3900 MHz	4			69		
Fin = 4700 MHz	4			66		
Fin = 5500 MHz	4			62		
Fin = 5900 MHz	4			61		
At -18 dBFS output level - Δ FIN = 10 MHz						
Fin = 100 MHz	4	IMD3 dBFS		74		(1)
Fin = 700 MHz	4			73		
Fin = 1500 MHz	4			72		
Fin = 2300 MHz	4			75		
Fin = 3100 MHz	4			73		
Fin = 3900 MHz	4			76		
Fin = 4700 MHz	4			74		
Fin = 5500 MHz	4			71		
Fin = 5900 MHz	4			70		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ		Max	Note
				Nominal mode	Without H2 – H3		
THD - Total harmonic distortion - Single tone - 1-channel mode – 6.4 GSps							
At -1 dBFS output level							
Fin = 98 MHz	4	THD dBFS		-70.2	-71.1		(1) (4)
Fin = 778 MHz	4			-70.2	-72.9		
Fin = 1578 MHz	4			-61.7	-65.8		
Fin = 2230 MHz	1A/1D			-62.9		-54	
Fin = 2378 MHz	4			-61.3	-67.4		
Fin = 3178 MHz	4			-55.5	-67.5		
Fin = 3978 MHz	4			-49.3	-63.6		
Fin = 4778 MHz	4			-45.1	-71.3		
Fin = 5578 MHz	4			-45.8	-70.8		
At -3 dBFS output level							
Fin = 98 MHz	4	THD dBFS		-64.7	-67.8		(1) (4)
Fin = 778 MHz	4			-68.7	-70.9		
Fin = 1578 MHz	4			-66.5	-67.3		
Fin = 2230 MHz	4			-66.6			
Fin = 2378 MHz	4			-66.9	-68.5		
Fin = 3178 MHz	4			-63.3	-71.8		
Fin = 3978 MHz	4			-56.4	-68.6		
Fin = 4778 MHz	4			-50.4	-71.2		
Fin = 5578 MHz	4			-50.1	-71.1		
At -8 dBFS output level							
Fin = 98 MHz	4	THD dBFS		-71.0	-73.7		(1) (4)
Fin = 778 MHz	4			-69.0	-73.4		
Fin = 1578 MHz	4			-68.8	-73.2		
Fin = 2230 MHz	4			-70.4			
Fin = 2378 MHz	4			-69.5	-72.8		
Fin = 3178 MHz	4			-52.1	-72.4		
Fin = 3978 MHz	4			-68.3	-72.8		
Fin = 4778 MHz	4			-61.1	-71.2		
Fin = 5578 MHz	4			-62.9	-73.5		
At -12 dBFS output level							
Fin = 98 MHz	4	THD dBFS		-72.2	-73.2		(1) (4)
Fin = 778 MHz	4			-71.4	-72.8		
Fin = 1578 MHz	4			-71.2	-71.8		
Fin = 2230 MHz	4			-73.0			
Fin = 2378 MHz	4			-70.7	-71.7		
Fin = 3178 MHz	4			-69.9	-71.7		
Fin = 3978 MHz	4			-70.7	-71.9		
Fin = 4778 MHz	4			-68.2	-71.8		
Fin = 5578 MHz	4			-70.4	-72.1		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ		Max	Note
				Nominal	ILG recal at Fin (**)		
TILD - Total InterLeaving Distortion - Single tone - 1-channel mode – 6.4 GSps							
At -1 dBFS output level							
Fin = 98 MHz	4	TILD dBFS		-62.7	-67.1		(1) (4) (5)
Fin = 778 MHz	4			-59.6	-69.5		
Fin = 1578 MHz	4			-57.1	-68.3		
Fin = 2230 MHz	1A/1D			-61.8		-51(*)	
Fin = 2378 MHz	4			-60.5	-64.4		
Fin = 3178 MHz	4			-51.8	-66.9		
Fin = 3978 MHz	4			-46.0	-65.3		
Fin = 4778 MHz	4			-41.8	-61.7		
Fin = 5578 MHz	4			-38.3	-59.5		
At -3 dBFS output level							
Fin = 98 MHz	4	TILD dBFS		-64.3	-68.0		(1) (4) (5)
Fin = 778 MHz	4			-62.5	-70.0		
Fin = 1578 MHz	4			-58.8	-69.8		
Fin = 2230 MHz	4			-64.1			
Fin = 2378 MHz	4			-61.7	-66.9		
Fin = 3178 MHz	4			-54.0	-69.0		
Fin = 3978 MHz	4			-48.0	-67.6		
Fin = 4778 MHz	4			-43.7	-63.2		
Fin = 5578 MHz	4			-40.5	-58.5		
At -8 dBFS output level							
Fin = 98 MHz	4	TILD dBFS		-67.1	-70.8		(1) (4) (5)
Fin = 778 MHz	4			-65.9	-69.9		
Fin = 1578 MHz	4			-61.6	-70.8		
Fin = 2230 MHz	4			-66.1			
Fin = 2378 MHz	4			-65.4	-70.7		
Fin = 3178 MHz	4			-60.6	-72.9		
Fin = 3978 MHz	4			-53.0	-70.0		
Fin = 4778 MHz	4			-48.8	-66.3		
Fin = 5578 MHz	4			-45.6	-60.7		
At -12 dBFS output level							
Fin = 98 MHz	4	TILD dBFS		-66.9	-72.8		(1) (4) (5)
Fin = 778 MHz	4			-66.8	-73.3		
Fin = 1578 MHz	4			-63.5	-73.3		
Fin = 2230 MHz	4			-66.2			
Fin = 2378 MHz	4			-67.3	-71.0		
Fin = 3178 MHz	4			-62.2	-74.1		
Fin = 3978 MHz	4			-56.8	-70.8		
Fin = 4778 MHz	4			-52.9	-67.0		
Fin = 5578 MHz	4			-49.6	-63.4		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ	Max	Note
SNR - Signal to noise ratio - Single tone - 1-channel mode – 6.4 GSps						
At -1 dBFS output level						
Fin = 98 MHz	4	SNR dBFS		54.2		(1) (4) (5)
Fin = 778 MHz	4			53.9		
Fin = 1578 MHz	4			53.1		
Fin = 2230 MHz	1A/1D		49	51.0		
Fin = 2378 MHz	4			51.0		
Fin = 3178 MHz	4			50.0		
Fin = 3978 MHz	4			49.0		
Fin = 4778 MHz	4			48.0		
Fin = 5578 MHz	4			47.1		
At -3 dBFS output level						
Fin = 98 MHz	4	SNR dBFS		54.3		(1) (4) (5)
Fin = 778 MHz	4			54.1		
Fin = 1578 MHz	4			53.6		
Fin = 2230 MHz	4			51.7		
Fin = 2378 MHz	4			51.7		
Fin = 3178 MHz	4			50.9		
Fin = 3978 MHz	4			50.1		
Fin = 4778 MHz	4			49.3		
Fin = 5578 MHz	4			48.5		
At -8 dBFS output level						
Fin = 98 MHz	4	SNR dBFS		54.5		(1) (4) (5)
Fin = 778 MHz	4			54.5		
Fin = 1578 MHz	4			54.3		
Fin = 2230 MHz	4			52.6		
Fin = 2378 MHz	4			52.6		
Fin = 3178 MHz	4			52.9		
Fin = 3978 MHz	4			51.9		
Fin = 4778 MHz	4			51.5		
Fin = 5578 MHz	4			51.1		
At -12 dBFS output level						
Fin = 98 MHz	4	SNR dBFS		54.7		(1) (4) (5)
Fin = 778 MHz	4			54.7		
Fin = 1578 MHz	4			54.6		
Fin = 2230 MHz	4			53.0		
Fin = 2378 MHz	4			53.0		
Fin = 3178 MHz	4			52.9		
Fin = 3978 MHz	4			52.7		
Fin = 4778 MHz	4			52.5		
Fin = 5578 MHz	4			52.3		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ		Max	Note
				Nominal mode	ILG recal at Fin (**)		
SINAD - Signal to noise and distortion ratio - Single tone - 1-channel mode – 6.4 GSps							
At -1 dBFS output level							
Fin = 98 MHz	4	SINAD dBFS		53.5	54.0		(1) (4) (5)
Fin = 778 MHz	4			52.8	53.8		
Fin = 1578 MHz	4			51.2	52.5		
Fin = 2230 MHz	1A/1D		48(*)	50.4			
Fin = 2378 MHz	4			50.2	50.6		
Fin = 3178 MHz	4			47.1	48.7		
Fin = 3978 MHz	4			43.1	45.1		
Fin = 4778 MHz	4			39.5	42.9		
Fin = 5578 MHz	4			37.1	42.3		
At -3 dBFS output level							
Fin = 98 MHz	4	SINAD dBFS		53.5	53.9		(1) (4) (5)
Fin = 778 MHz	4			53.4	53.9		
Fin = 1578 MHz	4			52.2	53.4		
Fin = 2230 MHz	4			51.3			
Fin = 2378 MHz	4			51.1	51.5		
Fin = 3178 MHz	4			49.0	50.6		
Fin = 3978 MHz	4			45.5	48.6		
Fin = 4778 MHz	4			42.0	46.2		
Fin = 5578 MHz	4			39.5	45.4		
At -8 dBFS output level							
Fin = 98 MHz	4	SINAD dBFS		54.2	54.5		(1) (4) (5)
Fin = 778 MHz	4			54.0	54.3		
Fin = 1578 MHz	4			53.4	54.2		
Fin = 2230 MHz	4			52.3			
Fin = 2378 MHz	4			52.3	52.5		
Fin = 3178 MHz	4			51.2	52.1		
Fin = 3978 MHz	4			49.4	51.8		
Fin = 4778 MHz	4			46.8	50.9		
Fin = 5578 MHz	4			44.4	50.4		
At -12 dBFS output level							
Fin = 98 MHz	4	SINAD dBFS		54.4	54.7		(1) (4) (5)
Fin = 778 MHz	4			54.3	54.6		
Fin = 1578 MHz	4			54.0	54.6		
Fin = 2230 MHz	4			52.7			
Fin = 2378 MHz	4			52.8	53.0		
Fin = 3178 MHz	4			52.3	52.9		
Fin = 3978 MHz	4			51.2	52.7		
Fin = 4778 MHz	4			49.6	52.3		
Fin = 5578 MHz	4			47.7	51.9		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ		Max	Note
				Nominal	ILG recal at Fin		
ENOB - Effective Number Of Bits - Single tone - 1-channel mode – 6.4 GSps							
At -1 dBFS output level							
Fin = 98 MHz	4	ENOB Bit_FS		8.6	8.7		(1) (4) (5)
Fin = 778 MHz	4			8.5	8.6		
Fin = 1578 MHz	4			8.2	8.4		
Fin = 2230 MHz	1A/1D		7.7(*)	8.1			
Fin = 2378 MHz	4			8.0	8.1		
Fin = 3178 MHz	4			7.5	7.8		
Fin = 3978 MHz	4			6.9	7.2		
Fin = 4778 MHz	4			6.3	6.8		
Fin = 5578 MHz	4			5.9	6.7		
At -3 dBFS output level							
Fin = 98 MHz	4	ENOB Bit_FS		8.6	8.7		(1) (4) (5)
Fin = 778 MHz	4			8.6	8.7		
Fin = 1578 MHz	4			8.4	8.6		
Fin = 2230 MHz	4			8.2			
Fin = 2378 MHz	4			8.2	8.3		
Fin = 3178 MHz	4			7.8	8.1		
Fin = 3978 MHz	4			7.3	7.8		
Fin = 4778 MHz	4			6.7	7.4		
Fin = 5578 MHz	4			6.3	7.2		
At -8 dBFS output level							
Fin = 98 MHz	4	ENOB Bit_FS		8.7	8.8		(1) (4) (5)
Fin = 778 MHz	4			8.7	8.7		
Fin = 1578 MHz	4			8.6	8.7		
Fin = 2230 MHz	4			8.4			
Fin = 2378 MHz	4			8.4	8.4		
Fin = 3178 MHz	4			8.2	8.4		
Fin = 3978 MHz	4			7.9	8.3		
Fin = 4778 MHz	4			7.5	8.2		
Fin = 5578 MHz	4			7.1	8.1		
At -12 dBFS output level							
Fin = 98 MHz	4	ENOB Bit_FS		8.7	8.8		(1) (4) (5)
Fin = 778 MHz	4			8.7	8.8		
Fin = 1578 MHz	4			8.7	8.8		
Fin = 2230 MHz	4			8.5			
Fin = 2378 MHz	4			8.5	8.5		
Fin = 3178 MHz	4			8.4	8.5		
Fin = 3978 MHz	4			8.2	8.5		
Fin = 4778 MHz	4			7.9	8.4		
Fin = 5578 MHz	4			7.6	8.3		

Parameter	Test Level AQ600/AQ605	Symbol Unit	Min	Typ	Max	Note
NSD - Noise Spectral Density - 1-channel mode – 6.4 GSps						
At -1 dBFS output level						
1st Nyquist (NFPBW)	4	NSD dBm/Hz		-148		
At -8 dBFS output level						
1st Nyquist (NFPBW)	4	NSD dBm/Hz		-149		
2nd Nyquist (EFPBW)	4			-147		
NPR - Noise Power Ratio - 1-channel mode – 6.4 GSps						
At loading factor = -12 dBFS – 2560 MHz noise pattern width - 5 MHz notch centered at Fs/4						
1st Nyquist (NFPBW)	4	NPR dB		44		

(*): Performance with temperature interpolation for the AQ600 and performance with customer recalibration for AQ605

(**) ILG recal at Fin: Performance after recalibration at measurement frequency

Notes:

1. Optimal bandwidth selection depends on signal characteristics. The bandwidth selection allows optimizing noise and linearity trade-off. For signals below 1.5 GHz, the bandwidth selection must be set to Nominal. For signals beyond this frequency, the bandwidth select must be set to Extended. The extended bandwidth degrades noise floor up to 1dB, compensated at high frequency by inputing signals with lower signal attenuation.
2. Linearity of high frequencies is dominated by H3 and H2, stepping back 3 or 6 dB on input signals involving signifiant improvement on SFDR figures. For narrow band operation (10 MHz or 50 MHz), a carefuly chosen frequency plan allows rejection of these folded harmonics up to H8 beyond the band of interest.
3. SFDR without H3 harmonic is better than 60 dB_{FS} at -1 dB_{FS}. Removing H2 and H3 allows an SFDR performance higher than 68 dB_{FS} up to 5580 MHz. H3 dominates up to 5300 MHz, then H2 dominates above 5300 MHz.
4. For input frequencies < 800 MHz, the SFDR is given for with interleaving calibration set CALSET2. For input frequencies > 800 MHz, the SFDR is given with CALSET0. See 8.3.
5. Interleaving performance (1-channel and 2-channel mode) are given for IN0 only. For IN3, interleaving calibration must be done to achieve those performances.
6. Adjustment of input common mode can also be used to optimize ADC linearity.

3.11 Transient, Switching and Timing Characteristics

Unless otherwise specified:

- Typical values are given for typical supplies VCCA = 3.3 V, VCCD = 1.2 V, VCCO = 2.5 V at room temperature with Fclk = 6.4 GHz and with nominal mode of the SPI (SDA, CLKOUT and SYNCO disabled).
- Minimum and Maximum values are given over temperature and power supplies.
- ADC output level -1 dBFS.
- Clock input differentially driven @ +1 dBm at ADC input.
- Non interleaved ADC.
- Reduced swing.

Table 8. Transient characteristics

Parameter	Test level	Symbol	Min	Typ	Max	Unit	Note
TRANSIENT PERFORMANCE							
Conversion Error Rate at 1.6 GSps Less than 128 LSB (TBC)	4	CER		$10E^{-15}$		Error/ sample	(1)
Serial link Bit Error Rate at 12.8 Gbps	4	BER		$10E^{-16}$		Error/ sample	
Overvoltage Recovery Time	5	ORT		625		ps	

Notes:

1. Measured with 95% confidence level and a threshold of 100 LSB (<2.5% full scale). Fs = 1.6 GSps, T_J = 110 °C. For Tj=125 °C, CER value is $10E^{-12}$

Table 9. Switching characteristics

Parameters	Test level	Symbol	Min	Typ	Max	Unit	Note
SWITCHING PERFORMANCE AND CHARACTERISTICS (Any Output Mode)							
External Clock low frequency range	4	F_{CLK}	800		2000	MHz	
External Clock high frequency range			4500		6400	MHz	
Sampling Clock low frequency range per core	4	Fs	200		500	MSps	
Sampling Clock high frequency range per core			1125		1600	MSps	
Sampling Clock to CLKOUT delay	4	Tclkout		170		ps	
Max crosstalk from CLKOUT on clock input signal@ 12.8 Gbps	4	XTALK_CKO2CK			-60	dB	
Aperture Delay (SDA disabled)	5	T_A		TBD		ps	
Sampling Delay Tuning Range (SDA enabled)	4		0.03		120	ps	
ADC Aperture uncertainty (SDA disabled)	4	$JITTER_{SDA\_OFF}$		125		fs_{rms}	(1)
ADC Aperture uncertainty (SDA enabled min)	4	$JITTER_{SDA\_MIN}$		220		fs_{rms}	
ADC Aperture uncertainty (SDA enabled max)	4	$JITTER_{SDA\_MAX}$		270		fs_{rms}	
CLKOUT jitter	5			70		fs_{rms}	
Digital reset duration	4		10			µs	
ADC settling time after power up		TS		NA		µs	(5)
Minimum SYNC pulse width	4æ	TSYNC		2		External Clock cycles	
SWITCHING PERFORMANCE AND CHARACTERISTIC (SSO, SYNCO)							
Output rise time (20%-80%)	4	TR		250		ps	(2)
Output fall time (20%-80%)		TF		250		ps	(2)

Parameters	Test level	Symbol	Min	Typ	Max	Unit	Note
CLK to SYNCO pipeline delay sync_edge rising	4	TPD_{SYNCO}		1		External Clock cycles	
CLK to SYNCO pipeline delay sync_edge falling	4	TPD_{SYNCO}		0.5		External Clock cycles	
CLK to SYNCO delay	4	TD_{SYNCO}		350		ps	
CLK to SSO delay	4	TD_{SSO}		1.2		ns	
SWITCHING PERFORMANCE AND CHARACTERISTIC (Serial output)							
Output Data delay (pipeline + delay)	4	TPD		30		External Clock cycles	
		TOD		2		ns	
Output rise time for DATA (20%-80%)	4	TR		31		ps	(2)
Output fall time for DATA (20%-80%)		TF		31		ps	(2)
Total jitter (BER=10^{-15}) @ 12.8 Gbps	4	2XT1		25		ps	(2),(4)
First time to get YT2 amplitude voltage @ 12.8 Gbps	4	XT2		25		ps	(2),(4)
Maximum amplitude voltage @ 12.8 Gbps	4			400		mV	(2),(4)
Skew between serial output signal P and N	4	Tskew			3.5	ps	(2)
Conversion Core latency	5			5		External Clock cycles	(3)
Total conversion latency	4		126		142	External Clock cycles	(3)
Crosstalk between xSL1 and xSL0@ 12.8 Gbps (x= A, B, C or D)	4	XTALK_SL2SL			-60	dB	(2)
Max crosstalk between output serial link and analog input signal @ 12.8 Gbps		XTALK_SL2IN			-80	dB	(2)

Notes:

1. See Definition of Terms.
2. 100 Ω load + PCB line 7 cm + cable 60 cm.
3. The latency of the conversion core is fixed. The total latency of the ADC (including the serial interface) can take any system external clock cycle between 126 and 142. ESIstream protocol wipes out the variable latency on the receiver's end due to its intrinsic synchronization procedure.
4. See Figure 3 for illustration of these values on the eye diagram of the serial links.
5. Serial link output frame initialization masks the analog input setting time.

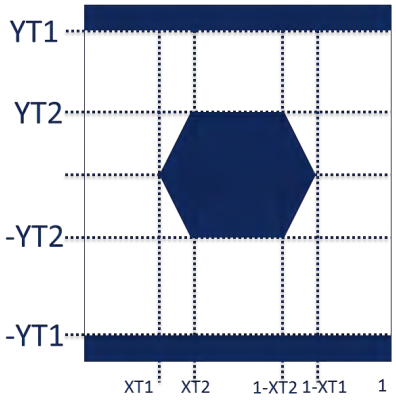


Figure 3 Serial link eye diagram

Table 10. SPI Timing characteristics

Parameter	Test Level	Symbol	Value			Unit	Note
			Min	Typ	Max		
RSTN pulse length	4	T_{RSTN}	10			µs	
SCLK frequency	4	F_{SCLK}			10	MHz	
CSN to SCLK delay	4	$T_{CSN-SCLK}$	0.5			T_{SCLK}	
MISO setup time	4	T_{setup}	3			ns	
MISO hold time	4	T_{hold}	3			ns	
MOSI output delay	4	T_{delay}			10	ns	

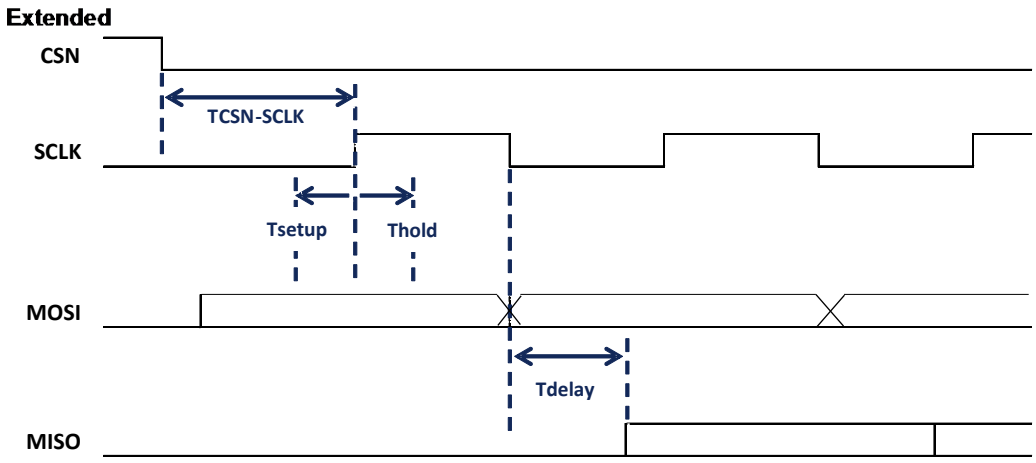


Figure 4: SPI timing diagram

3.12 Latency

The latency is defined as the number of clock cycles between the availability of the data (1st bit) on the serial links (xSL0 and xSL1, x= A, B, C or D) and the sampled input signal (INx, x= 0, 1, 2 or 3).
Both xSL0 and xSL1 (x= A, B, C or D) have the same latency.

For each core and each SYNC (synchronous or asynchronous), the total latency is in the interval of [126,142] clock cycles as following:

- 5 clock cycles for the core conversion
- 121 clock cycles for the data encoding and serialization (ESIstream protocol)
- 0 to 16 clock cycles for the intrinsic synchronization feature (ESIstream protocol).

As an example 1, latency could be:

- Latency DATA IN0 to ASL0/ASL1 = 126 clock cycles
- Latency DATA IN1 to BSL0/BSL1 = 132 clock cycles
- Latency DATA IN2 to CSL0/CSL1 = 140 clock cycles
- Latency DATA IN3 to DSL0/DSL1 = 139 clock cycles

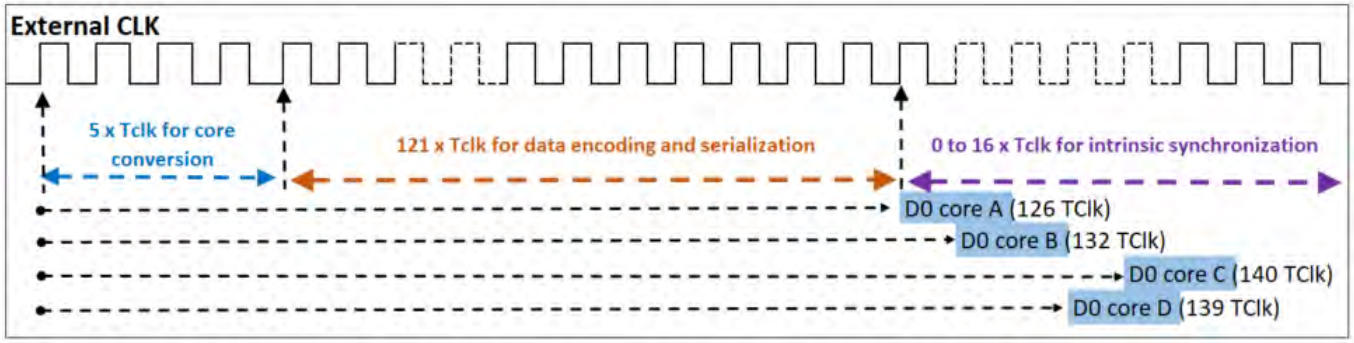


Figure 5: Latency example 1

As the example 2, new latency could be

- Latency DATA IN0 to ASL0/ASL1 = 130 clock cycles
- Latency DATA IN1 to BSL0/BSL1 = 140 clock cycles
- Latency DATA IN2 to CSL0/CSL1 = 135 clock cycles
- Latency DATA IN3 to DSL0/DSL1 = 142 clock cycles

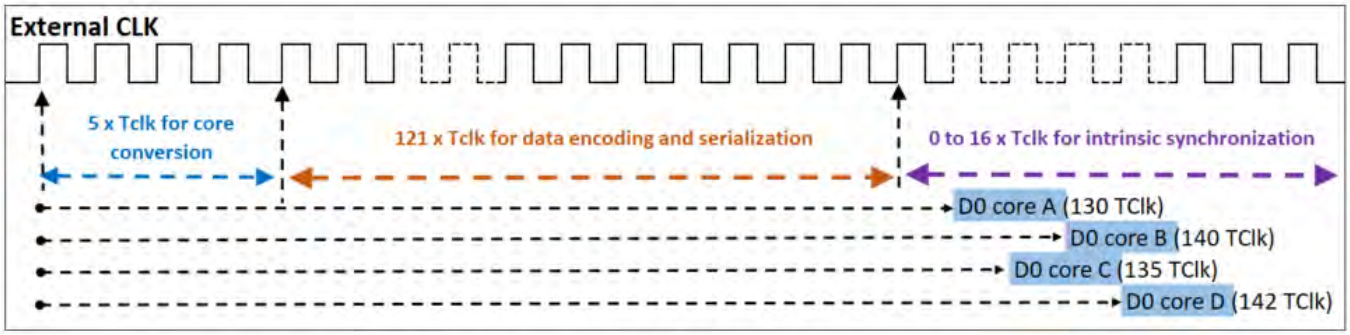


Figure 6: Latency example 2

3.13 Digital Output Coding

Table 11. ADC Digital output coding table

Differential analog input	Voltage level	Binary MSB (bit 11)……LSB (bit 0)	InRange
> + 500.125 mV	>Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1	0
+ 500.125 mV + 500 mV	Top end of full scale + ½ LSB Top end of full scale - ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	1 1
+ 0.125 mV - 0.125 mV	Mid scale + ½ LSB Mid scale - ½ LSB	1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1	1 1
- 500 mV -500.125 mV	Bottom end of full scale + ½ LSB Bottom end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	1 1
< - 500.125 mV	< Bottom end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 0 0	0

3.14 Definition of Terms

Table 12. Definition of terms

Abbreviation	Term	Definition
(INL)	Integral non linearity	The Integral Non Linearity for an output code “I” is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
(DNL)	Differential Non Linearity	The Differential Non Linearity for an output code is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
(FPBW)	Full Power Bandwidth	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for an input at Full Scale -1 dB (-1 dBFS).
(EFPBW)	Extended Full Power Bandwidth	FPBW in extended mode
(NFPBW)	Nominal Full Power Bandwidth	FPBW in nominal mode
(SFDR)	Spurious free dynamic range	Ratio expressed in dB of the RMS signal amplitude, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dBFS (i.e., related to converter 0 dB Full Scale), or in dBc (i.e, related to input signal level).
(THD)	Total Harmonic Distortion	Ratio expressed in dB of the RMS summed up to nth harmonic components (typical n=25) to the RMS input signal amplitude. It may be reported in dBFS (i.e, related to converter 0 dB Full Scale), or in dBc (i.e, related to input signal level).
(TILD)	Total InterLeaving Distortion	Ratio expressed in dB of the RMS sum up to interleaving spurs (Fclock/4 +/- Fin, Fclock/2 - Fin, Fclock/4 in QUAD mode, and Fclock/2 +/- Fin in DUAL mode).
(ILG)	InterLeavinG	Interleaving of the internal cores.
(IMD3)	InterModulation Distortion	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products.
(SNR)	Signal to noise ratio	Ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components excluding the nine first harmonics.
(SINAD)	Signal to noise and distortion ratio	Ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components except DC but including the harmonics and interleaving spurs.
(ENOB)	Effective Number Of Bits	$ENOB = \frac{SINAD - 1.76}{6.02}$
(NSD)	Noise Spectral Density	The NSD is the power spectral density magnitude of the ADC expressed in dBm/Hz.
(NPR)	Noise Power Ratio	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
(OTP)	One-Time Programmable	OTP memory cells are written during electrical test. They are used to store factory calibration values. They are loaded in SPI registers during device start-up (see §6)
(ORT)	Overvoltage recovery time	Time to recover 0.2 % accuracy at the output, after a 150 % full scale step applied on the input is reduced to midscale.
(T_A)	Aperture delay	Delay between the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point), and the time at which analog input (INxP, INxN where X = 0, 1, 2 or 3) is sampled.
(JITTER)	Aperture uncertainty	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.

Abbreviation	Term	Definition
(TOD)	Digital data Output delay	Delay from SYNC to serial link data output (first alignement frame)
(TPD)	Pipeline Delay	Number of clock cycles from SYNC to serial link data output (first alignement frame) .
(TR)	Rise time	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
(TF)	Fall time	Time delay for the output DATA signals to fall from 20% to 80% of delta between low level and high level.
(TS)	Settling time	Time delay to achieve 0.2 % accuracy at the converter output when a 80% Full Scale step function is applied to the differential analog input.
(TSYNC)	SYNC duration	External SYNC pulse width needed for SYNC function.
(CER)	Conversion Error Rate	Probability to exceed a specified error threshold for a sample at maximum specified sampling rate due to ADC quantization. An error code is a code that differs by more than +/- 128 LSB from the correct code.
(BER)	Bit Error Rate	Percentage of bits with errors divided by the total number of bits that have been transmitted, received or processed over a given time period.
(VSWR)	Voltage Standing Wave Ratio	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20 dB return loss (ie. 99% power transmitted and 1% reflected).

4 PACKAGE DESCRIPTION

4.1 Type /Outline

HiTCE Ceramic Ball Grid Array CBGA323

- High TCE Glass-Ceramic substrate
- Body size: 16.0x16.0 mm
- Lands Pitch: 0.80 mm
- Number of balls: 323
- Conductor: cofired copper

Package interconnection

- 18x18 BGA matrix (323 balls, A1 removed)
- 0.80 mm ball pitch
- Ball type : SAC305 (for both AQ600 and AQ605) or Pb90Sn10 (only available for AQ600)
- MSL3 (non-hermetic)

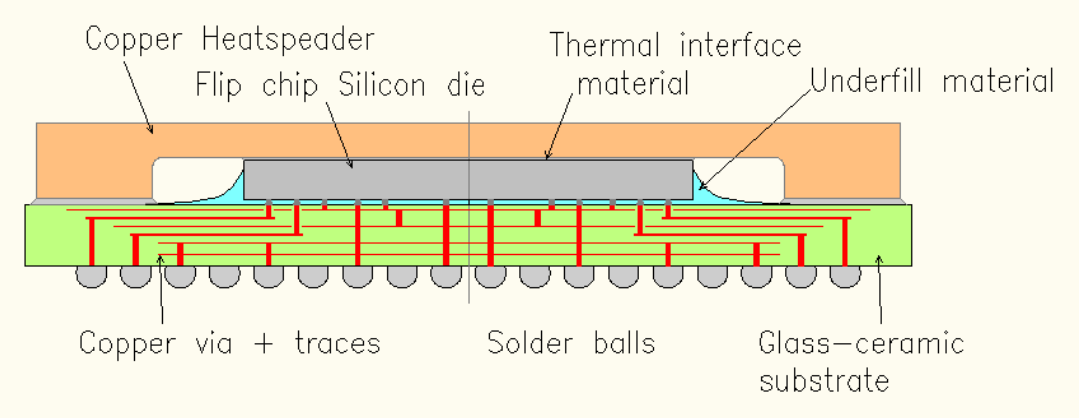


Figure 7: Package cross-section

Package outline for Pb90Sn10 balls

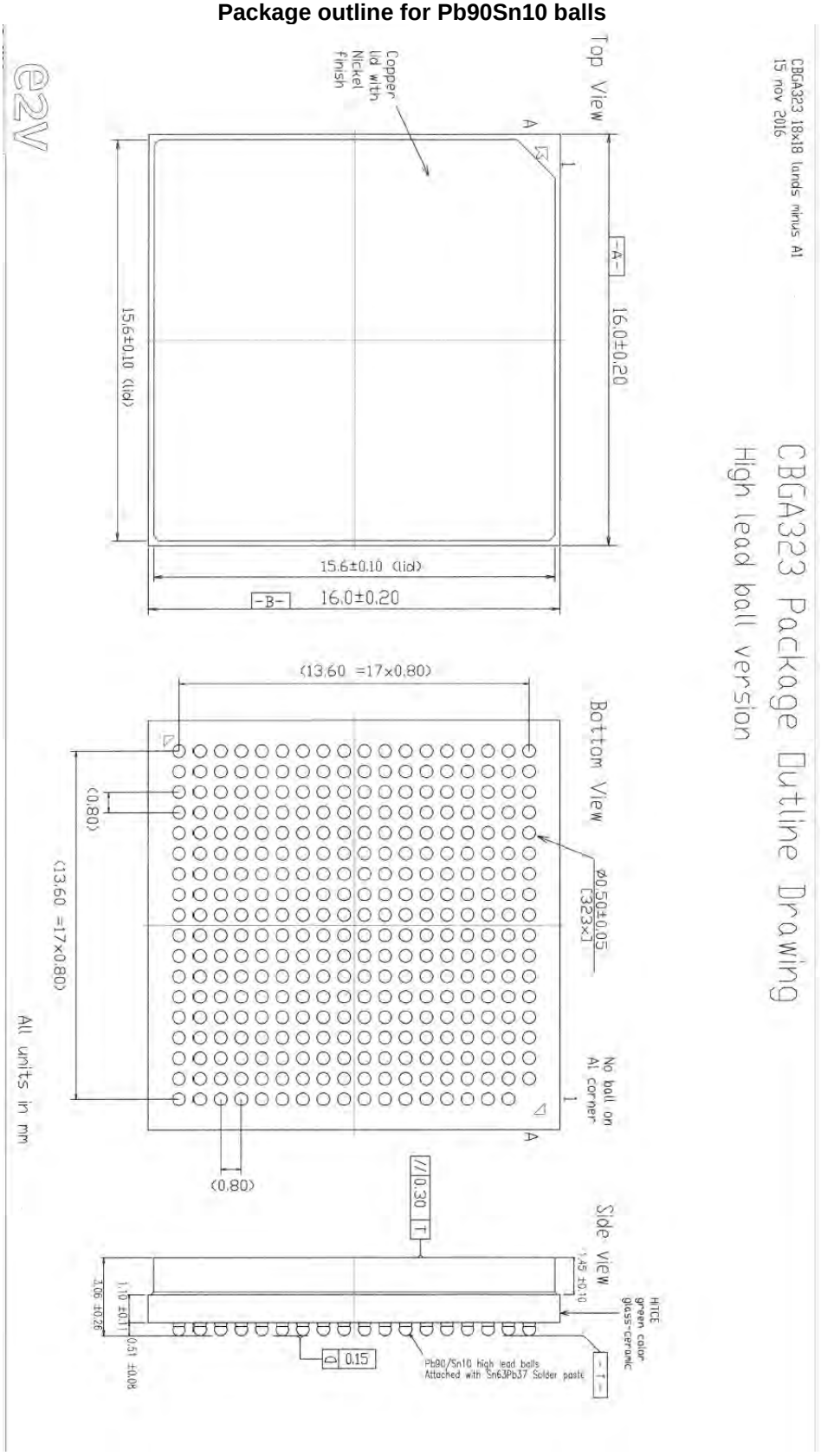


Figure 8: Package outline for Pb90Sn10 balls

Package outline for SAC305 balls

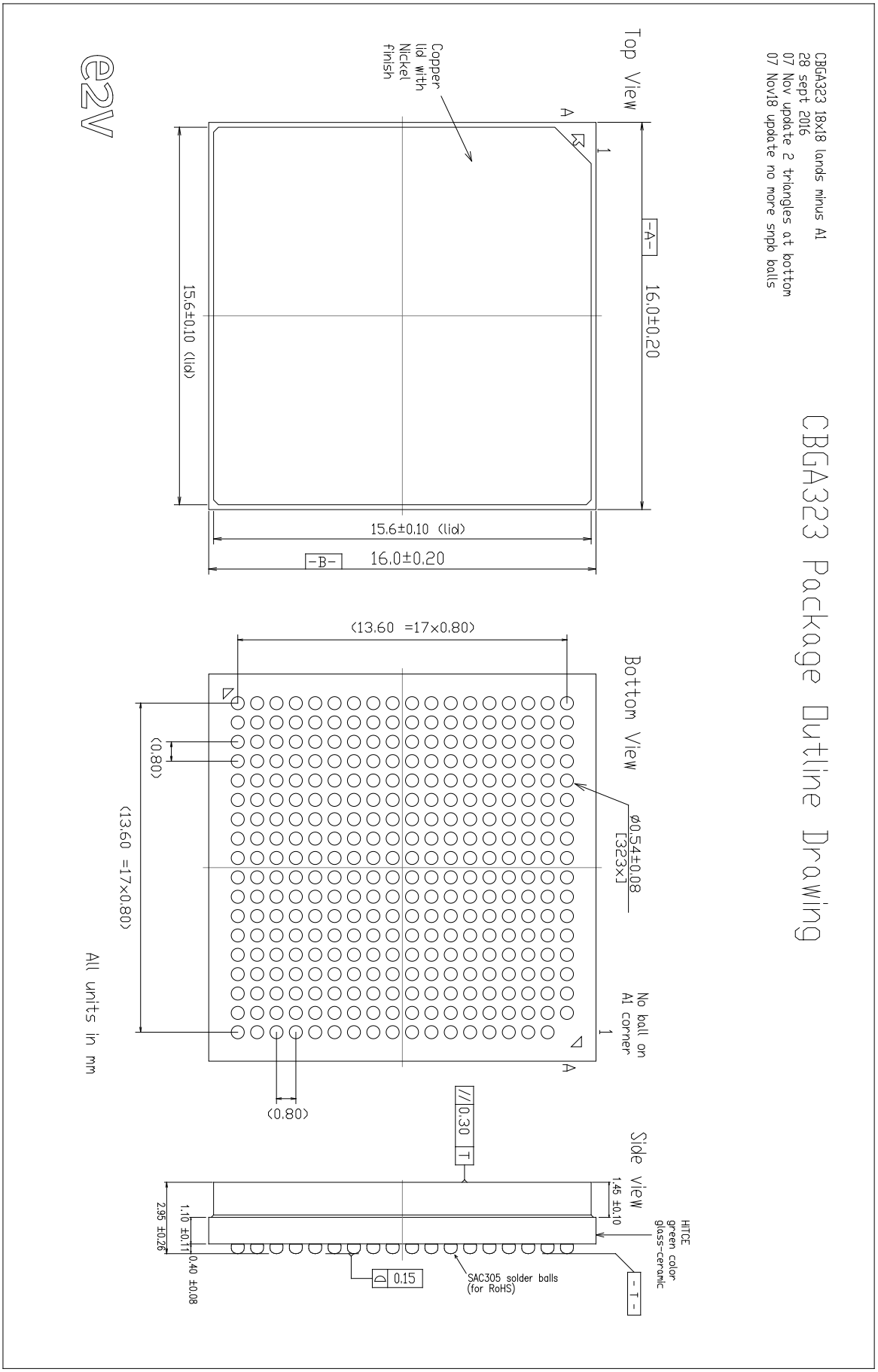


Figure 9: Package outline for SAC305 balls

4.2 Pinout top view

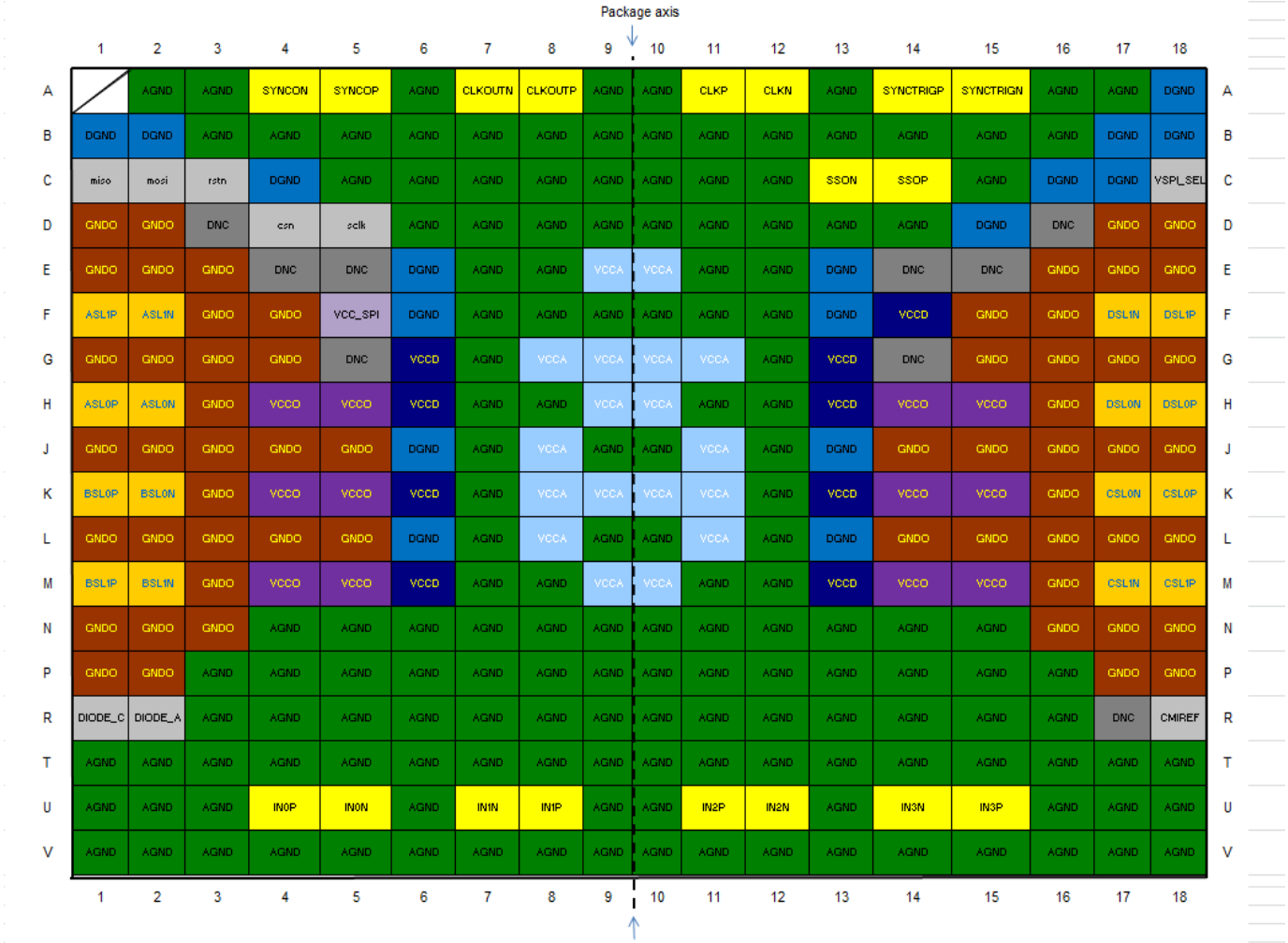


Figure 10: Pinout top view

4.3 Relative skew for serial links view

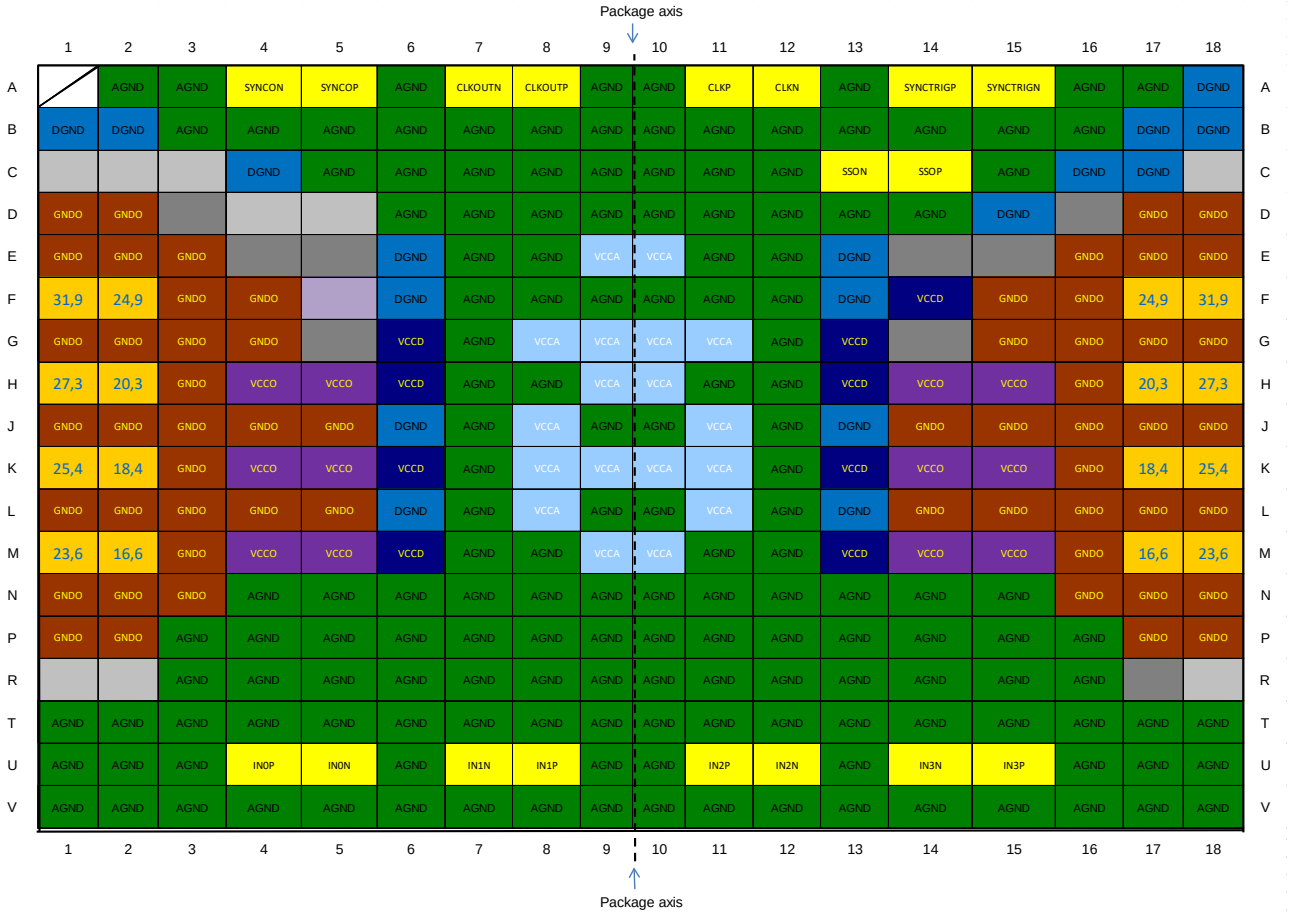
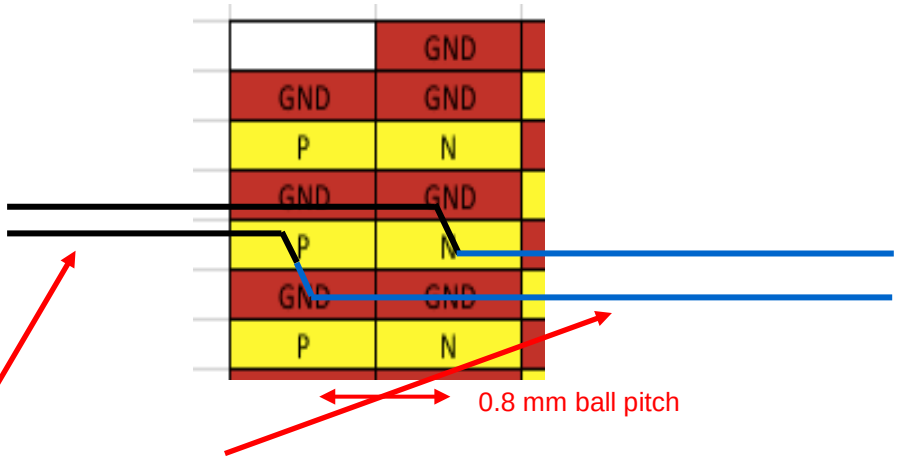


Figure 11: Skew mapping (values are in ps)

Those skew values are relative to the same reference. BSL1P skew value is 23.6 ps and BSL1N skew value is 16.6 ps. The relative skew value between BSL1P and BSL1N is 7 ps.

With a special care on the board routing, it is possible to compensate the relative skew between differential serial links (N&P).



Length on board + length on package are almost the same on N and P (less routing on board for P results from more routing inside package for P).

With this routing, Ansys HFSS simulations have shown only 0.7° phase difference between P and N at 6 GHz. This electrical compensation is not perfect because of board and package εr (relative permittivity) difference. HITCE package εr is 5.2 (higher value than for usual board).

4.4 Thermal characteristics

Table 13. Thermal characteristics

Parameter	Symbol	Value	Unit	Note
Thermal resistance from junction to bottom of balls	$Rth_{Junction\ to\ Bottom\ of\ balls}$	4.0	°C/Watt	(1)(2)
Thermal resistance from junction to board (JEDEC JESD51-8)	$Rth_{Junction\ -\ board}$	5.5	°C/Watt	(1)(2)
Thermal resistance from junction to top of lid	$Rth_{Junction\ –\ lid}$	2.05	°C/Watt	(1)(2)
Thermal resistance from junction to ambient (JEDEC standard)	$Rth_{Junction\ –\ ambient}$	19.2	°C/Watt	(1)(3)
Delta temperature Hot spot – temperature from diode		+6.2	°C	

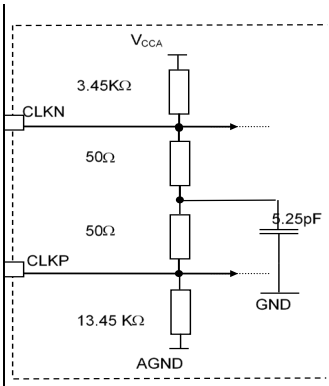
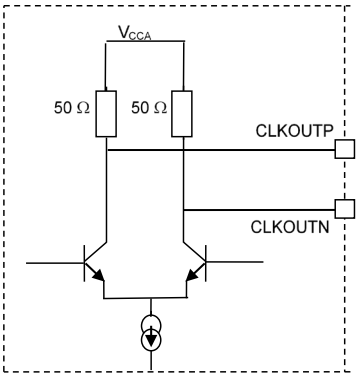
Notes:

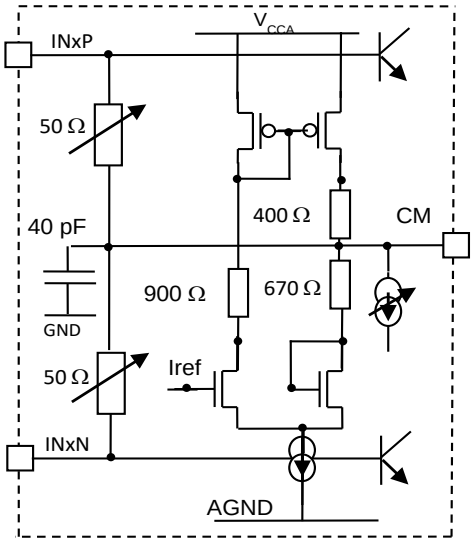
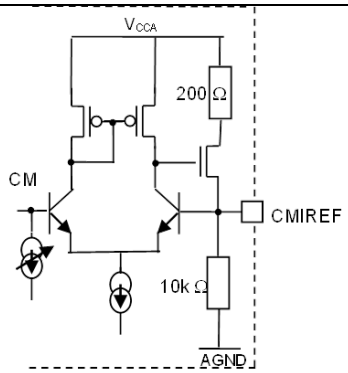
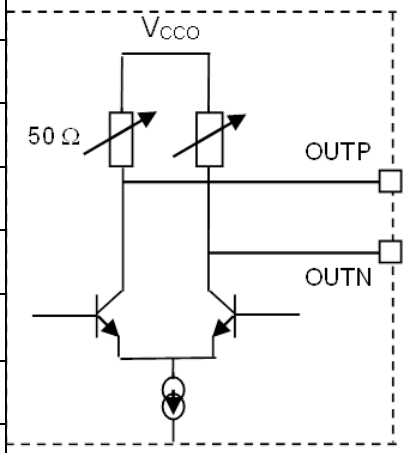
1. Rth are calculated from hot spot, not from average temperature of the die.
   They are thermal simulation results (finite elements method) with nominal cases.
2. Assumptions: no air, pure conduction, no radiation
3. Assumptions:
   - Convection according to JEDEC
   - Still air
   - Horizontal 2s2p board
   - Board size 114.3 x 76.2 mm, 1.6 mm thickness

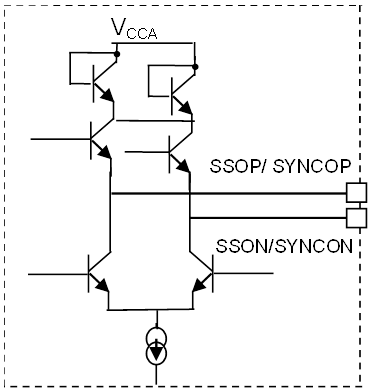
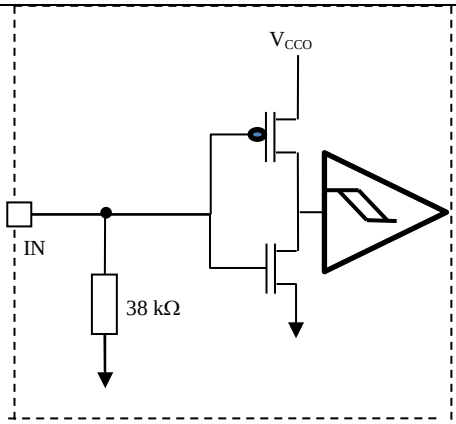
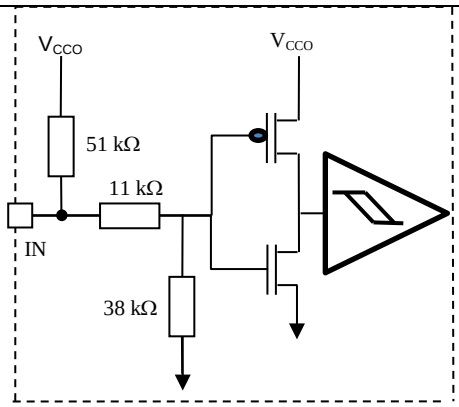
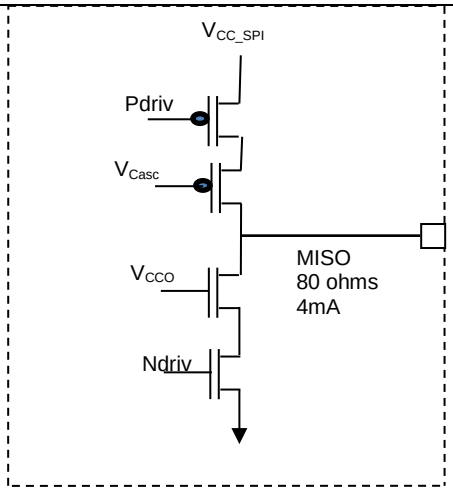
4.5 Pinout Table

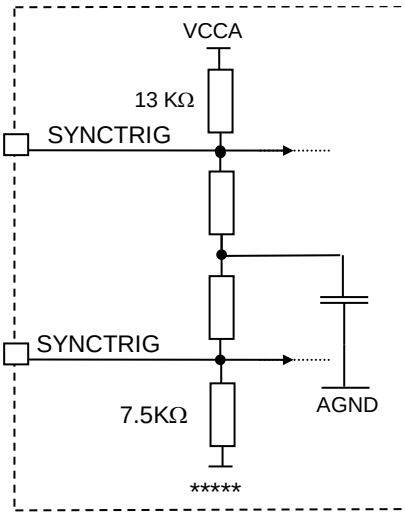
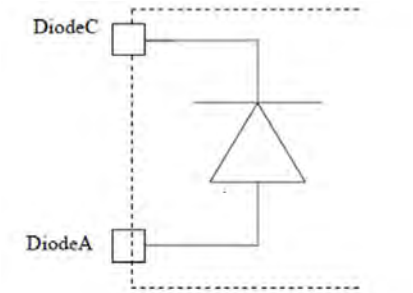
Table 14. Pinout Table

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Power supplies				
AGND	A2, A3, A6, A9, A10, A13, A16, A17; B3, B4, B5, B6, B7, B8, B9, B10, B11,B12, B13, B14, B15, B16; C5, C6, C7, C8, C9, C10, C11, C12, C15; D6, D7, D8, D9, D10, D11, D12, D13, D14; E7, E8, E11, E12 F7, F8, F9, F10, F11, F12; G7, G12; H7, H8, H11, H12; J7, J9, J10, J12; K7, K12; L7, L9, L10, L12; M7, M8, M11, M12; N4, N5, N6, N7, N8, N9, N10, N11, N12, N13, N14, N15; P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16; R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16; T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18; U1, U2, U3, U6, U9, U10, U13, U16, U17, U18; V1, V2, V3, V4, V5, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18;	Analog ground All ground pins must be connected to a one solid ground (analog + digital) plane on PCB		
DGND	A18; B1, B2, B17, B18; C4, C16, C17; D15; E6, E13; F6, F13; J6, J13; L6, L13;	Digital ground All ground pins must be connected to a one solid ground (analog + digital) plane on PCB		
GNDO	D1, D2, D17, D18; E1, E2, E3, E16, E17, E18; F3, F4, F15, F16; G1,G2, G3, G4, G15, G16, G17, G18; H3, H16;	Ground for Output buffers All ground pins must be connected to a one solid ground (analog + digital) plane on PCB		

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
	J1, J2, J3, J4, J5, J14, J15, J16, J17, J18; K3, K16; L1, L2, L3, L4, L5, L14, L15, L16, L17, L18; M3, M16 N1, N2, N3, N16, N17, N18; P1, P2, P17, P18;			
V_{CCA}	E9, E10; G8, G9, G10, G11; H9, H10; J8, J11; K8, K9, K10, K11; L8, L11; M9, M10;	Analog power supply		
V_{CC_SPI}	F5	SPI output power supply (2.5 V, 3.3 V)		
V_{CCD}	F14; G6, G13; H6, H13; K6, K13; M6, M13;	Digital power supply		
V_{CCO}	H4, H5, H14, H15; K4, K5, K14, K15; M4, M5, M14, M15;	Output power supply		
Clock signal				
CLKP CLKN	A11, A12	In phase and Out of phase input clock signal	I	
CLKOUTP CLKOUTN	A8, A7	In phase and Out of phase out clock signal	O	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Analog signals				
IN0P IN0N	U4, U5	In phase analog input 0 Out of phase analog input 0 (must be unconnected if not used)	I	
IN1P IN1N	U8, U7	In phase analog input 1 Out of phase analog input 1 (must be unconnected if not used)	I	
IN2P IN2N	U11, U12	In phase analog input 2 Out of phase analog input 2 (must be unconnected if not used)	I	
IN3P IN3N	U15, U14	In phase analog input 3 Out of phase analog input 3 (must be unconnected if not used)	I	
CMIREF	R18	Output voltage reference In AC coupling operation this output could be left floating (not used) In DC coupling operation, these pins provides an output voltage which is the common mode voltage for the analog input signal and should be used to set the common mode voltage of the input driving buffer.	O	
Digital Output signals (CML)				
ASL0P, ASL0N	H1, H2	Channel A output data serial link 0	O	
ASL1P, ASL1N	F1, F2	Channel A output data serial link 1	O	
BSL0P, BSL0N	K1, K2	Channel B output data serial link 0	O	
BSL1P, BSL1N	M1, M2	Channel B output data serial link 1	O	
CSL0P, CSL0N	K18, K17	Channel C output data serial link 0	O	
CSL1P, CSL1N	M18, M17	Channel C output data serial link 1	O	
DSL0P, DSL0N	H18, H17	Channel D output data serial link 0	O	
DSL1P, DSL1N	F18, F17	Channel D output data serial link 1	O	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Digital output Signal (LVDS)				
SSOP, SSON	C14, C13	In phase and out of phase Slow Synchro Output.Fsso=Fclk/32	O	
SYNCOP, SYNCON	A5, A4	In phase and out of phase Sync Output.	O	
Digital I/0 (CMOS)				
V_{SPI_SEL}	C18	used for logical level selection		
Sclk	D5	SPI signal Input SPI serial Clock Serial data is shifted into and out SPI synchronously to this signal on positive transition of sclk Internal pull-down	I	
Mosi	C2	SPI signal Data SPI Input signal (Master Out Slave In) Serial data input is shifted into SPI while sldn is active low Internal pull-down	I	
Csn	D4	SPI signal Input Chip Select signal (Active low) When this signal is active low, sclk is used to clock data present on MOSI or MISO signal Internal pull-up	I	
Rstn	C3	SPI signal Input Digital asynchronous SPI reset (Active low) This signal allows to reset the internal value of SPI to their default value Internal pull-up	I	
Miso	C1	SPI signal Data output SPI signal (Master In Slave Out) Serial data output is shifted out SPI while csn is active low.	O	

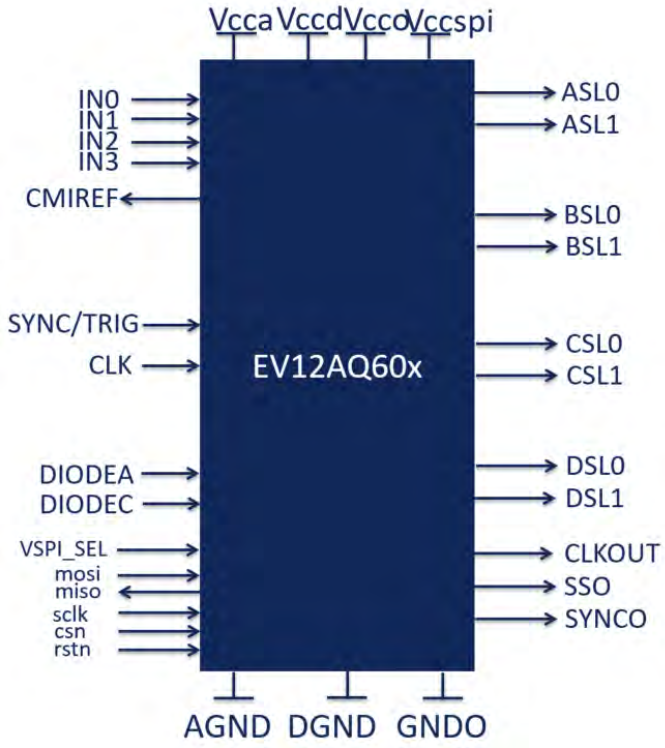
DIGITAL INPUT (LVDS)				
SYNCTRIGP SYNCTRIGN	A14, A15	Differential Input Synchronization signal (LVDS) Active high signal This signal is used to synchronize internal ADC, if enabled Equivalent internal differential 100Ω input resistor Functionality Sync or Trigger depends on SPI selection	I	
MISCELLANEOUS				
DiodeA, DiodeC	R2, R1	Junction Temperature Monitoring diode Anode Junction Temperature Monitoring diode Cathode Cathode must be connected to ground (AGND) externally	I	

5 THEORY OF OPERATION

Overview

Table 15. Functional description

Name	Function
V_{CCA}	Analog Power Supply
V_{CCD}	Digital Power Supply
V_{CCO}	Output buffer Power Supply
V_{CC_SPI}	SPI Output Power Supply (2.5V or 3.3V)
V_{SPI_SEL}	Selection of SPI logical levels
AGND	Analog Ground
DGND	Digital Ground
GNDO	Ground for Output buffer
IN0P, IN0N	Differential Analog Input for ADC core A, core B, core C or core D (depending on cross point switch chosen configuration)
IN1P, IN1N	Differential Analog Input for ADC core B
IN2P, IN2N	Differential Analog Input for ADC core C
IN3P, IN3N	Differential Analog Input for ADC core A, core B, core C or core D
CLKP,CLKN	Differential Clock Input
ASL0P, ASL0N	Channel A output, serial link0 (CML)
ASL1P, ASL1N	Channel A output, serial link1 (CML)
BSL0P, BSL0N	Channel B output, serial link0 (CML)
BSL1P, BSL1N	Channel B output, serial link1 (CML)
CSL0P, CSL0N	Channel C output, serial link0 (CML)
CSL1P, CSL1N	Channel C output, serial link1 (CML)
DSL0P, DSL0N	Channel D output, serial link0 (CML)
DSL1P, DSL1N	Channel D output, serial link1 (CML)
csn	SPI Chip Select Input (Active Low)
rstn	SPI Asynchronous Reset Input (Active Low)
sclk	SPI Input Clock



mosi	SPI input Data (Master Out Slave In)
miso	SPI Output Data (Master In Slave Out)
CMIRef	Input common Mode reference
DIODEA, DIODEC	Diode Anode and Cathode Inputs for die junction temperature monitoring
CLKOUTP, CLKOUTN	Differential output clock (copy of CLK)
SSOP, SSON	Slow Synchro Output clock
SYNCTRIGP, SYNCTRIGN	LVDS input: Synchronization of Data Ready, or TRIGGER input depending on SPI selection
SYNCOP, SYNCON	Synchro output, resynchronized SYNCTRIG signal

The EV12AQ60x could be configured as follow:

- Both the analog inputs settings and the associated clocking mode (in phase or interleaved) of the 4 cores can be selected though the SPI.
- Test modes can be selected though the SPI.
- Factory calibration or custom calibration can be loaded through the SPI.

Refer to §6 for registers description.

6 DIGITAL RESET AND START-UP PROCEDURE

Start-up procedure uses SPI instructions and signals. Refer to §7 for a detailed description.

RSTN is an asynchronous active low global reset for the SPI and OTP (One-Time programmable) memory cells. It is mandatory to put RSTN at low level during a minimum of 10 µs at power-up of the device. It sets all SPI registers to their default values.

Figure 12 presents the reset and synchronization to realize after power-up when the SPI is used (see §7 for more information on the SPI interface).

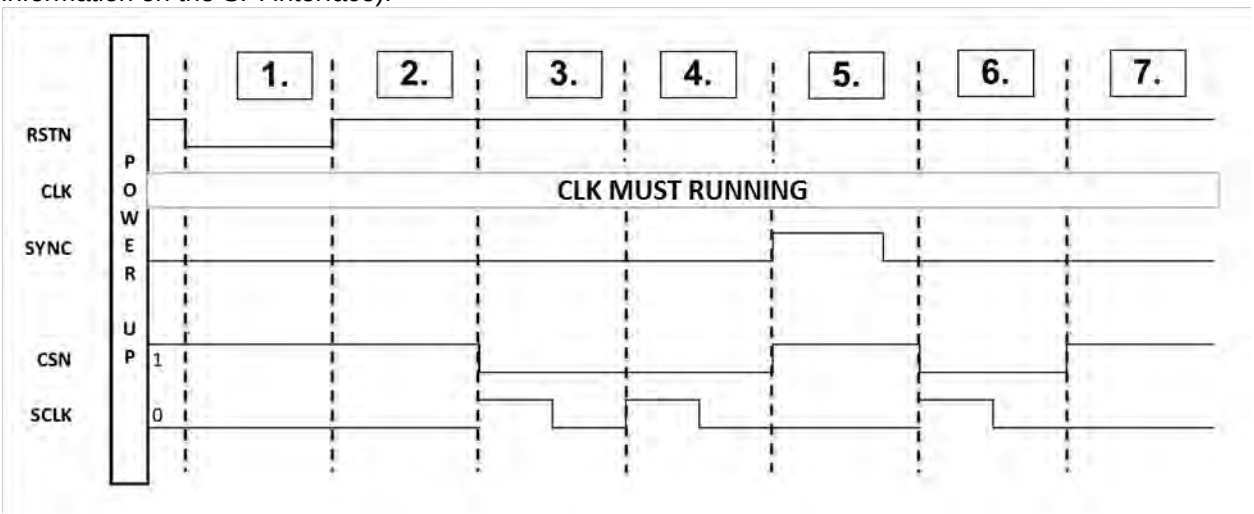


Figure 12: Start-up sequence when using the SPI interface

- 1. It is mandatory to reset the device at power-up through RSTN. It is active low and the pulse must be at least 10 µs. During the RSTN pulse, CSN must be held high and SCLK held low. The CLK must be provided before the RSTN pulse. The CLK can start before or after the power-up.
- 2. The OTP memory cells need 1 ms to wake up.
- 3. The SPI instruction WRITE @0x0001 =0b1 must be sent to the ADC. The OTP memory cells are loaded into the SPI registers at this point. There must be at least 1 ms between the RSTN pulse and this SPI instruction;
- 4. The ADC is configured through the SPI interface.
- 5. A pulse is applied onto the SYNCTRIG input to reset the internal clocks (SYNC signal in Figure 12). At this stage, the Trigger mode is disabled.
- 6. The ADC can be configured in Trigger mode and the EXTRA_SEE_PROTECT register can be activated – see §8.15.
- 7. Normal operation of the ADC.

7 SERIAL PERIPHERAL INTERFACE (SPI)

The digital interface will be a standard SPI with:

- 16 bits for the address A[15] to A[0] including a R/W bit (A[15] = R/W, being A[15] is the MSB);
- 16 bits of data D[15] to D[0] with D[15] the MSB.

5 signals are required:

- RSTN for the SPI reset;
- SCLK for the SPI clock;
- CSN for the Chip Select;
- MISO for the Master In Slave Out SPI Output;
- MOSI for the Master Out Slave In SPI Input.

The MOSI sequence should start with one R/W bit (A[15]):

- R/W = 0 is a read command
- R/W = 1 is a write command

7.1 SPI logic compatibility

Digital SPI CMOS input levels can be in 2.5 V or 3.3 V logic compatibility.
Digital SPI CMOS output levels can be configured in 2.5 V or 3.3 V logic compatibility[1].

Table 16 presents the SPI pins configuration depending on expected logic level.
The selection of logic compatibility is done in settings appropriate voltage levels to pins V_{CC_SPI} and V_{SPI_SEL}.
Default logic compatibility is 2.5 V.

Table 16. SPI pins configuration depending on logic voltage required

Logic Level	V_{CC_SPI} pin voltage	V_{SPI_SEL} pin voltage
2.5 V	2.5 V	0 V (GND)
3.3 V	3.3 V	3.3 V

7.2 SPI Read / Write command

All SPI registers must be addressed with 16-bit address followed by 16-bit data. The first bit A[15] (RW) is low for a read command and high for a write command.

Write command to access a 16-bit register:

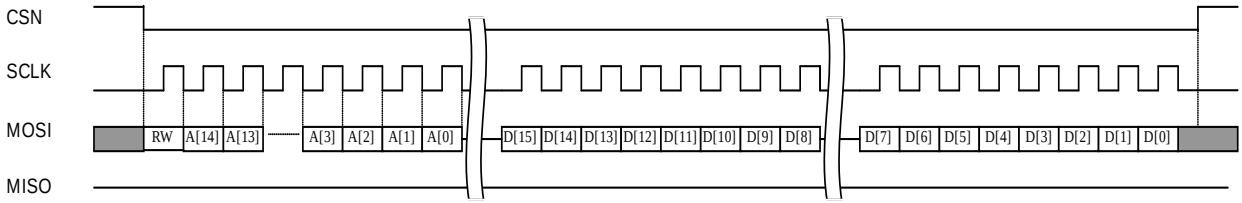


Figure 13: SPI writing

Read command to access a 16-bit register:

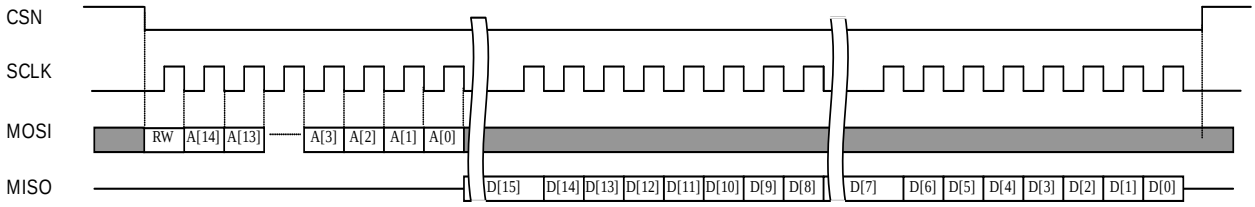


Figure 14: SPI reading

See §3.5 for SPI timing characteristics (max clock frequency…)

[1] It is also possible to drive SPI logic in CMOS 1.8 V levels:
- Output buffer configuration : V_{CC_SPI} = 1.8 V, and V_{SPI_SEL} = 0 V
- Input buffer: The user has to strictly ensure that V_{IH} is > 1.7 V

7.3 Register map

Table 17. SPI register map

Registers Names	@ hex	Default value hex	COMMENT	Refer to Table
OTP_LOADING	0x0001		The action of writing in this register causes the loading of OTP memory cells in secure SPI register	Table 42
EXTRA_SEE_PROTECT	0x0002	0	Additional protection against Single Event 0: major protection is available (default) 1: additional protection is available All SPI registers can't be access, except this registe SYNC is disabled The presence of the CLOCK SPI refreshes Triple Majority Redundancy registers	Table 44
OUTPUT_CLK_EN	0x0017	2	For all following bits : 0: disabled 1: enabled bit[0] = CLKOUT enabled (disabled by default) bit[1] = SSO enabled (enabled by default) bit[2] = SYNCO enabled (disabled by default)	Table 36
SYNCO_SSO_CLKOUT_FULL_SWING_EN	0x0005	0	For all following bits : 0: reduced 1: full swing bit[1] = LVDS full swing on SSO and SYNCO bit[0] = CML CLKOUT full swing	Table 37
AB_HSSL_FULL_SWING_EN	0x0006	0	bit[0] 0: HSSL output swing is reduced (default) 1: full HSSL output swing	Table 39
CD_HSSL_FULL_SWING_EN	0x0007	0	bit[0] 0: HSSL output swing is reduced (default) 1: full HSSL output swing	Table 39
EXT_BW_DISABLE	0x0008	0	bit[0] 0: extended bandwidth (default) 1: nominal bandwidth	Table 32
CAL_SET_SEL	0x0009	0	bit[0] = INL calibration set selection 0: set 0 selected (default value) 1: set 1 selected (not defined) bit[2:1] = phase/gain/offset calibration set selection 00: set 0 selected 01: set 1 selected 10: set 2 selected 11: set 3 selected	Table 28
CLK_MODE_SEL	0x000A	0	bit[1:0] = clock control 11: clock A=B=C=D , all clocks are identical 10: clock A=C, clock B=D 01: clock A=B, clock C=D 00: all clocks are interleaved (default)	Table 23
CPS_CTRL	0x000B	0	1-channel mode 000 : input 0 to core A & B & C & D (default) 001 : input 3 to core A & B & C & D 2-channel mode 010 : input 0 to core A & B input 3 to core C & D 011 : input 0 to core C & D input 3 to core A & B 4-channel mode 100 : input 0 to core A input 1 to core B	Table 22

Registers Names	@ hex	Default value hex	COMMENT	Refer to Table
			input 2 to core C input 3 to core D	
SYNC_CTRL	0x000C	0	bit[0] = sync_edge : Indicate system clock sampling edge for SYNC 0 : Positive edge 1 : Negative edge bit[2:1] = sync_shift : Add one(or more) system clock period on SYNC internal path 00 : No system clock period added 01 : One system clock period added 10 : two system clock periods added 11 : three system clock periods added	Table 35
SYNC_FLAG	0x000D	0	bit [0] = Indicate timing violation on SYNC bit [0] = 0 : SYNC has been correctly recovered bit [0] = 1 :Timing violation on SYNC	Table 33
SYNC_FLAG_RST	0x000E	0	bit [0] = 0 : reset the flag	Table 34
CHIP_ID	0x0011		Chip Identification number	Table 43
AB_HSSL_CFG	0x0013	18	bit[1:0] = Data selection CB1 00: InRange selected (default) 01: Trigger selected (=> Sync disabled) 10: Timestamp selected 11: Parity selected bit[3:2] = Data selection for CB2 00: InRange selected 01: Trigger selected (=> Sync disabled) 10: Timestamp selected (default) 11: Parity selected bit[4] = LSB first enabled 0: MSB first ‘ 1: LSB first (default)	Table 38
CD_HSSL_CFG	0x0014	18	Idem AB_HSSL_CFG	Table 38
AB_HSSL_POL	0x0015	06	For all following bits : 0: Pin N/P default 1: Pin N and P reversed bit[0] = Pin N/P config of serial output buffer 0 CHANNEL A bit[1] = Pin N/P config of serial output buffer 1 CHANNEL A bit[2] = Pin N/P config of serial output buffer 0 CHANNEL B bit[3] = Pin N/P config of serial output buffer 1 CHANNEL B	Table 40
CD_HSSL_POL	0x0016	09	For all following bits : 0: Pin N/P default 1: Pin N and P reversed bit[0] = Pin N/P config of serial output buffer 0 CHANNEL C bit[1] = Pin N/P config of serial output buffer 1 CHANNEL C bit[2] = Pin N/P config of serial output buffer 0 CHANNEL D bit[3] = Pin N/P config of serial output buffer 1 CHANNEL D	Table 40
OUTPUT_CLK_EN	0x0017	2	For all following bits : 0: disabled 1: enabled bit[0] = CLKOUT enabled (disabled by default) bit[1] = SSO enabled (enabled by default) bit[2] = SYNCO enabled (disabled by default)	Table 36

Registers Names	@ hex	Default value hex	COMMENT	Refer to Table
A_SET0_GAIN_CAL	0x0122	0800	A core Interleaving gain calibration	Table 25
A_SET0_PHASE_CAL	0x0123	0100	A core Interleaving phase calibration	Table 26
A_SET0_OFFSET_CAL	0x0124	0100	A core Interleaving offset calibration	Table 27
A_SET1_GAIN_CAL	0x0125	0800	A core Interleaving gain calibration	Table 25
A_SET1_PHASE_CAL	0x0126	0100	A core Interleaving phase calibration	Table 26
A_SET1_OFFSET_CAL	0x0127	0100	A core Interleaving offset calibration	Table 27
A_SET2_GAIN_CAL	0x0128	0800	A core Interleaving gain calibration	Table 25
A_SET2_PHASE_CAL	0x0129	0100	A core Interleaving phase calibration	Table 26
A_SET2_OFFSET_CAL	0x012A	0100	A core Interleaving offset calibration	Table 27
A_SET3_GAIN_CAL	0x012B	0800	A core Interleaving gain calibration	Table 25
A_SET3_PHASE_CAL	0x012C	0100	A core Interleaving phase calibration	Table 26
A_SET3_OFFSET_CAL	0x012D	0100	A core Interleaving offset calibration	Table 27
A_SDA_CTRL	0x012F	1000	A core Sampling Delay Adjust (0 to 120 ps with a step of 30 fs) bit[11:0] = SDA value bit[9:0]: fine delay, step 30 fs bit[11:10]: coarse delay, step 30 ps bit[12] = SDA disabled 0: enabled 1: disabled (default)	Table 46
B_SET0_GAIN_CAL	0x0322	0800	B core Interleaving gain calibration	Table 25
B_SET0_PHASE_CAL	0x0323	0100	B core Interleaving phase calibration	Table 26
B_SET0_OFFSET_CAL	0x0324	0100	B core Interleaving offset calibration	Table 27
B_SET1_GAIN_CAL	0x0325	0800	B core Interleaving gain calibration	Table 25
B_SET1_PHASE_CAL	0x0326	0100	B core Interleaving phase calibration	Table 26
B_SET1_OFFSET_CAL	0x0327	0100	B core Interleaving offset calibration	Table 27
B_SET2_GAIN_CAL	0x0328	0800	B core Interleaving gain calibration	Table 25
B_SET2_PHASE_CAL	0x0329	0100	B core Interleaving phase calibration	Table 26
B_SET2_OFFSET_CAL	0x032A	0100	B core Interleaving offset calibration	Table 27
B_SET3_GAIN_CAL	0x032B	0800	B core Interleaving gain calibration	Table 25
B_SET3_PHASE_CAL	0x032C	0100	B core Interleaving phase calibration	Table 26
B_SET3_OFFSET_CAL	0x032D	0100	B core Interleaving offset calibration	Table 27
B_SDA_CTRL	0x032F	1000	B core Sampling Delay Adjust (0 to 120 ps with a step of 30 fs) bit[11:0] = SDA value bit[9:0]: fine delay, step 30 fs bit[11:10]: coarse delay, step 30 ps bit[12] = SDA disabled 0: enabled 1: disabled (default)	Table 46

Registers Names	@ hex	Default value hex	COMMENT	Refer to Table
C_SET0_GAIN_CAL	0x0522		C core Interleaving gain calibration	Table 25
C_SET0_PHASE_CAL	0x0523		C core Interleaving phase calibration	Table 26
C_SET0_OFFSET_CAL	0x0524		C core Interleaving offset calibration	Table 27
C_SET1_GAIN_CAL	0x0525		C core Interleaving gain calibration	Table 25
C_SET1_PHASE_CAL	0x0526		C core Interleaving phase calibration	Table 26
C_SET1_OFFSET_CAL	0x0527		C core Interleaving offset calibration	Table 27
C_SET2_GAIN_CAL	0x0528		C core Interleaving gain calibration	Table 25
C_SET2_PHASE_CAL	0x0529		C core Interleaving phase calibration	Table 26
C_SET2_OFFSET_CAL	0x052A		C core Interleaving offset calibration	Table 27
C_SET3_GAIN_CAL	0x052B		C core Interleaving gain calibration	Table 25
C_SET3_PHASE_CAL	0x052C		C core Interleaving phase calibration	Table 26
C_SET3_OFFSET_CAL	0x052D		C core Interleaving offset calibration	Table 27
C_SDA_CTRL	0x052F	1000	C core Sampling Delay Adjust (0 to 120 ps with a step of 30 fs) bit[11:0] = SDA value bit[9:0]: fine delay, step 30 fs bit[11:10]: coarse delay, step 30 ps bit[12] = SDA disabled 0: enabled 1: disabled (default)	Table 46
D_SET0_GAIN_CAL	0x0722		D core Interleaving gain calibration	Table 25
D_SET0_PHASE_CAL	0x0723		D core Interleaving phase calibration	Table 26
D_SET0_OFFSET_CAL	0x0724		D core Interleaving offset calibration	Table 27
D_SET1_GAIN_CAL	0x0725		D core Interleaving gain calibration	Table 25
D_SET1_PHASE_CAL	0x0726		D core Interleaving phase calibration	Table 26
D_SET1_OFFSET_CAL	0x0727		D core Interleaving offset calibration	Table 27
D_SET2_GAIN_CAL	0x0728		D core Interleaving gain calibration	Table 25
D_SET2_PHASE_CAL	0x0729		D core Interleaving phase calibration	Table 26
D_SET2_OFFSET_CAL	0x072A		D core Interleaving offset calibration	Table 27
D_SET3_GAIN_CAL	0x072B		D core Interleaving gain calibration	Table 25
D_SET3_PHASE_CAL	0x072C		D core Interleaving phase calibration	Table 26
D_SET3_OFFSET_CAL	0x072D		D core Interleaving offset calibration	Table 27
D_SDA_CTRL	0x072F	1000	D core Sampling Delay Adjust (0 to 120 ps with a step of 30 fs) bit[11:0] = SDA value bit[9:0]: fine delay, step 30 fs bit[11:10]: coarse delay, step 30 ps bit[12] = SDA disabled 0: enabled 1: disabled (default)	Table 46
IN0_IN1_CMIREF	0x0905	14	Input common mode calibration for IN0 & IN1 analog inputs	Table 29
IN2_IN3_CMIREF	0x0906	14	Input common mode calibration for IN2 & IN3 analog inputs	Table 29
IN0_IN1_RIN	0x0907	10	Input impedance calibration for IN0 & IN1 analog inputs	Table 30
IN2_IN3_RIN	0x0908	10	Input impedance calibration for IN2 & IN3 analog inputs	Table 30

Registers Names	@ hex	Default value hex	COMMENT	Refer to Table
AB_ROUT_HSSL	0x0909	55	CALIBRATION R LOAD CML bit[1:0] = R_cml0 channel A (for link0) bit[3:2] = R_cml1 channel A (for link1) bit[5:4] = R_cml0 channel B (for link0) bit[7:6] = R_cml1 channel B (for link1)	Table 31
CD_ROUT_HSSL	0x090A	55	CALIBRATION R LOAD CML bit[1:0] = R_cml0 channel C (for link0) bit[3:2] = R_cml1 channel C (for link1) bit[5:4] = R_cml0 channel D (for link0) bit[7:6] = R_cml1 channel D (for link1)	Table 31
DATA_MODE_SEL	0x0B07	7	For all following bits : 0: disabled 1: enabled bit[0] = PRBS enabled bit[1] = DATA enabled (0 means DATA=0) bit[2] = DC-Balance enabled	Table 41
TEST_MODE	0x0B0A	0	For all following bits : 0: disabled 1: enabled bit[0] = ramp mode bit[1] = force VOH bit[2] = force VOL bit[3] = force decimation (/4)	Table 41
A_CALC_OTP_CRC	0x0B0B		CRC calculated after a OTP loading	Table 42
B_CALC_OTP_CRC	0x0B0C		CRC calculated after a OTP loading	Table 42
C_CALC_OTP_CRC	0x0B0E		CRC calculated after a OTP loading	Table 42
D_CALC_OTP_CRC	0x0B0F		CRC calculated after a OTP loading	Table 42
E_CALC_OTP_CRC	0x0B29		CRC calculated after a OTP loading	Table 42
F_CALC_OTP_CRC	0x0B2A		CRC calculated after a OTP loading	Table 42
A_OTP_CRC	0x0B14		CRC OTP reading	Table 42
B_OTP_CRC	0x0B15		CRC OTP reading	Table 42
C_OTP_CRC	0x0B17		CRC OTP reading	Table 42
D_OTP_CRC	0x0B18		CRC OTP reading	Table 42
E_OTP_CRC	0x0B2B		CRC OTP reading	Table 42
F_OTP_CRC	0x0B2C		CRC OTP reading	Table 42
AB_POWER_ON_PACK	0x0B02	FF	Power ON for A,B cores	Table 18
CD_POWER_ON_PACK	0x0B03	FF	Power ON for A,B cores	Table 18
AB_HSSL_POWER_ON	0x0B00	3	A,B Serial links Power ON	Table 19
CD_HSSL_POWER_ON	0x0B01	3	C,D Serial links Power ON	Table 19
CPS_POWER_ON	0x0B04	1	CPS_POWER_ON	Table 20
AB_HSSL_IO_POWER_ON	0x0B05	F	A,B CML ouput Buffers_POWER_ON	Table 21
CD_HSSL_IO_POWER_ON	0x0B06	F	C,D CML ouput Buffers_POWER_ON	Table 21

8 FUNCTIONALITIES DESCRIPTION

8.1 POWER ON mode

All internal blocks can be powered ON or OFF: CPS, anacore circuitry, digital circuitry, TH circuitry, latch circuitry, High Speed serial links (HSSL) and CML buffers (HSSL_IO).
Figure 15 details the layout of these different internal blocks and their respective POWER_ON registers.

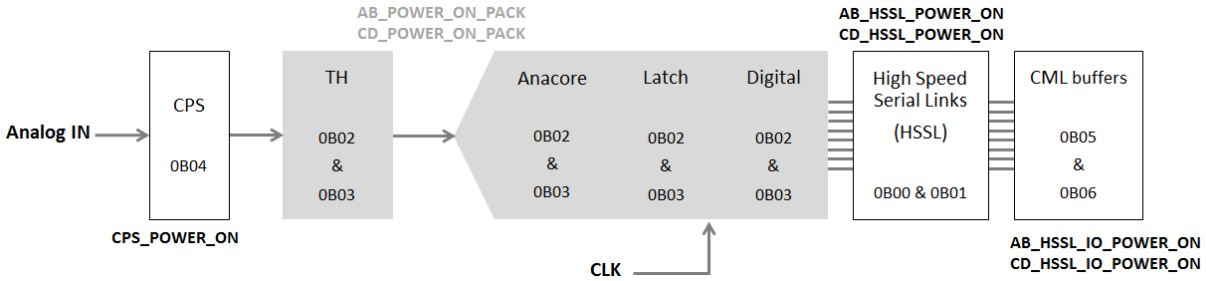


Figure 15: Different Internal blocks
Internal blocks that can be powered ON or OFF and their respective register addresses.

Power-on mode for TH, anacore, latch and digital circuitry can be controlled via AB_POWER_ON_PACK and CD_POWER_ON_PACK registers, described in Table 18.
CML buffers, HSSL and CPS blocks own dedicated registers described in Table 19 to Table 21.

Table 18. AB_POWER_ON_PACK and CD_POWER_ON_PACK registers description

Register Name	@	Type	Size	Default Value	Core	Comment
AB_POWER_ON_PACK	0x0B02	RW	8	0b1111111	A, B	bit[0] = power_on Latch A bit[1] = power_on Latch B bit[2] = power_on Digital A bit[3] = power_on Digital B bit[4] = power_on Anacore A bit[5] = power_on Anacore B bit[6] = power_on TH A bit[7] = power_on TH B 0 : power OFF 1 : power ON bit[15:8] = Reserved
CD_POWER_ON_PACK	0x0B03	RW	8	0b1111111	C, D	bit[0] = power_on Latch C bit[1] = power_on Latch D bit[2] = power_on Digital C bit[3] = power_on Digital D bit[4] = power_on Anacore C bit[5] = power_on Anacore D bit[6] = power_on TH C bit[7] = power_on TH D 0 : power OFF 1 : power ON bit[15:8] = Reserved

Other blocks such as HSSL, CPS and HSSL_IO are addressed through dedicated SPI registers as described below.

Table 19. AB_HSSL_POWER_ON and CD_HSSL_POWER_ON registers description

Register Name	@	Type	Size	Default Value	Core	Comment
AB_HSSL_POWER_ON	0x0B00	RW	2	0b11	A, B	bit[0] = power_on CHANNEL A serial link bit[1] = power_on CHANNEL B serial link 0 : power OFF 1 : power ON bit[15:2] = Reserved
CD_HSSL_POWER_ON	0x0B01	RW	2	0b11	C, D	bit[0] = power_on CHANNEL C serial link bit[1] = power_on CHANNEL D serial link 0 : power OFF 1 : power ON bit[15:2] = Reserved

Table 20. CPS_ POWER_ON register description

Register Name	@	Type	Size	Default Value	Core	Comment
CPS_ POWER_ON	0x0B04	RW	1	0b1	-	bit[0] = power_on CPS 0 : power OFF 1 : power ON bit[15:1] = Reserved

Table 21. AB_HSSL_IO_POWER_ON and CD_HSSL_IO_POWER_ON registers description

Register Name	@	Type	Size	Default Value	Core	Comment
AB_HSSL_IO_POWER_ON	0x0B05	RW	4	0b1111	A, B	CMLx : Serial link x buffer bit[0] = power_on CML1 channel A bit[1] = power_on CML2 channel A bit[2] = power_on CML1 channel B bit[3] = power_on CML2 channel B 0 : power OFF 1 : power ON bit[15:4] = Reserved
CD_HSSL_IO_POWER_ON	0x0B06	RW	4	0b1111	C, D	CMLx : Serial link x buffer bit[0] = power_on CML1 channel C bit[1] = power_on CML2 channel C bit[2] = power_on CML1 channel D bit[3] = power_on CML2 channel D 0 : power OFF 1 : power ON bit[15:4] = Reserved

In order to switch a core in its stand-by mode : latch, digital, anacore and TH circuitry, HSSL and CML buffers of the considered core are required to be powered-OFF.
A SYNC will be sufficient to apply the modifications done in the registers concerning blocks of the power-on mode.
To switch back a core in its power-on mode: all these registers are required to be powered-ON. A SYNC, and eventually a FPGA-RESET, has to follow the registers' switches.

8.2 ADC Synchronization Signal (SYNCTRIGP, SYNCTRIGN)

The SYNCTRIGP, SYNCTRIGN LVDS inputs deliver SYNC signal for synchronization or TRIGGER signal for data Triggering. This section focuses on using the SYNC signal.

Since SYNC is multiplexed with TRIGGER, to perform synchronization, the ADC must be configured in synchronization mode. The SYNC function is enabled by default. Refer to AB_HSSL_CFG and CD_ HSSL_CFG registers in Table 38.

The SYNC signal is mandatory in order to have a deterministic timing for the synchronization of the 4 cores (clock tree and digital reset) and for multiple ADCs time alignment.

It is asynchronous regarding the external clock. It is active high and should be compliant with the timing shown in the chronograms of Figure 12 and specified in Table 9 to work properly. It becomes effective on the rising edge of SYNCTRIGP, SYNCTRIGN.

8.3 Cross-point switch (CPS)

CPS functionality enables different input configurations by switching the signal to the dedicated core (A, B, C or D). IN0 and IN3 can address any core. IN1 and IN2 must be connected to core B and C if used, as described on the Figure 14 below:

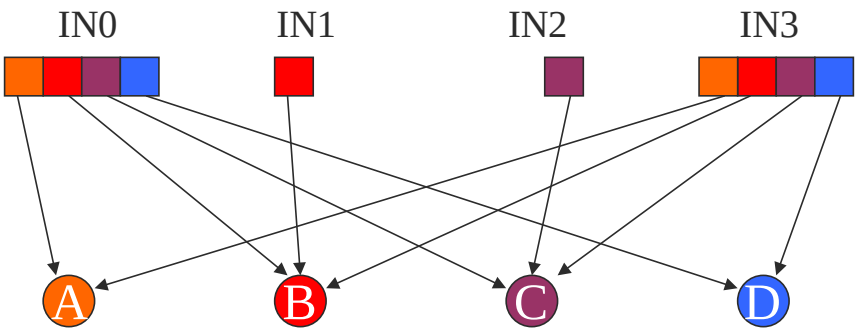


Figure 16: CPS configurations

To interleave A to D cores, IN0 input can be used and register CPS_CTRL has to be set to 0. The right clock distribution has to be chosen (see §8.4).
Different CPS capabilities are described in register CPS_CTRL.

Table 22. CPS_CTRL register description

Register Name	@	Type	Size	Default Value	Core	Comment
CPS_CTRL	0x000B	RW	3	0b0	All	1-channel mode bit[2:0] = 000 : input 0 to core A & B & C & D (default) bit[2:0] = 001 : input 3 to core A & B & C & D 2-channel mode bit[2:0] = 010 : input 0 to core A & B input 3 to core C & D bit[2:0] = 011 : input 0 to core C & D input 3 to core A & B 4-channel mode bit[2:0] = 100 : input 0 to core A input 1 to core B input 2 to core C input 3 to core D bit[15:3] = Reserved

8.4 Clock interleaving

Core A to D could be addressed one to one or interleaved two by two or all four together to reach 6.4 GSps. A dedicated register (CLK_MODE_SEL) has to be used to provide the right clock behavior to each core.

Table 23. CLK_MODE_SEL register description

Register Name	@	Type	Size	Default Value	Core	Comment
CLK_MODE_SEL	0x000A	RW	2	0b00	All	bit[1:0] = clock control 11: clock A=B=C=D , all clocks are in phase 10: clock A=C, clock B=D 01: clock A=B, clock C=D 00: all clocks are interleaved (default) bit[15:2] = Reserved

Detailed clocks chronograms for each configuration are given in Figure 17 to Figure 20.

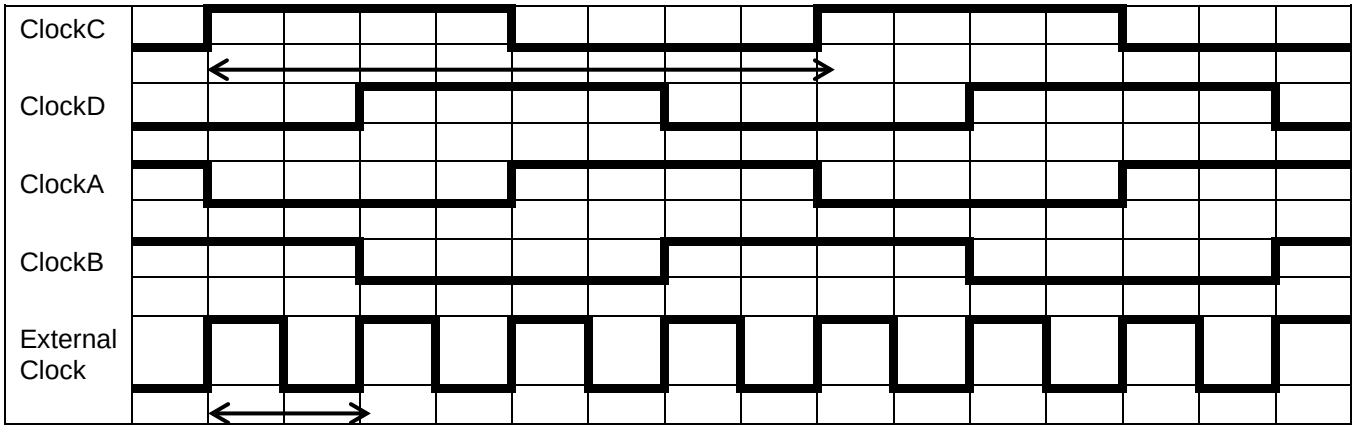


Figure 17: Clocks for four cores interleaved CLK_MODE_SEL = 0

Above clocks mode configuration has to be associated with the case one Input IN0 (or IN3) of the CPS.

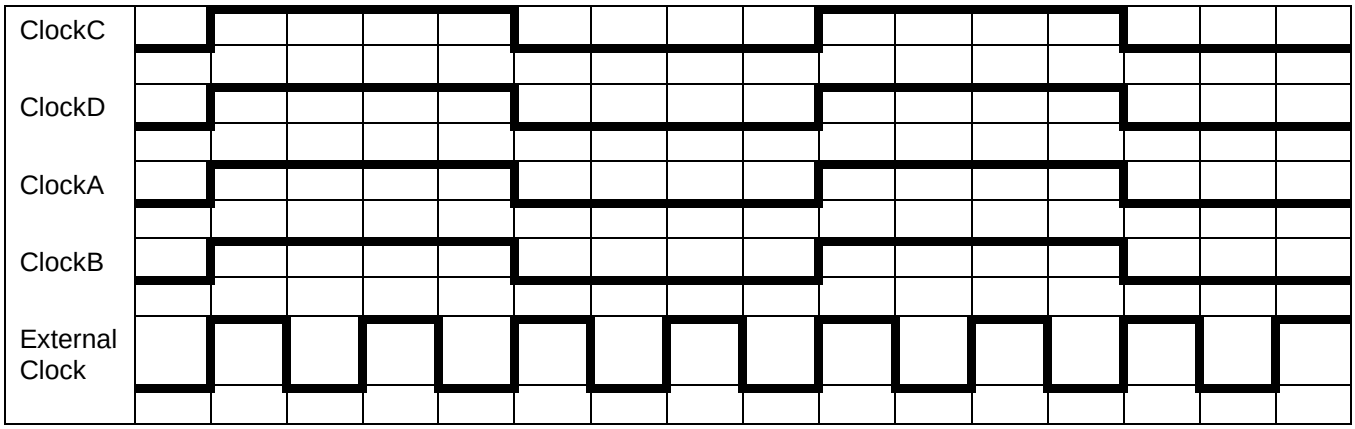


Figure 18: Clocks for four cores aligned averaging or four channels, CLK_MODE_SEL = 3

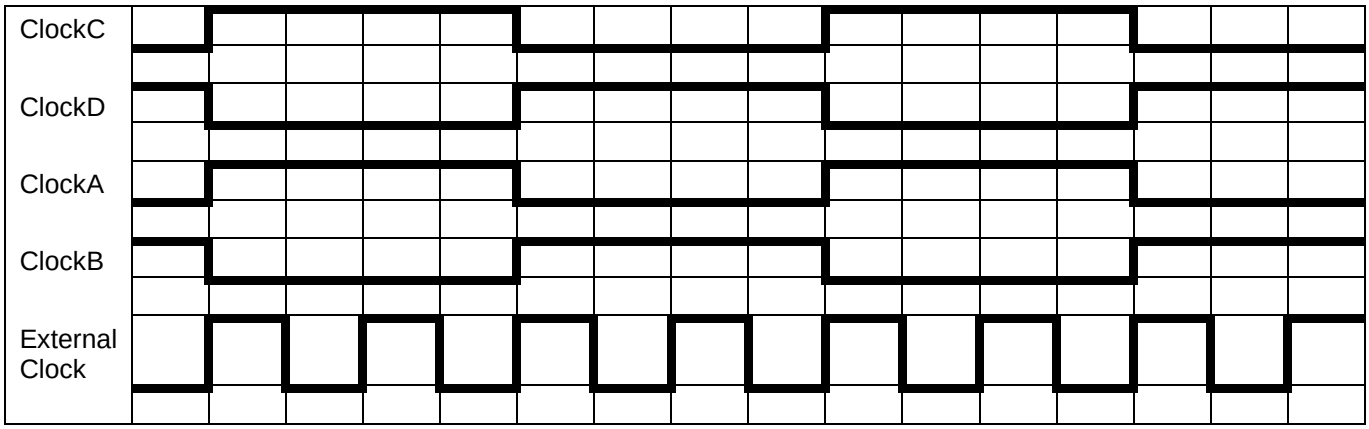


Figure 19: Clocks for two cores interleaving - configuration 1: Interleaved of A and B and interleaved of C and D CLK_MODE_SEL = 1

In this configuration, IN0 and IN3 inputs are used: IN0 provides signal to two cores while IN3 provides the two other cores input.

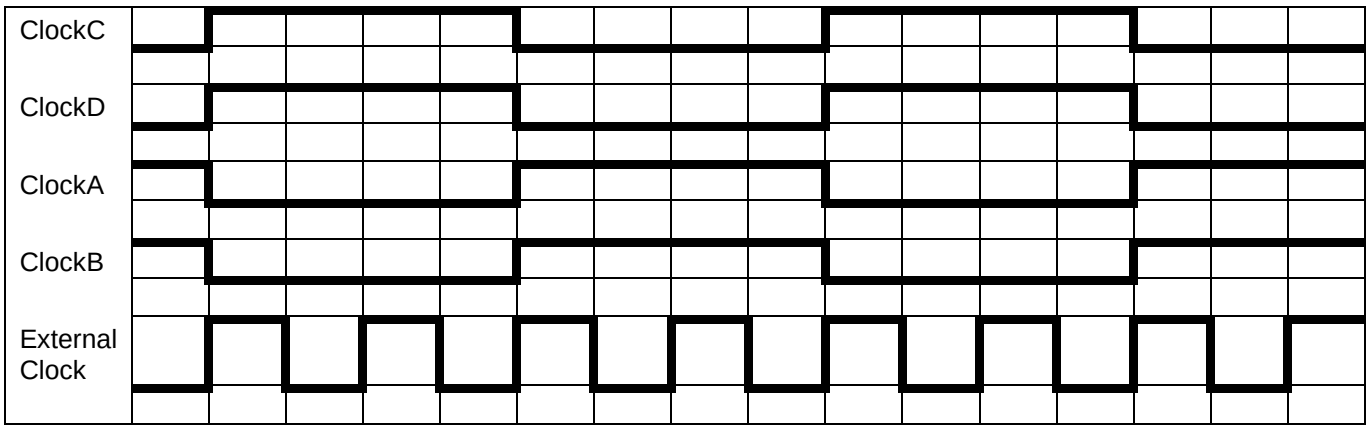


Figure 20: Clocks for two cores interleaving - configuration 2: Interleaving of A and C and interleaving of B and D CLK_MODE_SEL = 2

8.5 Calibrations

Table 24. Functions summary

Calibration	Description
Core gain adjust	ADC gain adjustment
Core phase adjust	ADC sampling phase adjustment
Core offset adjust	ADC DC offset adjustment
CMiref	Input common mode adjustment
Input impedance	100 ohm differential impedance adjustment
CML buffer output impedance	100 ohm differential impedance adjustment

The above functions are accessible through registers described in the following sections.
Factory calibrated values are available in OTP memory cells and are loaded in registers by writing in OTP_LOADING register (Table 42).

8.5.1 Core gain adjustment

The gain of each ADC core is independently adjustable thanks to built-in 12-bit DACs. 16 registers (y_SETx_GAIN_CAL with x=0, 1, 2, 3 and y= A, B, C, D) are available.

Table 25. y_SETx_GAIN_CAL, registers description (x=0, 1, 2, 3 and y= A, B, C, D)

Register Name	@	Type	Size	Default Value	Core	Comment
A_SET0_GAIN_CAL	0x0122	W	12	0x800	A	bit[11:0] = Gain value bit[15:12] = Reserved
B_SET0_GAIN_CAL	0x0322	W	12	0x800	B	
C_SET0_GAIN_CAL	0x0522	W	12	0x800	C	
D_SET0_GAIN_CAL	0x0722	W	12	0x800	D	
A_SET1_GAIN_CAL	0x0125	W	12	0x800	A	bit[11:0] = Gain value bit[15:12] = Reserved
B_SET1_GAIN_CAL	0x0325	W	12	0x800	B	
C_SET1_GAIN_CAL	0x0525	W	12	0x800	C	
D_SET1_GAIN_CAL	0x0725	W	12	0x800	D	
A_SET2_GAIN_CAL	0x0128	W	12	0x800	A	bit[11:0] = Gain value bit[15:12] = Reserved
B_SET2_GAIN_CAL	0x0328	W	12	0x800	B	
C_SET2_GAIN_CAL	0x0528	W	12	0x800	C	
D_SET2_GAIN_CAL	0x0728	W	12	0x800	D	
A_SET3_GAIN_CAL	0x012B	W	12	0x800	A	bit[11:0] = Gain value bit[15:12] = Reserved
B_SET3_GAIN_CAL	0x032B	W	12	0x800	B	
C_SET3_GAIN_CAL	0x052B	W	12	0x800	C	
D_SET3_GAIN_CAL	0x072B	W	12	0x800	D	

The tuning range is equivalent to a 456 LSB variation of full scale (step of 0.11 LSB).

y_SETx_GAIN_CAL (hexa)	Fullscale variation (LSB)
0	264
800	0
FFF	-192
Excursion	456
Step	0.11

8.5.2 Core phase adjustment

The phase of each ADC core is independently adjustable thanks to built-in 9-bit DACs. 16 registers (y_SETx_PHASE_CAL with x=0, 1, 2, 3 and y= A, B, C, D) are available.

Table 26. y_SETx_PHASE_CAL registers description (x=0,1, 2, 3 and y= A, B, C, D)

Register Name	@	Type	Size	Default Value	Core	Comment
A_SET0_PHASE_CAL	0x0123	W	9	0x0100	A	bit[11:0] = Phase value bit[15:12] = Reserved
B_SET0_PHASE_CAL	0x0323	W	9	0x0100	B	
C_SET0_PHASE_CAL	0x0523	W	9	0x0100	C	
D_SET0_PHASE_CAL	0x0723	W	9	0x0100	D	
A_SET1_PHASE_CAL	0x0126	W	9	0x0100	A	bit[11:0] = Phase value bit[15:12] = Reserved
B_SET1_PHASE_CAL	0x0326	W	9	0x0100	B	
C_SET1_PHASE_CAL	0x0526	W	9	0x0100	C	
D_SET1_PHASE_CAL	0x0726	W	9	0x0100	D	
A_SET2_PHASE_CAL	0x0129	W	9	0x0100	A	bit[11:0] = Phase value bit[15:12] = Reserved
B_SET2_PHASE_CAL	0x0329	W	9	0x0100	B	
C_SET2_PHASE_CAL	0x0529	W	9	0x0100	C	
D_SET2_PHASE_CAL	0x0729	W	9	0x0100	D	
A_SET3_PHASE_CAL	0x012C	W	9	0x0100	A	bit[11:0] = Phase value bit[15:12] = Reserved
B_SET3_PHASE_CAL	0x032C	W	9	0x0100	B	
C_SET3_PHASE_CAL	0x052C	W	9	0x0100	C	
D_SET3_PHASE_CAL	0x072C	W	9	0x0100	D	

The tuning range is equivalent to ± 4.5 ps (step of 17 fs).
For wider range, SDA operation described hereafter could also be used.

y_SETx_PHASE_CAL (hexa)	phase variation
0	-4 ps
100	0
1FF	5 ps
Excursion	9 ps
Step	17 fs

8.5.3 Core offset adjustment

The Offset of each ADC core is independently adjustable thanks to built-in 9-bit DACs. 16 registers (y_SETx_PHASE_CAL with x=0, 1, 2, 3 and y= A, B, C, D) are available.

Table 27. y_SETx_OFFSET_CAL registers description (x=0,1, 2, 3 and y= A, B, C, D)

Register Name	@	Type	Size	Default Value	Core	Comment
A_SET0_OFFSET_CAL	0x0124	W	9	0x0100	A	bit[11:0] = Offset value bit[15:12] = Reserved
B_SET0_OFFSET_CAL	0x0324	W	9	0x0100	B	
C_SET0_OFFSET_CAL	0x0524	W	9	0x0100	C	
D_SET0_OFFSET_CAL	0x0724	W	9	0x0100	D	
A_SET1_OFFSET_CAL	0x0127	W	9	0x0100	A	bit[11:0] = Offset value bit[15:12] = Reserved
B_SET1_OFFSET_CAL	0x0327	W	9	0x0100	B	
C_SET1_OFFSET_CAL	0x0527	W	9	0x0100	C	
D_SET1_OFFSET_CAL	0x0727	W	9	0x0100	D	
A_SET2_OFFSET_CAL	0x012A	W	9	0x0100	A	bit[11:0] = Offset value bit[15:12] = Reserved
B_SET2_OFFSET_CAL	0x032A	W	9	0x0100	B	
C_SET2_OFFSET_CAL	0x052A	W	9	0x0100	C	
D_SET2_OFFSET_CAL	0x072A	W	9	0x0100	D	
A_SET3_OFFSET_CAL	0x012D	W	9	0x0100	A	bit[11:0] = Offset value bit[15:12] = Reserved
B_SET3_OFFSET_CAL	0x032D	W	9	0x0100	B	
C_SET3_OFFSET_CAL	0x052D	W	9	0x0100	C	
D_SET3_OFFSET_CAL	0x072D	W	9	0x0100	D	

The tuning range is equivalent to +/- 75 LSB (step of 0.29 LSB)

y_SETx_OFFSET_CAL (hexa)	offset variation (LSB)
0	-75
100	0
1FF	75
Excursion	150
Step	0.29

8.5.4 Calibration selection

The device contains 4 predefined calibration sets. These sets address interleaving Gain, Phase and Offset registers. They ensure optimal interleaving performance depending on the condition of use.
See §9.3.1 for detailed application information.
One set is selected thanks to CAL_SET_SEL register.

Table 28. CAL_SET_SEL register description

Register Name	@	Type	Size	Default Value	Core	Comment
CAL_SET_SEL (*)	0x0009	RW	3	0b000	All	bit [0] = reserved bit[2:1] = phase/gain/offset calibration set selection 00: CalSet0 selected 01: CalSet1 selected 10: CalSet2 selected 11: CalSet3 selected bit[15:3] = Reserved

(*) Only CalSet0 and CalSet1 are available for AQ605

8.5.5 Input common mode calibration

ADC analog input can operates in DC coupling or AC coupling mode. To cope with previous amplifier output stage, ADC input common mode (CMIREF) can be trimmed via IN0_IN1_CMIREF and IN2_IN3_CMIREF registers described below.
Adjustment of input common mode can also be used to optimize ADC linearity.

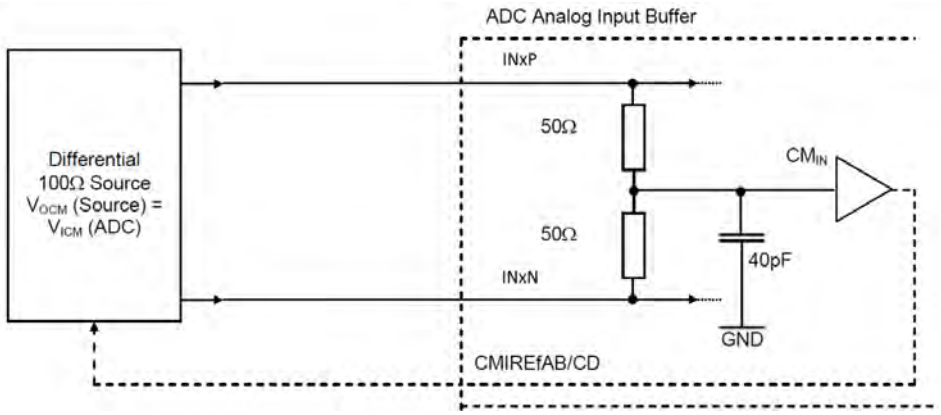


Figure 21: Differential analog input implementation (DC coupled)

Table 29. IN0_IN1_CMIREF and IN2_IN3_CMIREF registers description

Register Name	@	Type	Size	Default Value	Core	Comment
IN0_IN1_CMIREF	0x0905	R/W	5	0x14	A, B	bit[4:0] = Input common mode calibration for A & B cores bit[15:5] = Reserved
IN2_IN3_CMIREF	0x0906	R/W	5	0x14	C, D	bit[4:0] = Input common mode calibration for C &D cores bit[15:5] = Reserved

IN0_IN1_CMIREF IN2_IN3_CMIREF (hexa)	CMIREF (V)
1F	1.555
10	1.580
0	1.680
Excursion	0.125
Step	4.10^{-3}

8.5.6 Input impedance calibration

ADC impedance matching is important to maximize power transmission. DC impedance can be trimmed digitally to 100 (Ω) with IN0_IN1_RIN and IN2_IN3_RIN registers to compensate process variation or optimized power transmission, with 2% accuracy.

Table 30. IN0_IN1_RIN and IN2_IN3_RIN registers description

Register Name	@	Type	Size	Default Value	Core	Comment
IN0_IN1_RIN	0x0907	R/W	5	0x10	A, B	bit[4:0] = Value bit[15:1] = Reserved
IN2_IN3_RIN	0x0908	R/W	5	0x10	C, D	bit[4:0] = Value bit[15:5] = Reserved

IN0_IN1_RIN IN2_IN3_RIN (hexa)	Rin (Ω)
0	140
10	116
1F	85
Excursion	55
Step	1.7

8.5.7 CML output impedance calibration

ADC impedance matching is important to maximize power transmission. DC impedance of CML output buffers can be trimmed digitally to 100 (Ω) with AB_ROUT_HSSL (or CD_ROUT_HSSL) register on both cores A and B (C and D respectively) to compensate process variation or to optimize power transmission, with 5% accuracy.
Note: CLKOUT CML output buffers impedance cannot be trimmed.

Table 31. AB_ROUT_HSSL and CD_ROUT_HSSL registers description

Register Name	@	Type	Size	Default Value	Core	Comment
AB_ROUT_HSSL	0x909	R/W	8	0x55	A, B	CALIBRATION R LOAD CML bit[1:0] = R_cml0 channel A (for link0) bit[3:2] = R_cml1 channel A (for link1) bit[5:4] = R_cml0 channel B (for link0) bit[7:6] = R_cml1 channel B (for link1) bit[15:8] = Reserved
CD_ROUT_HSSL	0x90A	R/W	8	0x55	C, D	CALIBRATION R LOAD CML bit[1:0] = R_cml0 channel C (for link0) bit[3:2] = R_cml1 channel C (for link1) bit[5:4] = R_cml0 channel D (for link0) bit[7:6] = R_cml1 channel D (for link1) bit[15:8] = Reserved

AB_ROUT_HSSL CD_ROUT_HSSL bit[2n+1;2n] (bin)	ROUT (Ω)
[0;0]	83
[0;1]	100
[1;1]	125

n = 0, 1, 2 or 3.

8.6 Analog bandwidth

The ADC core Analog Bandwidth can be selected thanks to EXT_BW_DISABLE register (refer to dynamic characteristic on Table 7).

Table 32. EXT_BW_DISABLE register description

Register Name	@	Type	Size	Default Value	Core	Comment
EXT_BW_DISABLE	0x0008	W	1	0b0	All	bit[0] = 0: extended bandwidth (default) 1: nominal bandwidth bit[15:1] = Reserved

8.7 SYNC, slow and fast output clocks (SSO, CLKOUT)

To use the SYNC signal internally, it should first be sampled by the internal clock. Though, as the SYNC is asynchronous, it may lead to metastability when the internal sampling clock edge is simultaneous with the SYNC signal transition. To prevent this phenomenon, different SPI registers have to be used.

SYNC_FLAG indicates whether the SYNC has been correctly recovered by the system clock or not.

Table 33. SYNC_FLAG register description

Register Name	@	Type	Size	Default Value	Core	Comment
SYNC_FLAG	0x000D	R	1	0b0	All	bit [0] = Indicate timing violation on SYNC 0 : SYNC has been correctly recovered 1 :Timing violation on SYNC

The flag is reset by writing at the SYNC_FLAG_RST register address:

Table 34. SYNC_FLAG_RST register description

Register Name	@	Type	Size	Default Value	Core	Comment
SYNC_FLAG_RST	0x000E	W	1	0b0	All	bit [0] = 0 : reset the flag

Two other SYNC_CTRL register's bits are used to configure the ADC. The first one, described in Table 35, is the sync_edge. It indicates to the ADC the system clock edge to use in order to recover it. The other one is the sync_shift, helpfull to add one to three external clock delays before resetting the ADC timing. Thanks to these registers, the ADC timing can be reset and multiple ADCs can be synchronized.

Table 35. SYNC_CTRL register description

Register Name	@	Type	Size	Default Value	Core	Comment
SYNC_CTRL	0x000C	W	3	0b00	All	bit[0] = sync_edge:Indicate system clock sampling edge for SYNC 0 : Positive edge 1 : Negative edge bit[2:1] = sync_shift : Add one (or more) system clock period on SYNC internal path 00 : No system clock period added 01 : One system clock period added 10 : Two system clock periods added 11 : Three system clock periods added

The slow output clock SSO (used in synchronization, frequency generation and as reference clock for serial link receiver) is not affected by SYNCTRIGP, SYNCTRIGN (not interrupted). It is an LVDS output generated by a 32 times division of the input clock.

The SYNC signal also starts the synchronization sequence of the serial interface.
CLKOUT is an output clock signal provided by the circuit as a clock reference to other ADCs. It has the same frequency as input clock CLKP, CLKN. The output signals SYNCOP, SYNCON result from the sampling of SYNCTRIGP, SYNCTRIGN signals by the system clock.

In order to reach deterministic resynchronization of several ADCs, it is recommended to chain the SYNC of ADC part N on the SYNCO of ADC part N-1. By this way, the delay between the different ADCs will be deterministic, and SYNC tree is still possible.

SYNCO, CLKOUT or SSO signals can be deactivated to save power when multiple ADC chaining is not used. The deactivation is done though OUTPUT_CLK_EN register:

Table 36. OUTPUT_CLK_EN register description

Register Name	@	Type	Size	Default Value	Core	Comment
OUTPUT_CLK_EN	@0x0017	W	3	0b010	All	For all following bit : 0: disabled 1: enabled bit[0] = CLKOUT enabled (disabled by default) bit[1] = SSO enabled (enabled by default) bit[2] = SYNCO enabled (disabled by default)

The signals swing can be reduced to save power though SYNCO_SSO_CLKOUT_FULL_SWING_EN register:

Table 37. SYNCO_SSO_CLKOUT_FULL_SWING_EN register description

Register Name	@	Type	Size	Default Value	Core	Comment
SYNCO_SSO_CLKOUT_FULL_SWING_EN	@0x0005	W	2	0b00	All	For all following bit : 0: reduced 1: full swing bit[1] = LVDS full swing on SSO and SYNCO bit[0] = CML CLKOUT full swing

8.8 Input signal dynamic in-range detection (InRange mode)

InRange mode is activated using AB_HSSL_CFG and CD_HSSL_CFG registers (Table 38).

CB1 or/and CB2 control bits of the serial output frame (see §9.2) is/are low when the ADC input signal is over the ADC dynamic range.

Table 38. AB_HSSL_CFG and CD_HSSL_CFG registers description

Register Name	@	Type	Size	Default Value	Core	Comment
AB_HSSL_CFG	0x0013	W	5	0b11000	A, B	bit[1:0] = CB1 configuration (see §9.2) 00: InRange selected (default) 01: Trigger selected (=> Sync disabled) 10: Timestamp selected 11: Parity selected bit[3:2] = CB2 configuration (see §9.2) 00: InRange selected 01: Trigger selected (=> Sync disabled) 10: Timestamp selected (default) 11: Parity selected bit[4] = LSB first enabled 0: MSB first 1: LSB first (default) bit[15:5] = Reserved
CD_HSSL_CFG	0x0014	W	5	0b11000	C, D	bit[1:0] = CB1 configuration (see §9.2) 00: InRange selected (default) 01: Trigger selected (=> Sync disabled) 10: Timestamp selected 11: Parity selected bit[3:2] = CB2 configuration (see §9.2) 00: InRange selected 01: Trigger selected (=> Sync disabled) 10: Timestamp selected (default) 11: Parity selected bit[4] = LSB first enabled 0: MSB first 1: LSB first (default) bit[15:5] = Reserved

8.9 Trigger mode

Trigger mode is activated using AB_HSSL_CFG and CD_HSSL_CFG registers (Table 38).

The SYNCTRIG input is an LVDS signal. It can be used in 2 different modes: Sync mode (refer to §8.7) or Trigger mode.
CB1 or/and CB2 control bits of the serial output frame (see §9.2) contain a copy of the SYNCTRIG input with the same pipeline delay as the sampled data (refer to timing diagram in the figure below).

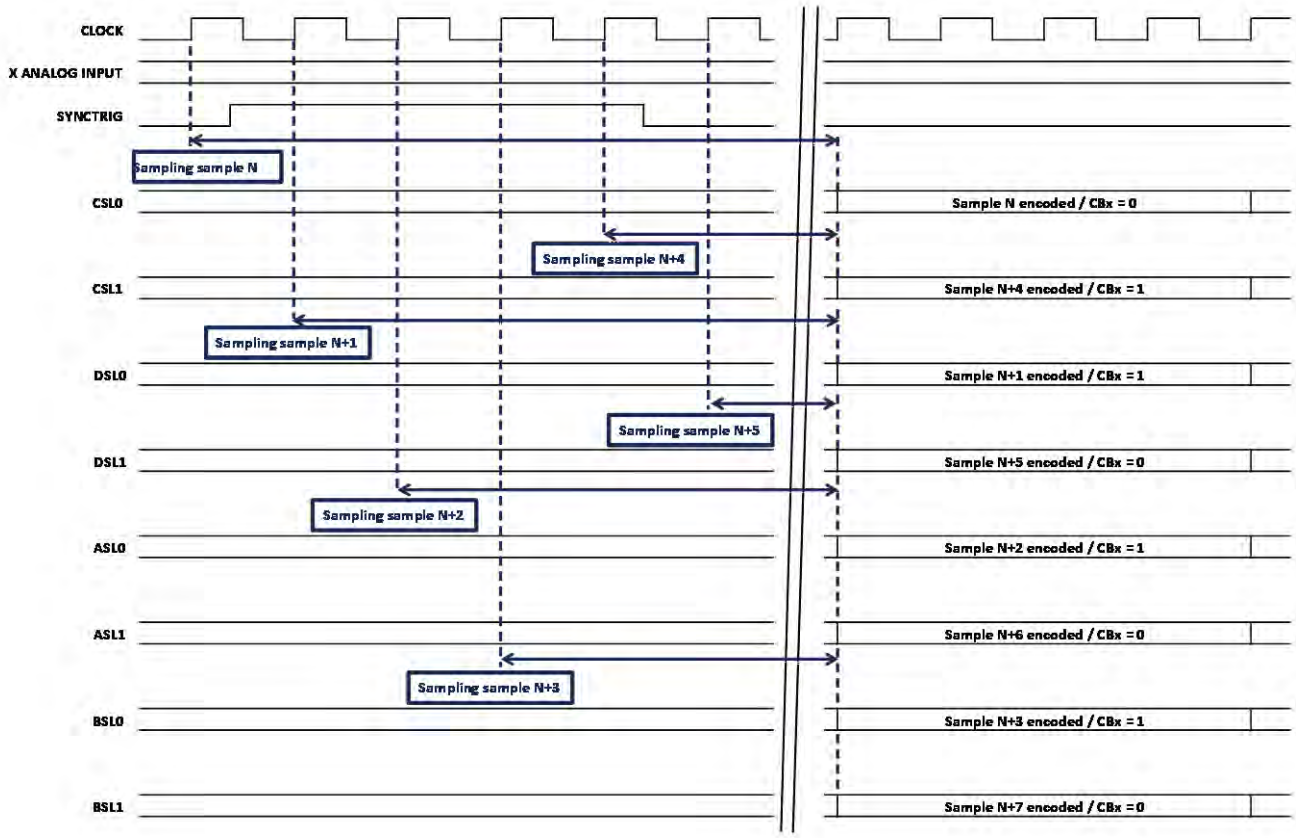


Figure 22: Trigger mode timing diagram in serial interface

8.10 Serial output frame configuration

8.10.1 Serial output frame swing and polarity

IO‘s consumption represents a non-negligible part of dissipation. In case of short routing (in the range of 10 cm) or lower receiver input swing capability, it is possible to reduce the output dynamic and so the consumption by using “swing adjust”. IO’s consumption can be reduced by 1/3.
Note: CLKOUT, SSO, SYNCO and serial link buffers (HSSL links) have independent dynamic settings. Refer to registers of Table 37 for CLKOUT, SSO and SYNCO swing setting.
The configuration is done via registers AB_HSSL_FULL_SWING_EN and CD_HSSL_FULL_SWING_EN.

Table 39. AB_HSSL_FULL_SWING_EN and CD_HSSL_FULL_SWING_EN registers description

Register Name	@	Type	Size	Default Value	Core	Comment
AB_HSSL_FULL_SWING_EN	0x0006	W	1	0b0	A, B	bit[0] = 0: HSSL output swing is reduced (default) 1: full HSSL output swing bit[15:1] = Reserved
CD_HSSL_FULL_SWING_EN	0x0007	W	1	0b0	C, D	bit[0] = 0: HSSL output swing is reduced (default) 1: full HSSL output swing bit[15:1] = Reserved

It is also possible to invert the polarity of serial links outputs thanks to registers AB_HSSL_POL and CD_HSSL_POL.

Table 40. AB_HSSL_POL and CD_HSSL_POL registers description

Register Name	@	Type	Size	Default Value	Core	Comment
AB_HSSL_POL	0x0015	W	4	0b110	A, B	For all following bits : 0: Pin N/P default

Register Name	@	Type	Size	Default Value	Core	Comment
						1: Pin N and P reversed bit[0] = Pin N/P configuration of serial output buffer 0 CHANNEL A bit[1] = Pin N/P configuration of serial output buffer 1 CHANNEL A bit[2] = Pin N/P configuration of serial output buffer 0 CHANNEL B bit[3] = Pin N/P configuration of serial output buffer 1 CHANNEL B bit[15:4] = Reserved
CD_HSSL_POL	0x0016	W	4	0b110	C, D	For all following bits : 0: Pin N/P default 1: Pin N and P reversed bit[0] = Pin N/P configuration of serial output buffer 0 CHANNEL C bit[1] = Pin N/P configuration of serial output buffer 1 CHANNEL C bit[2] = Pin N/P configuration of serial output buffer 0 CHANNEL D bit[3] = Pin N/P configuration of serial output buffer 1 CHANNEL D bit[15:4] = Reserved

When these options are set, samples are output on serial links in one channel interleaved mode according to the timing diagram on Figure 23:

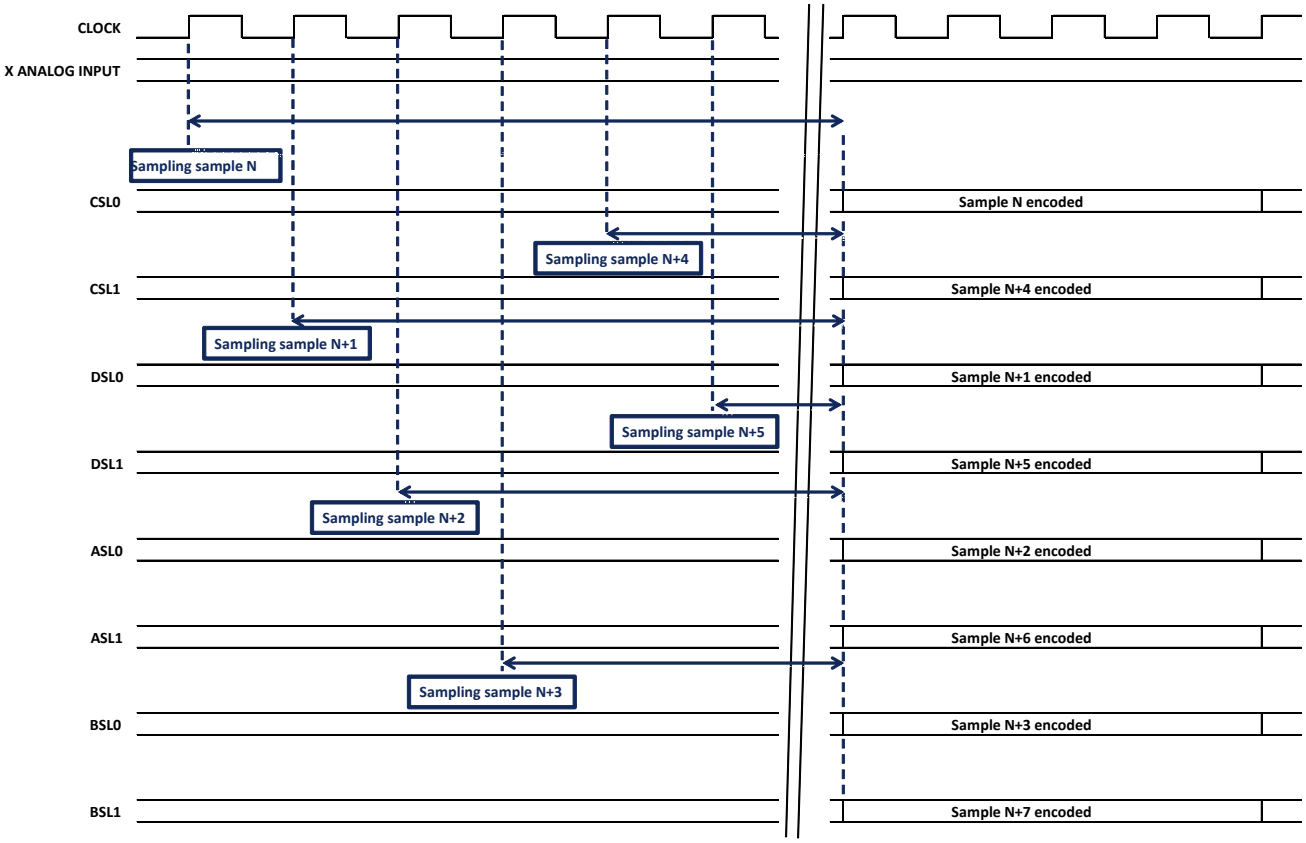


Figure 23: Timing diagram in serial interface in 1-channel mode

In dual interleaved mode, to reconstruct the output signal, BA (or CD) samples have to be considered such as on Figure 24:

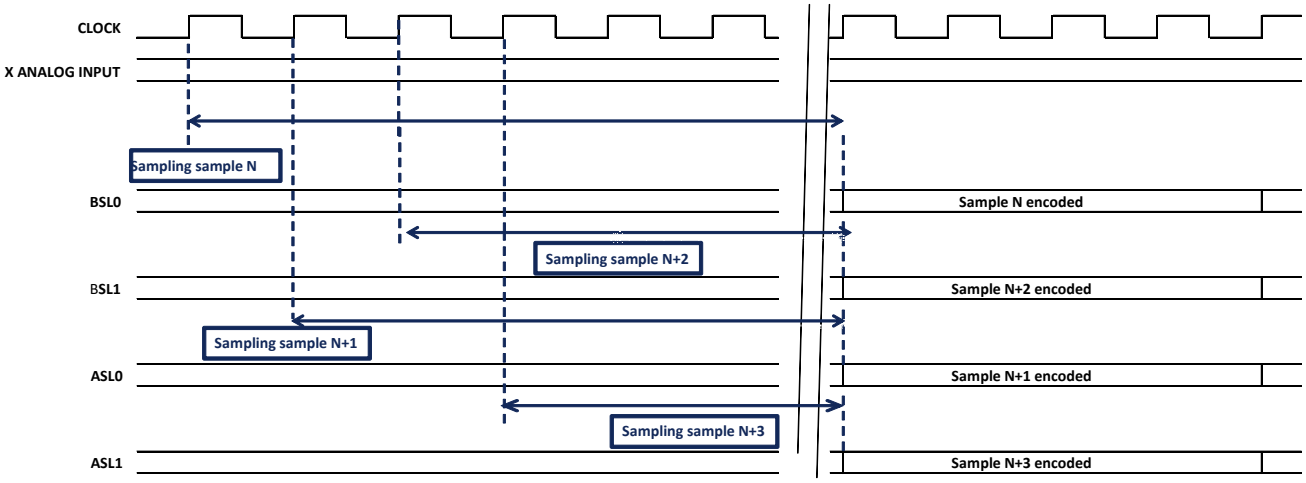


Figure 24: Timing diagram in serial interface in 2-channel mode

8.10.2 Frame order identification (Timestamp mode)

Timestamp mode is activated using AB_HSSL_CFG and CD_HSSL_CFG registers (Table 38).

CB1 or/and CB2 control bits of the serial output frame (see §9.2) contain one bit of a 127-bit PRBS sequence. Every 127 frames, it starts again with bit0.

The PRBS sequence is based on an LFSR of Galois architecture with the polynomial X^7+X^6+1.
It is the same sequence for all links and is reset on SYNCTRIG pulse.
It can be used to identify the samples order and/or check the synchronization of the serial interface.

8.10.3 12-bit data parity (Parity mode)

Parity mode is activated using AB_HSSL_CFG and CD_HSSL_CFG registers (Table 38).

CB1 or/and CB2 control bits of the serial output frame (see §9.2) contain the parity of the 12-bit data.

It is calculated by performing an XOR combination between the 12 bits. It is output in the same frame as the data.

To enable this function, AB_HSSL_CFG and CD_HSSL_CFG registers (Table 38) must be used.

8.10.4 Serial link bits order

In the serial link output frame (see §9.2), using AB_HSSL_CFG and CD_HSSL_CFG registers bit[4], it is possible to define the order (MSB or LSB first) of the converted data (bit[11:0])

8.11 Serial link decimation

Figure 25 shows how the data is outputted on the 2 serial links of each ADC core, xSL0 & xSL1 where x can be A, B, C or D. Link0 outputs data N+2k while link1 outputs data N+(2k+1) (with k ∈|N).

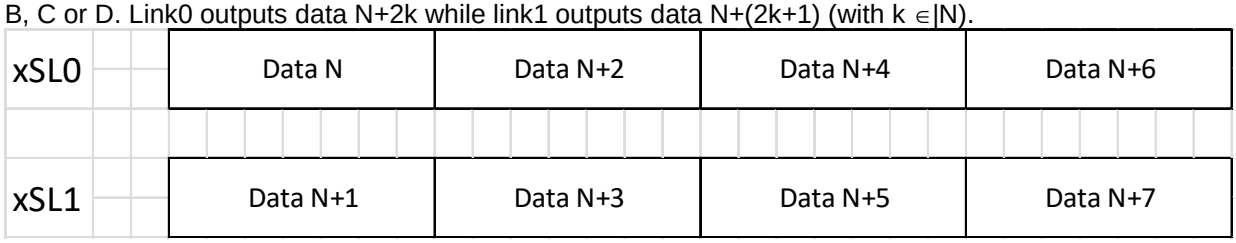


Figure 25: Output data on each serial link.

Powering down one of the links provides a simple way to decimate the output data flow by 2 while lowering power consumption.

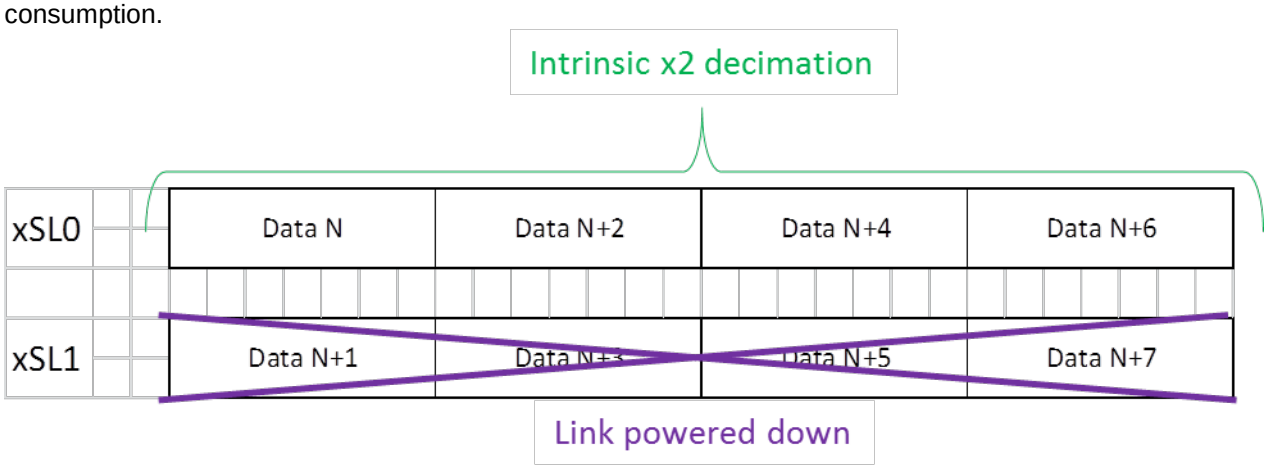


Figure 26: Powering down 1 link gives a x2 decimation.

Serial link can be powered down by using the registers described in AB_HSSL_IO_POWER_ON and CD_HSSL_IO_POWER_ON registers (Table 21).

8.12 Test modes and Data modes

Multiple test modes are available and can be generated by the ADC:

- PRBS : generates a pseudo-random binary sequence on the output
- Ramp : generates a ramp on the output

See below the registers used to enable or disable the different test modes:

Table 41. TEST_MODE & DATA_MODE_SEL registers description

Register Name	@	Type	Size	Default Value	Core	Comment
TEST_MODE	@0x0B0A	W	4	0b0000	All	For all following bits : 0: disabled 1: enabled bit[0] = ramp mode
DATA_MODE_SEL	@0x0B07	W	3	0b111	All	For all following bits : 0: disabled 1: enabled (default) bit[0] = PRBS enabled bit[1] = DATA enabled (0 means DATA=0) bit[2] = DC-Balance enabled

8.12.1 Ramp mode

In ramp mode, the data encoded corresponds to a 12-bit ramp value with only the even values on lane 1 and the odd values on lane 2.

See below the chronogram of the ramp test mode. The data shown in the following figure 24 only presents the 14 bits data from the ADC (12 bits sample value plus 2 control bits CB1 and CB2) and does not include the encoding of the ESIstream protocol which is used on the serial interface, in order to understand the ramp test mode (for more information on CB1 and CB2, see paragraph □).

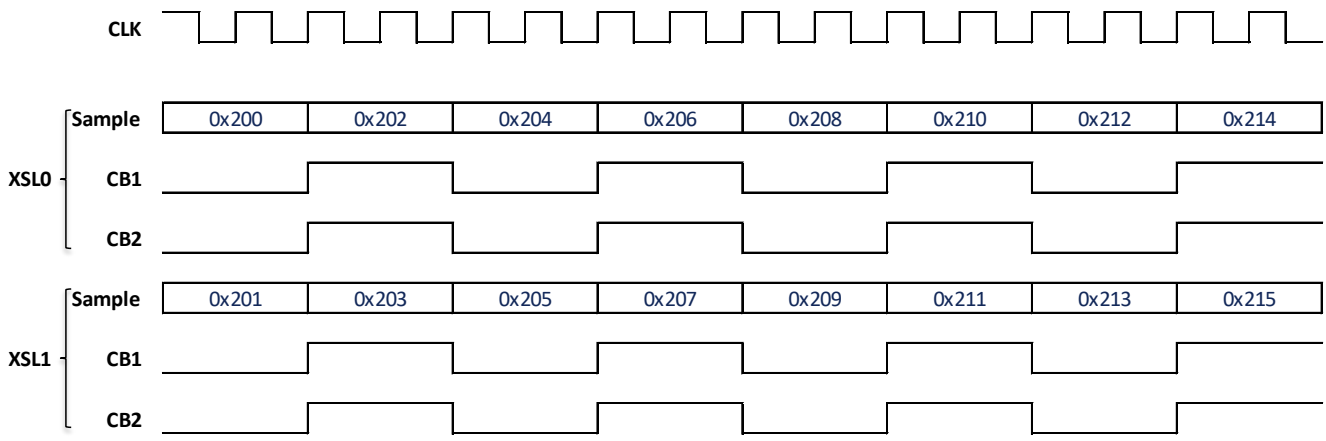


Figure 27: Chronogram of the Ramp test mode

8.12.2 PRBS and DATA

If PRBS is enabled, Pseudo Random Bit Sequence is generated. It can be:

- Added to data (PRBS enabled and DATA enabled)
- Outputted without data (PRBS enabled and DATA disabled)

PRBS and DATA modes are enabled by default and scrambling is done using a LFSR (Linear Feedback Shift Register). See ESIstream protocol §9.2.1

8.12.3 DC balance

There are two main issues in serial transmission. First, the transmission must be DC balanced to avoid voltage imbalance issues while allowing AC coupling between transmitter and receiver. The second issue is brought by the CDR in the receiver. This component uses the edges in the transmission to recover the clock. Thus, if there are long series of '1' or '0', the lock can be lost in the receiver.
To avoid this kind of problem, a DC balance can be added using bit[15] of the ESIstream protocol frame: if bit[15] is set to 1, the bits parity is inverted. Otherwise, nothing is done.

8.13 CRC CHECKING

In order to check OTP cells are not corrupted and have been successfully loaded in SPI registers during device start-up (see §6), CRCs (Cyclic Redundancy Check) are calculated and written in OTP cells during electrical test. Those are the CRC reference values.

During device start-up,

- OTP memory cells are loaded in SPI registers
- In particular, CRC reference values are loaded in x_OTP_CRC registers (x = A, …, F)
- CRC of the SPI registers are calculated and written in x_CALC_OTP_CRC registers (x = A, …, F)

By comparing x_OTP_CRC registers (x = A, …, F) and x_CALC_OTP_CRC registers (x = A, …, F), it is possible to detect any cells corruption.

Table 42. CRC registers description

Register Name	@	Type	Size	Default Value	Core	Comment
OTP_LOADING	@0x0001	W	1	NA	All	bit[0] = to load OTP values into the SPI registers. 0 or 1 : load OTP values into SPI registers This is a write only register
A_CALC_OTP_CRC	@0x0B0B	R	16	N/A	A	CRC of SPI registers calculated after a OTP loading
B_CALC_OTP_CRC	@0x0B0C	R	16	N/A	B	CRC of SPI registers calculated after a OTP loading
C_CALC_OTP_CRC	@0x0B0E	R	16	N/A	C	CRC of SPI registers calculated after a OTP loading
D_CALC_OTP_CRC	@0x0B0F	R	16	N/A	D	CRC of SPI registers calculated after a OTP loading
E_CALC_OTP_CRC	@0x0B29	R	16	N/A	A & B	CRC of SPI registers calculated after a OTP loading
F_CALC_OTP_CRC	@0x0B2A	R	16	N/A	C & D	CRC of SPI registers calculated after a OTP loading

Register Name	@	Type	Size	Default Value	Core	Comment
A_OTP_CRC	@0x0B14	R	16	N/A	A	CRC of OTP cells
B_OTP_CRC	@0x0B15	R	16	N/A	B	CRC of OTP cells
C_OTP_CRC	@0x0B17	R	16	N/A	C	CRC of OTP cells
D_OTP_CRC	@0x0B18	R	16	N/A	D	CRC of OTP cells
E_OTP_CRC	@0x0B2B	R	16	N/A	A & B	CRC of OTP cells
F_OTP_CRC	@0x0B2C	R	16	N/A	C & D	CRC of OTP cells

8.14 CHIP ID

Chip_ID can be read though dedicated register CHIP_ID described below:

Table 43. CHIP_ID register description

Register Name	@	Type	Size	Default Value	Core	Comment
CHIP_ID	0x0011	R	16	0x914	-	Chip id value is 0x914

8.15 Single event protection

All sensitive areas of the device have been protected to increase robustness. This includes but is not limited to clock circuitry and SPI registers. To improve even more the robustness, an extra protection mode has been implemented. It can be activated through the EXTRA_SEE_PROTECT register.

Table 44. EXTRA_SEE_PROTECT register description

Register Name	@	Type	Size	Default Value	Core	Comment
EXTRA_SEE_PROTECT	0x0002	RW	1	0b0	All	Additional protection against Single Event 0: major protection is available (default) 1: additional protection is available _ All SPI registers can't be accessed, except this register _ SYNC is disabled _ The presence of the CLOCK SPI refreshes Triple Majority Redundancy registers

Enabling register EXTRA_SEE_PROTECT by writing ‘1’ disables the SYNCTRIG input when in SYNC mode and thus prevents unwanted timing reset of the ADC (see §8 for more information). It prevents as well any modification on the SPI registers. The SPI clock (SCLK) can be provided from time to time to refresh the SPI (and flush out any SE that would have impacted one branch of the TMR). When it is necessary to modify the configuration of the device or synchronize the ADC, this register needs to be set back to ‘0’.
The consequences of extra SEE protection activation are described in Table 45.

Table 45. Consequences of extra SEE protection activation

	PROTECTION OFF	PROTECTION ON
SYNC mode	SYNC possible	SYNC deactivated
Trigger mode	No SYNC possible, Trigger mode operating	
Registers	Registers can be modified by OTP or SPI	Registers cannot be modified

8.16 SDA operation

The effective sampling instant of each ADC core can be adjusted independently via registers x_SDA_CTRL (with x=A, B, C or D) thanks to two built-in fine and coarse internal clock shifters (fine: 1023 steps of 37 fs, coarse: addition of 0, 1, 2 or 3 delay of 37 ps).
The total tuning range is 150 ps. Delay is set only through SPI instructions. By default, SDA is disabled (by-passed). Activating the SDA has an impact on the jitter performance of the device.

This function is available in 2-channel and 4-channel modes. Contact GRE-HOTLINE-BDC@TELEDYNE.COM for availability in 1-channel mode.

Table 46. A_SDA_CTRL, B_SDA_CTRL, C_SDA_CTRL and D_SDA_CTRL registers description

Register Name	@	Type	Size	Default Value	Core	Comment
A_SDA_CTRL	0x012F	W	13	0x1000	A	A core Sampling Delay Adjust (0 to 150 ps with a step of 37 fs) bit[11:0] = SDA value bit[9:0]: fine delay, step 37 fs bit[11:10]: coarse delay, step 37 ps bit[12] = SDA disabled 0: enabled 1: disabled (default) bit[15:13] = Reserved
B_SDA_CTRL	0x032F	W	13	0x1000	B	B core Sampling Delay Adjust (0 to 150 ps with a step of 37 fs) bit[11:0] = SDA value bit[9:0]: fine delay, step 37 fs bit[11:10]: coarse delay, step 37 ps bit[12] = SDA disabled 0: enabled 1: disabled (default) bit[15:13] = Reserved
C_SDA_CTRL	0x052F	W	13	0x1000	C	C core Sampling Delay Adjust (0 to 150 ps with a step of 37 fs) bit[11:0] = SDA value bit[9:0]: fine delay, step 37 fs bit[11:10]: coarse delay, step 37 ps bit[12] = SDA disabled 0: enabled 1: disabled (default) bit[15:13] = Reserved
D_SDA_CTRL	0x072F	W	13	0x1000	D	D core Sampling Delay Adjust (0 to 150 ps with a step of 37 fs) bit[11:0] = SDA value bit [9:0]: fine delay, step 37 fs bit[11:10]: coarse delay, step 37 ps bit[12] = SDA disabled 0: enabled 1: disabled (default) bit[15:13] = Reserved

8.17 Die junction temperature monitoring diode

Two pins are provided so that the diode can be probed using standard temperature sensors. Maximum current allowed on this pin is 1.2 mA.
The diode measures the junction temperature which is 7.5 °C below the hot spot (but higher than die average temperature)

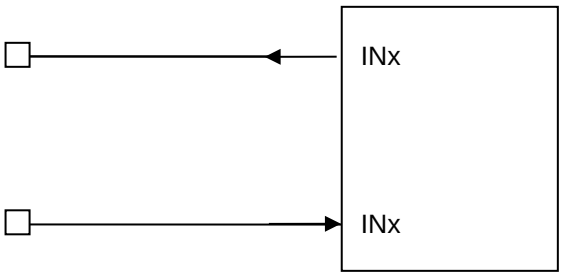


Figure 28: Junction temperature monitoring diode system

Note: If the diode function is not used, the diode pins can be left unconnected (open). If diode is used it is mandatory to connect DiodeC to GND.

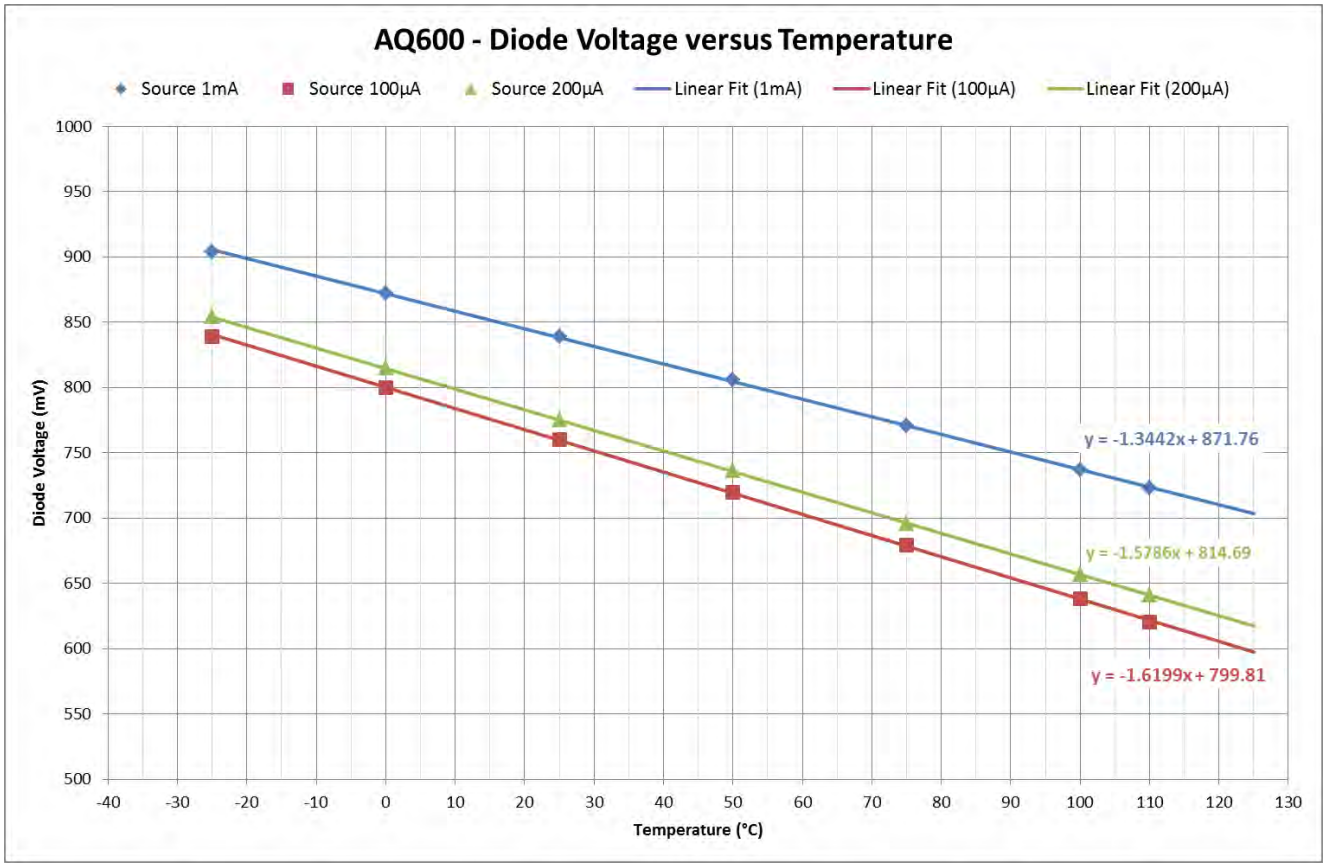


Figure 29: Diode voltage vs temperature for 3 different input currents
(blue: 1 mA, green: 200 µA, red: 100 µA)

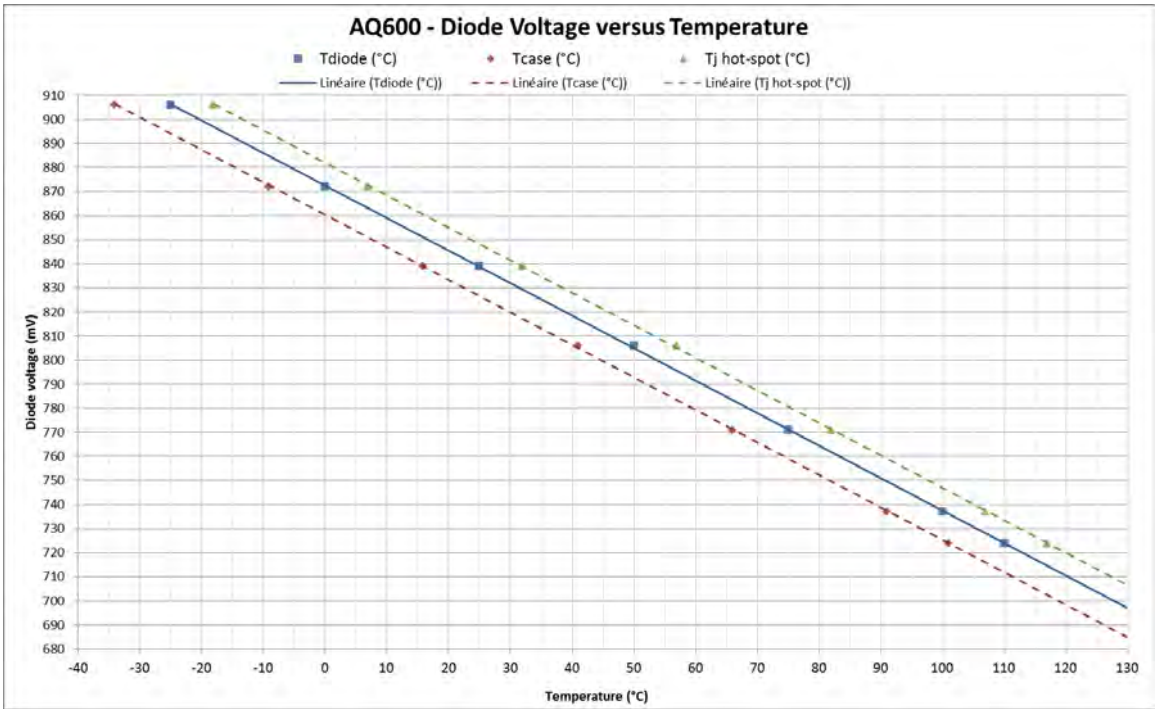


Figure 30: Voltage vs temperature.
Blue=diode voltage - Green=hot-spot junction voltage- Red=case voltage.

8.18 Default mode

- 4 ADC cores are interleaved (1).
- Serial buffer in reduced swing (low power) mode
- Extended analog bandwidth selected

(1) To maximize interleaved performances refer to §9.2.3

Table 47. Functionalities summary

Functionality / mode	By default(1)	Description
Decimation	Disabled	8 HSSL lanes by default
Swing adjust	Enabled	Reduced swing
Input common mode value	1.6 V	
Input impedance value	100 Ω	
CML impedance value	100 Ω	
Gain Adjust	0 LSB	
Offset Adjust	0 LSB	
Phase adjust	0 ps	
SDA	Disabled	Function available in 2-channel and 4-channel modes(2)
Power ON Mode	No standby	
InRange	Enabled	Input signal in the ADC dynamic range or not
Sync / Trigger mode	Sync mode	
Test mode	Disabled	Input signal is sampled and encoded (instead of an internal ramp)
Analog bandwidth	Extended	
SEE protection	Disabled	
Junction temperature monitoring	NA	Refer to §8.17

Note (1): After the Start-up procedure (refer to §6).

Note (2): Contact GRE-HOTLINE-BDC@TELEDYNE.COM for availability of SDA function in 1-channel mode.

9 APPLICATION INFORMATION

9.1 Power supplies

9.1.1 Power supply ramp-up

Supplies settling time should be faster than 10 ms. No specific power sequencing is required. However, in order to avoid possible current peak at Start-up, it is recommended to use the following sequence: V_{CCD}/V_{CCO}/V_{CCA}. V_{CC_SPI} can be powered up at any time.

9.1.2 Decoupling and grounding

As close as possible to each power supply sources (V_{CCA}, V_{CCO}, V_{CCD}, V_{CC_SPI}) and depending on the linear regulators specifications, 100 nF and 22 µF capacitors in parallel are recommended.

As close as possible to the EV12AQ60x power supply pins, it is recommended to add a decoupling capacitors for each V_{CCA}-AGND, V_{CCD}-DGND, V_{CCO}-GNDO neighboring pins described in Figure 10 and Table 48 to Table 50. The value of the capacitance for each neighboring pins is provided in Figure 31.

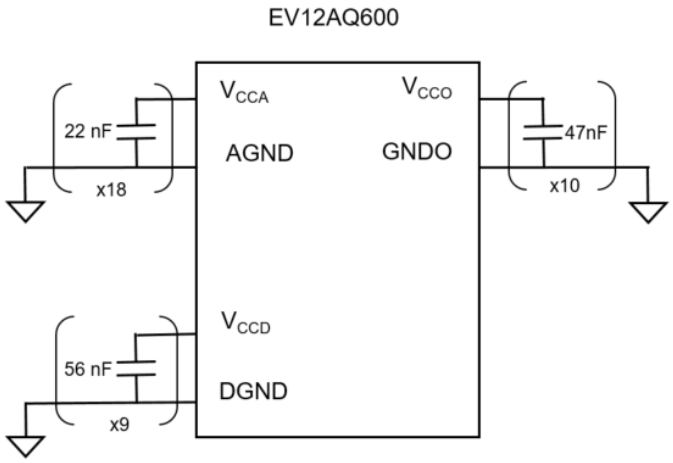


Figure 31: Power Supplies decoupling scheme

Table 48. List of recommended neighboring pins for V_{CCA} decoupling

(V_{CCA} - AGND)
Pins (E9-D9) (E10-D10) (G9-F9) (G10-F10) (G11-F11) (G8-F8) (J8-H8) (J11-H11) (H9-J9) (H10-J10) Pins (K8-K7) (K11-K12) (K9-L9) (K10-L10) (L8-M8) (L11-M11) (M9-N9) (M10-N10)

Table 49. List of recommended neighboring pins for V_{CCD} decoupling

(V_{CCD} - DGND)
Pins (G6-G7) (H6-J6) (K6-L6) (M6-N6) Pins (G13-G12) (H13-J13) (K13-L13) (M13-N13) (F14-F13)

Table 50. List of recommended neighboring pins for V_{CCO} decoupling

(V_{CCO} – GNDO)
Pins (H4-J4) (M4-L4) (K4-K3) (H5-J5) (M5-L5) Pins (H14-J14) (M14-L14) (K15-K16) (H15-J15) (M15-L15)

9.2 High Speed Serial Interface

More information on the ESIstream protocol can be found on www.esistream.com.

ESIstream provides an efficient 14b/16b High-Speed serial data transmission protocol deploying Current Mode Logic (CML) transceivers. It is open-source and supports in particular serial communication between FPGAs and High-Speed data converters.

ESIstream protocol initiated by Teledyne-e2v is born from a severe need of the following combination:
Reduced data overhead on serial links, as low as possible.
Increased rate of useful data when linking ADCs operating at GSPS speeds with FPGAs on a serial interface.
Simplified hardware implementation, simple enough to be built on RF SiGe technologies.

An ESIstream system comprises at a minimum a transmitter and a receiver.
A transmitter can be an ADC or an FPGA or an ASIC
A receiver can be a DAC or an FPGA or an ASIC
A number of lanes (L ≥ 1) to transmit serial data
A synchronization signal (sync) to initialize the communication.

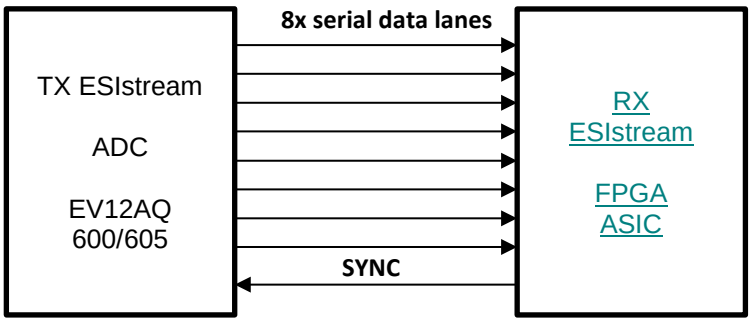


Figure 32: ESIstream system example using EV12AQ60x ADC

ESIStream uses 14/16 bit coding giving it a 87.5% data rate efficiency. In other words, the encoding takes 14-bit of raw data and adds two bits of protocol overhead. The overhead comprises a clock bit which provides a data lane monitor of continuous link synchronization. The second bit of overhead is the disparity bit which is used to ensure DC balance is maintained in each data lane. The 16-bit ESIstream frame comprises a scrambled version of the data word combined with the overhead bits.

Each 14-bit of raw data contain 12-bit sample data and 2 control bits, CB1 & CB2 (defined using AB_HSSL_CFG and CD_HSSL_CFG registers (Table 38)), are added.
This 14-bit frame is first scrambled (to ensure statistical DC balanced transmission). The ESIstream transmit encoding system comprises a linear feedback shift register (LFSR) which generates a pseudo random binary sequence (PRBS), based on a Fibonacci polynomial, which is used to scramble raw data.

Figure 33: 14-bit scrambled frame

Then the 14-bits frame is encoded Encoding process comprises concatenation of the clock bit to the 14-bit frame, a disparity processing applied on the 15-bits frame (raw data & clock bit) and concatenation of the disparity bit.

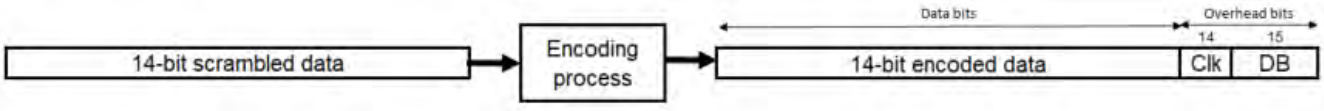


Figure 34: 16-bit encoded frame

The 16-bit frame thus obtained is sent through high-speed serial link.

During normal operation, the synchronization of the serial links can be monitored through the Clk bit. If the receiver does not detect that the Clk bit is toggling properly, then it can state that the link is not synchronous or has lost its synchronization and restart the synchronization process. Another option is to use the timestamp control bit (§8.10.2) of the ADC to monitor the interface synchronization.

9.2.1 ESIstream protocol

9.2.1.1 Synchronization

The link must be synchronized to align the frames between the transmitter and the receiver and to synchronize the reception scrambler with the transmission scrambler. The synchronization is controlled through the SYNC signal sent by the receiver (FPGA/ASIC) to the transmitter (EV12AQ60x).

The synchronization works in 2 steps and starts when the ADC receives a SYNCTRIG pulse in SYNC mode (refer to §8).

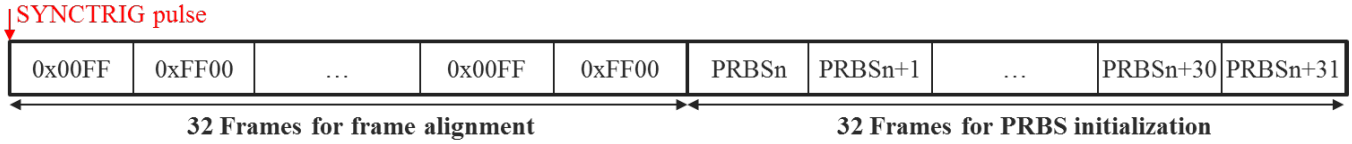


Figure 35: Synchronization sequence

When the ADC detects the SYNCTRIG pulse, it will send an alignment pattern which is 32 frames alternating between 0xFF00 and 0x00FF. The sequence bypasses the scrambling and disparity processing (as the sequence is already DC balanced). This alignment pattern should be used by the receiver to align its data on the transmitter output data. After these 32 frames, the transmitter starts sending 32 additional frames containing the scrambling PRBS alone. These frames contain 14 bits of the PRBS, a reserved bit and the disparity bit (they go through the disparity processing, as the PRBS value will start to impact the running disparity of the transmission).

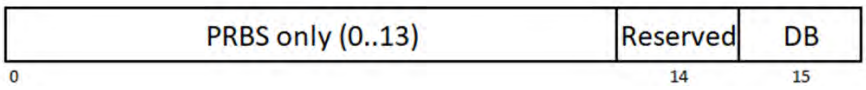


Figure 36: Frame sent for PRBS initialization

The receiver will detect the transition from the alignment pattern 0xFF0000FF to the PRBS alone (passive detection). The ESIstream receive decoding system also comprises a linear feedback shift register (LFSR) which generates a PRBS based on the same Fibonacci polynomial, which is used to descramble raw data.

The receiver LFSR module rebuilds an LFSR initialization values from a minimum of two PRBS data frames sent by the TX to be synchronized with the transmit LFSR mode and properly descramble data. Generally this should be the first data immediately after the frame alignment sequence. When frame data is not the comma code, then the Rx knows the next data frames represent the start of the PRBS alignment sequence.
LFSR uses this initialization value to generate the same PRBS values used by the TX to scramble data. Then the decoding module uses these residual PRBS values to descramble data applying bit-to-bit exclusive ORing operation between aligned data and RX PRBS values.

After these 2 steps, the synchronization of the link is complete.

The PRBS sequence is reset upon reception of a SYNCTRIG pulse in SYNC mode.

9.2.1.2 Scrambling

Applying scrambling ensures a statistical DC balanced transmission. It also statistically ensures that there are enough transitions within the transmitted data stream to ensure the link remains locked at the receive end of the link. It is necessary to comply with these constraints otherwise the Clock and Data Recovery (CDR) module used by the receiver may lose its lock and the data would be corrupted.

The scrambling technique used in ESIstream is an additive scrambling to avoid error propagation in case of a single bit error. It is based on Fibonacci architecture using the following polynomial: $X^{17}+X^{3}+1$. It has a run length of 2^{17} -

1. Instead of using a shift of one bit per operation, it uses shifts of 14 bits per operation to adapt to the size of the data being scrambled.
The equations to use to generate this PRBS are as follow:

$$LFSR_{n+1}(0) = LFSR_n(14)$$
$$LFSR_{n+1}(1) = LFSR_n(15)$$
$$LFSR_{n+1}(2) = LFSR_n(16)$$
$$LFSR_{n+1}(3) = LFSR_n(0) \text{ xor } LFSR_n(3)$$
$$LFSR_{n+1}(4) = LFSR_n(1) \text{ xor } LFSR_n(4)$$
$$LFSR_{n+1}(5) = LFSR_n(2) \text{ xor } LFSR_n(5)$$
$$LFSR_{n+1}(6) = LFSR_n(3) \text{ xor } LFSR_n(6)$$
$$LFSR_{n+1}(7) = LFSR_n(4) \text{ xor } LFSR_n(7)$$
$$LFSR_{n+1}(8) = LFSR_n(5) \text{ xor } LFSR_n(8)$$
$$LFSR_{n+1}(9) = LFSR_n(6) \text{ xor } LFSR_n(9)$$
$$LFSR_{n+1}(10) = LFSR_n(7) \text{ xor } LFSR_n(10)$$
$$LFSR_{n+1}(11) = LFSR_n(8) \text{ xor } LFSR_n(11)$$
$$LFSR_{n+1}(12) = LFSR_n(9) \text{ xor } LFSR_n(12)$$
$$LFSR_{n+1}(13) = LFSR_n(10) \text{ xor } LFSR_n(13)$$
$$LFSR_{n+1}(14) = LFSR_n(11) \text{ xor } LFSR_n(14)$$
$$LFSR_{n+1}(15) = LFSR_n(12) \text{ xor } LFSR_n(15)$$
$$LFSR_{n+1}(16) = LFSR_n(13) \text{ xor } LFSR_n(16)$$

The PRBS is applied to the raw data (or useful data) as follow; the 14 LSB of the PRBS are the bits used to scramble the data.

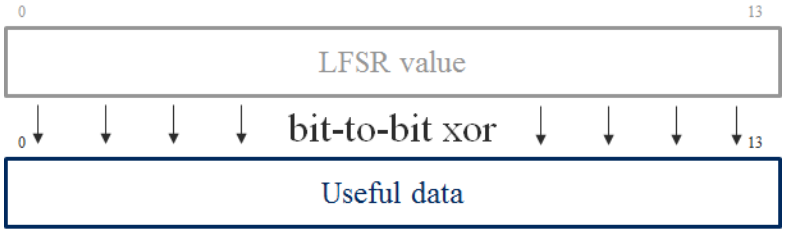


Figure 37: LFSR operation

9.2.1.3 **Encoding**

After encoding, a frame contains 16 bits (14 bits of scrambled data and 2 bits of overhead). The first overhead bit is the clk bit; it toggles at every frame. The other is the disparity bit of the 14-bit scrambled data + clock bit. Its objective is to ensure deterministically the advantages brought statistically by the scrambling process.

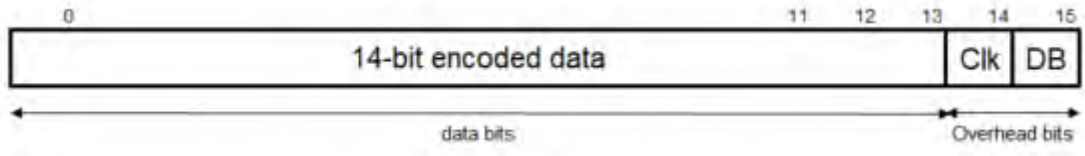


Figure 38: Frame format after encoding

Even with scrambling, large running disparity can still occur with very low probability and could produce excessive eye shifts. These eye shifts could be balanced by a more complicated equalization stage in the receiver if the running disparity was still limited. However, a PRBS does not bind the running disparity deterministically, thus the data could be corrupted on the reception end and it could eventually cause the CDR to lose its lock. To prevent this, the disparity bit is implemented.

The running disparity of the transmission is constantly monitored by the transmitter on each link.
For each frame, its disparity is calculated, 2 cases can occur on the running disparity:

- The running disparity of the transmission does not increase above +/- 15 (+15 and -15 included). In this case, the disparity bit is set to ‘0’ and the 15 bits of data (scrambled data + clk bit) are transmitted as such.
- The running disparity of the transmission does increase above +/-15 (+15 and -15 excluded). In this case, the 15 bits of data (scrambled data + clk bit) are inverted, using a bit-to-bit not operation, and the disparity bit is set to ‘1’.

The running disparity is updated with the disparity of the frame. This disparity bit ensures that the longest possible series of ’1’ or ‘0’ transmitted is of 48 bits (the clk bit reduces this value effectively to 32). It also ensures that the running disparity does not exceed +/- 15 (included) which satisfies the DC balance condition.

In normal operating mode, the receiver will check the disparity bit first. If it is high then it will invert the received data and then descramble them. Otherwise it will directly descramble them.

9.2.1 Multi-lanes synchronization

In a system with multiples lanes, the latency is composed of the TX latency, lane propagation delays and RX latency. These delays (latencies and propagation delays) may differ between lanes. The lane propagation delay will depend on the PCB trace length, the skew between the lanes. One of the advantages of serial interfaces is that the constraint on the trace lengths matching is much smaller compared to parallel interface and so it is only limited by the RX buffer size and the trace attenuation. The TX and RX latencies will depend on the use of elastic buffer introducing variable latencies on each lane.
Additional processing needs to be implemented to compensate the skew between lanes introduced by these delays at RX HSSL inputs and to ensure all lanes are aligned at the RX stage outputs. To achieve that, ESIstream RX integrates an output buffer to compensate each the skew between each lane. This buffer can be a shift register or a FIFO.
The idea is that on each lane, the transfer from the frame alignment sequence to the PRBS alignement sequence would be recovered. When it is found on a lane, its data starts to be written in the buffer. When it has been found on all lanes (lanes_ready signal), the data starts to be read from the buffer. This ensures that all lanes are aligned at the output of the buffer. The buffer can also be used to separate clock domains, using a dual clock FIFO.
At the output of the buffer, after synchronization, all lanes are aligned.

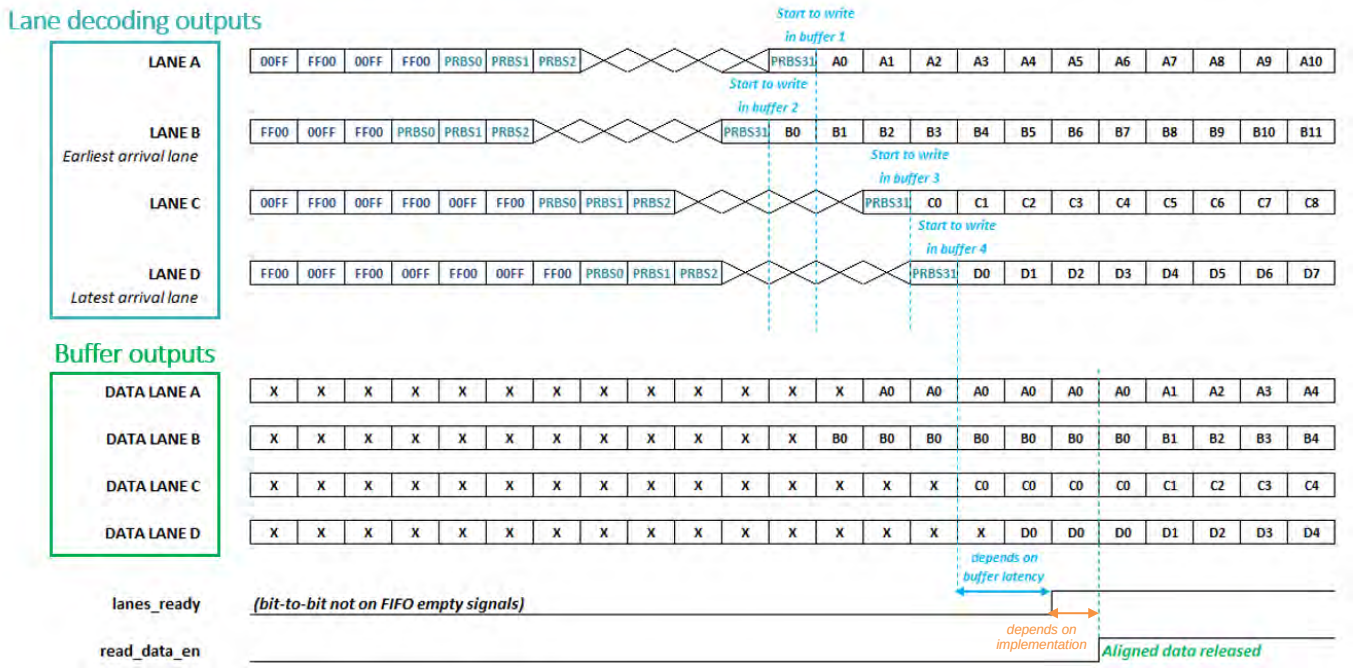


Figure 39: Multi-lanes synchronization time chart ; using FIFO as output buffer

9.2.2 Deterministic latency

ESIstream ensures a deterministic latency using synchronization signal (SYNC) which triggers a counter thereby defining a deterministic time base. When the counter reaches its end value then data are released at buffer output.

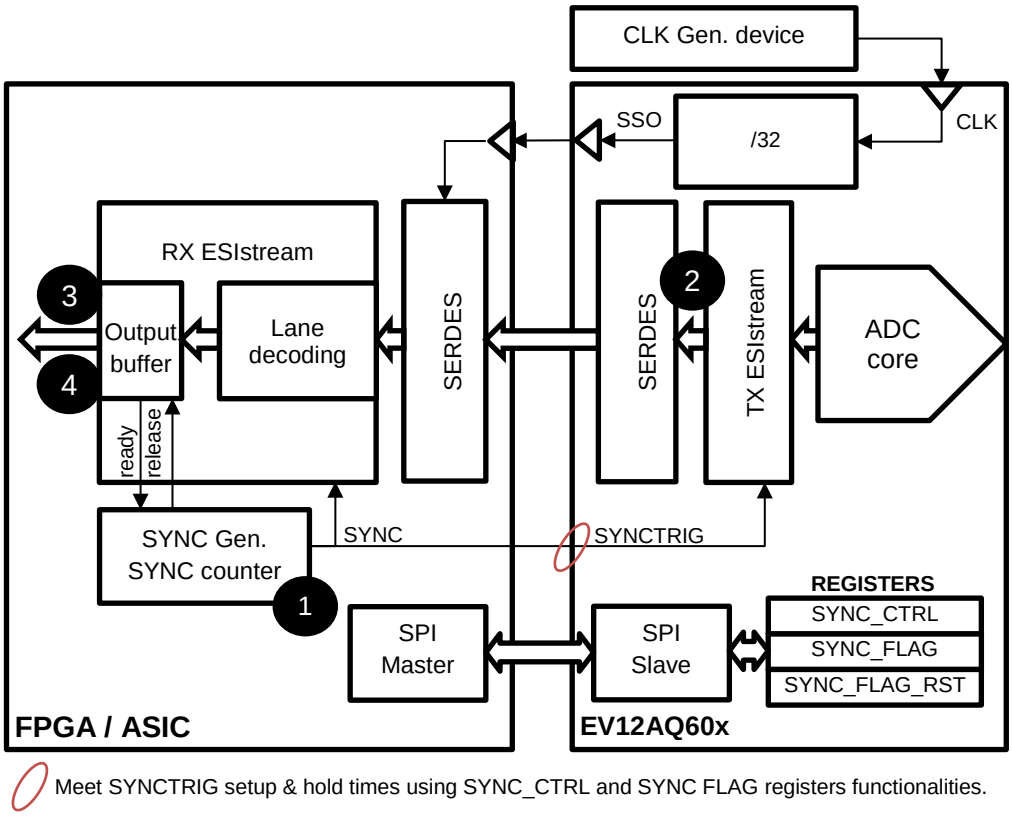


Figure 40: Deterministic latency architecture ; using SSO

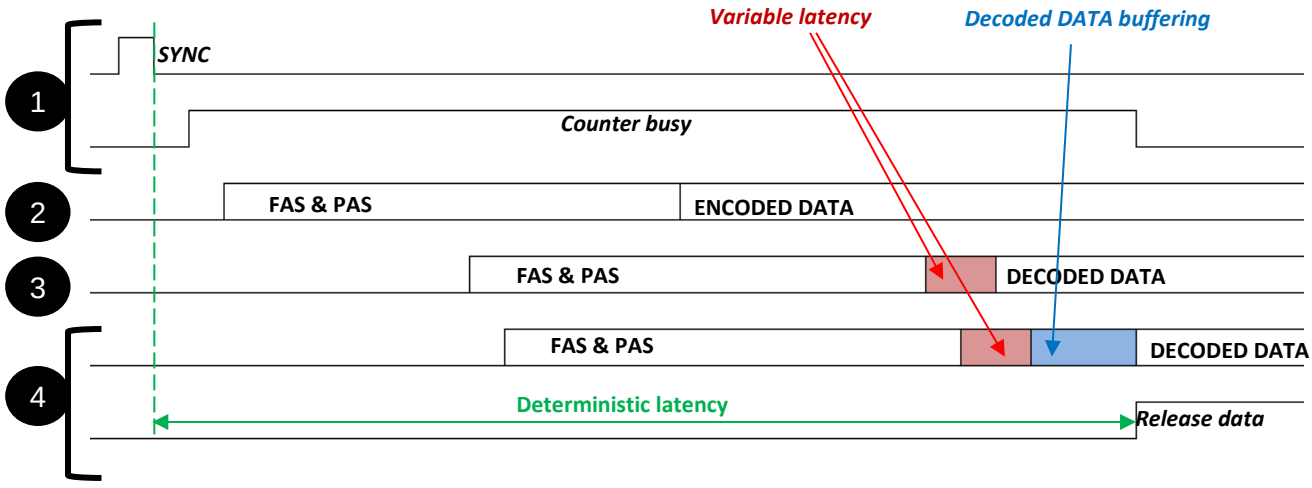


Figure 41: Deterministic latency time chart

- 1 - The transmitter sends a synchronization (SYNC) pulse to initiate lanes synchronization. On the receiver side, the SYNC pulse starts the deterministic counter and initializes the RX ESIstream module waiting for the ESIstream synchronization sequence (Frame Alignment Sequence, FAS, & PRBS Alignment Sequence, PAS).

- 2 - Receiving the SYNC pulse, the transmitter sends the ESIstream synchronization sequence on each lane then it sends encoded data.

- 3 - The receiver aligns the ESIstream frames on the COMMA (0xFF0000FF or 0x00FFFF00), initializes its PRBS to descramble received data and so decodes data. A FIFO buffer (Output buffer module) allows to deskew all lanes between them releasing decoded data when each lane FIFO contains at least one decoded data. At this point all lanes are aligned (or synchronized) but a variable latency can be introduced by the design (using fifo or elastic buffer to transfer data between two clock domains) or by Process, Voltage, Temperature effects (PVT).

- 4 - Data buffering coupled with a deterministic release data event allows to compensate variable latency. The deterministic release data event is the moment when the deterministic counter reaches its end value. The end value of the counter is determined after a training sequence. In training mode, the counter can be configured through registers accesses to save its current value when all lane FIFOs contain at least one decoded data (after a SYNC pulse sent by transmitter). User can access to this value through accessing to registers. Then, user can increment this value to compensate the maximum variable latency on the link. The increment value should be characterized. The end of counter value so found can be load into FPGA register and the deterministic counter can be configured in normal mode.

Deterministic latency requirements:

- Meet setup and hold times on SYNCTRIG inputs using SYNC_CTRL and SYNC_FLAG registers functionalities.

- Transceiver reference, frame clock, converter master clock (CLK for EV12AQ60x) and generally all clocks involved in data serialization must be synchronous.

- Use the SYNC counter end value as a deterministic reference trigger to release data from output buffers. The SYNC counter module clock should be deterministic and synchronous with the converter master clock (CLK for EV12AQ60x). The SYNC counter module clock frequency must be used by the output buffer read port to output data, must be equal to the RX ESIstream frame clock frequency and must be used to generate the SYNC pulse.

9.2.3 Multi-devices synchronization

ESIstream protocol combined with SYNC signals capabilities allows simplifying the synchronization across a multi-channel system.
Different multi-devices synchronization architecture (S/W and H/W) are possible (see Figure 42, Figure 43, Figure 44).
For more information on SYNC chaining feature, refer to technical note: SYNCHRONIZATION CHAINING, Simplifying Multi-channel Synchronization in Gigahertz Data Converters.
The SYNC chaining feature helps to reduce complexity in challenging high performance multichannel sampling systems as phased array systems employing digital beam-forming techniques and MIMO equipment.

Although SYNC chaining greatly simplifies design of a synchronized multi-devices system, it is still possible to use a SYNC point-to-point architecture.

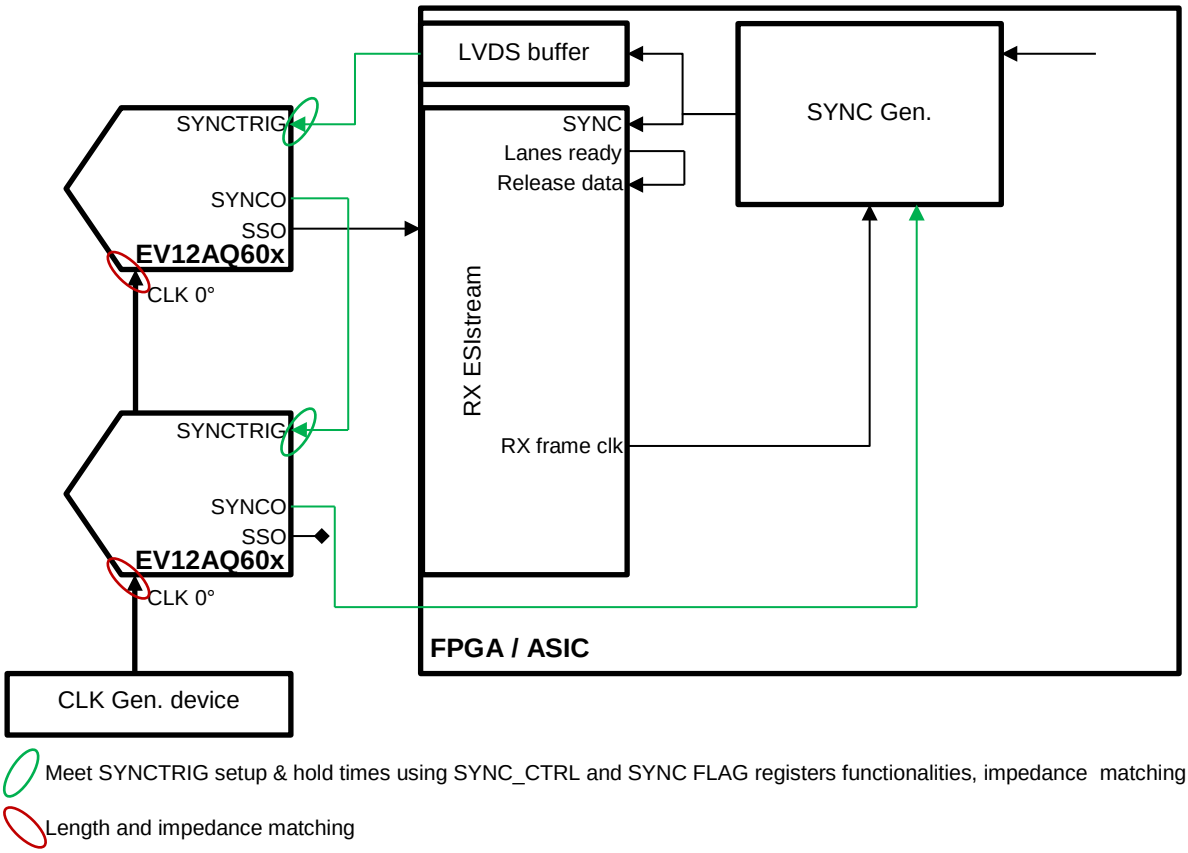


Figure 42: Multi-devices synchronization ; using sync chaining

Without need of deterministic latency in a system, SYNC counter can be removed and data can be released from output buffers directly when all buffers contain at least one valid data or when all lanes are synchronized.

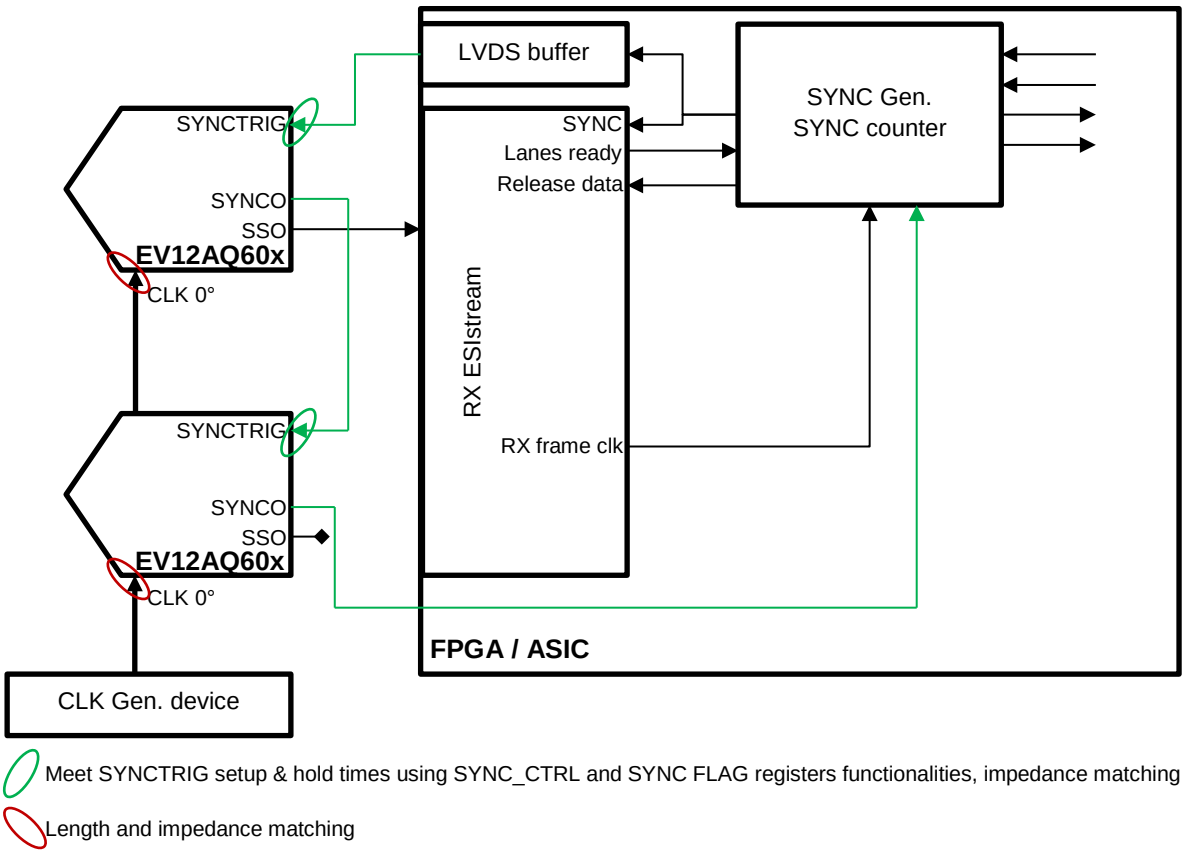


Figure 43: Multi-devices synchronization deterministic system ; using sync chaining

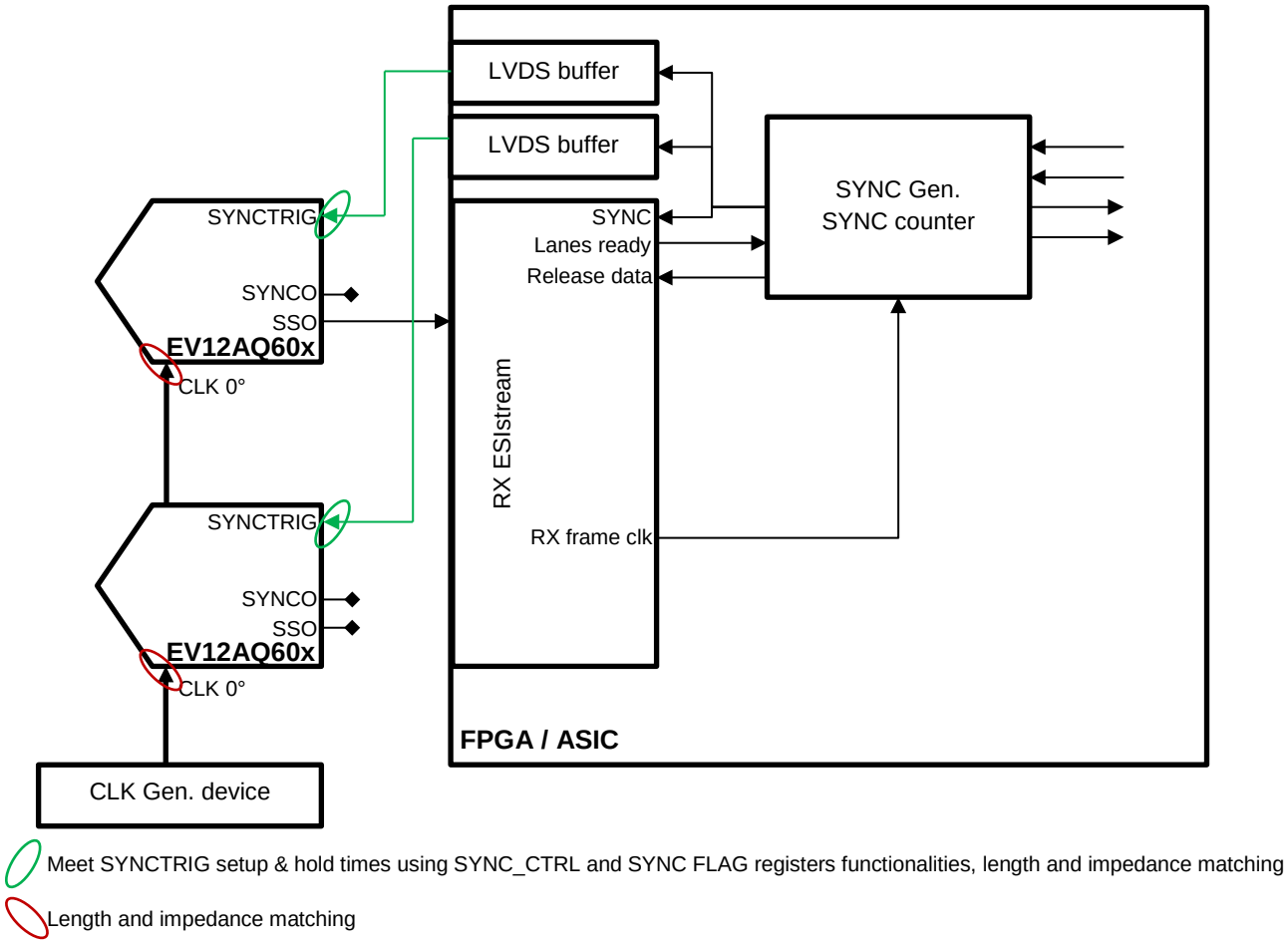


Figure 44: Multi-devices synchronization deterministic system ; using sync point-to-point

9.3 Interleaving performance improvement

To reduce interleaving spurs level, gain, phase and offset mismatch between ADC cores must be corrected. There are 3 possibilities.

9.3.1 Using factory calibration sets

4 factory calibration sets are available in OTP memory cells (2 for AQ605). They are optimized for IN0 and following conditions:

Table 51. Calibration sets description for AQ600

Calibration sets	Region of interest	Calibration frequency	Calibration temperature (Td)
CalSet0	800 MHz to 6GHz	2230 MHz	60 °C
CalSet1	800 MHz to 6GHz	2230 MHz	100 °C
CalSet2	DC to 800 MHz	100 MHz	60 °C
CalSet3	DC to 800 MHz	100 MHz	100 °C

Table 52. Calibration sets description for AQ605

Calibration sets	Region of interest	Calibration frequency	Calibration temperature (Td)
CalSet0	800 MHz to 6GHz	2230 MHz	55 °C

CalSet2	DC to 800 MHz	100 MHz	55 °C

It is also possible to use factory calibration sets with other calibration frequencies. In case of interest, contact GRE-HOTLINE-BDC@TELEDYNE.COM.

To select one calibration set, following sequence must be applied:
Step #1: Load all OTPs values in SPI registers: Write in OTP_LOADING register (Table 42). This is already done with the start-up procedure (see §6).
Step #2: Select the desired calibration set: Use CAL_SET_SEL register (Table 28)

Table 53. CalSetx (x=0, 1, 2, 3) registers mapping (see Table 25, Table 26, Table 27)

Calibration sets	Core A	Core B	Core C	Core D
CalSet0	A_SET0_OFFSET_CAL A_SET0_GAIN_CAL A_SET0_PHASE_CAL	B_SET0_OFFSET_CAL B_SET0_GAIN_CAL B_SET0_PHASE_CAL	C_SET0_OFFSET_CAL C_SET0_GAIN_CAL C_SET0_PHASE_CAL	D_SET0_OFFSET_CAL D_SET0_GAIN_CAL D_SET0_PHASE_CAL
CalSet1 (1)	A_SET1_OFFSET_CAL A_SET1_GAIN_CAL A_SET1_PHASE_CAL	B_SET1_OFFSET_CAL B_SET1_GAIN_CAL B_SET1_PHASE_CAL	C_SET1_OFFSET_CAL C_SET1_GAIN_CAL C_SET1_PHASE_CAL	D_SET1_OFFSET_CAL D_SET1_GAIN_CAL D_SET1_PHASE_CAL
CalSet2	A_SET2_OFFSET_CAL A_SET2_GAIN_CAL A_SET2_PHASE_CAL	B_SET2_OFFSET_CAL B_SET2_GAIN_CAL B_SET2_PHASE_CAL	C_SET2_OFFSET_CAL C_SET2_GAIN_CAL C_SET2_PHASE_CAL	D_SET2_OFFSET_CAL D_SET2_GAIN_CAL D_SET2_PHASE_CAL
CalSet3 (1)	A_SET3_OFFSET_CAL A_SET3_GAIN_CAL A_SET3_PHASE_CAL	B_SET3_OFFSET_CAL B_SET3_GAIN_CAL B_SET3_PHASE_CAL	C_SET3_OFFSET_CAL C_SET3_GAIN_CAL C_SET3_PHASE_CAL	D_SET3_OFFSET_CAL D_SET3_GAIN_CAL D_SET3_PHASE_CAL

Notes:
1. Not available for AQ605

9.3.2 Using interpolation with temperature

This feature is available for AQ600 only.

To further enhance performance and compensate the roll-off effect with temperature, the user can interpolate the GAIN, PHASE and OFFSET registers according to the 2 temperature given calibration sets (CalSet0/CalSet1 or CalSet2/CalSet3). A simple linear interpolation will lead to new register values that will improve performance.
The following equation applies:

$$Reg\ value(T) = \frac{Reg\ value(100\,°C) - Reg\ value(60\,°C)}{100\,°C - 60\,°C} \times T + Reg\ value\ (60\,°C) - \frac{Reg\ value(100\,°C) - Reg\ value(60\,°C)}{100\,°C - 60\,°C} \times 60\,°C$$

The original register values (@60 °C and @100 °C respectively) are to be read in the appropriate SPI register (see Table 53). Once the derived register value is found, the user shall write it (through SPI) in place of the previous calibration set used.

Example: the user is working at 3GHz with CalSet1 (Fcal=2230 MHz, Tcal=100 °C) loaded into SPI, the current device temperature drops to 40°C and the system can adjust the registers to match this new temperature.

Table 54. Example of Interleaving registers interpolation

Register type	ADC Core	Value @60 °C	Value @100 °C	Interpolated value @40 °C	Target address (SPI)
GAIN	A	76D	774	76A	0x0125
	B	714	719	712	0x0325
	C	88B	886	88E	0x0525
	D	8E3	8DE	8E6	0x0725
PHASE	A	0E5	0F3	DE	0x0126
	B	12D	125	131	0x0326

	C	0DE	0E3	DC	0x0526
	D	0E4	0ED	E0	0x0726
OFFSET	A	0DE	0E3	DC	0x0127
	B	124	121	126	0x0327
	C	120	11B	123	0x0527
	D	125	11E	129	0x0727

See §10.10 for dynamic performance versus temperature.

9.3.3 Using user defined calibration

Based on specific conditions of use, it is also possible to define phase, gain and offset values (see Table 25, Table 26 and Table 27) using the methodology described in §9.3.3.1 and §9.3.3.2.

9.3.3.1 Offset interleaving calibration

To set offset, DC value should be extracted with high precision to quantify offset unbalance between cores. Offset adjust 9-bit DAC should be set at the right value to decrease DC offset mismatch.

Protocol:

- Use single core output data with or without input signal
- Calculate output data average for each core DCcoreX (X= A, B, C, D)
- Apply DC correction equal to:

$$DC_{correction}X = \frac{DC_{core}X - DC_{ref}}{DAC\_LSB_{DCcorex}}$$

With:

- $\boldsymbol{DC_{correction}X}$ = DAC code to compensate corex DC offset (X = A, B, C, D)
- $\boldsymbol{DC_{core}X}$ = DC offset at coreX output (X = A, B, C, D)
- $\boldsymbol{DC_{ref}}$= reference value to align cores DC offset. It can be set to 2048 or to one core offset value
- $\boldsymbol{DAC\_LSB_{DCcorex}}$= core X DC offset DAC calibration LSB (X = A, B, C, D)

CoreX DC offset DAC calibration LSB is determined by measuring corex DC offset at maximum and minimum correction.

$$LSB_{DCcorex} = \frac{DC_{core}X@maxcode - DC_{core}X@mincode}{maxcode - mincode - 1}$$

With:

- $\boldsymbol{DC_{core}X@maxcode}$ = core X DC offset at maximum DC offset correction code
- $\boldsymbol{DC_{core}X@mincode}$ = core X DC offset at minimum DC offset correction code
- $\boldsymbol{maxcode = 511}$
- $\boldsymbol{mincode = 0}$

9.3.3.2 Gain and phase interleaving calibration

By using FFT on each core output, gain and phase of each core can be estimated at input frequency Fin of interest. Correction is calculated as follow:

$$Gain_{correction}X = \frac{Gain_X - Gain_{ref}}{LSB_{Gain\ X}}$$

$$Phase_{correction}X = \frac{Phase_X - Phase_{ref}}{LSB_{Phase\ X} * (360.F_{in})}$$

With:

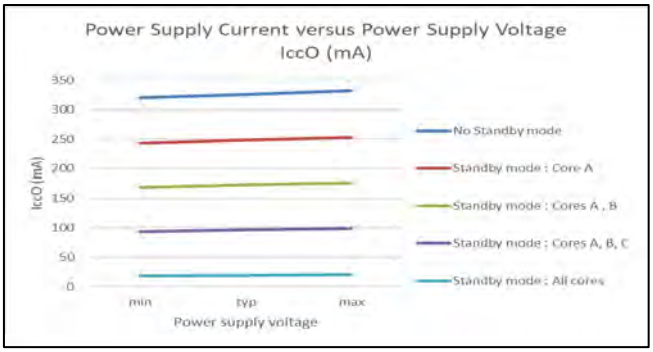
$Core\ X$	: core to be calibrated (X = A, B, C, D)
$Gain_X$	: corex gain in dB
$Gain_{ref}$	: core gain reference in dB
$Phase_X$	: corex phase in degree
$Phase_{ref}$	: core phase reference in degree
F_{in}	: frequency of interest

Gain and phase measurement accuracy should be negligible regarding ADC LSB.

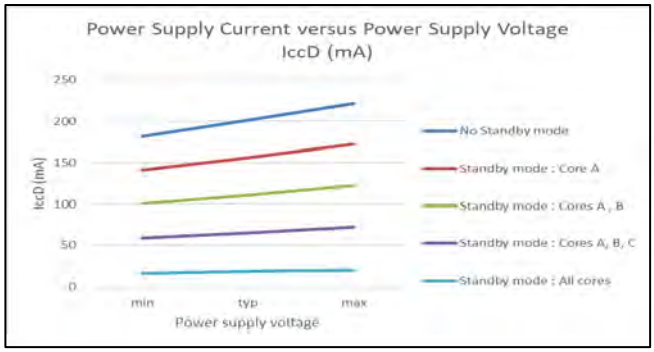
10 CHARACTERIZATION RESULTS

10.1 Power consumption

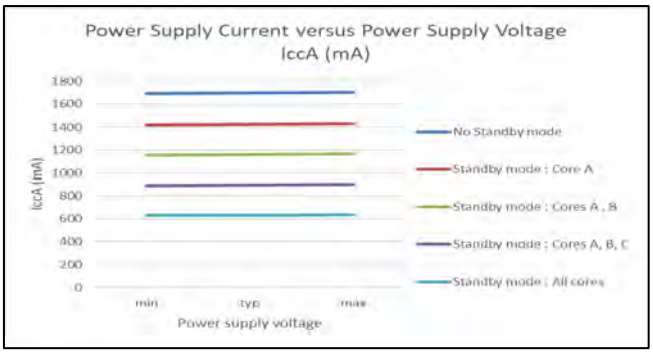
10.1.1 Versus Power supply voltage



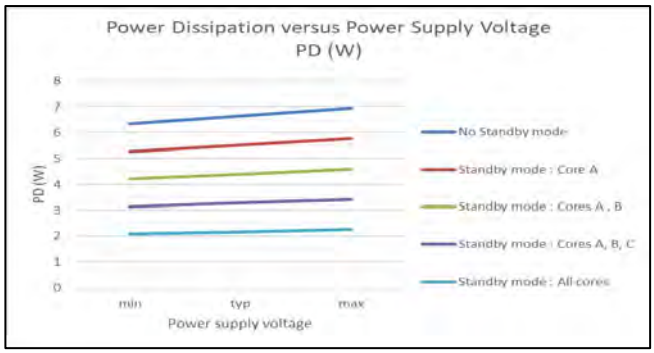
IccO (mA)



IccD (mA)



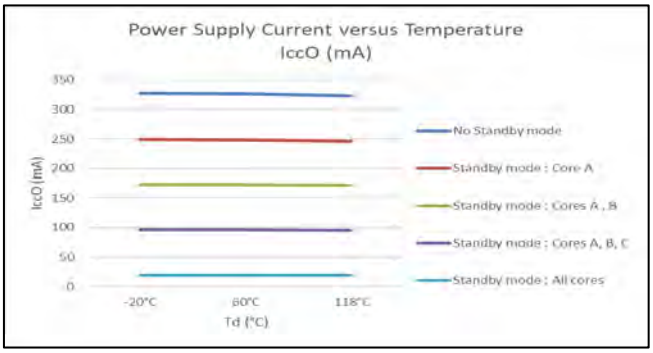
IccA (mA)



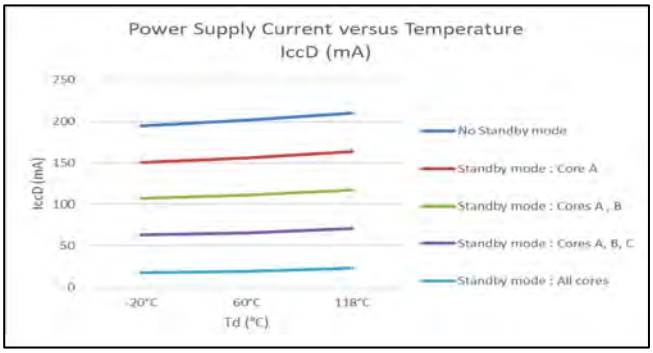
Power dissipation (W)

Figure 45: Current consumption and power dissipation versus supply voltage and standby mode

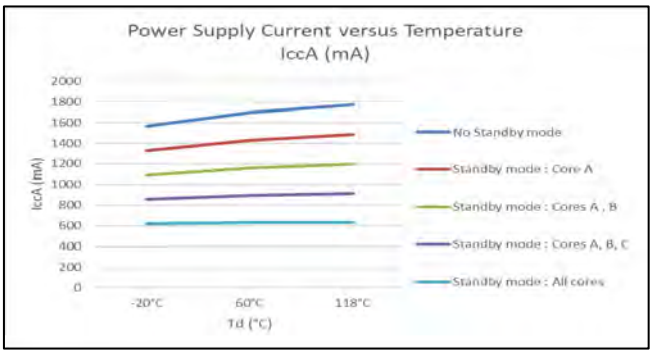
10.1.2 Versus Temperature



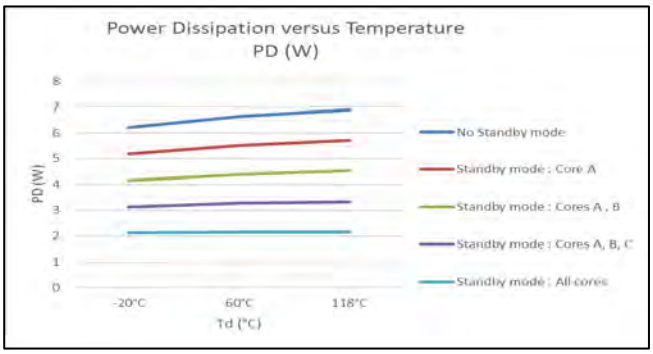
IccO (mA)



IccD (mA)



IccA (mA)



Power dissipation (W)

Figure 46: Current consumption and power dissipation versus temperature and standby mode

10.2 Analog Bandwidth and Band flatness

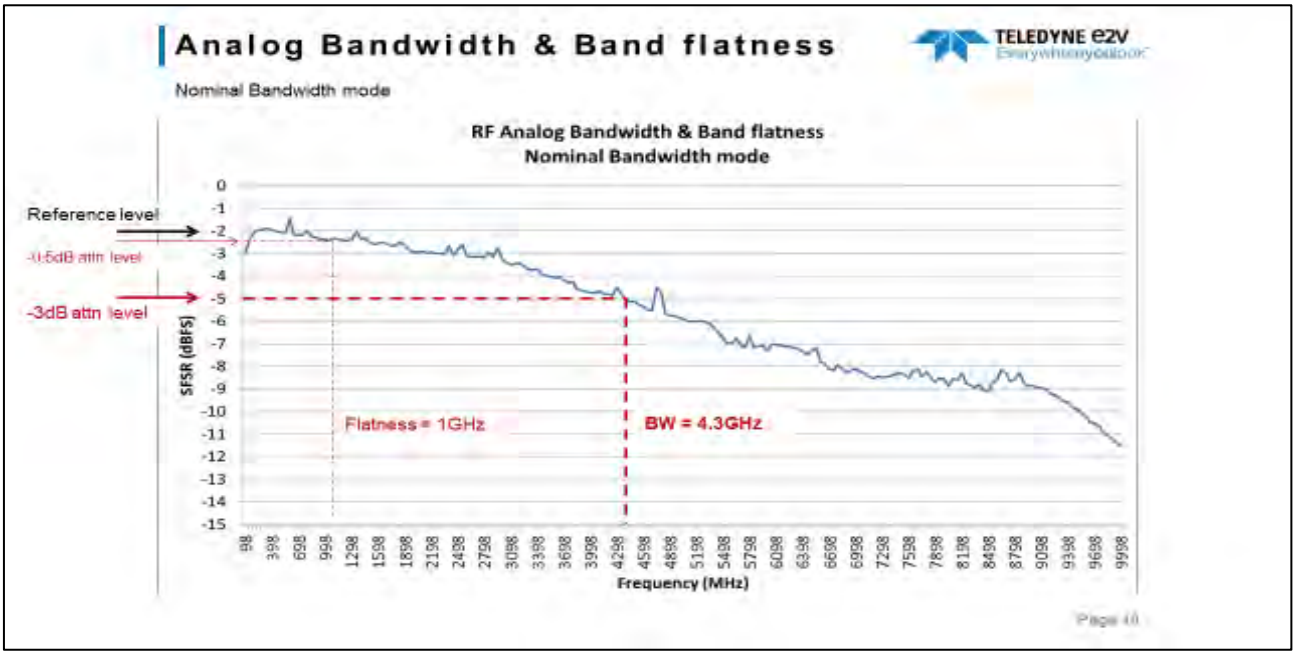


Figure 47: Nominal Bandwidth

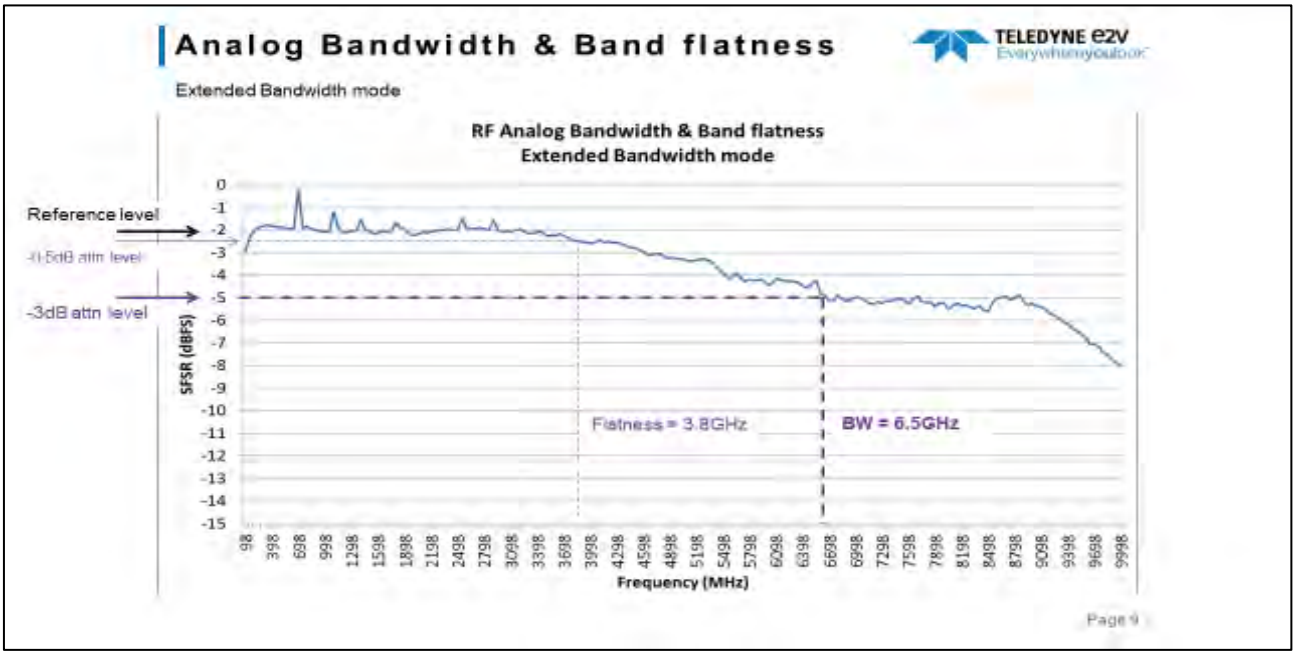


Figure 48: Extended Bandwidth

10.3 Cross-talk

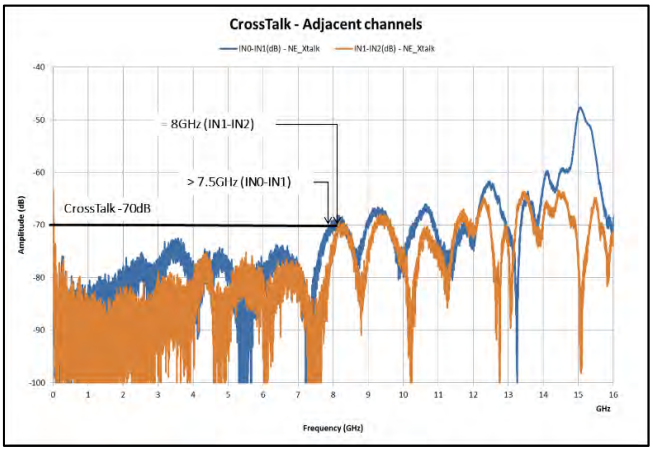


Figure 49: Cross-talk between analog input channels

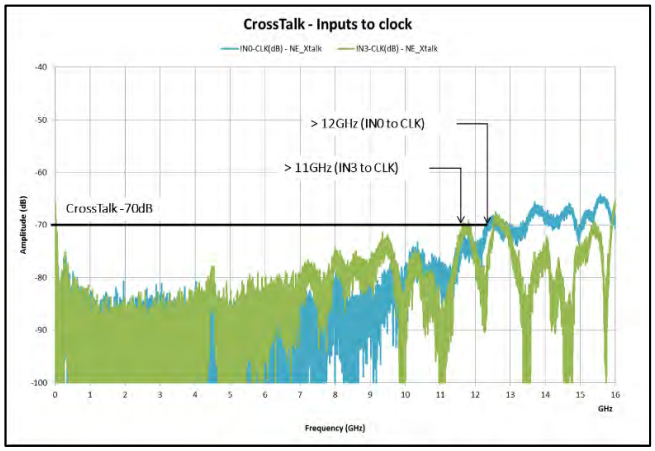


Figure 50: Cross-talk between analog inputs and clock

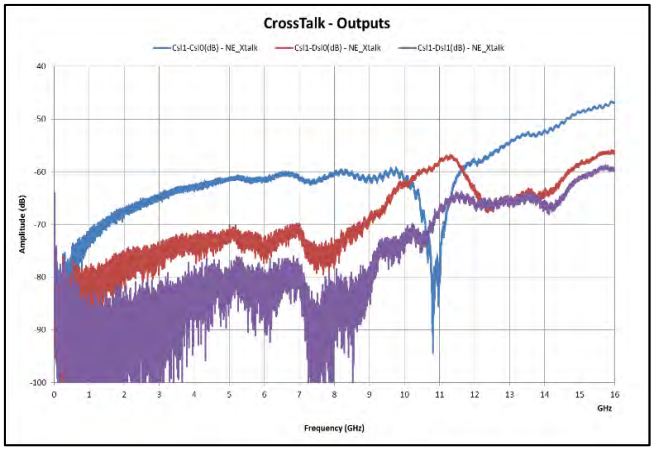


Figure 51: Cross-talk between serial outputs

10.4 VSWR

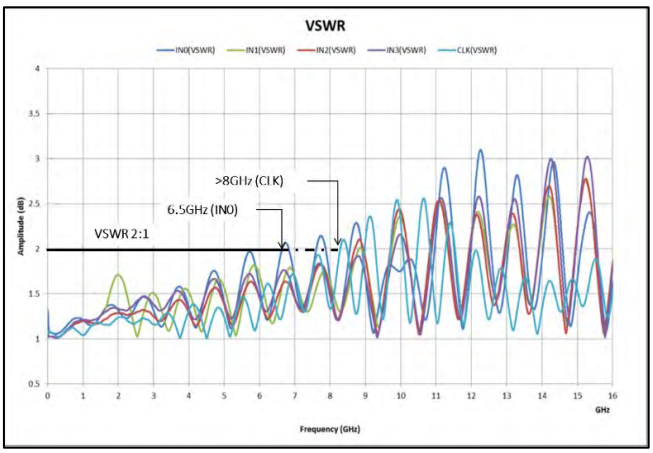


Figure 52: VSWR on analog inputs and clock

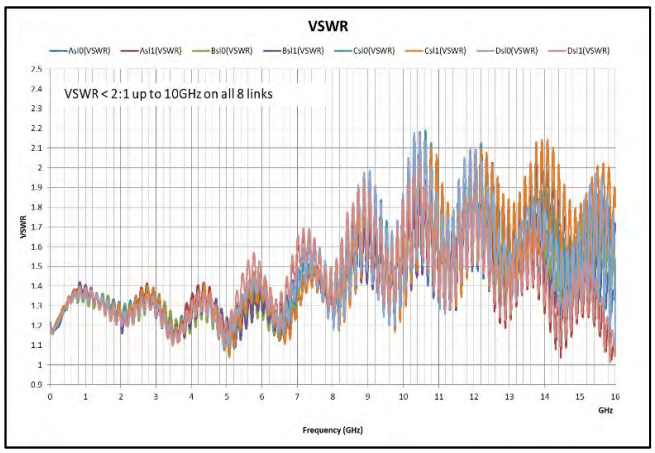


Figure 53: VSWR on serial output

10.5 INL

INL at Analog input frequency = 98 MHz – Pout = -1 dBFS

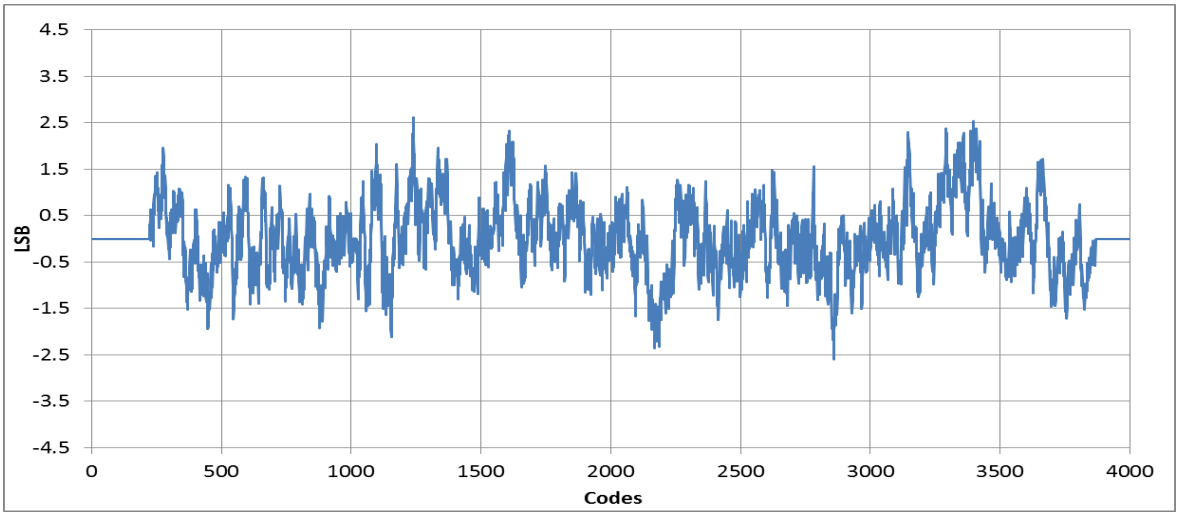


Figure 54: INL - 4-channel mode – 1.6 GSps

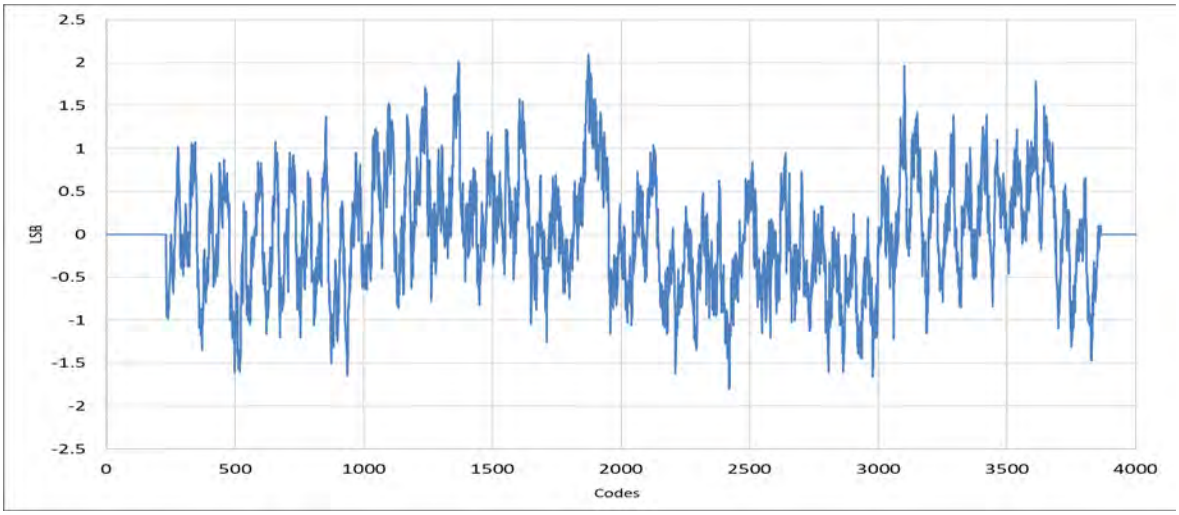


Figure 55: INL - 2-channel mode – 3.2 GSps

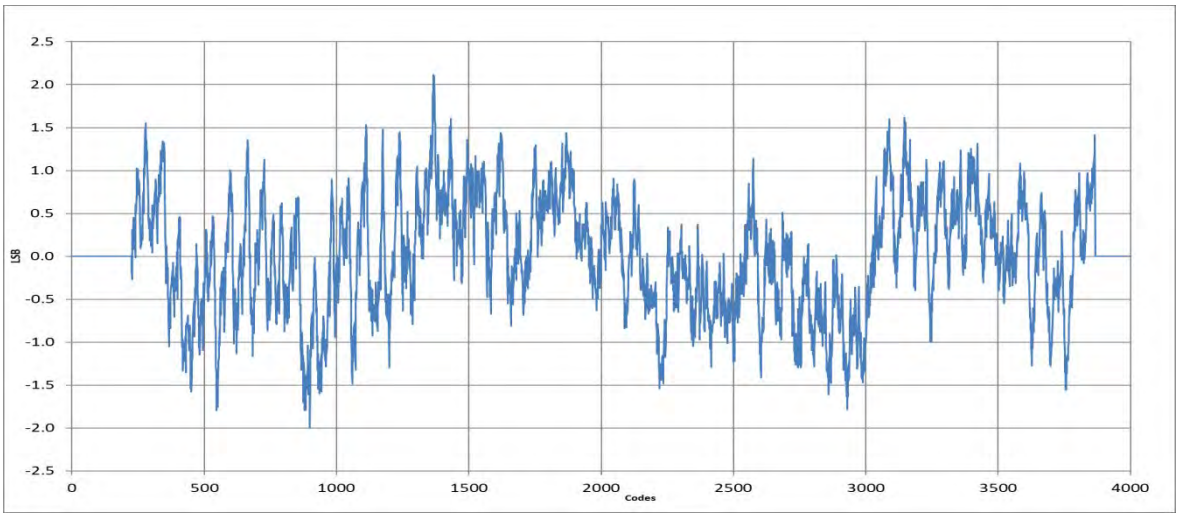


Figure 56: INL - 1-channel mode – 6.4 GSps

10.6 DNL

DNL at Analog input frequency 98MHz – Pout = -1 dBFS

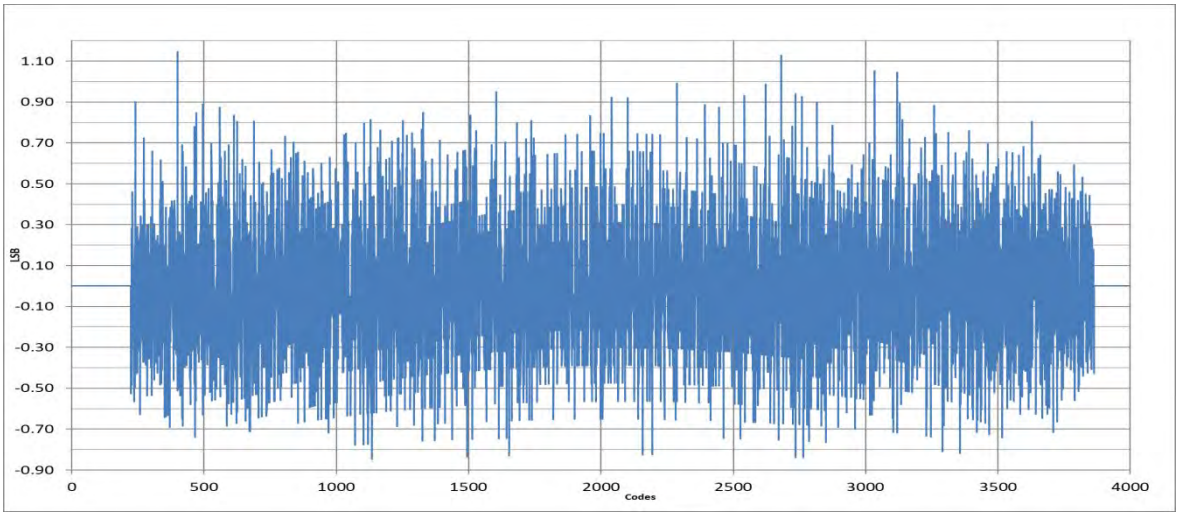


Figure 57: DNL - 4-channel mode – 1.6 GSps

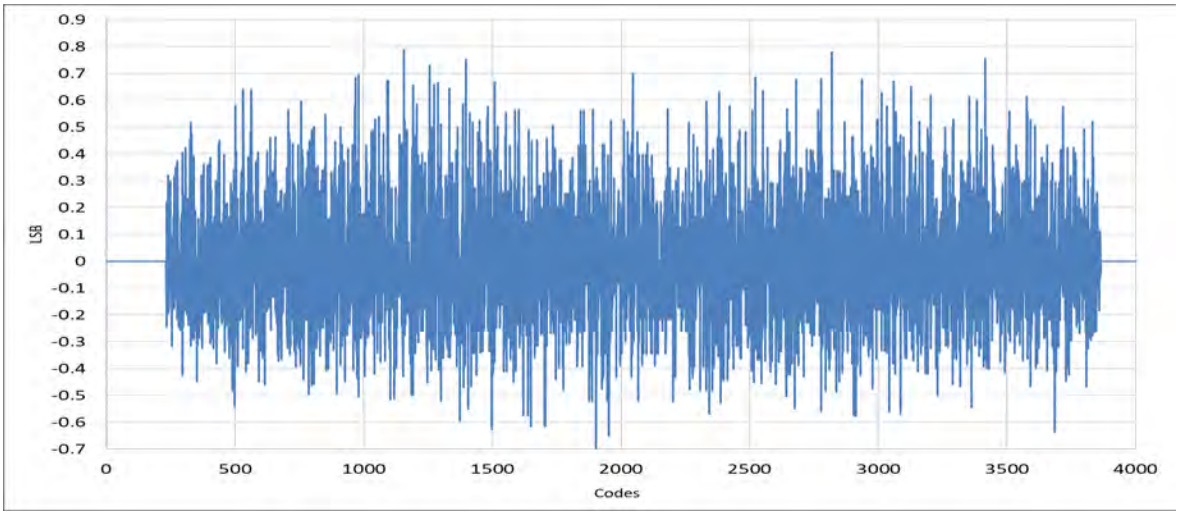


Figure 58: DNL - 2-channel mode – 3.2 GSps

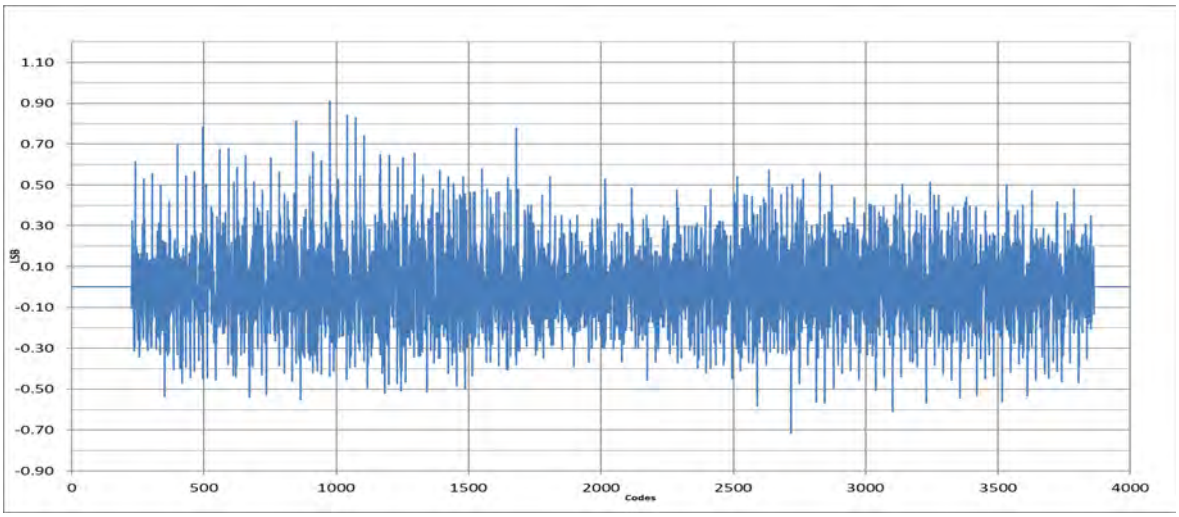
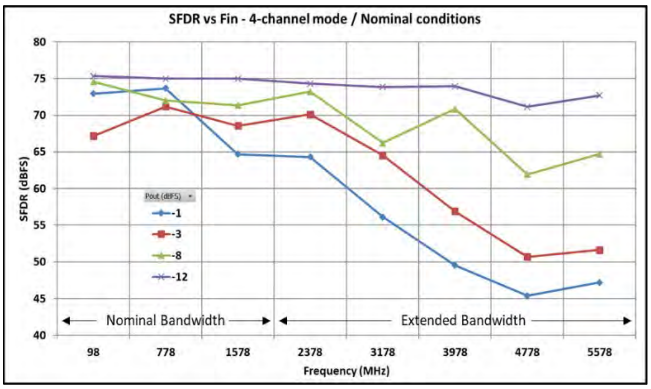


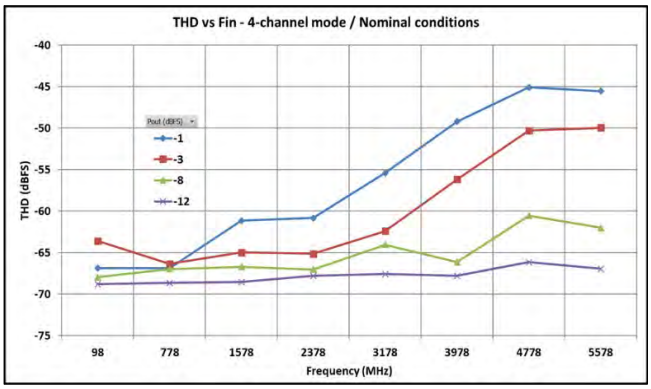
Figure 59: DNL - 1-channel mode – 6.4 GSps

10.7 Dynamic Performances versus Analog input frequencies

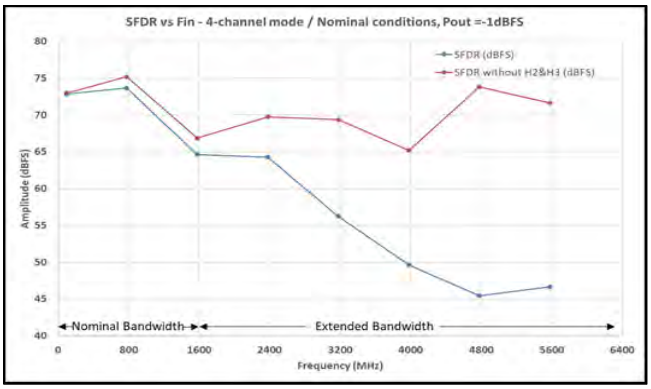
10.7.1 4-channel mode – 1.6 GSps



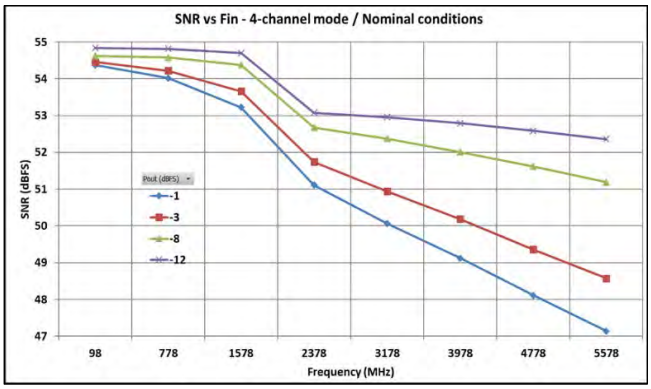
SFDR vs Fin



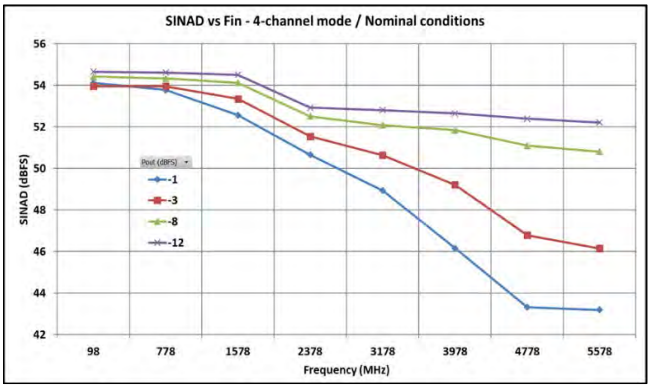
THD vs Fin



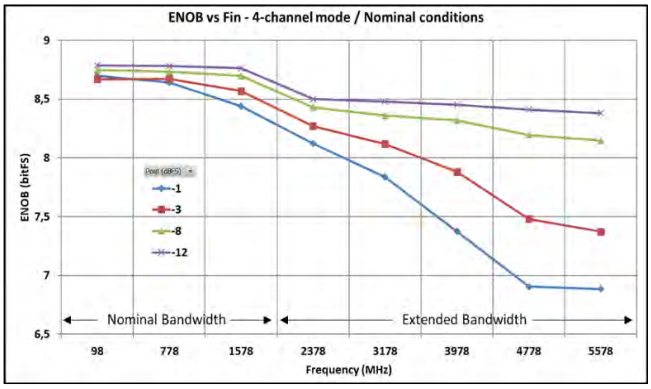
SFDR without H2/H3



SNR vs Fin



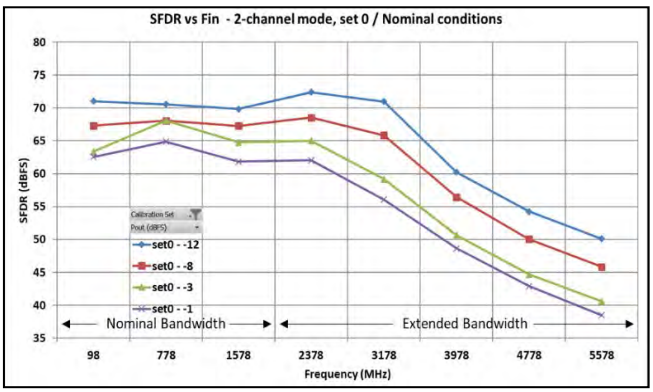
SINAD vs Fin



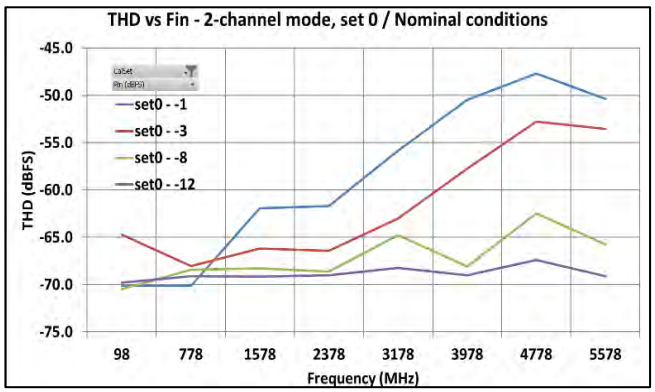
ENOB vs Fin

Figure 60: Performance vs Analog input frequencies - 4-channel mode – 1.6 GSps

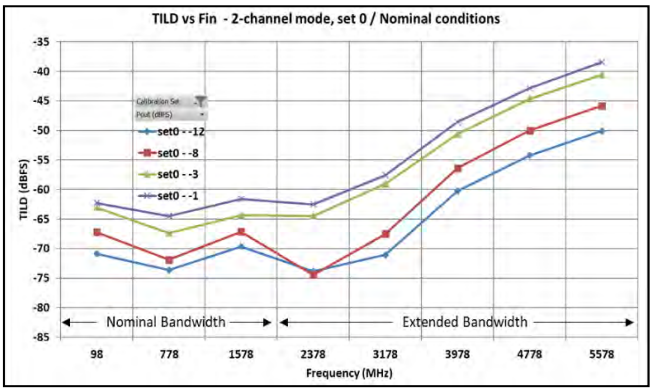
10.7.2 **2-channel mode– 3.2 GSps**



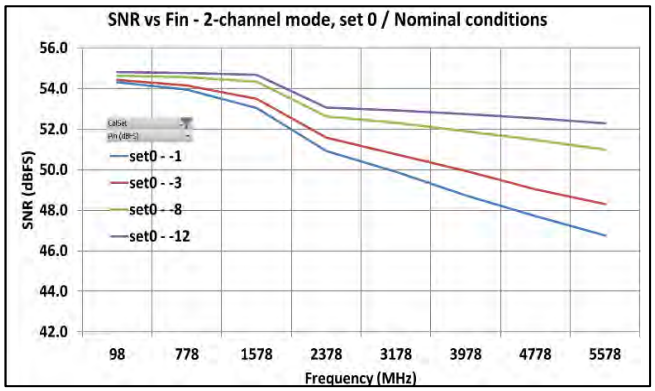
SFDR vs Fin



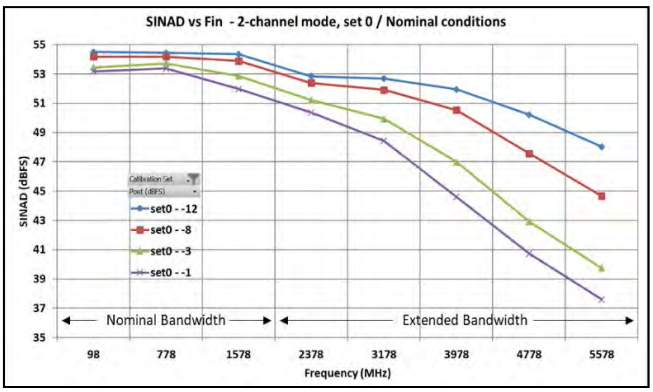
THD vs Fin



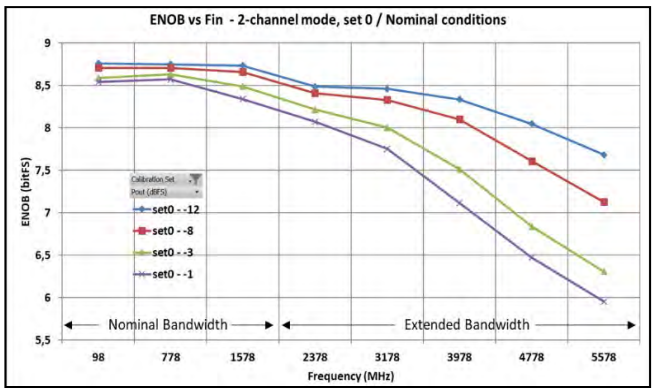
TILD vs Fin



SNR vs Fin

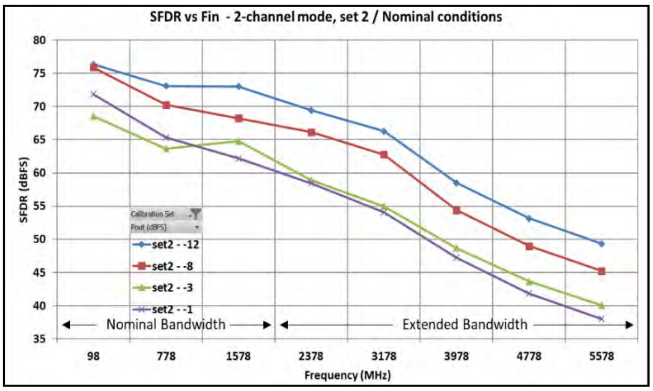


SINAD vs Fin

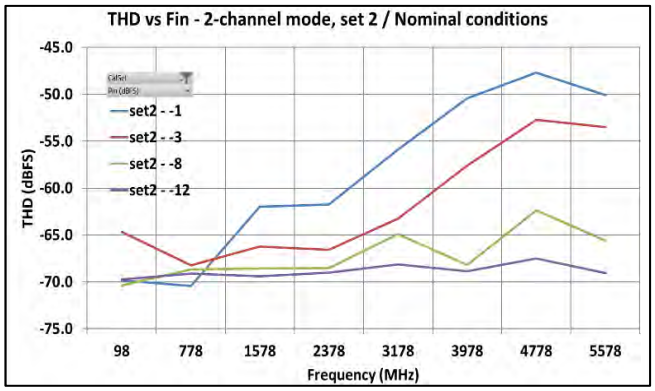


ENOB vs Fin

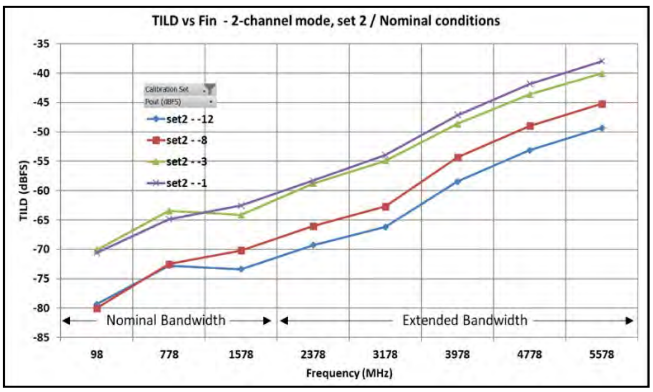
Figure 61: Performance vs Analog input frequencies - 2-channel mode – 3.2 GSps - Calibration set: CalSet0 -



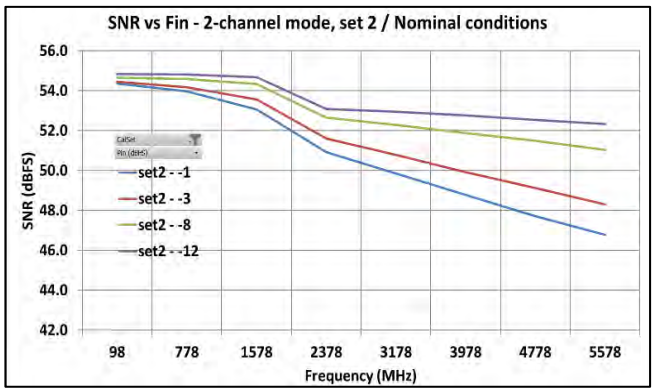
SFDR vs Fin



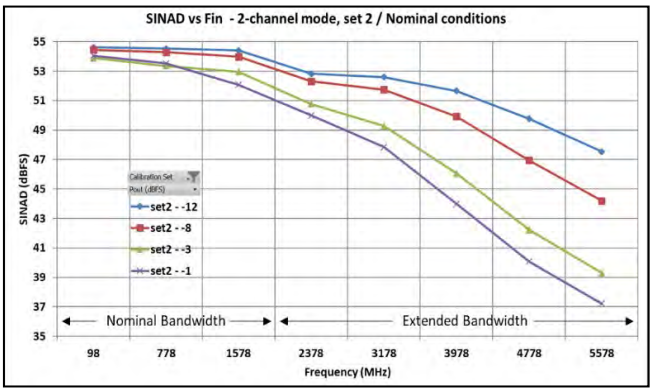
THD vs Fin



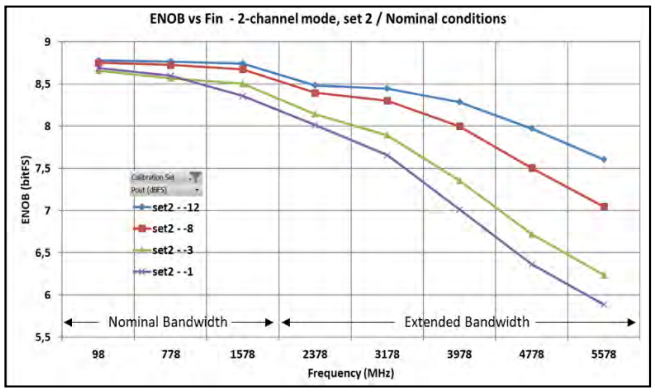
TILD vs Fin



SNR vs Fin



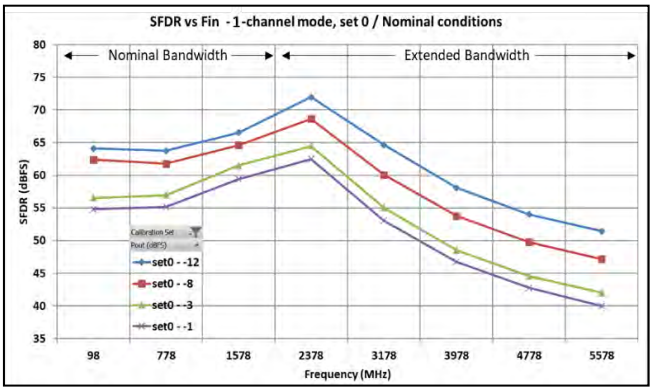
SINAD vs Fin



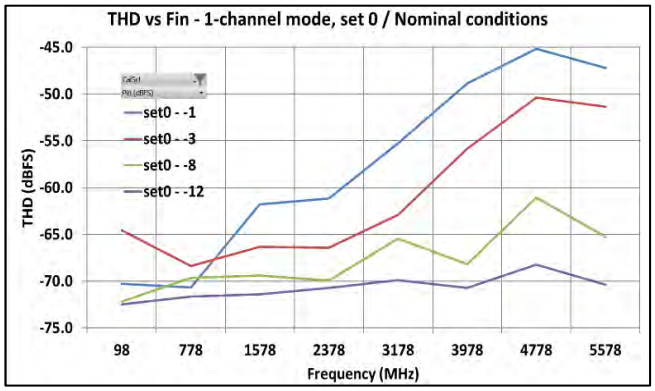
ENOB vs Fin

Figure 62: Performance vs Analog input frequencies - 2-channel mode – 3.2 GSps - Calibration set: CalSet2 -

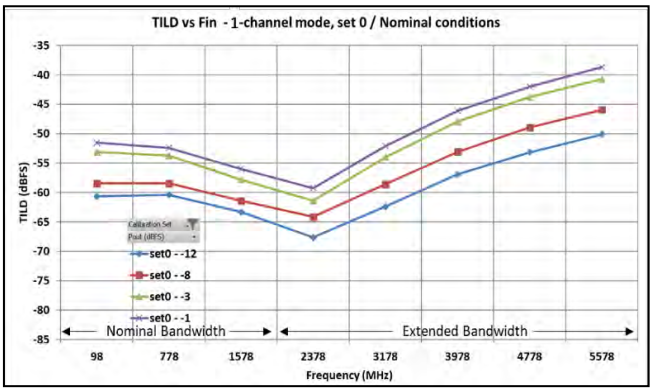
10.7.3 **1-channel mode– 6.4 GSps**



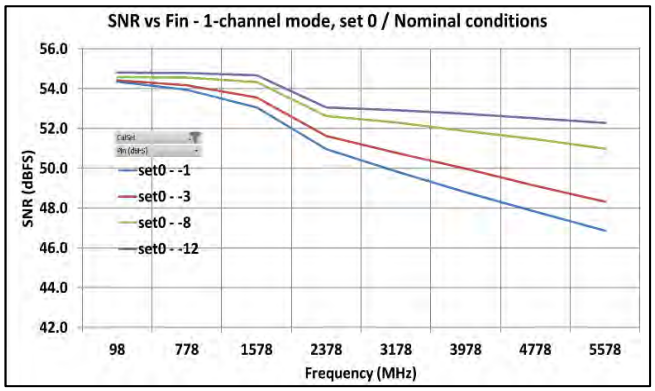
SFDR vs Fin



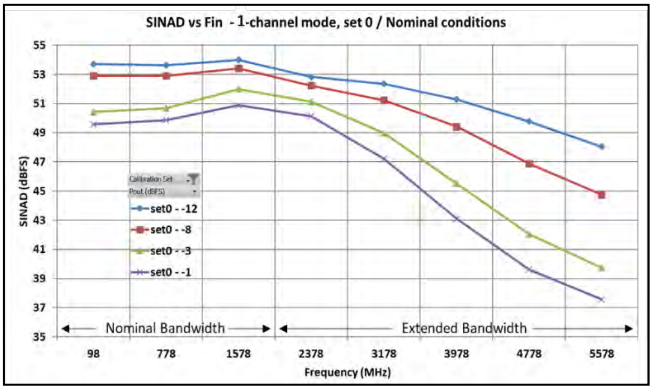
THD vs Fin



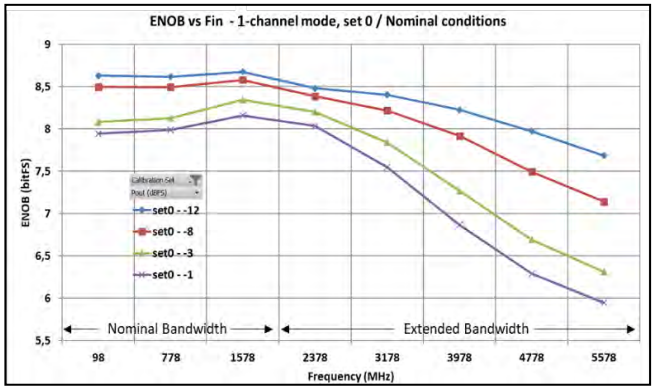
TILD vs Fin



SNR vs Fin

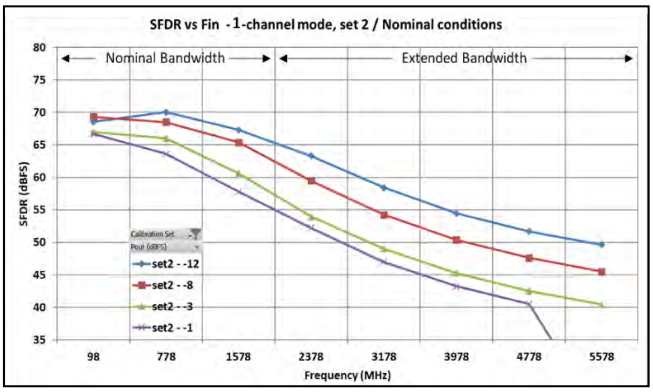


SINAD vs Fin

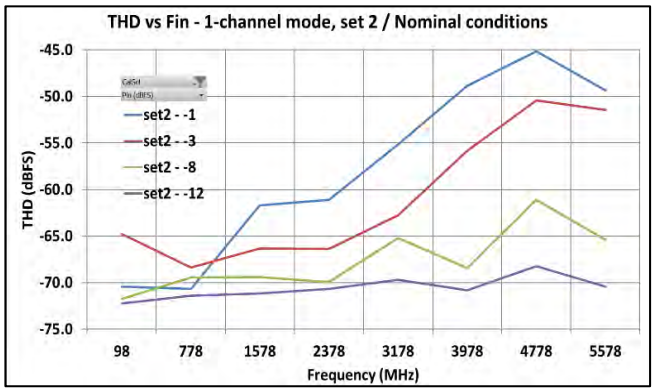


ENOB vs Fin

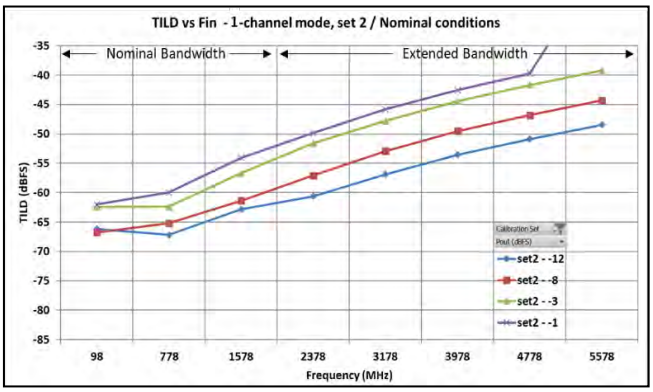
Figure 63: Performance vs Analog input frequencies - 1-channel mode – 6.4 GSps - Calibration set: CalSet0 -



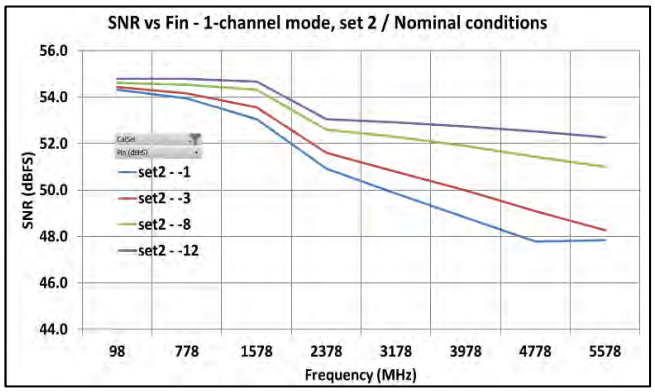
SFDR vs Fin



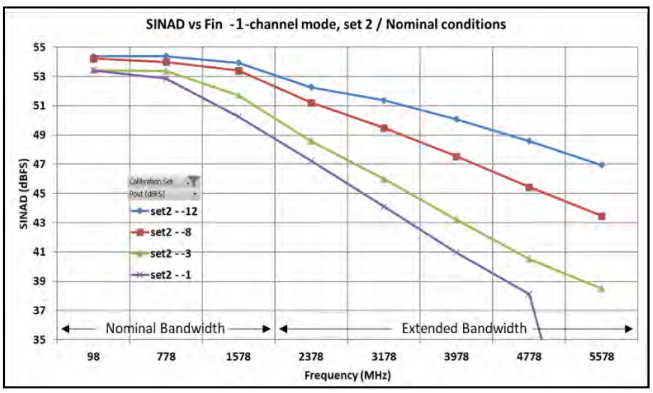
THD vs Fin



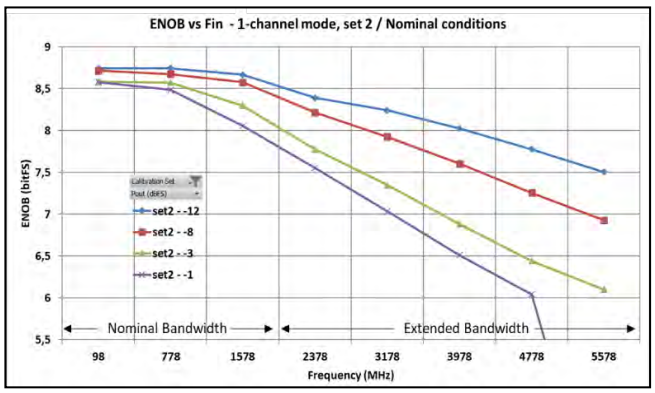
TILD vs Fin



SNR vs Fin



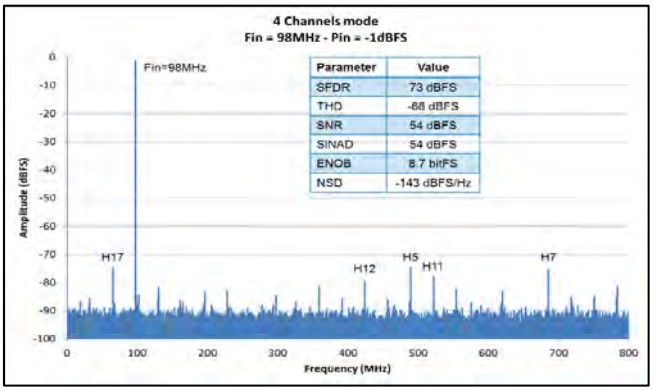
SINAD vs Fin



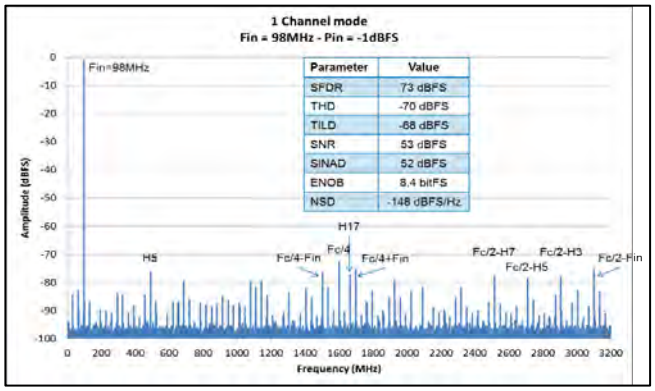
ENOB vs Fin

Figure 64: Performance vs Analog input frequencies - 1-channel mode – 6.4 GSps - Calibration set: CalSet2 -

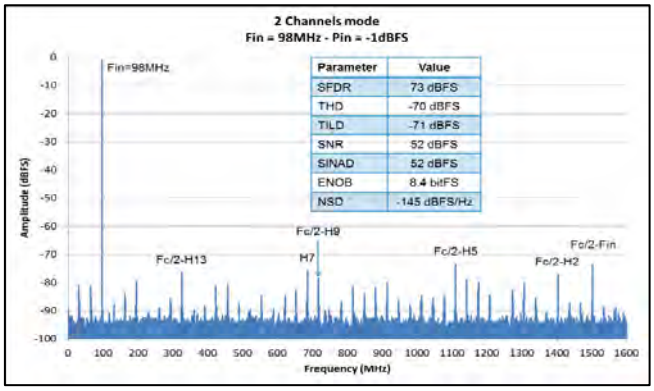
10.7.4 **Spectra**



4-channel mode – 1.6 GSps

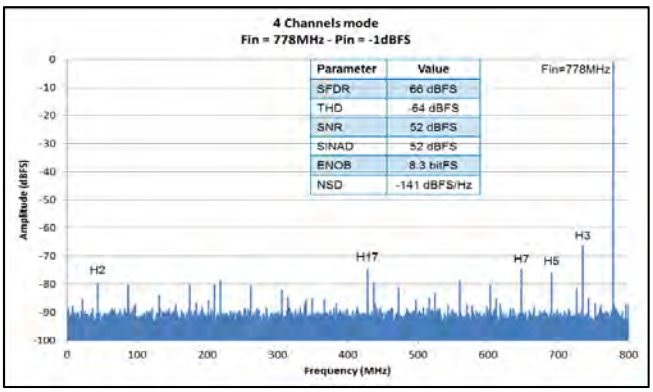


2-channel mode – 3.2 GSps

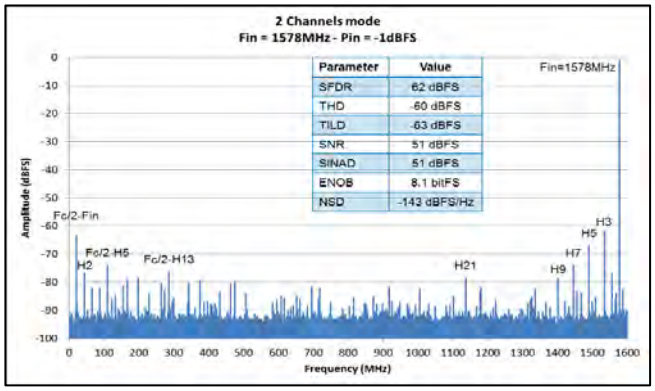


1-channel mode – 6.4 GSps

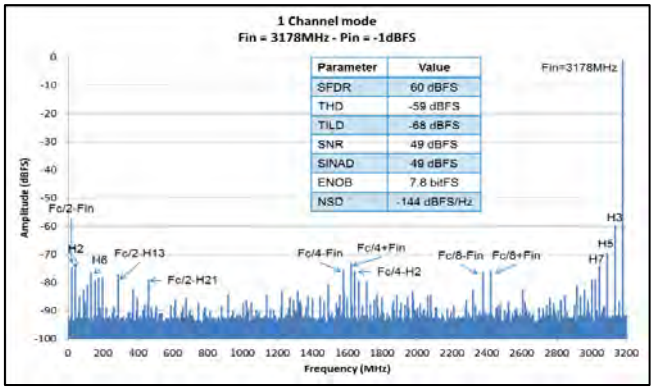
Figure 65: Spectra at Analog input frequency = 98 MHz, Pout = -1 dBFS



4-channel mode – 1.6 GSps – Fin = 778 MHz

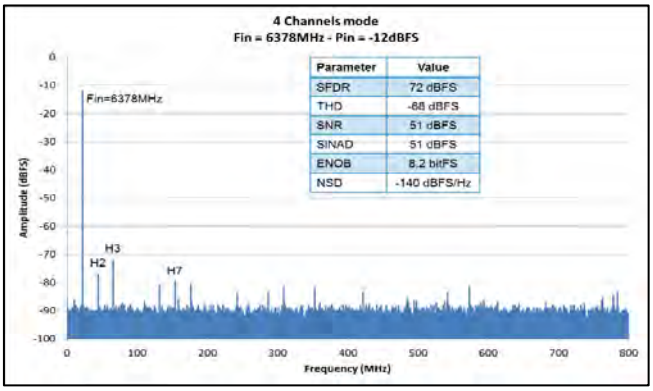


2-channel mode – 3.2 GSps – Fin = 1578 MHz

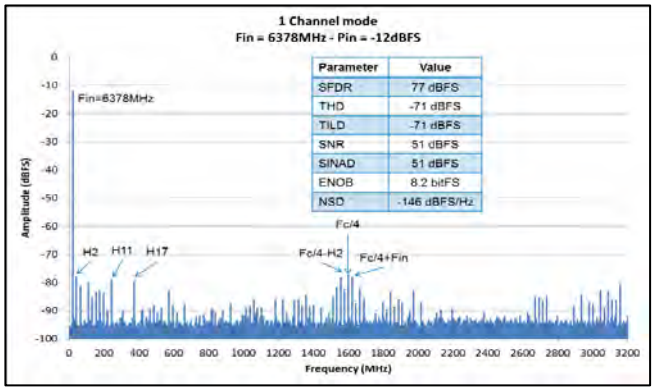


1-channel mode – 6.4 GSps – Fin = 3178 MHz

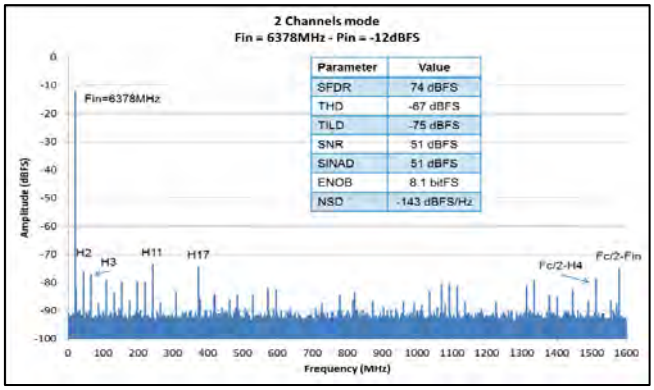
Figure 66: Spectra at Analog input frequency end of 1st Nyquist zone (mode dependent). Pout = -1 dBFS.



4-channel mode – 1.6 GSps – Fin folded from 8th Nyquist zone

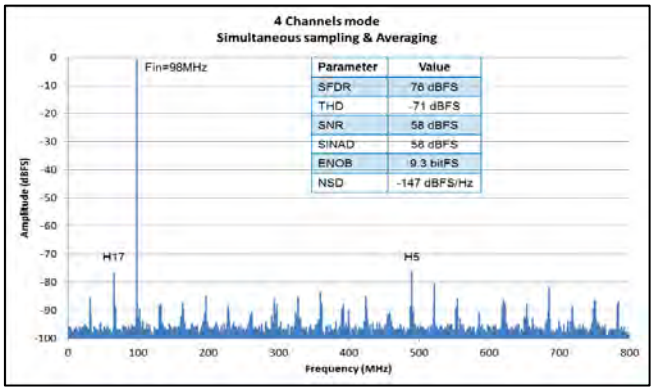


2-channel mode – 3.2 GSps – Fin folded from 4th Nyquist zone



1-channel mode – 6.4 GSps – Fin folded from 2nd Nyquist zone

Figure 67: Spectra at Analog input frequency = 6378 MHz. Pout = -12 dBFS

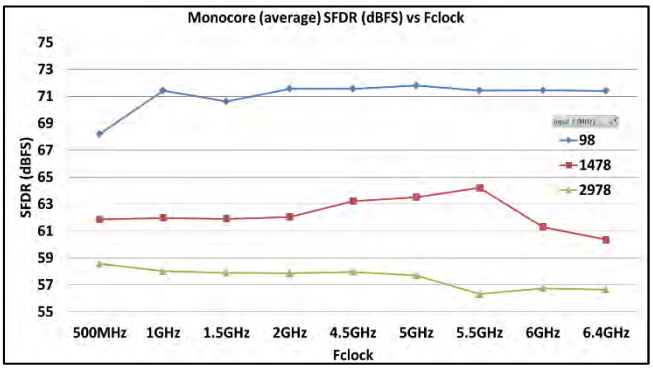


Simultaneous sampling and averaging – 1.6 GSps

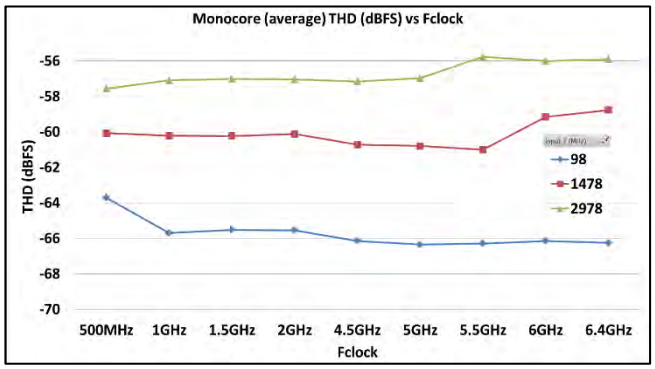
Figure 68: Spectra at Analog input frequency = 98 MHz, Pout = -1 dBFS. Simultaneous sampling and averaging (based on 4-channel mode)

10.8 Performance versus Clock Input Frequency

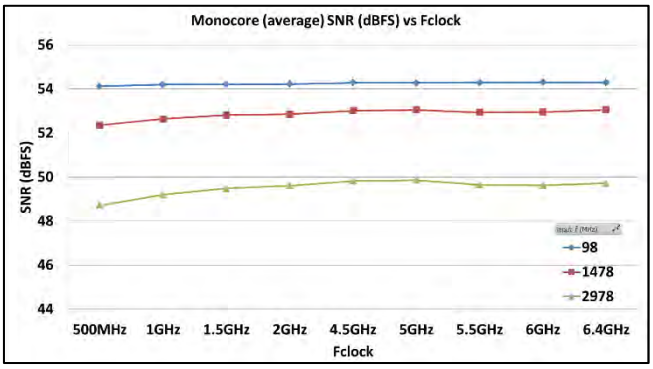
10.8.1 4-channel mode – 1.6 GSps



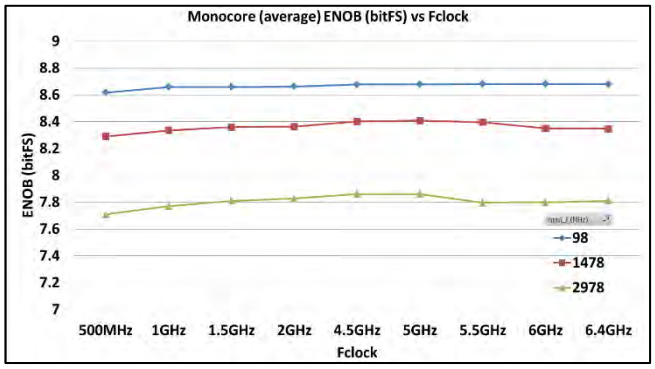
SFDR vs FClock



THD vs FClock



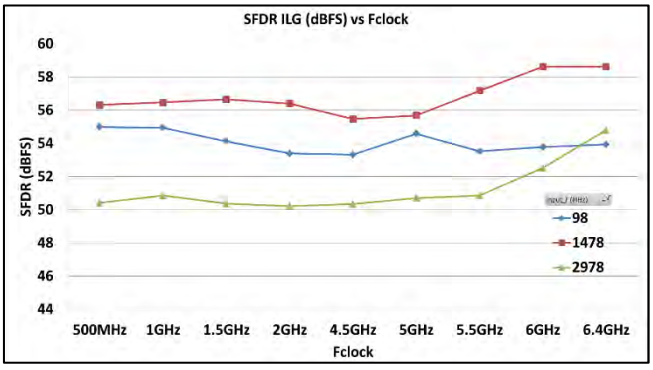
SNR vs FClock



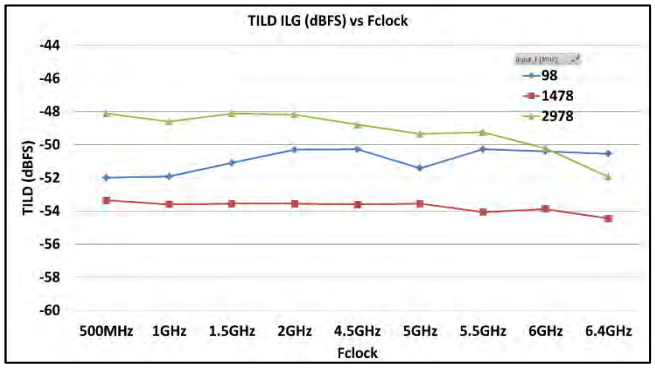
ENOB vs FClock

Figure 69: Performance vs Fclock - 4-channel mode – 1.6 GSps

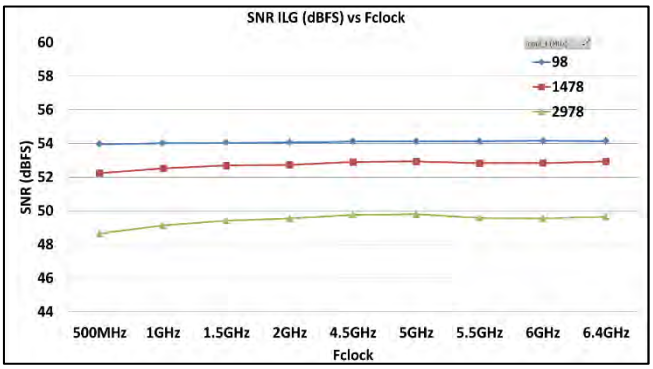
10.8.2 1-channel mode – 6.4 GSps



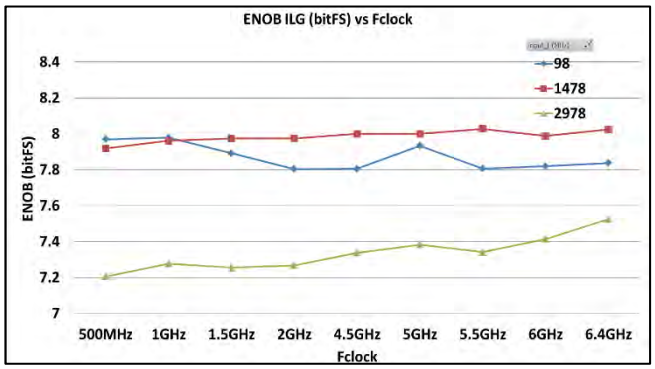
SFDR vs FClock



TILD vs FClock



SNR vs FClock

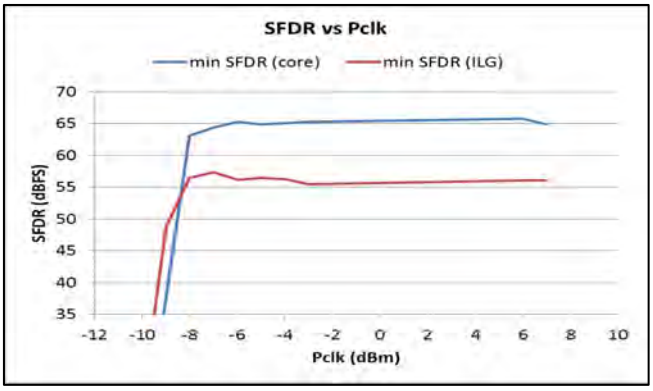


ENOB vs FClock

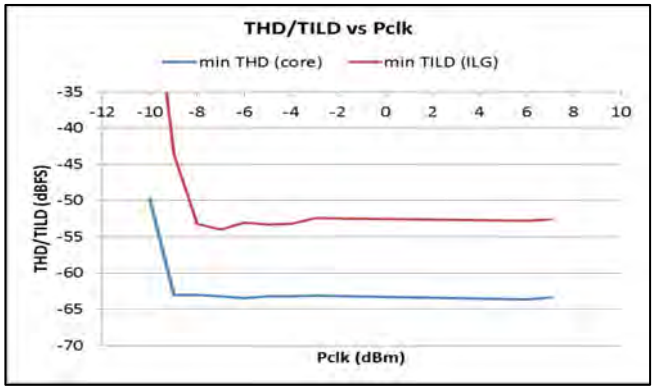
Figure 70: Performance vs Fclock - 1-channel mode – 6.4 GSps

10.9 Performance versus Clock Input Power

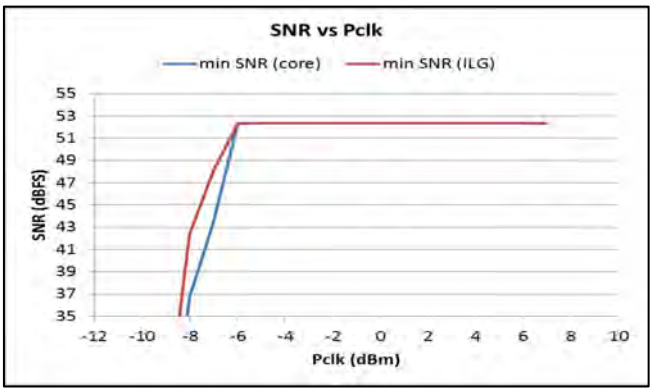
10.9.1 1-channel mode – 6.4 GSps



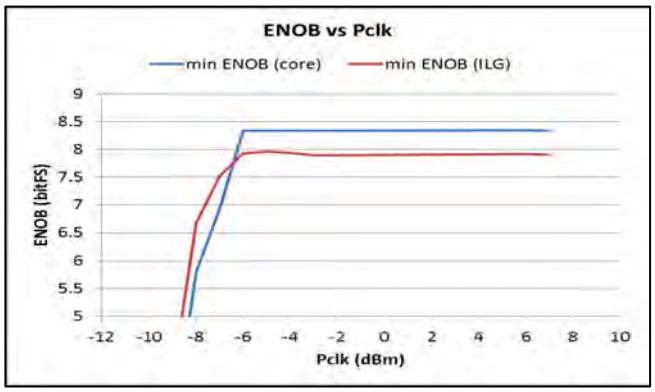
SFDR versus Clock input power



THD/TILD versus Clock input power



SNR versus Clock input power

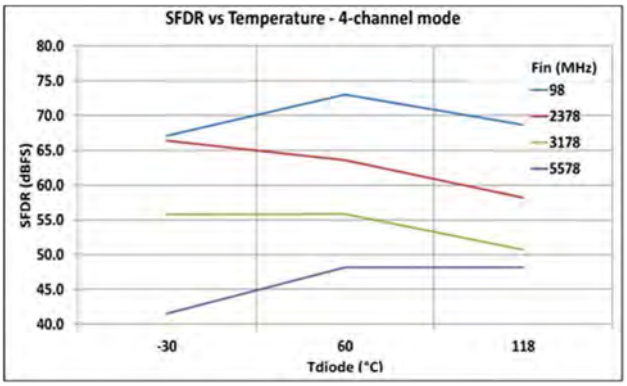


ENOB versus Clock input power

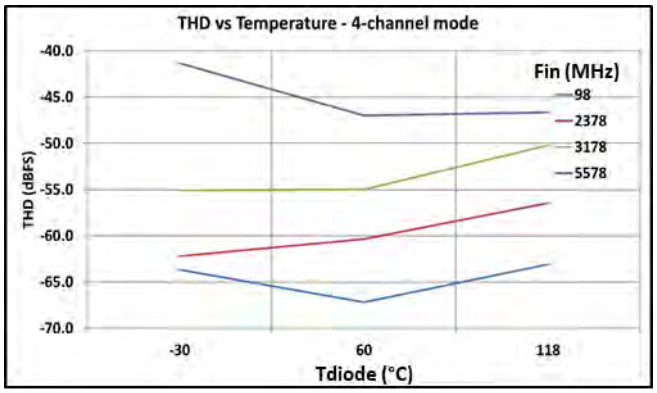
Figure 71: Performance vs Pclock - 4-channel mode – 1.6 GSps

10.10 Dynamic Performance versus Temperature

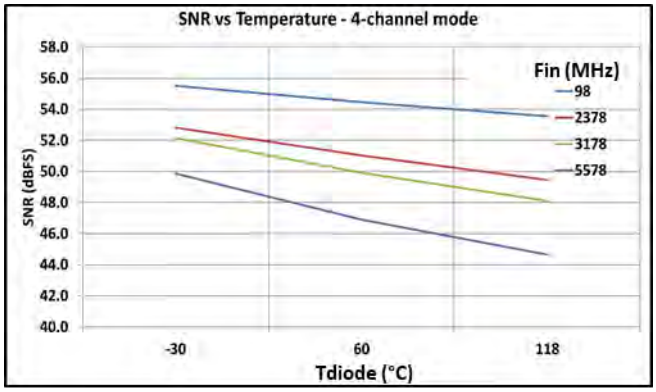
10.10.1 4-channel mode – 1.6 GSps



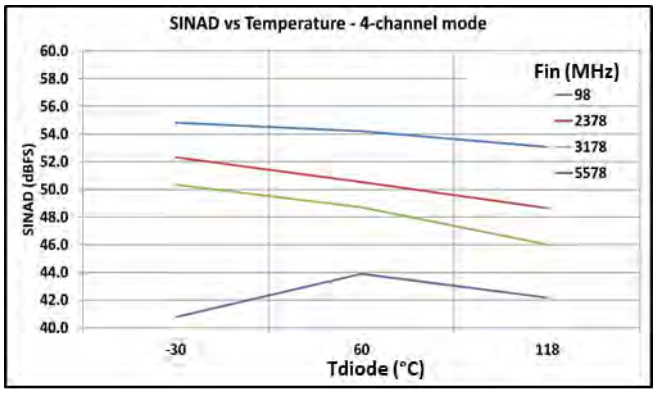
SFDR vs temperature



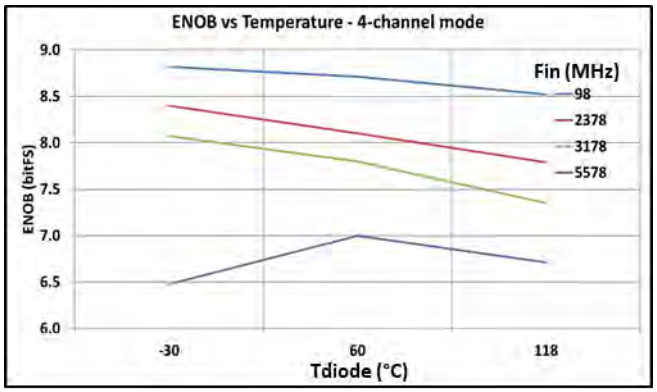
THD vs temperature



SNR vs temperature



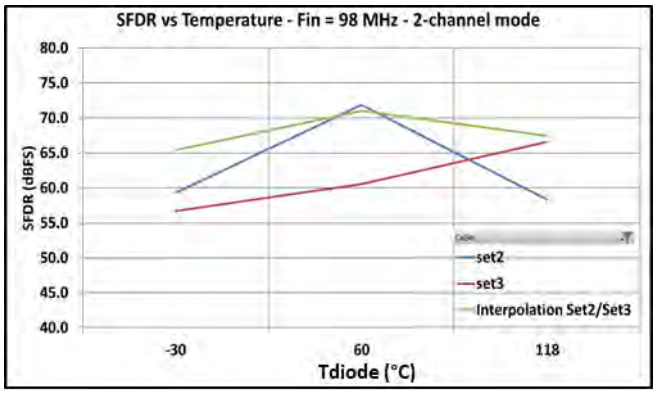
SINAD vs temperature



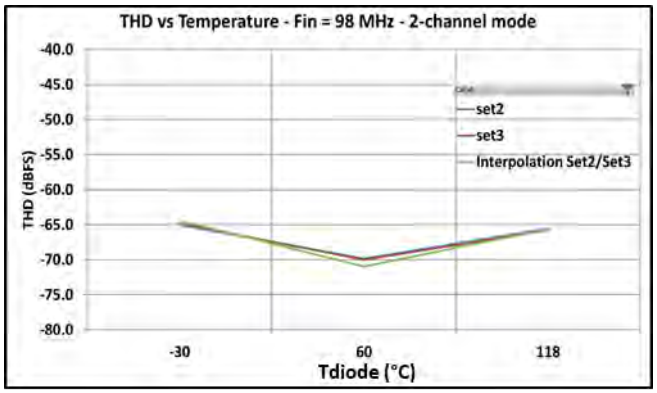
ENOB vs temperature

Figure 72: Performance vs Temperature – vsFin - Pout = -1 dBFS

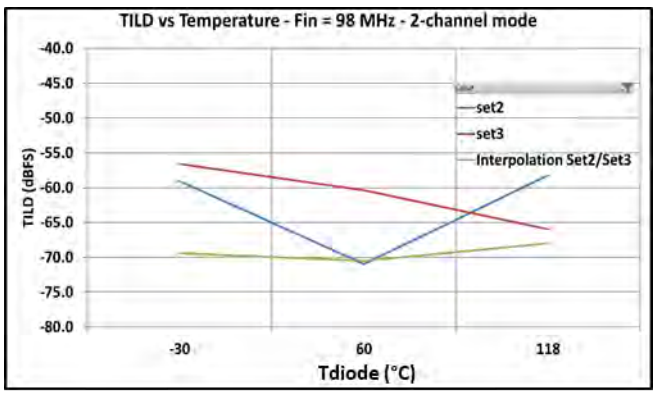
10.10.2 **2-channel mode - 3.2 GSps**



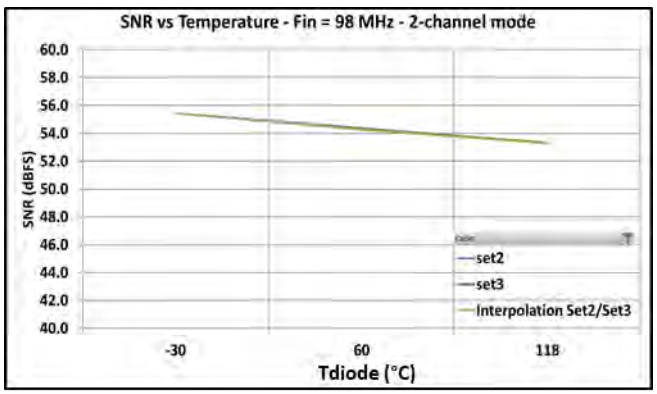
SFDR vs temperature



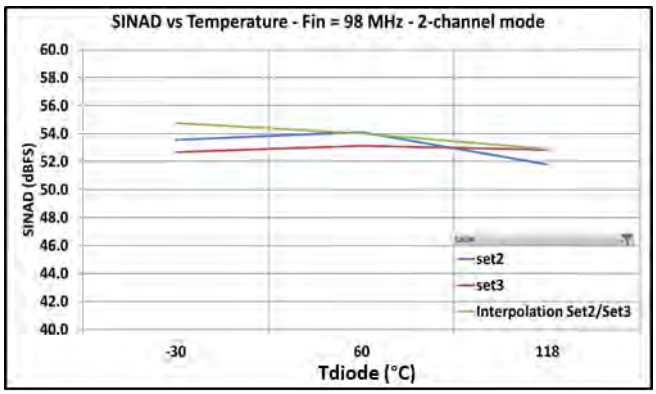
THD vs temperature



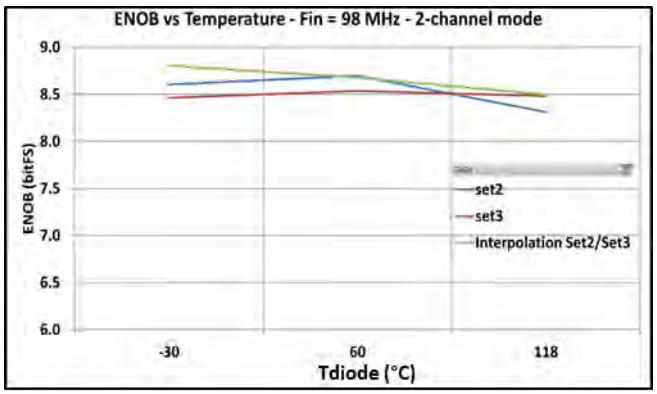
TILD vs temperature



SNR vs temperature

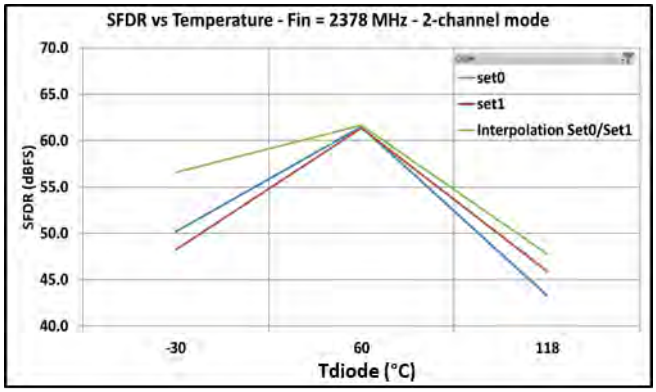


SINAD vs temperature

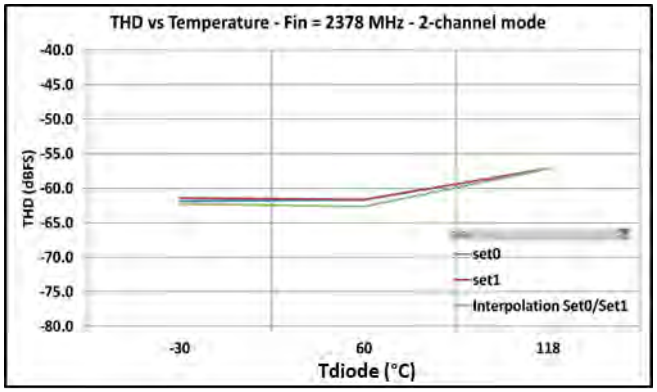


ENOB vs temperature

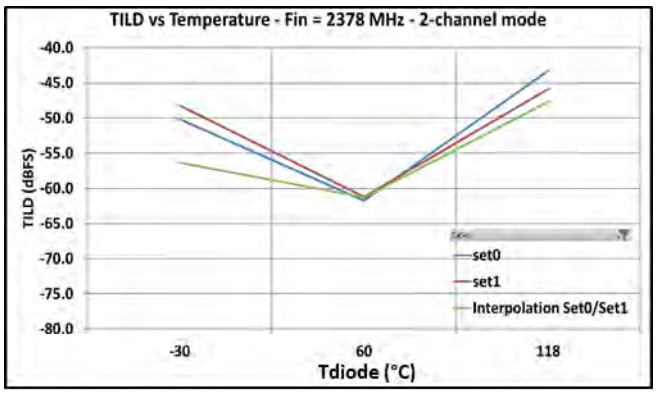
Figure 73: Performance vs Temperature - Fin= 98 MHz - Pout= -1 dBFS
Note : Calibration set Set3 and interpolation only available on AQ600 device



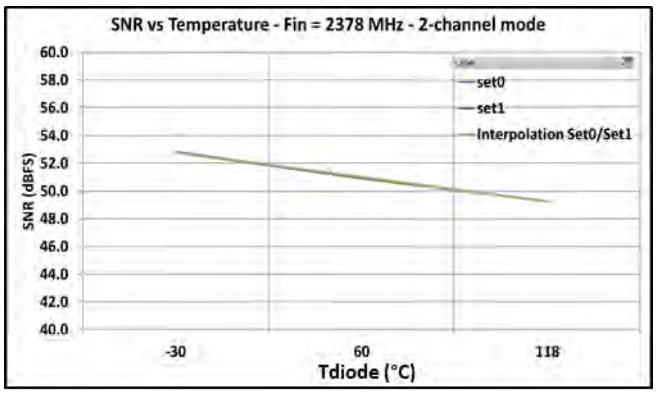
SFDR vs temperature



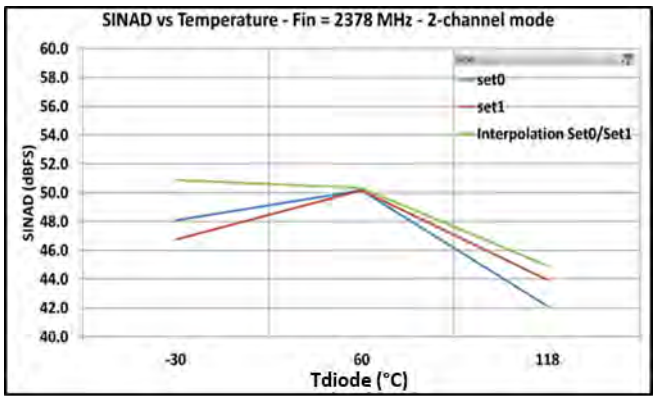
THD vs temperature



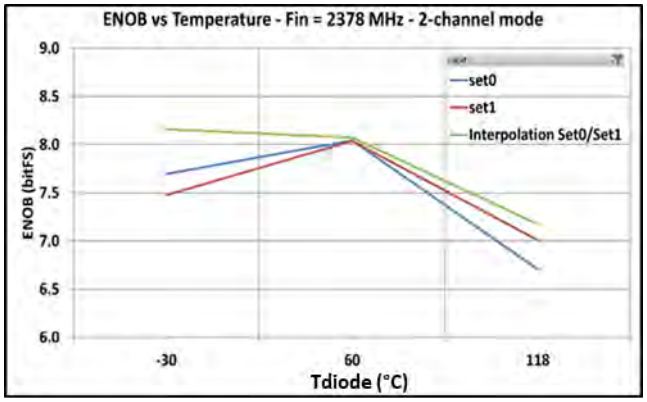
TILD vs temperature



SNR vs temperature



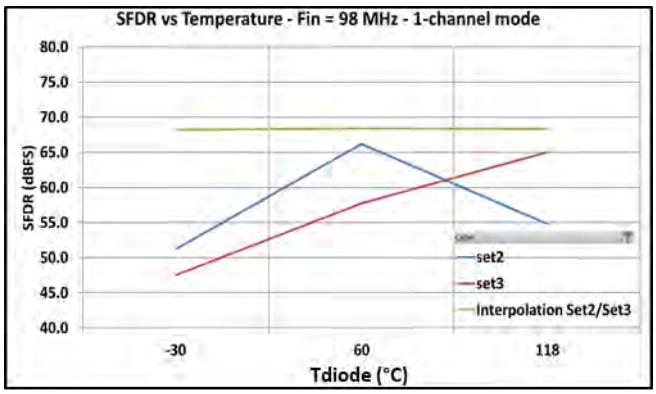
SINAD vs temperature



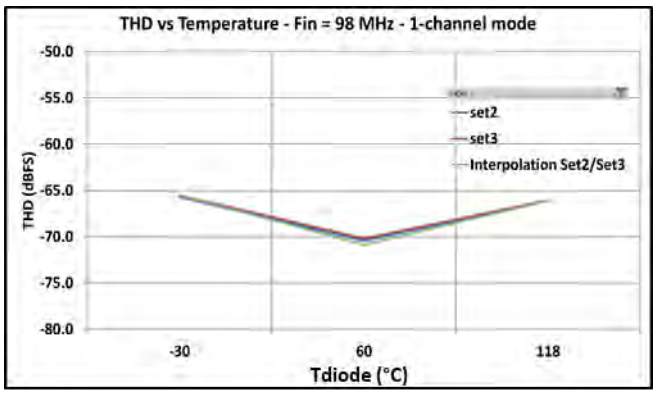
ENOB vs temperature

Figure 74: Performance vs Temperature - Fin= 2378 MHz - Pout= -1 dBFS
Note : Calibration set Set1 and interpolation only available on AQ600 device

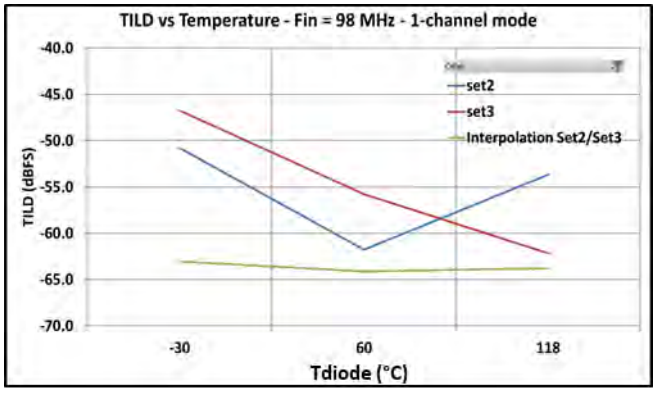
10.10.3 **1-channel mode – 6.4 GSps**



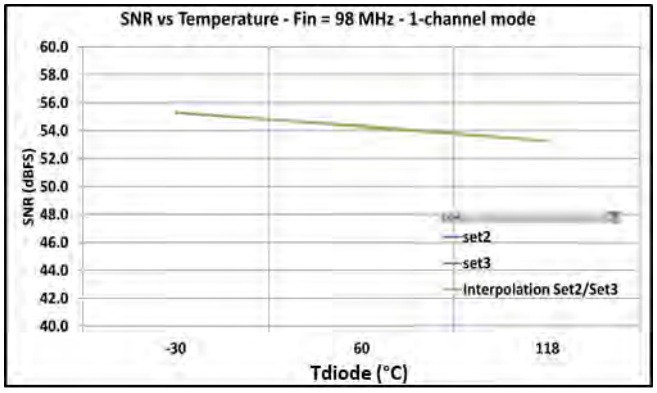
SFDR vs temperature



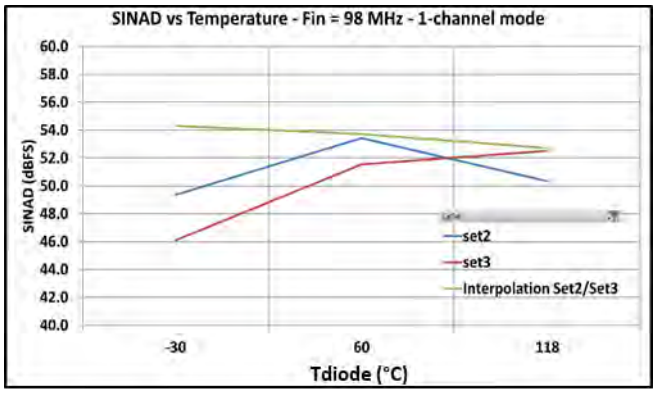
THD vs temperature



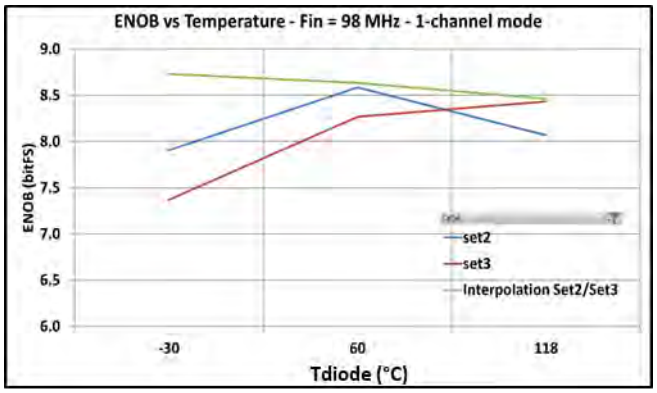
TILD vs temperature



SNR vs temperature

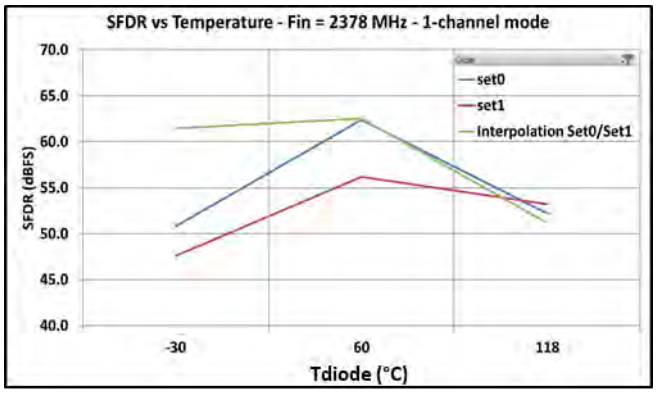


SINAD vs temperature

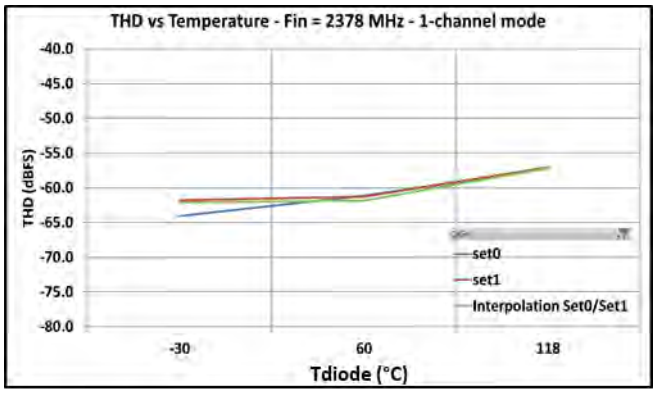


ENOB vs temperature

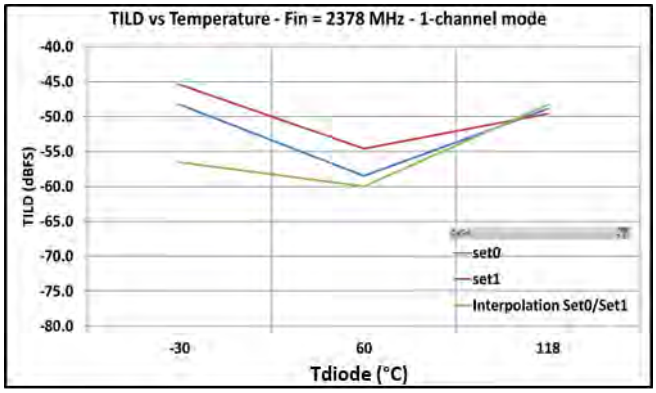
Figure 75: Performance vs Temperature - Fin= 98 MHz - Pout= -1 dBFS
Note : Calibration set Set3 and interpolation only available on AQ600 device



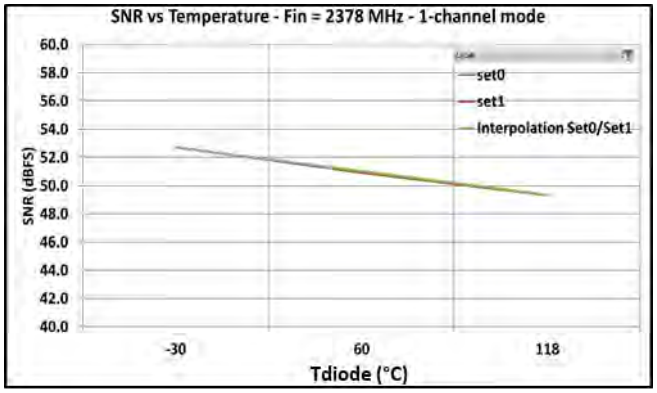
SFDR vs temperature



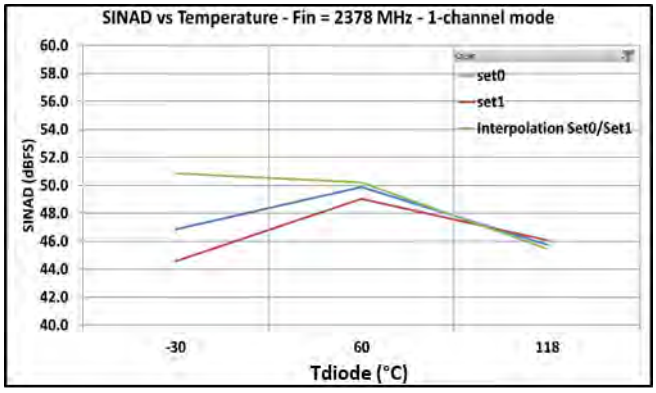
THD vs temperature



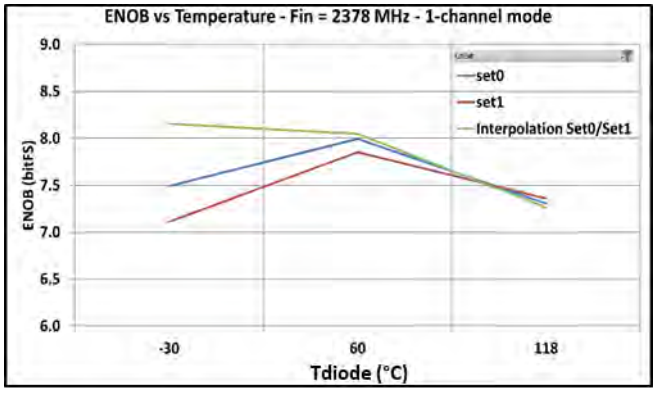
TILD vs temperature



SNR vs temperature



SINAD vs temperature

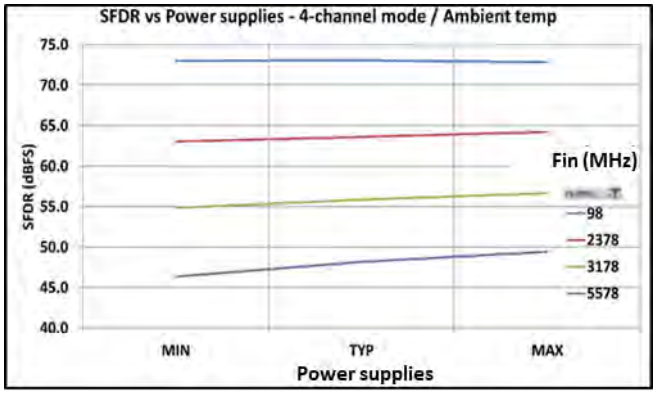


ENOB vs temperature

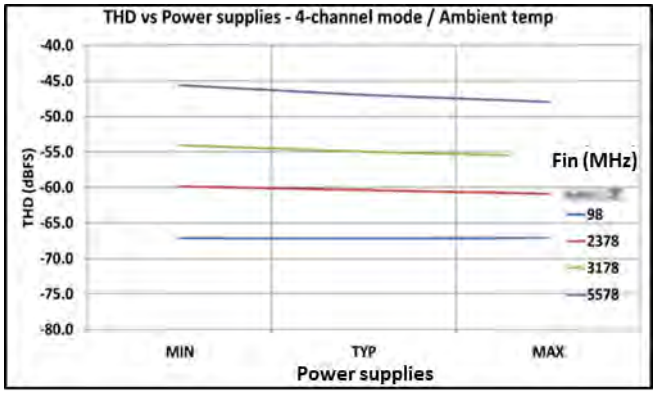
Figure 76: Performance vs Temperature - Fin= 2378 MHz - Pout= -1 dBFS
Note : Calibration set Set1 and interpolation only available on AQ600 device

10.11 Dynamic Performance versus Power supplies

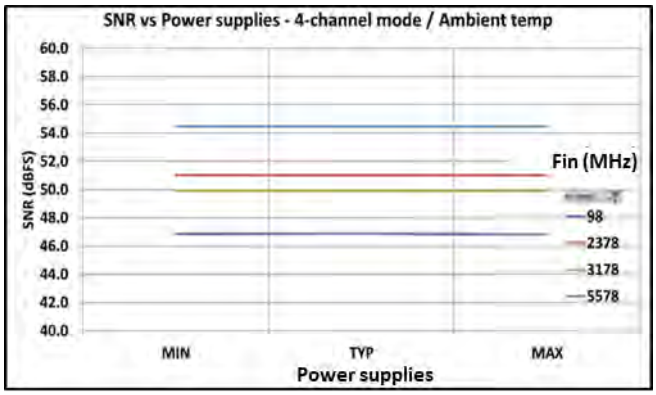
10.11.1 4-channel mode – 1.6 GSps



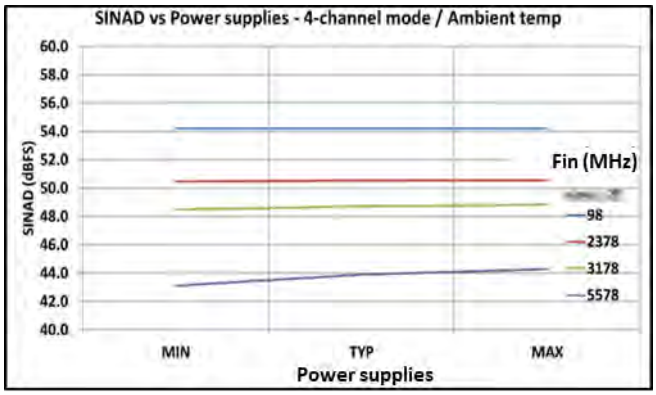
SFDR vs power supplies



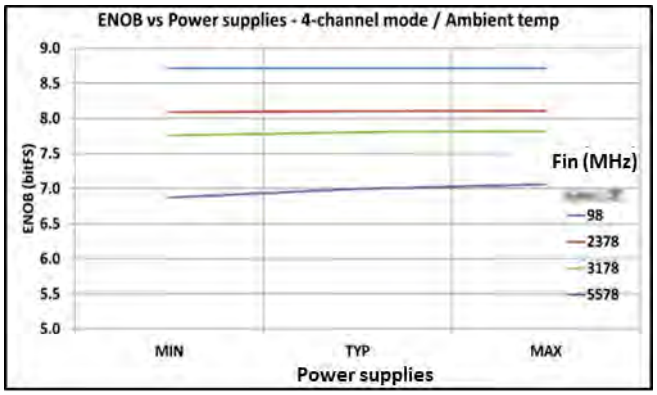
THD vs power supplies



SNR vs power supplies



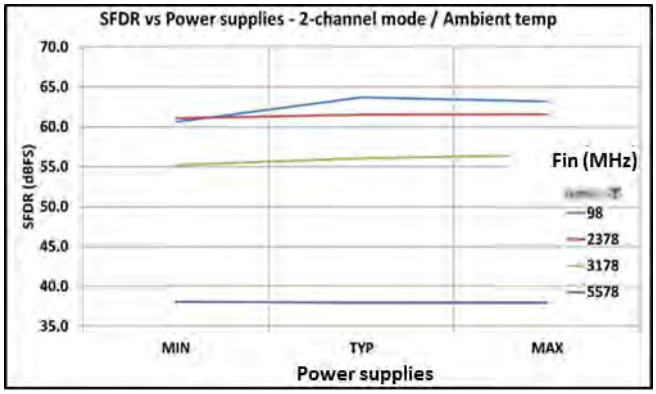
SINAD vs power supplies



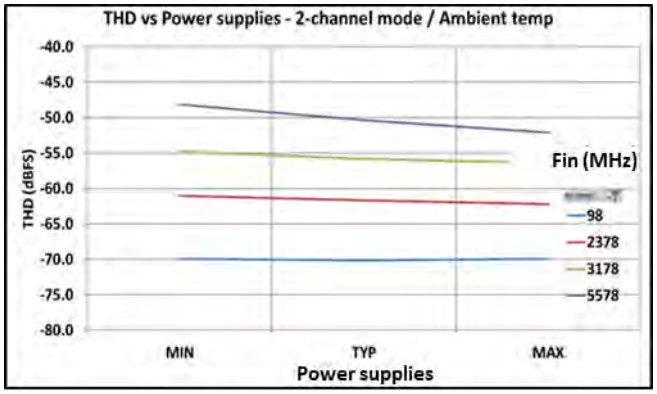
ENOB vs power supplies

Figure 77: Performance vs Power Supply - Pout= -1 dBFS

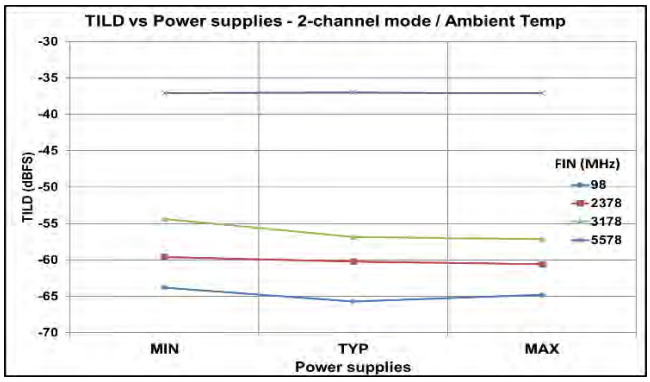
10.11.2 **2-channel mode – 3.2 GSps**



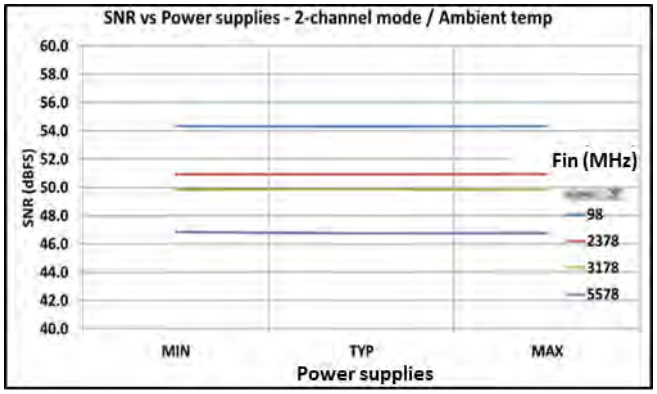
SFDR vs power supplies



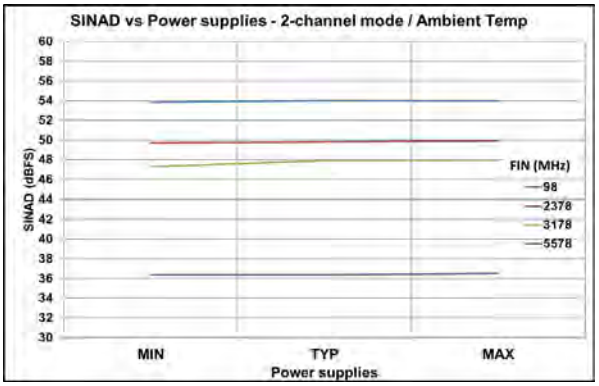
THD vs power supplies



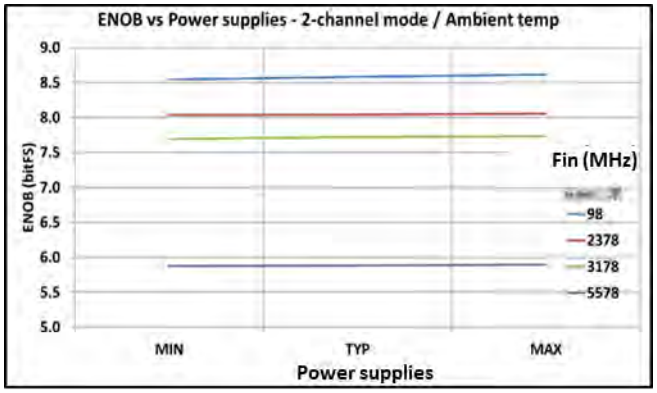
TILD vs power supplies



SNR vs power supplies



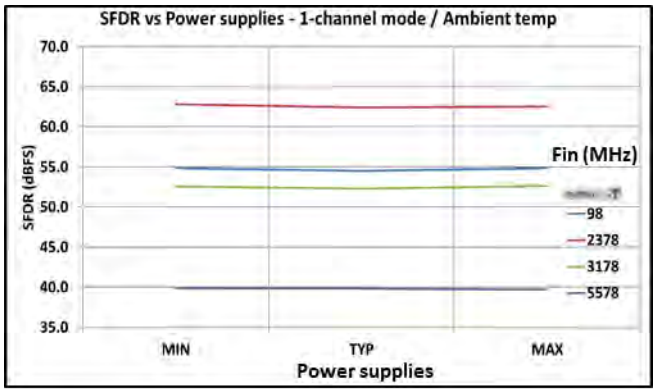
SINAD vs power supplies



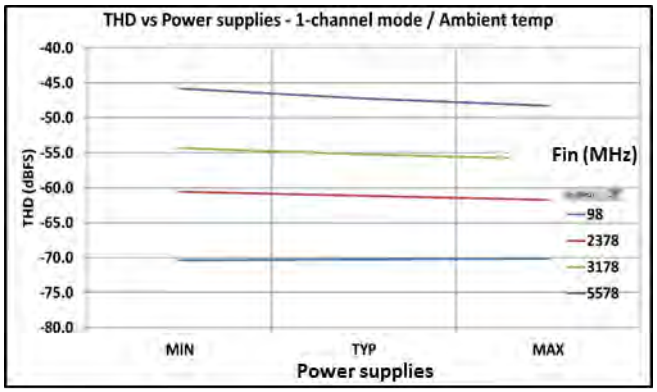
ENOB vs power supplies

Figure 78: Performance vs Power Supply - Pout= -1 dBFS
- Calibration set: CalSet0 -

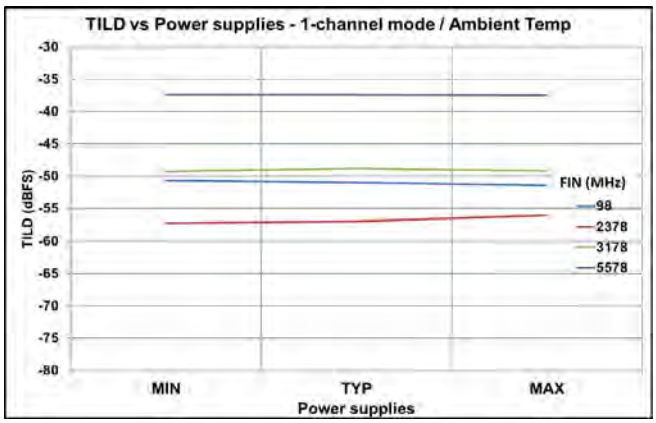
10.11.3 **1-channel mode – 6.4 GSps**



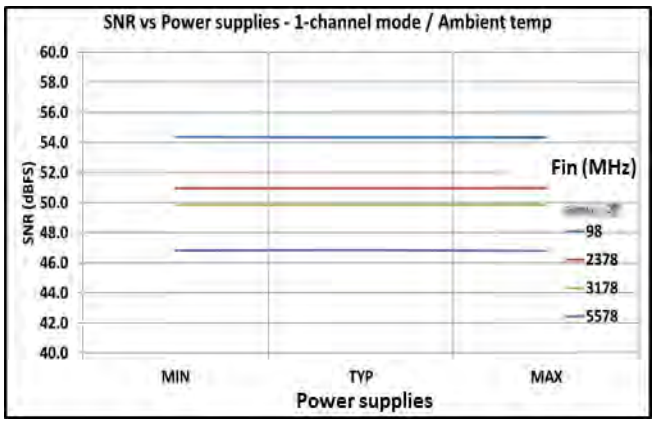
SFDR vs power supplies



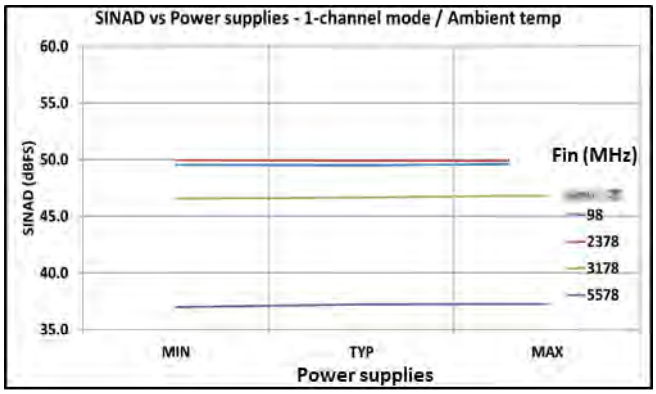
THD vs power supplies



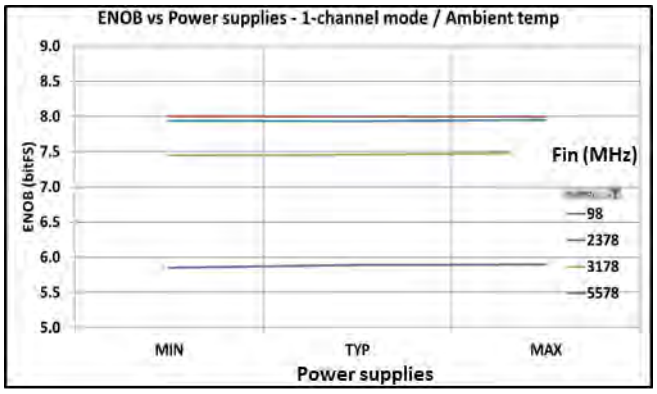
TILD vs power supplies



SNR vs power supplies



SINAD vs power supplies



ENOB vs power supplies

Figure 79: Performance vs Power Supply - Pout= -1 dBFS
- Calibration set: CalSet0 –

10.12 IMD3 – 3rd order InterModulation Distortion

10.12.1 Analog Input frequency 100 MHz - 1-channel mode – 6.4 GSps

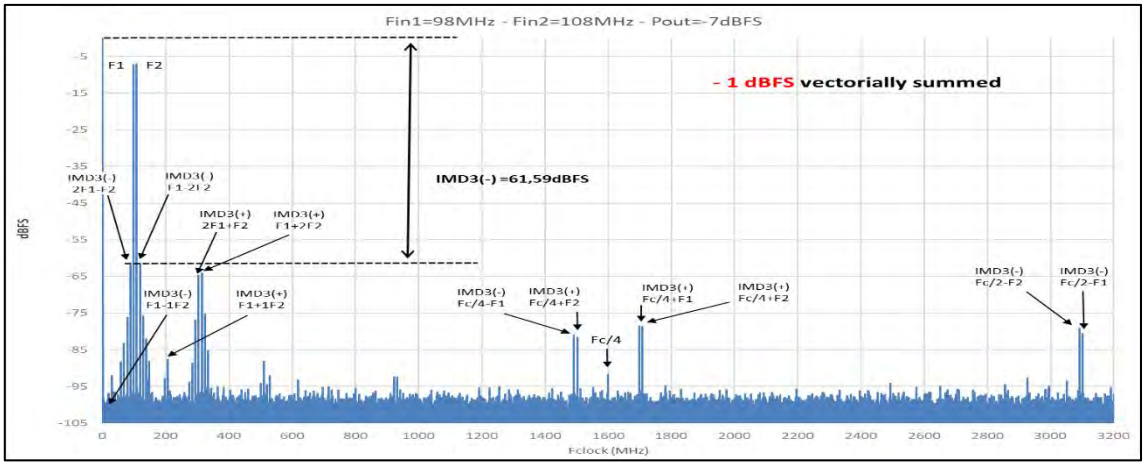


Figure 80: IMD3 – Analog Input frequency 100 MHz – Pout = -7 dBFS

10.12.2 Analog Input frequency 3100 MHz - 1-channel mode – 6.4 GSps

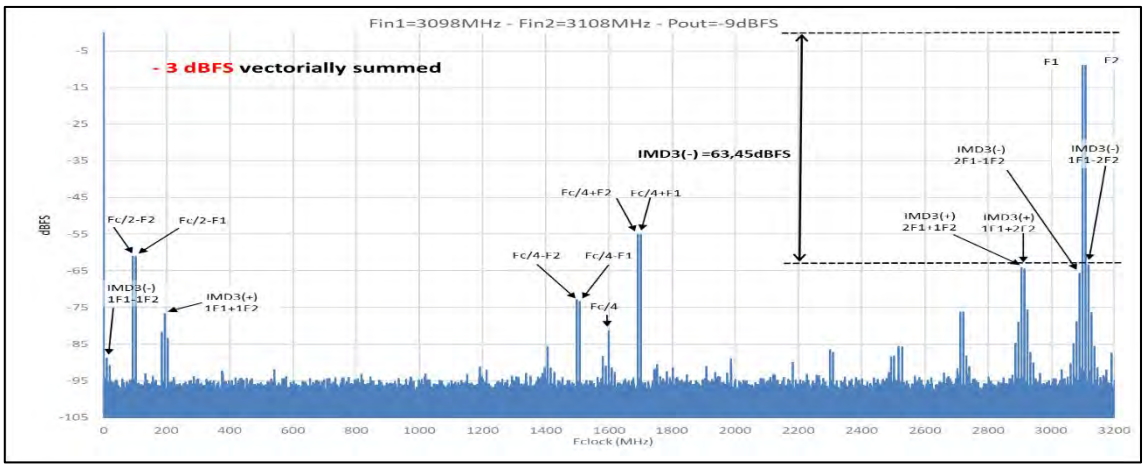


Figure 81: IMD3 – Analog Input frequency 3100 MHz – Pout = -9 dBFS

10.12.3 Analog Input frequency 5900 MHz - 1-channel mode – 6.4 GSps

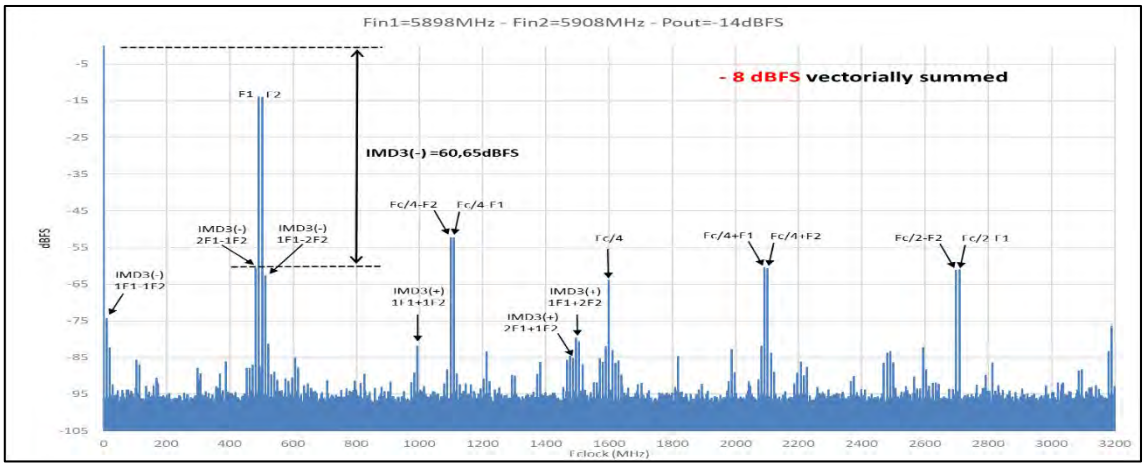


Figure 82: IMD3 – Analog Input frequency 5900 MHz – Pout = -14 dBFS

10.13 NPR – Noise Power Ratio

10.13.1 Mono core NPR performance in nominal conditions

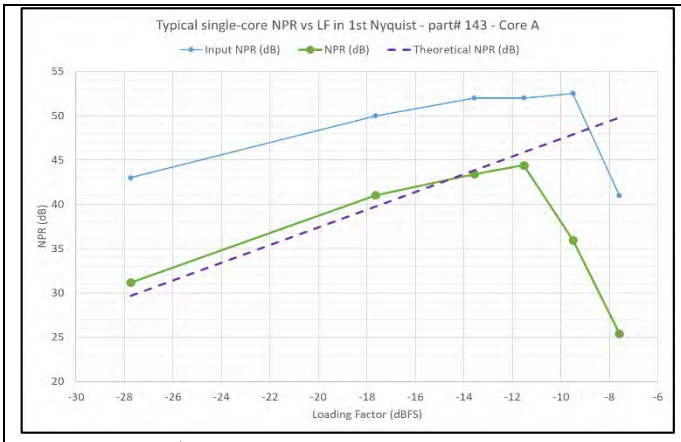


Figure 83: 1st Nyquist NPR versus loading factor. Fs = 1.6 GSps.

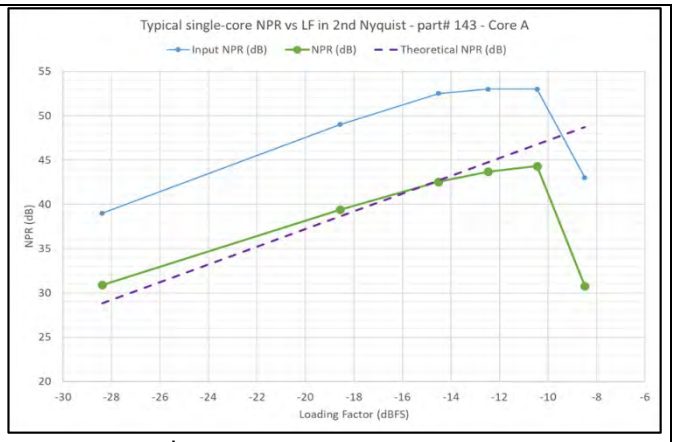


Figure 84: 2nd Nyquist NPR versus loading factor. Fs = 1.6 GSps.

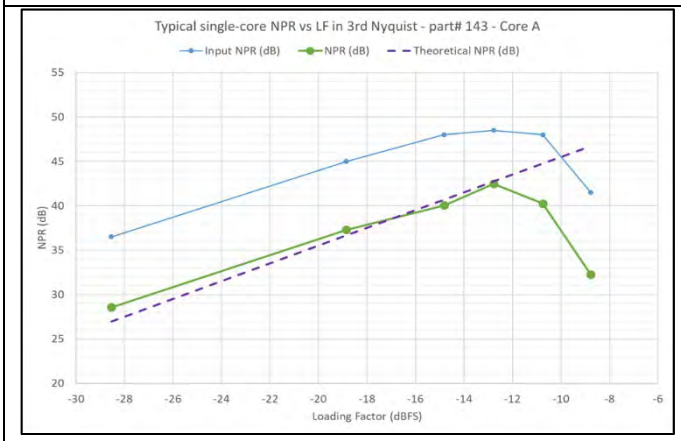


Figure 85: 3rd Nyquist NPR versus loading factor. Fs = 1.6 GSps.

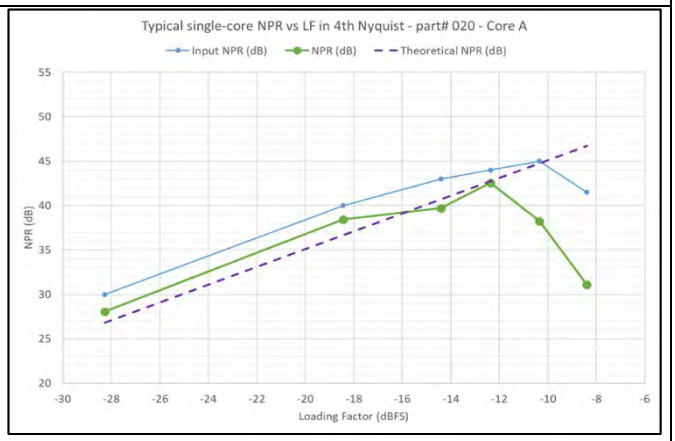


Figure 86: 4th Nyquist NPR versus loading factor. Fs = 1.6 GSps.

11 AQ600 ORDERING INFORMATION

Table 55. Prototypes

Part Number	Temperature Range	Screening Level	RoHS compliance	Comments
EVP12AQ600SH	Ambient	Prototype	RoHS	Beta sampling
EVX12AQ600AGH	Ambient	Prototype	Non RoHS	General samples
EVX12AQ600ASH	Ambient	Prototype	RoHS	General samples

Table 56. Evaluation kit

Part Number	Temperature Range	Screening Level	RoHS compliance	Comments
EV12AQ600-ADX4-EVM	Ambient	Prototype	RoHS	
EV12AQ600-2ADC-EVM	Ambient	Prototype	RoHS	

Table 57. Ordering codes

Part Number	Temperature Range	Screening Level	RoHS compliance	Comments
EV12AQ600ACSH	Tc 0°C, Tj +90°C	Standard	RoHS	
EV12AQ600AVSH	Tc -40°C, Tj +110°C	Standard	RoHS	
EV12AQ600AMSH	Tc -55°C, Tj +125°C	Standard	RoHS	
EV12AQ600AMGH	Tc -55°C, Tj +125°C	Standard	Non RoHS	

Table 58. Engineering, Engineering Qualification and Flight Models ordering codes

Part Number	Temperature Range	Screening Level	RoHS compliance	Comments
EV12AQ600AMGHD/T	Tc -55°C, Tj +125°C	Standard +168h burn-in	Non RoHS	Contact marketing
EV12AQ600AMGHEQM	Tc -55°C, Tj +125°C	Engineering Qualification Model	Non RoHS	Contact marketing
EV12AQ600AMGH-Y	Tc -55°C, Tj +125°C	QML-Y compliant	Non RoHS	Contact marketing
EV12AQ600AMGH9NB1	Tc -55°C, Tj +125°C	ESCC9000 compliant	Non RoHS	Contact marketing

12 AQ605 ORDERING INFORMATION

Table 59. Prototypes

Part Number	Temperature Range	Screening Level	RoHS compliance	Comments
EVP12AQ605SH	Ambient	Prototype	RoHS	Beta sampling

Table 60. Evaluation kit

Part Number	Temperature Range	Screening Level	RoHS compliance	Comments
EV12AQ605-ADX4-EVM	Ambient	Prototype	RoHS	

Table 61. Ordering codes

Part Number	Temperature Range	Screening Level	RoHS compliance	Comments
EV12AQ605ACSH	Tc 0°C, Tj +90°C	Standard	RoHS	Pending qualification
EV12AQ605AVSH	Tc -40°C, Tj +110°C	Standard	RoHS	Pending qualification

13 REVISION HISTORY

Issue	Date	Comments
A	24/10/2019	Creation (replace EV12AQ600 datasheet) Datasheet for EV12AQ600 and EV12AQ605 products
B	20/02/2020	EV12AQ600AMGH order entry opened Add EV12AQ600AMGHEQM P/N Electrical Characteristics Table 5 updated