e2v

Low Power 12-bit 3 Gsps DAC with 4/2:1 MUX

Datasheet - *Preliminary*

MAIN FEATURES

- 12-bit resolution
- 3 Gsps guaranteed Conversion rate
- 4:1 or 2:1 integrated parallel MUX (selectable)
- Low latency time 3.5 clock cycle.
- 1.2 Watt Power Dissipation
- Functions
  - Selectable MUX ratio 4:1 (full speed), 2:1 (half speed)
  - User-friendly functions:
    - Return to Zero, Non Return to Zero, RF modes
    - Gain Adjustment
    - Diode for die junction temperature monitoring
    - Setup time and Hod time violation flags (STVF, HTVF)
    - Clock phase shift select for synchronization with DSP (PSS[2:0])
    - Output clock division selection (possibility to change the division ratio of the DSP clock)
    - Input data check bit (IDC_P, IDC_N) for timing with FPGA check
- LVDS differential data input and DSP clock output
- Analog output swing: 1Vpp differential (100Ω differential impedance)
- Power up reset
- External asynchronous reset for synchronization of multiple MuxDACs
- Power supplies : 3.3 V (Digital), 3.3V & 5V (Analogue)
- fpBGA 196 Package (15 x 15 mm body size, 1 mm pitch)
- Evaluation board with state of the art FPGA for full speed testing

PERFORMANCES

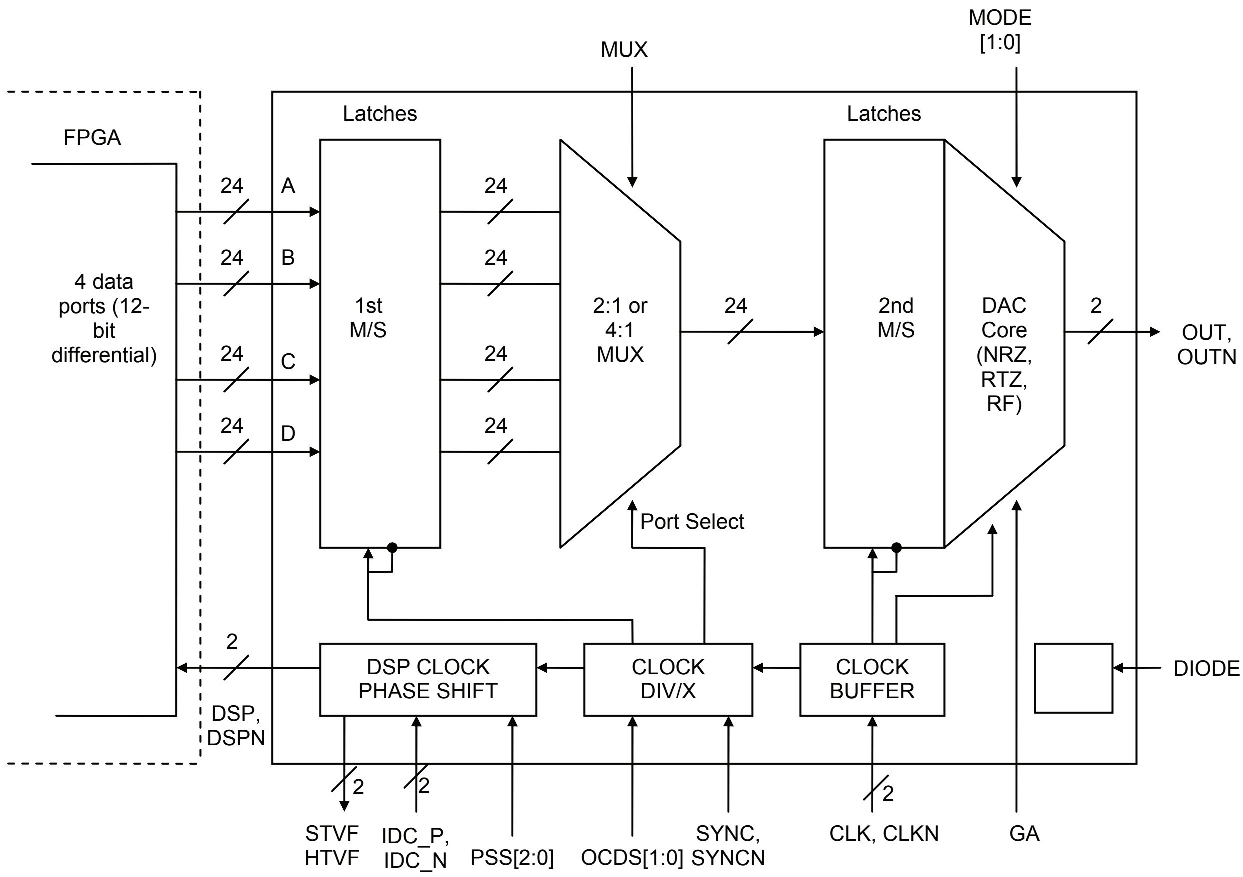
- **Broadband**
  - NPR (-12 dBFS peak to RMS loading factor): 52 dB at Fs = 3 Gsps: 10 Bit equivalent
    (20 MHz to 900 MHz Broadband pattern, 25 MHz notch centered around 450 MHz)
- **Single tone**
  - SFDR in Baseband (NRZ):
    62 dBc(-70 dBm highest spur level) at Fs = 3 Gsps over Full Nyquist zone (Full Scale output)
    66 dBc (-70 dBm highest spur level) at Fs = 3 Gsps over Full Nyquist zone (-3 dBFS output)
  - SFDR in 2nd Nyquist Zone (RTZ)
    66 dBc (-77 dBm highest spur level) at Fs = 3 Gsps over Full Nyquist zone (Full Scale output)
    63 dBc (-77 dBm highest spur level) at Fs = 3 Gsps over Full Nyquist zone (-3 dBFS output).
  - SFDR in 2nd and 3rd Nyquist Zones (RF)
    66dBc (-76 dBm highest spur level) at Fs = 3Gsps over Full second and third Nyquist Zones (Full Scale output)
    63dBc (-76 dBm highest spur level) at Fs=3Gsps over Full second and third Nyquist Zones (-3dBFS output)

APPLICATIONS

- Direct Digital Synthesis (DDS) for Broadband Applications
- Automatic Test Equipment (ATE)
- Arbitrary waveform generators
- Satellite up-conversion sub-systems
- Radar Waverform signal Synthesis
- DOCSIS 3.0 Systems

1. BLOCK DIAGRAM

Figure 1. Simplified Block Diagram



2. DESCRIPTION

The EV12DS130A is a 12-bit 3 Gsps DAC with an integrated 4:1 or 2:1 multiplexer, allowing easy interface with standard LVDS FPGAs.

The Noise Power Ratio (NPR) performance , which is 10 Bit equivalent at 3 GSPS, over more than 900 MHz instantaneous bandwidth, and the 70 dB linearity (SFDR, IMD) over full 1st Nyquist zone at 3 GSPS (NRZ feature), makes this product well suited for in high-end applications such as arbitrary waveform generators and broadband DDS systems.

3. ELECTRICAL CHARACTERISTICS

3.1. Absolute Maximum Ratings

Table 1. Absolute Maximum ratings

Parameter	Symbol	Value	Unit
Positive Analogue supply voltage	V_{CCA5}	6	V
Positive Analogue supply voltage	V_{CCA3}	3.6	V
Positive Digital supply voltage	V_{CCD}	3.6	V
Maximum difference between power supplies	V_{CCA5} - V_{CCD}	TBD	
Maximum difference between power supplies	V_{CCA3} - V_{CCD}	TBD	
Maximum difference between power supplies	V_{CCA5} - V_{CC3}	TBD	
Digital inputs (on each single-ended input) and IDC signal Port P = A, B, C, D V_{IL} V_{IH} Swing	[P0..P11], [P0N…P11N] IDC_P, IDC_N	TBD	V V mV
Maximum difference between differential Digital inputs	PiN – Pi	TBD	
Master clock input	CLK, CLKN	TBD	
Maximum difference between differential master clock inputs	CLKN - CLK	TBD	
Master clock input power level (single-ended mode)	P_{CLK}	12	dBm
Control functions inputs V_{IL} V_{IH}	MUX, MODE[0..1], PSS[0..2], OCDS[0..1]	-0.4V V_{CCD}+0.4	V V
Control functions outputs, maximum short current	STVF, HTVF	TBD	mA
Gain Adjustment function	GA	TBD	V
Reset (Sync)	SYNC, SYNCN	TBD	
Junction Temperature	TJ	125°C	°C
Storage Temperature	Tstg	-65 to 150	°C

Notes: - Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
- All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.
- Maximum ratings enable active inputs with DAC powered off.
- Maximum ratings enable floating inputs with DAC powered on.

3.2. Recommended Conditions Of Use

Table 2. Recommended Conditions of Use

Parameter	Symbol	Comments	Recommended Value	Unit
Positive analogue supply voltage	V_{CCA5}		5	V
Positive analogue supply voltage	V_{CCA3}		3.3	V
Positive digital supply voltage	V_{CCD}		3.3	V
Digital inputs (on each single-ended input) and IDC signal V_{IL} V_{IH} Swing	A0..A11, A0N..A11N B0..B11, B0N..B11N C0..C11, C0N..C11N D0..D11, D0N..D11N IDC_P, IDC_N		1.075 1.425 350	
Master clock input	CLK, CLKN		1.2	Vpp
Master clock input power level Differential mode	P_{CLK}		3	dBm
Control functions inputs	MUX, OCDS, PSS, MODE, PSS	V_{IL} V_{IH}	0 V_{CCD}	V V
Gain Adjustment function	GA		V_{CCA3} /2 +/- 0.5	V
Reset function	SYNC, SYNCN		1.075 1.425 350	
Operating Temperature Range	T_c T_j	Commercial “C” grade Industrial “V” grade	T_c >0°C < T_j < 90°C T_c>-40°C < T_j < 110°C	°C

Notes : Analog output is in differential
Single-ended operation is not recommended. Optimum performance is only in differential configuration.

3.3. Electrical Characteristics

Unless otherwise specified:
V_{CCA} = 5V, V_{CCA} = 3.3V, V_{CCD} = 3.3V

Table 3. Electrical characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
RESOLUTION			12		**bit**	
ESD CLASSIFICATION			Class 1B			
POWER REQUIREMENTS						
Power Supply voltage - Analogue - Analogue - Digital	 V_{CCA5} V_{CCA3} V_{CCD}	 4.75 3.15 3.15	 5 3.3 3.3	 5.25 3.45 3.45	V V	
Power Supply current (4:1 MUX) - Analogue - Analogue - Digital	 I_{CCA5} I_{CCA3} I_{CCD}			 95 110 200	 mA mA mA	
Power Supply current (2:1 MUX) - Analogue - Analogue - Digital	 I_{CCA5} I_{CCA3} I_{CCD}			 95 110 170	 mA mA mA	
Power dissipation (4:1 MUX)	P_D		1.33		W	
Power dissipation (2:1 MUX)	P_D		1.25		W	
DIGITAL DATA INPUTS, SYNC and IDC INPUTS						
Logic compatibility			LVDS			
Digital input voltages: - Logic 0 - Logic 1 - Differential input voltage - Common mode	 V_{IL} V_{IH} V_{ID} V_{CM}		 1.075 1.425 350 1.250		 V V Vpp V	
Input capacitance from each single input to ground				2	pF	1
Differential Input resistance			100		Ω	
CLOCK INPUTS						
Input voltages (Differential operation swing)			1.2		Vpp	
Power level (Differential operation)			3		dBm	
Common mode		2.46	2.47	2.49	V	
Input capacitance from each single input to ground (at die level)				2	pF	
Differential Input resistance:			100		Ω	
DSP CLOCK OUTPUT						
Logic compatibility			LVDS			
Digital output voltages: - Logic 0 - Logic 1 - Differential output voltage - Common mode	 V_{OL} V_{OH} V_{OD} V_{CM}		 1.075 1.425 350 1.250		 V V mV V	
ANALOG OUTPUT						
Full-scale Differential output voltage (100 Ω differentially terminated)			1		Vpp	
Full-scale output power (differential output)			-1		dBm	
Full-scale output power with 1/√2 balun (50 Ω terminated)			TBD			

Parameter	Symbol	Min	Typ	Max	Unit	Notes
output common mode voltage (50 Ω terminated)			V_{CCA5} – 0.3		V	
Output capacitance				1.5	pF	
Output internal dual single-ended resistance			50		Ω	1
Output VSWR (using EV12DS130AZPY-EB evaluation board – package + board dominated) 1.5GHz 3 GHz 4.5 GHz				1.1 1.6 2		
Deviation from theoretical Sinx/x (first order bandwidth limitation)			7		GHz	
FUNCTIONS						
Digital functions: MODE, OCDS, PSS, MUX - Logic 0 - Logic 1	V_{IL} V_{IH}	 1.45	0 V_{CCD}	1V	V V	
Gain Adjustment function	GA		V_{CCA3} /2 ± 0.5		V	
Digital output function (HTVF, STVF) Logic 0 Logic 1	V_{OL} V_{OH}	- 2.4	- -	0.8 -	V V	
DC ACCURACY						
Differential Non-Linearity	DNL+			0.5	LSB	
Differential Non-Linearity	DNL-	-0.5			LSB	
Integral Non-Linearity	INL+			1.5	LSB	
Integral Non-Linearity	INL-	-1.5			LSB	
DC gain: - Initial gain error - DC gain dispersion - DC gain sensitivity to power supplies - DC gain drift over temperature			0	+/-2	%FS %FS %FS ppm/°C	3
Analogue output offset voltage			V_{CCA5} – 0.3		V	4

Notes: 1. Given by design.

2. Initial gain error corresponds to the deviation of the DC gain center value from unity gain. The gain can be set to 1 thanks to the GA function.

3. DC gain dispersion excludes initial gain error.

4. Analogue output offset voltage is measured with a 100 Ω differential load on the DAC outputs.

3.4. AC Electrical Characteristics

Unless otherwise specified:
V_{CCA} = 5V, V_{CCA} = 3.3V, V_{CCD} = 3.3V

Table 4. **AC Electrical Characteristics NRZ Mode (First nyquist Zone)**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Single-tone Spurious Free Dynamic Range First Nyquist (Full Zone) Fs = 3 Gsps Full scale Output Fs = 3 Gsps -3 dBFS Output	SFDR		62 66		dBc dBc	1
Highest spur level First Nyquist (Full Zone) Fs = 3 Gsps Full scale Output Fs = 3 Gsps -3 dBFS Output			-70 -70		dBm dBm	
SFDR sensitivity over temperature and power supplies					dBm	
Signal independent Spur (clock-related spur)						
Fc			-60		dBm	
Fc/2			-60		dBm	
Fc/4			<-80		dBm	
Signal to Noise Ratio (thermal noise contribution)			62		dB	
Noise Power Ratio -14 dBFS peak to rms loading factor Fs = 3 Gsps 20 MHz to 900 MHz broadband pattern, 25 MHz notch centered on 450 MHz	NPR		52		dB	2
Equivalent ENOB **Computed from NPR figure**			10		Bit	

Notes: 1. Ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured over the first Nyquist frequency band (DC to Fs/2).
2. NPR band limitations are only due to measurement equipment limitations not to the component itself. Figures provided in the table are applicable (analytical validation) for bands beyond 650, 680 and 880 MHz.

Table 5. AC Electrical Characteristics RTZ Mode (Second Nyquist Zone)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Single-tone Spurious Free Dynamic Range Second Nyquist: Fs = 3 Gsps Full scale Output Fs = 3 Gsps -3 dBFS Output	|SFDR|		66 63		dBc dBc	1
Highest spur level Second Nyquist: Fs = 3 Gsps Full scale Output Fs = 3 Gsps -3 dBFS Output			-77 -77		dBm dBm	
SFDR sensitivity over temperature and power supplies					dBm	
Signal independent Spur (clock-related spur)						
Fc			-35	-30	dBm	
Fc/2			-50		dBm	
Fc/4			<-85		dBm	
Signal to Noise Ratio (thermal noise contribution)			64		dB	
Noise Power Ratio (2nd Nyquist) -14 dBFS peak to rms loading factor Fs = 3 Gsps 1520 MHz to 2200 MHz broadband pattern, 25 MHz notch centered on 1850 MHz	NPR		54		dB	2
Equivalent ENOB **Computed from NPR figure**			10		Bit	

Notes: 1. Ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured over the second Nyquist frequency band (Fs/2 to Fs).
2. NPR band limitations are only due to measurement equipment limitations not to the component itself. Figures provided in the table are applicable (analytical validation) for bands beyond 650, 680 and 880 MHz.

Table 6. AC Electrical Characteristics RF Mode (Second and Third Nyquist Zones), *target figures*.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Single-tone Spurious Free Dynamic Range Second Nyquist (Full Zone): Fs = 3 Gsps Full scale Output Fs = 3 Gsps -3 dBFS Output	|SFDR|		66 63		dBc dBc	1
Highest spur level Second Nyquist (Full Zone): Fs = 3 Gsps Full scale Output Fs = 3 Gsps -3 dBFS Output			-76 -76		dBm dBm	
Single-tone Spurious Free Dynamic Range Third Nyquist (Full Zone): Fs = 3 Gsps Full scale Output Fs = 3 Gsps -3 dBFS Output	|SFDR|		66 63		dBc dBc	2
Highest spur level Third Nyquist (Full Zone): Fs = 3 Gsps Full scale Output Fs = 3 Gsps -3 dBFS Output			-76 -76		dBm dBm	
SFDR sensitivity over temperature and power supplies					dBm	
Signal independent Spur (clock-related spur)						
Fc			-60		dBm	
Fc/2			-60		dBm	
Fc/4			<-80		dBm	
Signal to Noise Ratio (thermal noise contribution)			64		dB	
Noise Power Ratio (2nd Nyquist) -14 dBFS peak to rms loading factor Fs = 3 Gsps 1520 MHz to 2200 MHz broadband pattern, 25 MHz notch centered on 1850 MHz	NPR		54 target		dB	3
Noise Power Ratio -14 dBFS peak to rms loading factor Fs = 3 Gsps 2200 MHz to 2880 MHz broadband pattern, 25 MHz notch centered on 2550 MHz	NPR		54 target		dB	3
Noise Power Ratio -14 dBFS peak to rms loading factor Fs = 3 Gsps 3050 MHz to 3700 MHz broadband pattern, 25 MHz notch centered on 3375 MHz	NPR		54 target		dB	3

Notes: 1. Ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured over the second Nyquist frequency band (Fs/2 to Fs).
2. Ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured over the third Nyquist frequency band (Fs to 3Fs/4).
3. NPR band limitations are only due to measurement equipment limitations not to the component itself. Figures provided in the table are applicable (analytical validation) for bands beyond 650, 680 and 880 MHz.

3.5. Timing Characteristics and Switching Performances

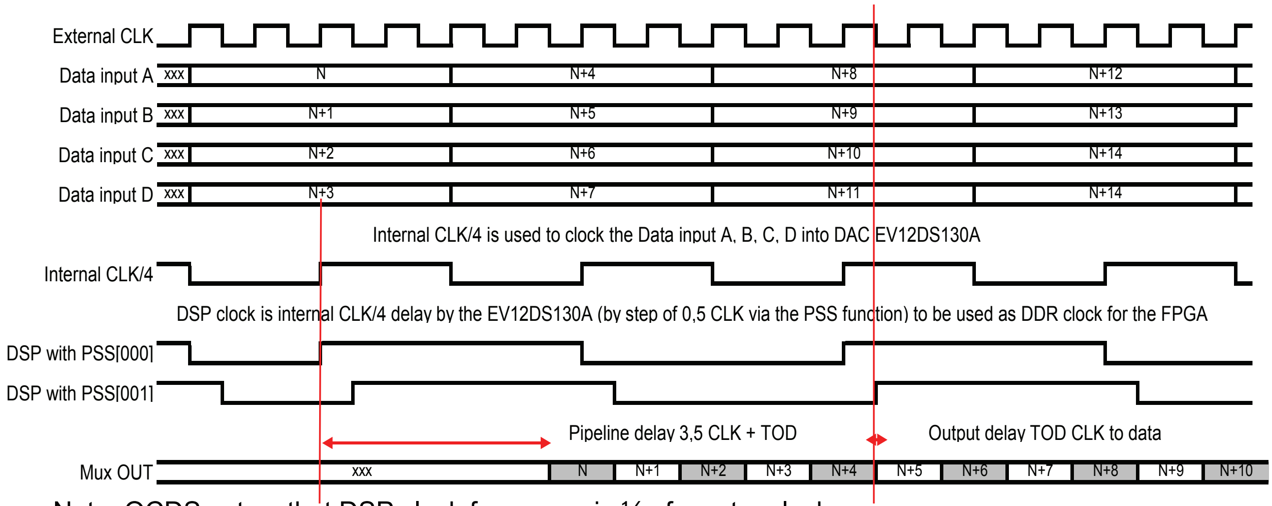
Table 7. Timing characteristics and Switching Performances

Parameter	Symbol	Min	Typ	Max	Unit	Note
SWITCHING PERFORMANCE AND CHARACTERISTICS						
Maximum operating clock frequency 4:1 MUX mode 2:1 MUX mode			1.5	3 2 (TBC)	GHz	1
Minimum operating clock frequency		0			MHz	2
Maximum analogue output frequency				4.5	GHz	
Minimum analogue output frequency		0			MHz	2
TIMING CHARACTERISTICS						
Input data rise/fall time	Tdata rise/Tdata fall		50		ps	3
Tsetup (Fc = 3 Gsps)			570 (TBC)		ps	4
Thold (Fc = 3 Gsps)			570 (TBC)		ps	4
Input data rate				750	Msps	
Input data pulse width		1.15			ns	
Master clock input frequency			3		GHz	
Master clock input jitter				500	fs rms	5
CLK to DSP clock output delay (clock shift = 000)			2		ns	
CLK to DSP clock output delay (clock shift = 111)			2.75		ns	
DSP clock phase tuning range		0		+3.5	Clock Cycle	6
DSP clock phase tuning steps			0.5		Clock cycle	6
Master clock to DSP, DSPN delay	TDSP		2 (TBC)		ns	
SYNC to DSP, DSPN				660 (TBC)	ps	
Pipeline delay MUX 4:1 MUX 2:1	TDP		3.5 4.5		Clock cycles	
Output delay	TOD		160		ps	

Notes: 1. In 2:1 MUX mode, target is to reach 2GHz sampling clock. This figure is TBC.
2. Minimum operating clock frequency can be DC. It depends on the clock input AC coupling capacitor used in the final application. Refer to 6.2.
Minimum analogue output frequency depends on the AC coupling scheme used on the differential analogue output signal and on the DAC mode selected (refer to section 5.2, to Figure 22 and Figure 23).
3. Digital input data rise/fall time defined between 20% to 80%.
4. Exclusive of period (pp) jitter on Data.
5. Master clock input jitter defined over 5 GHz bandwidth.
6. Guaranteed by design.

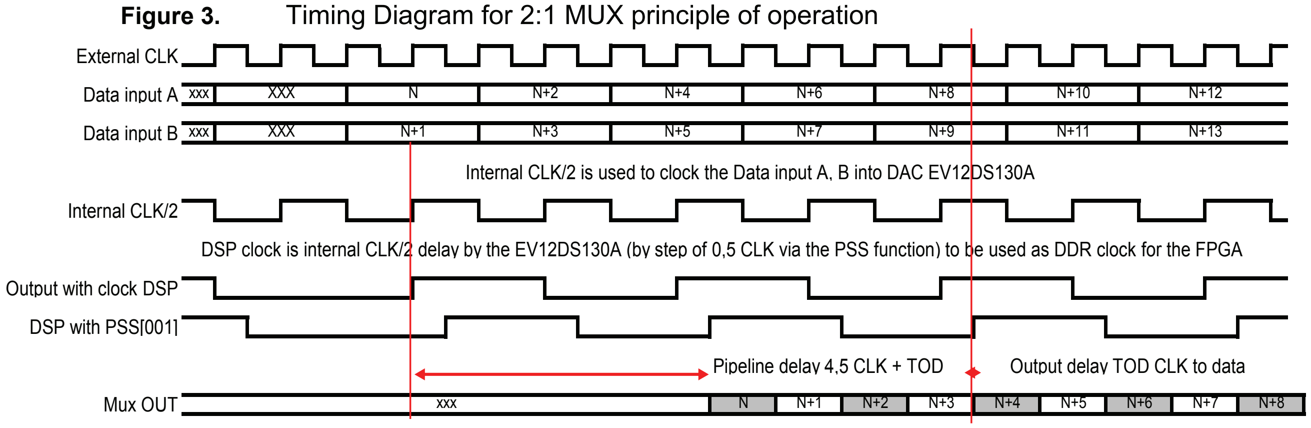
3.6. Timing Information

Figure 2. Timing Diagram for 4:1 MUX principle of operation



Note: OCDS set so that DSP clock frequency is ¼ of master clock

Figure 3. Timing Diagram for 2:1 MUX principle of operation



Note: OCDS set so that DSP clock frequency is ¼ of master clock

3.7. Digital Input Coding Table

Table 8. Coding Table

Digital output msb………..lsb	Differential analog output
000000000000	-500mV
010000000000	-250mV
011000000000	-125mV
100000000000	0mV
101000000000	+125mV
110000000000	+250mV
111111111111	+500mV

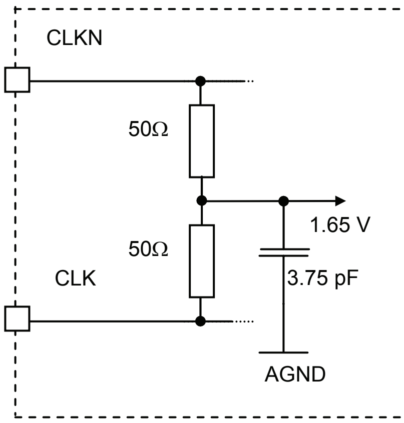
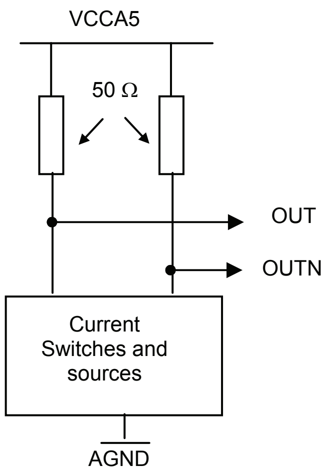
4. PIN DESCRIPTION

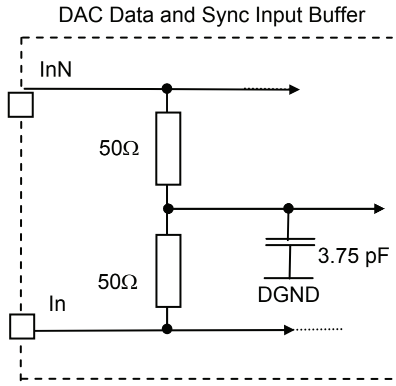
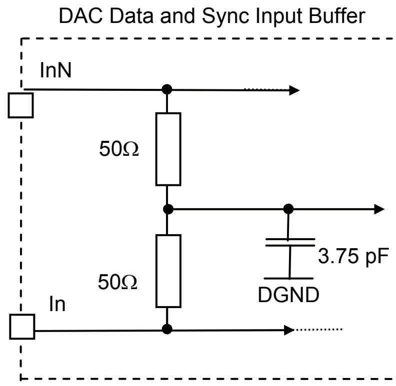
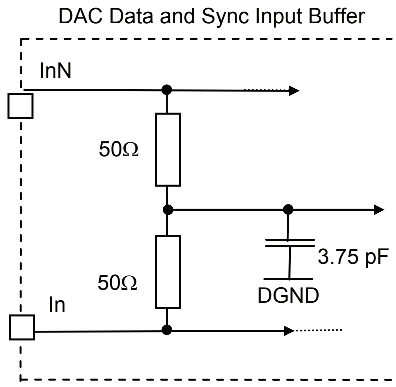
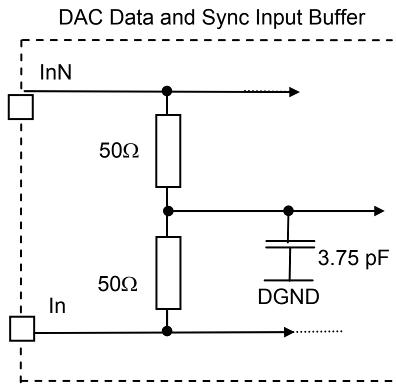
Figure 4. Pinout view fpBGA196 (Top view)

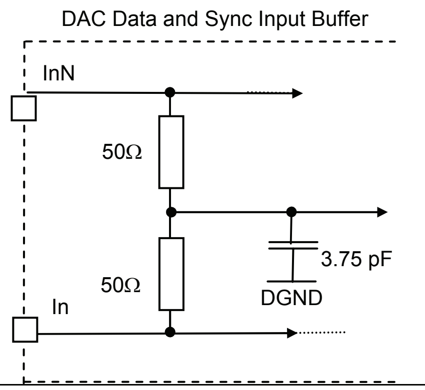
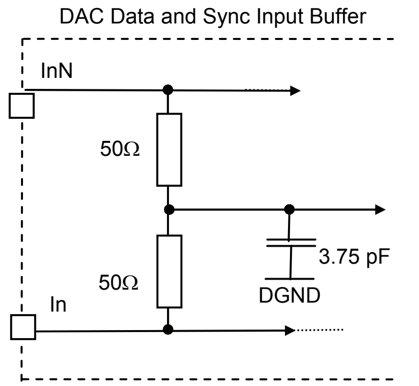
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DGND	B5	B6	B6N	B9	B9N	B11	C11	C9N	C9	C6N	C6	C5	DGND	A
B	B3	B4	B5N	B7	B8	B10	B11N	C11N	C10	C8	C7	C5N	C4	C3	B
C	B1N	B3N	B4N	B7N	B8N	B10N	DGND	DGND	C10N	C8N	C7N	C4N	C3N	C1N	C
D	B1	B2	B2N	DGND	DGND	VCCD	VCCD	VCCD	VCCD	DGND	DGND	C2N	C2	C1	D
E	A10N	B0	B0N	DGND	DGND	VCCD	VCCD	VCCD	VCCD	DGND	DGND	C0N	C0	D10N	E
F	A10	A11	A11N	VCCD	VCCD	AGND	AGND	AGND	AGND	VCCD	VCCD	D11N	D11	D10	F
G	A8	A8N	A9	A9N	DGND	AGND	AGND	AGND	AGND	DGND	D9N	D9	D8N	D8	G
H	A6	A6N	A7	A7N	DGND	AGND	AGND	AGND	AGND	DGND	D7N	D7	D6N	D6	H
J	A3N	A5	A5N	VCCA3	VCCA3	AGND	AGND	AGND	AGND	VCCA3	VCCA3	D5N	D5	D3N	J
K	A3	A4	A4N	DGND	DGND	AGND	VCCA5	VCCA5	AGND	DGND	DGND	D4N	D4	D3	K
L	A1N	A2	A2N	DGND	Diode	VCCA5	VCCA5	VCCA5	VCCA5	DGND	MUX	D2N	D2	D1N	L
M	A1	A0N	GA	HTVF	STVF	VCCA5	VCCA5	AGND	AGND	MODE0	MODE1	PSS2	D0N	D1	M
N	A0	DSPN	IDC_P	SYNCN	CLKN	AGND	AGND	AGND	AGND	AGND	AGND	OCDS1	OCDS0	D0	N
P	DGND	DSP	IDC_N	SYNC	CLK	AGND	AGND	AGND	OUT	OUTN	AGND	PSS0	PSS1	DGND	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Table 9. **Pinout Table fpBGA196**

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
Power supplies				
VCCA5	K7, K8, L6, L7, L8, L9, M6, M7	5V analogue power supplies Referenced to AGND	N/A	
VCCA3	J4, J5, J10, J11	3.3V analogue power supply Referenced to AGND	N/A	
VCCD	D6, D7, D8, D9, E6, E7, E8, E9, F4, F5, F11	3.3V digital power supply Referenced to DGND	N/A	
AGND	F6, F7, F8, F9, G6, G7, G8, G9, H6,	Analogue Ground AGND plane should be	N/A	

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
	H7, H8, H9, J6, J7, J8, J9, K6, K9, M8, M9, N6, N7, N8, N9, N10, N11, P6, P7, P8, P11	separated from DGND on the board (the two planes can be connected by 0 ohm resistors)		
DGND	A1, A14, C7, C8, D4, D5, D10, D11, E4, E5, E10, E11, G5, G10, H5, H10, K4, K5, K10, K11, L4, L10, P1, P14	Digital Ground AGND plane should be separated from DGND on the board (the two planes can be connected by 0 ohm resistors)	N/A	
Clock signals				
CLK CLKN	P5 N5	Master sampling clock input (differential) with internal common mode at 2.65V It should be driven in AC coupling. Equivalent internal differential 100 Ω input resistor.	I	
DSP DSPN	P2 N2	Output clock (in-phase and inverted phase	O	
Analog output signal				
OUT OUTN	P9 P10	In phase and Inverted phase analogue output signal (differential termination required)	O	
Digital Input signals				

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
A0, A0N A1, A1N A2, A2N A3, A3N A4, A4N A5, A5N A6, A6N A7, A7N A8, A8N A9, A9N A10, A10N A11, A11N	N1, M2 M1, L1 L2, L3 K1, J1 K2, K3 J2, J3 H1, H2 H3, H4 G1, G2 G3, G4 F1, E1 F2, F3	Differential Digital input Port A Data A0, A0N is the LSB Data A11, A11N is the MSB	I	
B0, B0N B1, B1N B2, B2N B3, B3N B4, B4N B5, B5N B6, B6N B7, B7N B8, B8N B9, B9N B10, B10N B11, B11N	E2, E3 D1, C1 D2, D3 B1, C2 B2, C3 A2, B3 A3, A4 B4, C4 B5, C5 A5, A6 B6, C6 A7, B7	Differential Digital input Port B Data B0, B0N is the LSB Data B11, B11N is the MSB	I	
C0, C0N C1, C1N C2, C2N C3, C3N C4, C4N C5, C5N C6, C6N C7, C7N C8, C8N C9, C9N C10, C10N C11, C11N	E13, E12 D14, C14 D13, D12 B14, C13 B13, C12 A13, B12 A12, A11 B11, C11 B10, C10 A10, A9 B9, C9 A8, B8	Differential Digital input Port C Data C0, C0N is the LSB Data C11, C11N is the MSB	I	
D0, D0N D1, D1N D2, D2N D3, D3N D4, D4N D5, D5N D6, D6N D7, D7N D8, D8N D9, D9N D10, D10N D11, D11N	N14, M13 M14, L14 L13, L12 K14, J14 K13, K12 J13, J12 H14, H13 H12, H11 G14, G13 G12, G11 F14, E14 F13, F12	Differential Digital input Port D Data D0, D0N is the LSB Data D11, D11N is the MSB	I	
Control signals				
HTVF	M4	Setup time violation flag	O	

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
STVF	M5	Hold time violation flag	O	
IDC_P, IDC_N	N3 P3	Input data check	I	
PSS0 PSS1 PSS2	P12 P13 M12	Phase Shift Select (PSS2 is the MSB)	I	
MODE0 MODE1	M10 M11	DAC Mode selection bits: - RTZ - NRZ - Reshaped mixed RF - Pure RF	I	
MUX	L11	MUX selection: - High ('1') or floating = 2:1 MUX mode - Low ('0') = 4:1 MUX mode	I	
OCDS0 OCDS1	N13 N12	Output Clock Division Select = these bits allow to select the clock division factor applied on the DSP, DSPN signal. - By 2N (OCDS0=0, OCDS1 = 0) - By 2N*2 (OCDS0=1, OCDS1=0) - By 2N*4 (OCDS0=1, OCDS1=0) - By 2N*8 (OCDS0=1, OCDS1=1) With N = MUX ratio	I	
SYNC, SYNCN	P4 N4	In phase and Inverted phase reset signal	I	
GA	M3	Gain adjust	I	
Diode	L5	Diode for die junction temperature monitoring	I	

5. FUNCTIONAL DESCRIPTION

Figure 5. DAC functional diagram

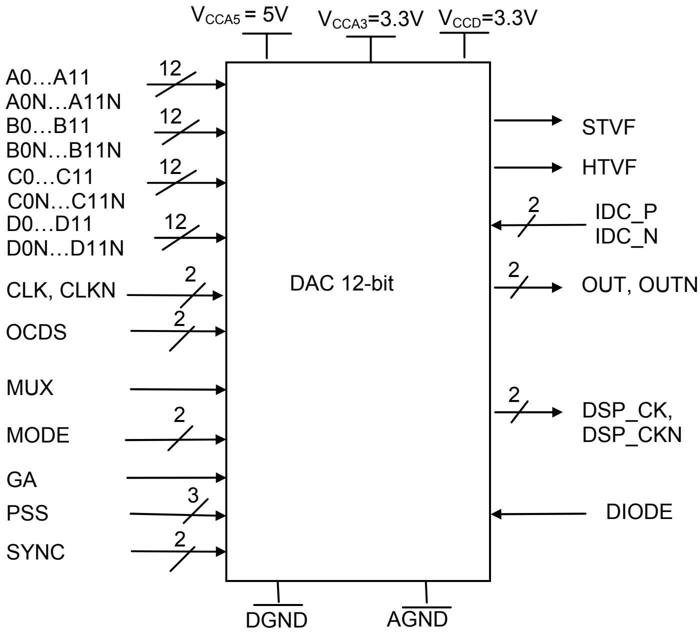


Table 10. **Functions Description**

Name	Function	Name	Function
V_{CCD}	3.3V Digital Power Supply	CLK	In-phase Master clock
V_{CCA5}	5V Analog Power Supply	CLKN	Inverted phase Master clock
V_{CCA3}	3.3V Analog Power Supply	DSP_CK	In-phase Output clock
DGND	Digital Ground	DSP_CKN	Inverted phase Output clock
AGND	Analog ground (for analog supply reference)	PSS[0..2]	Phase shift select
A[11…0]	In-phase digital input Port A	GA	Gain Adjust (+/- 0.5V around V_{CCA5}/2)
A[11..0]N	Inverted phase digital input Port A	MUX	MUX Selection
B[11…0]	In-phase digital input Port B	MODE[0..1]	DAC Mode: Return To Zero, Non Return to Zero, RF
B[11..0]N	Inverted phase digital input Port B	STVF	Setup time Violation flag
C[11…0]	In-phase digital input Port C	HTVF	Hold time Violation flag
C[11..0]N	Inverted phase digital input Port C	IDC_P, IDC_N	Input data check
D[11…0]	In-phase digital input Port D	OCDS[0..1]	Output Clock Division factor Selection (by 4, 8, 16 or 32)
D[11..0]N	Inverted phase digital input Port D	Diode	Diode for temperature monitoring
OUT	In-phase analog output	SYNC/ SYNCN	Synchronization signal (Active High)
OUTN	Inverted phase analog output		

5.1. MUX

Two modes for the MUX ratio are allowed:

- 4:1, which allows operation at full sampling rate (ie. 3 GHz);
- 2:1, which can only be used up to 1.5 GHz sampling rate.

Label	Value	Description	Comments
MUX	0	4:1 mode	Refer to Timing Information
	1	2:1 mode	Refer to Timing Information

In 2:1 MUX ratio, the unused data ports (ports C and D) can be left open.

5.2. MODE function

Label	Value	Description	Default setting
MODE[1:0]	00	NRZ mode	00 NRZ mode
	01	Reshaped NRZ (i.e Narrow RTZ)	
	10	RTZ Mode (50%)	
	11	Reshaped RF mode	

The MODE function allows choosing between NRZ, RTZ and RF functions. NRZ and reshaped NRZ should be chosen for use in 1st Nyquist zone while RTZ should be chosen for use in 2nd and RF for 3rd Nyquist zones.

Figure 6. NRZ, RTZ and RF transfer functions

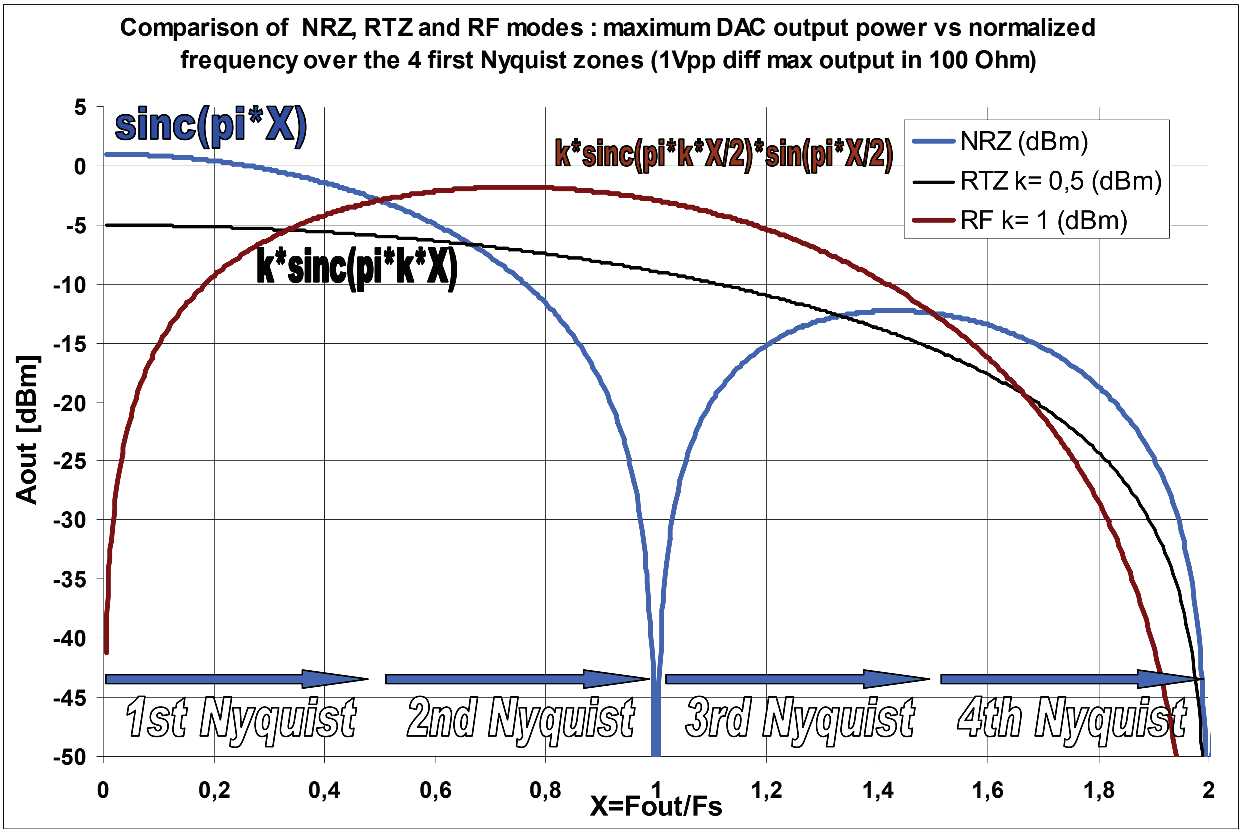
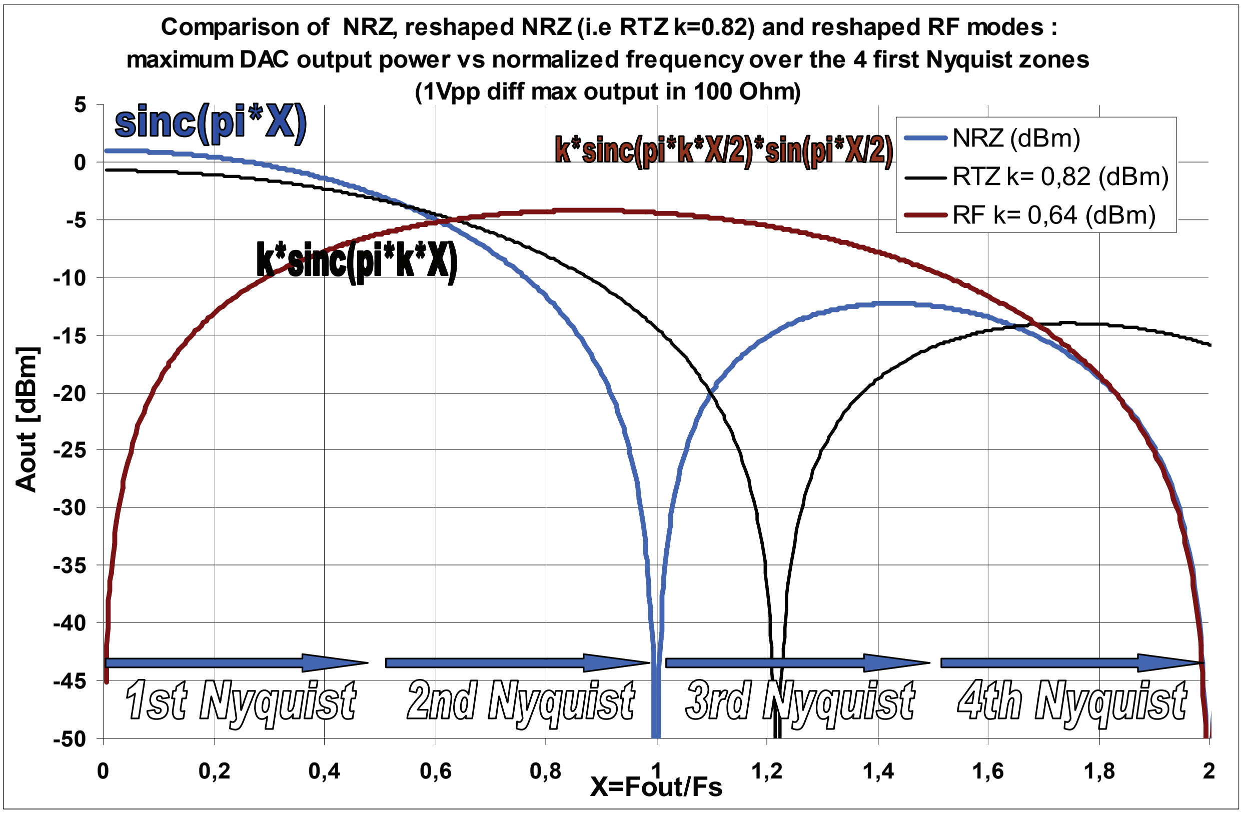


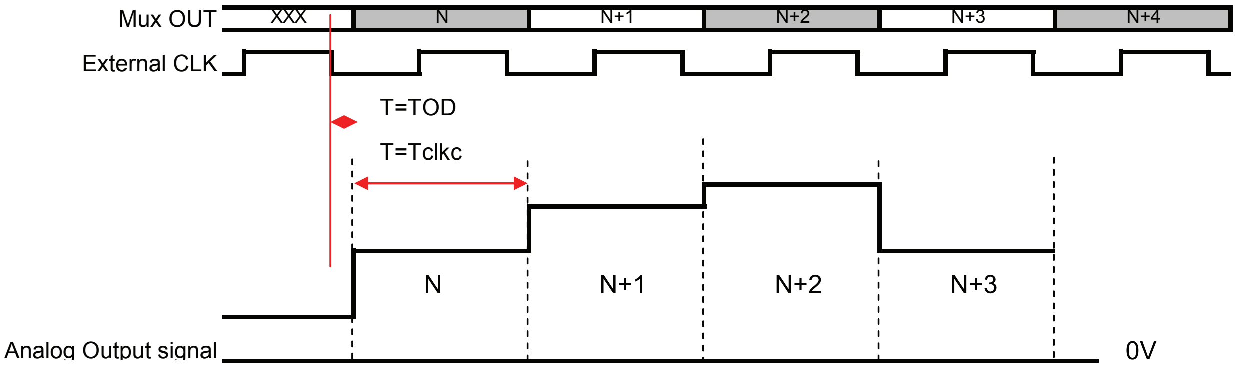
Figure 7. NRZ and reshaped NRZ transfer functions



5.2.1.NRZ architecture

This architecture does not allow for operation in the 2nd Nyquist zone because of the Sinx/x notch. The advantage is that it gives good results in the 1st Nyquist zone (less attenuation than in RTZ architecture), it removes the parasitic spur at the clock frequency (in differential).

Figure 8. NRZ timing diagram

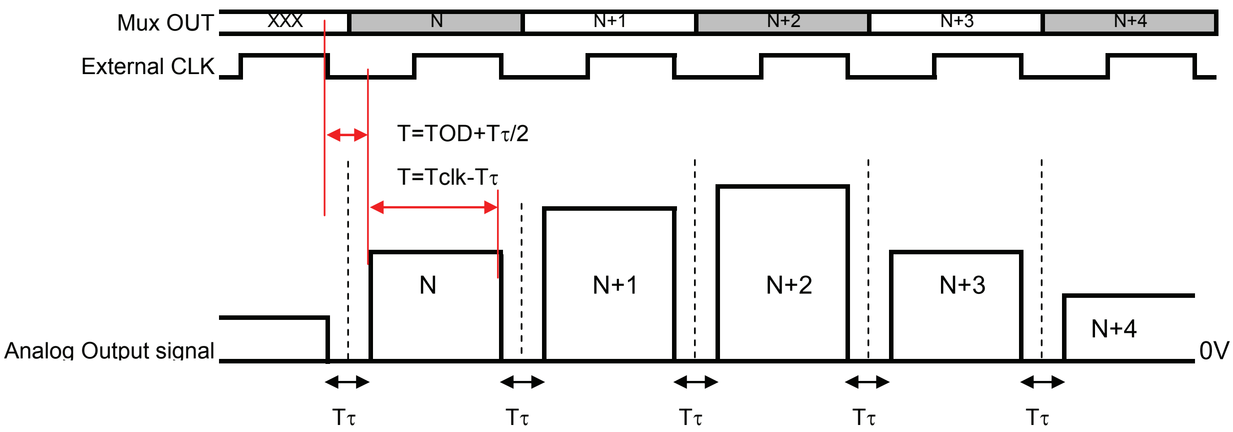


5.2.2.Reshaped NRZ (Narrow RTZ) architecture

This architecture has the following advantages:

- Optimized power in 1st Nyquist zone
- Extended dynamic through elimination of hazardous transitions
- Trade off between NRZ and RTZ

Figure 9. Reshaped NRZ timing diagram



5.2.3.RTZ architecture

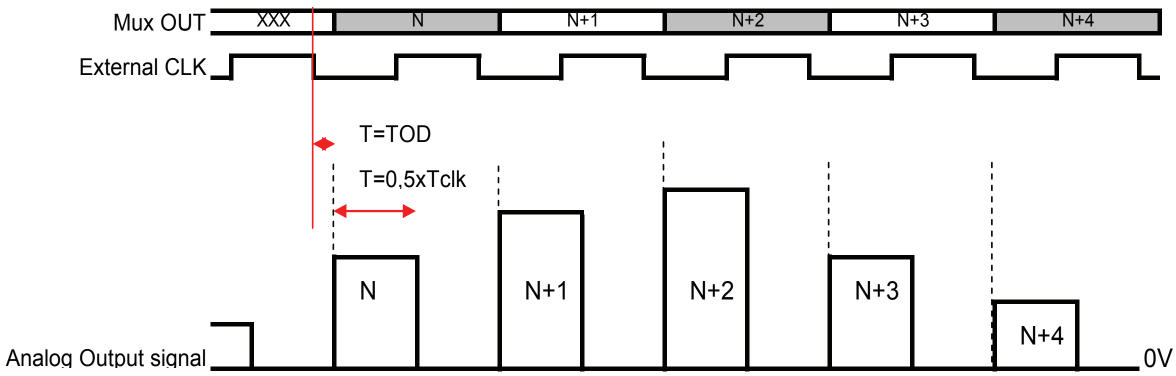
The advantage of the RTZ structure is to enable the operation in the 2nd zone but the drawback is clearly to attenuate more the signal in the first Nyquist zone.
Advantages:

- Extended roll off of sinc
- Extended dynamic through elimination of hazardous transitions

Weakness:

- By construction clock spur at Fs.

Figure 10. RTZ timing diagram

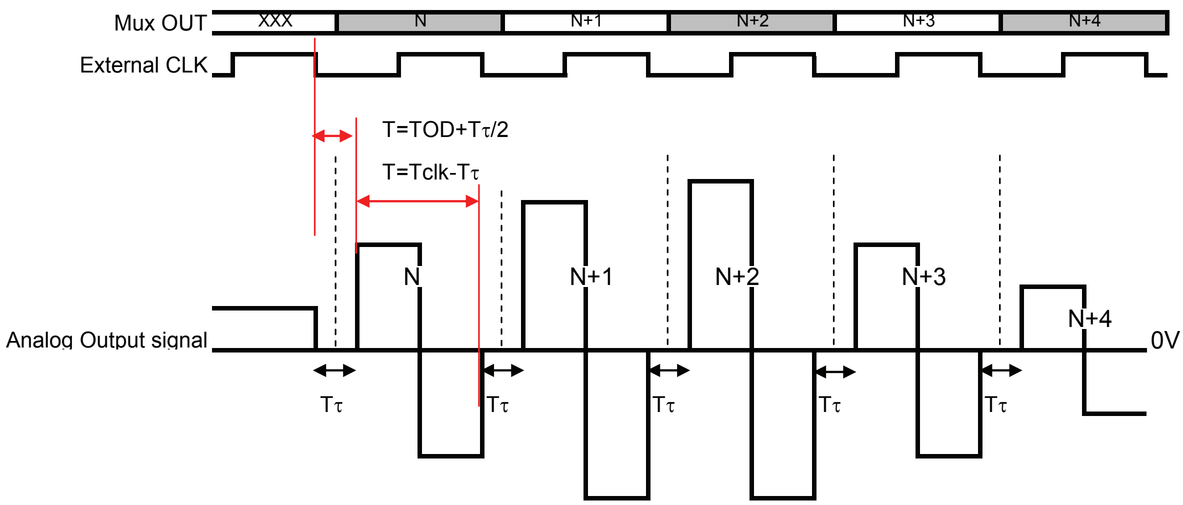


5.2.4.Reshaped RF architecture

RF mode is optimal for operation at high input frequency, since the decay with frequency occurs at higher frequency than for RTZ. Unlike NRZ or RTZ modes, RF modes presents notch DC and 2N*Fs, and minimum attenuation for Fout=Fs.
Advantages:

- Optimized for 2nd and 3rd Nyquist operation
- Extended dynamic range through elimination of hazardous transitions.
- Clock spur pushed to 2.Fs

Figure 11. Reshaped RF timing diagram



NOTE: the central transition is not hazardous but its elimination allows to push clock spur to 2.Fs

5.3. PSS (Phase shift Select function)

It is possible to adjust the timings between the sampling clock and the DSP output clock (which frequency is given by the following formula: Sampling clock / 2NX where N is the MUX ratio, X the output clock division factor).
The DSP clock output phase can be tuned over a range of 3.5 input clock cycles (7 steps of half a clock cycle) in addition to the intrinsic propagation delay between the DSP clock (DSP, DSPN) and the sampling clock (CLK, CLKN).
Three bits are provided for the phase shift function: PSS[2:0].
By setting these 3 bits to 0 or 1, one can add a delay on the DSP clock in order to properly synchronize the input data of the DAC and the sampling clock (the DSP clock should be applied to the FPGA and should be used to clock the DAC digital input data).

Table 11. PSS coding table

Label	Value	Description
PSS[2:0]	000	No additional delay on DSP clock
	001	0.5 input clock cycle delay on DSP clock
	010	1 input clock cycle delay on DSP clock
	011	1.5 input clock cycle delay on DSP clock
	100	2 input clock cycle delay on DSP clock
	101	2.5 input clock cycle delay on DSP clock
	110	3 input clock cycle delay on DSP clock
	111	3.5 input clock cycle delay on DSP clock

In order to determine how much delay needs to be added on the DSP clock to ensure the synchronization between the input data and the sampling clock within the DAC, the HTVF and STVF bits should be monitored. Refer to sections 5.5

Note: In MUX 4:1 mode the 8 settings are relevant, in MUX 2:1 only the four first settings are relevant since the four last setting will yield exactly the same results.

Figure 12. PSS timing diagram for 4:1 MUX

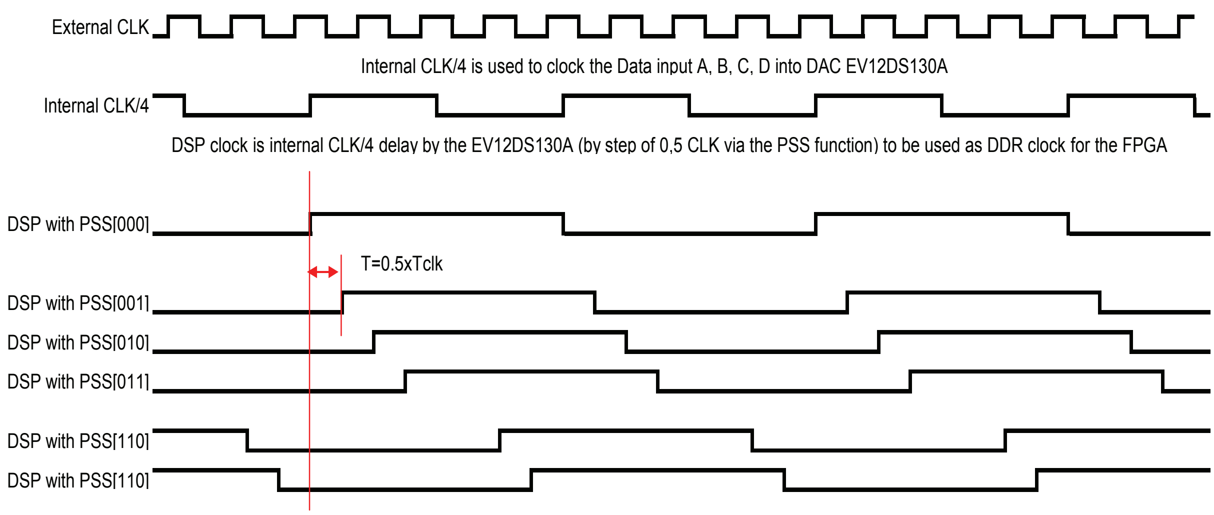
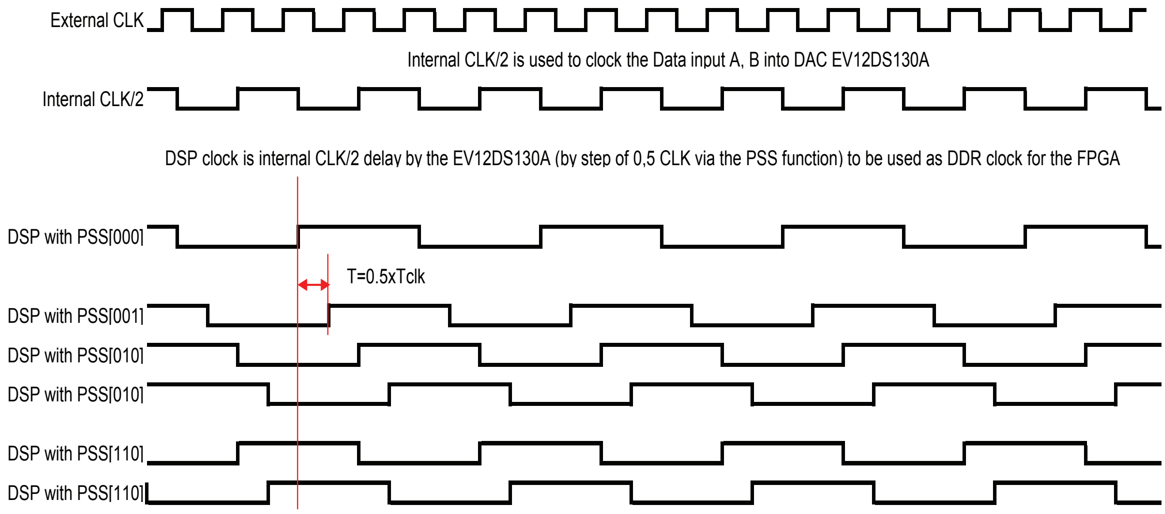


Figure 13. PSS timing diagram for 2:1 MUX



5.4. Output Clock Division Select function OCDS[1:0]

It is possible to change the DSP clock internal division factor from 1 to 2, 4 and 8 with respect to the sampling clock/2N where N is the MUX ratio. This is possible via the OCDS "Output Clock Division Select" bits.

Table 12. OCDS[1:0] coding table

Label	Value	Description
OCDS [1:0]	00	DSP clock frequency is equal to the sampling clock divided by 2N
	01	DSP clock frequency is equal to the sampling clock divided by 2N*2
	10	DSP clock frequency is equal to the sampling clock divided by 2N*4
	11	DSP clock frequency is equal to the sampling clock divided by 2N*8

Figure 14. OCDS timing diagram for 4:1 MUX

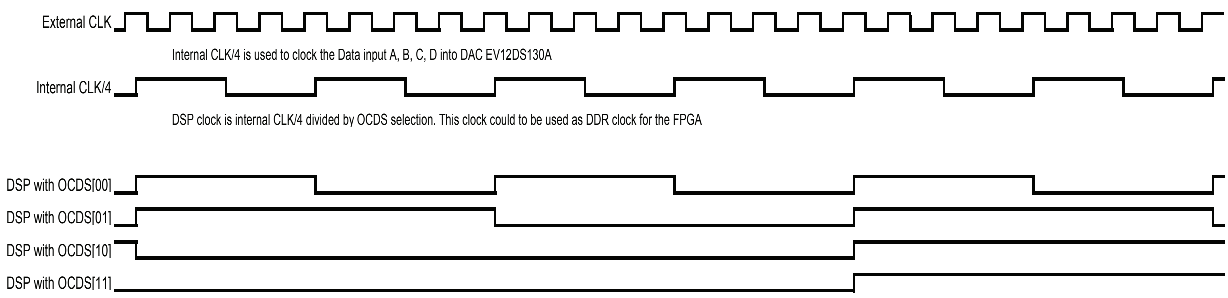
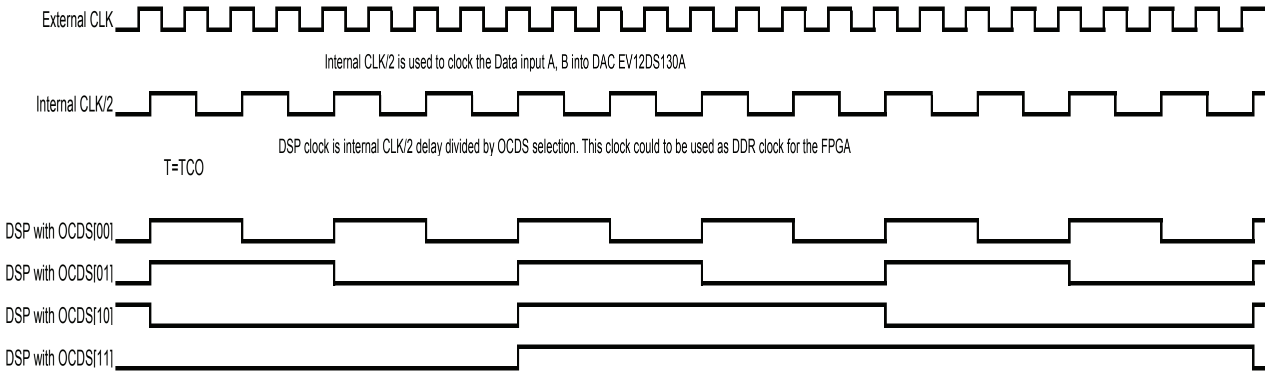


Figure 15. OCDS timing diagram for 4:1 MUX



5.5. Synchronization FPGA-DAC: IDC_P, IDC_N, HTVF and STVF functions

IDC_P, IDC_N: Input Data check function (LVDS signal).
HTVF: Hold Time Violation Flag.
STVF: Setup Time Violation Flag.

The IDC_P, IDC_N signal is an LVDS signal (same buffer as for data on FPGA and on DAC sides). This signal is toggling at each cycle synchronously with other data bits.
This signal should be generated by the FPGA so that the DAC can check in real-time if the timings between the FPGA and the DAC are correct. The information on the timings is then given by HTVF, STVF signals.
When used, it should be routed as the data signals (same layout rules and same length).
It should be driven to an LVDS low or high level if not used.

Figure 16. IDC timing vs data input

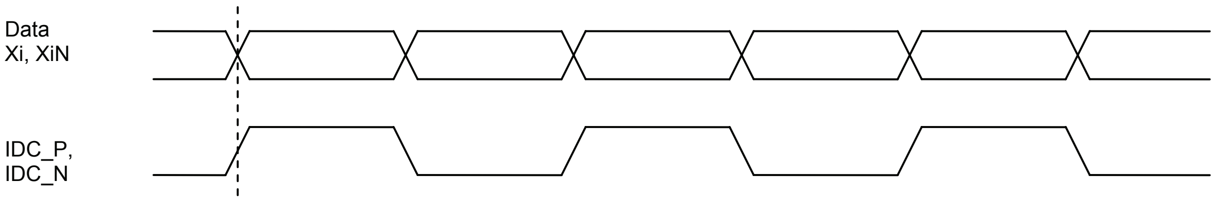
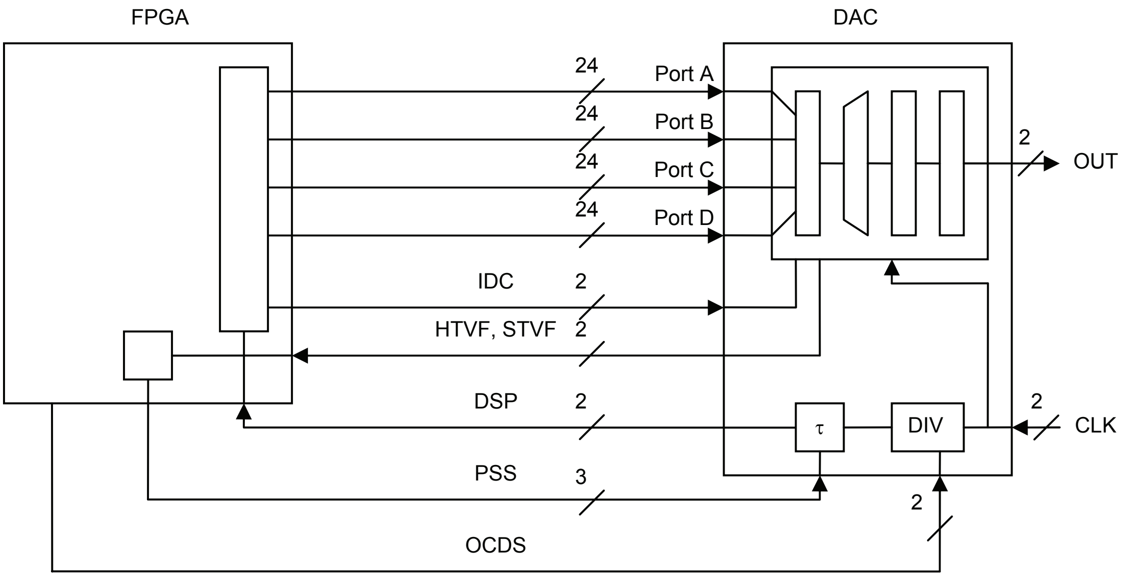


Figure 17. FPGA to DAC synoptic



HTVF and STVF is a CMOS 3.3V output signal, theses signals indicate if the DAC and the FPGA are synchronised.

Table 13. HTVF, STVF coding table

Label	Value	Description
HTVF	0	SYNCHRO OK
	1	Data Hold time violation detected
STVF	0	SYNCHRO OK
	1	Data Setup time violation detected

Note: During Monitoring STVF indicates setup time of data violation (Low➔ OK, High ➔ Violation), HTVF indicates hold time of data violation (Low➔ OK, High ➔ Violation).

Principle of Operation:
The Input Data Check pair (IDC_P, IDC_N) will be sampled three times with half a master clock period shift (the second sample being synchronous with all the data sampling instant), these three samples will be compared, and depending on the results of the comparison a violation may be signalled.

If a violation of setup time ➔ STVF is high level
If a violation of hold time ➔ HTVF is high level

In case of violation of timing (setup or hold) the user has two solutions,

- Shift phase in the FPGA PLL (if this functionality is available in FPGA) for changing the internal timing of DATA and Data Check signal inside FPGA.
- Shift the DSP clock timing (Output clock of the DAC which can be used for FPGA synchronization – refer to sections 5.6 and 5.3), in this case this shift also shift the internal timing of FPGA clock.

5.6. DSP output clock

The DSP output clock DSP, DSPN is an LVDS signal which is used to synchronize the FPGA generating the digital patterns with the DAC sampling clock.
The DSP clock frequency is a fraction of the sampling clock frequency. The division factor depends on OCDS settings. The DSP clock frequency is equal to (sampling frequency / [2N*X]) where N is the MUX ratio and X is the output clock division factor, determined by OCDS[0..1] bits.
For example, in a 4:1 MUX ratio application with a sampling clock of 3 GHz and OCDS set to “00” (ie. Factor of 1), the input data rate is 750 Msps and the DSP clock frequency is 375 MHz.

This DSP clock is used in the FPGA to control the digital data sequencing. Its phase can be adjusted thanks to the PSS[2:0] bits (refer to Section 5.3) in order to ensure a proper synchronization between the data coming to the DAC and the sampling clock.
The HTVF and STVF bits should be used to check whether the timing between the FPGA and the DAC is correct. HTVF and STVF bits will indicate whether the DAC and FPGA are aligned or not. PSS bits should then be used to shift the DSP clock and thus the input data of the DAC, so that a correct timing is achieved between the FPGA and the DAC.

5.7. OCDS, MUX combinations summary

Table 14. OCDS, MUX, PSS combination summary

MUX		OCDS		PSS range	Data rate	Comments
0	4:1	00	DSP clock division factor 8	0 to 7/(2Fs) by 1/(2Fs) steps	Fs/4	Refer to 5.4
0		01	DSP clock division factor 16			
0		10	DSP clock division factor 32			
0		11	DSP clock division factor 64			
1	2:1	00	DSP clock division factor 4	0 to 7/(2Fs) by 1/(2Fs) steps	Fs/2	Refer to 5.4
1		01	DSP clock division factor 8			
1		10	DSP clock division factor 16			
1		11	DSP clock division factor 32			

5.8. Reset function

There are two reset functions integrated in this DAC :

- a power up reset, which is triggered by the power supplies;
- an asynchronous reset (SYNC, SYNCN), which is an external reset and which should ensure the synchronization of multiple DACs.

The external asynchronous reset is LVDS compatible (same buffer as for the digital input data).
It is active high.

Figure 18. Reset timing diagram (4:1 MUX)

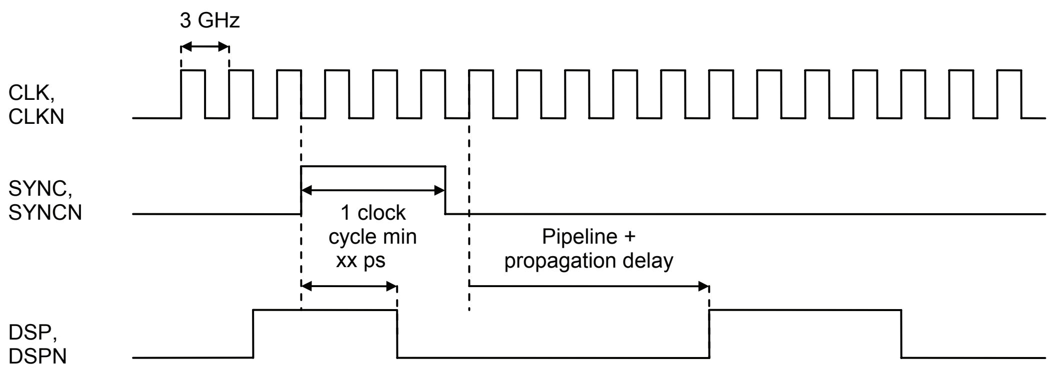
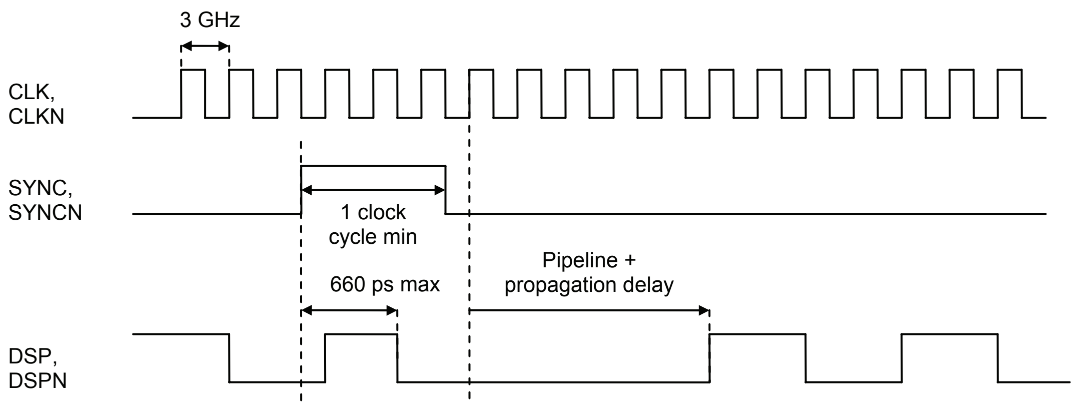


Figure 19. Reset timing diagram (2:1 MUX)



5.9. GA function

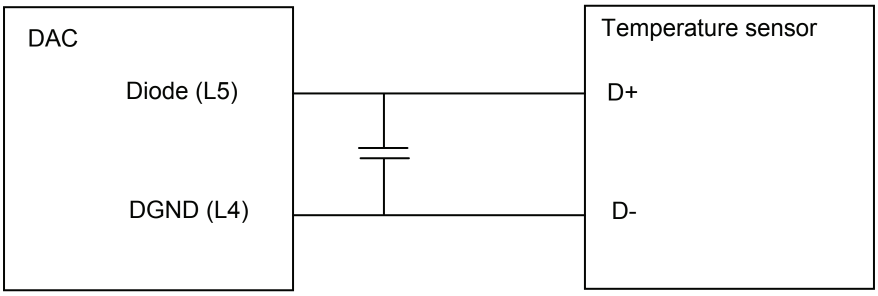
This function allows you to adjust the internal gain of the DAC so that it can be always equal to unity gain.
The gain of the DAC can be adjusted by +/-7% by tuning the voltage applied on GA by ±0.5V around $V_{CCA3}/2$

5.10. Diode function

A diode for die junction temperature monitoring is available in this DAC. It is constituted by an ESD diode. In order to monitor the die junction temperature of the DAC,

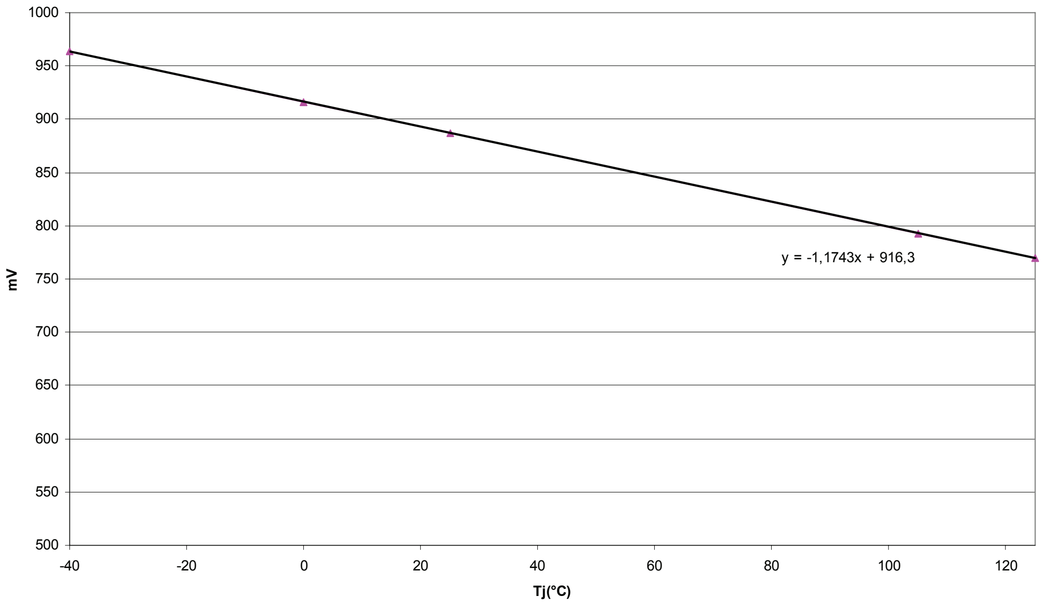
For the measurement of die junction temperature, you could use (temperature sensor).

Figure 20. Temperature DIODE implementation



In characterization a current of 1mA has to be applied on the DIODE pin. The voltage across the DIODE pin (L5) and the DGND pin (L4) provides the junction temperature of the die thanks to the intrinsic diode characteristics provided in Figure 8.

Figure 21. Diode characteristics for Die junction monitoring (to be updated with final silicon version)



6. APPLICATION INFORMATION

6.1. Analogue Output (OUT/OUTN)

The analogue output should be used in differential fashion as described in the figures below.
If the application requires a single-ended analogue output, then a balun is necessary to generate a single-ended signal from the differential output of the DAC.

Figure 22. Analogue output differential termination

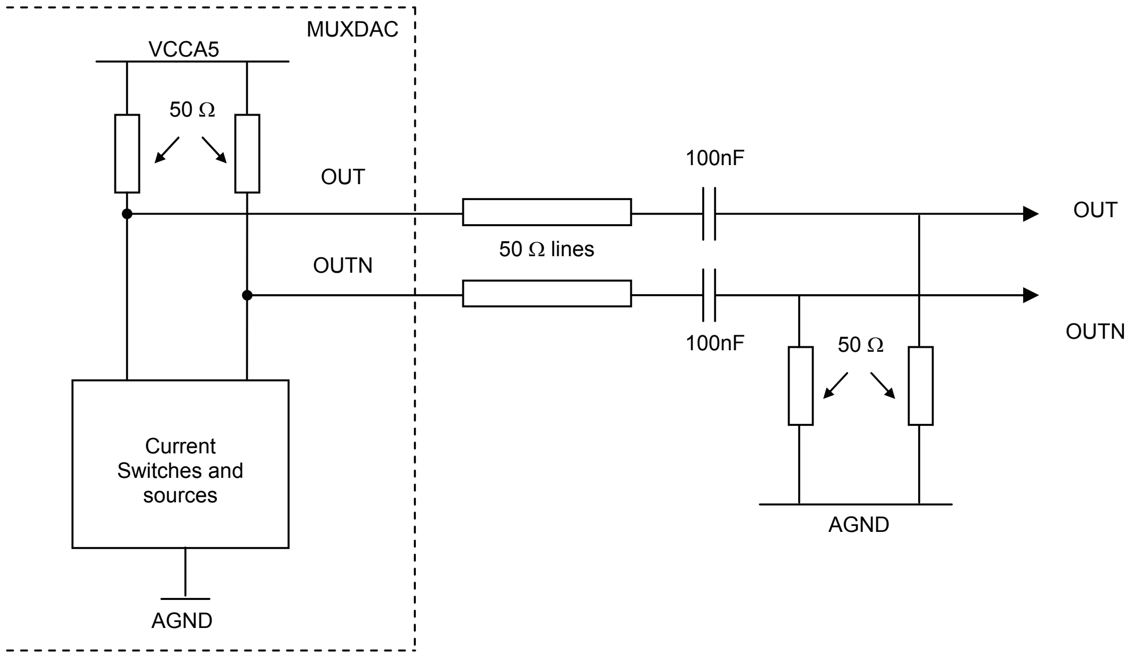
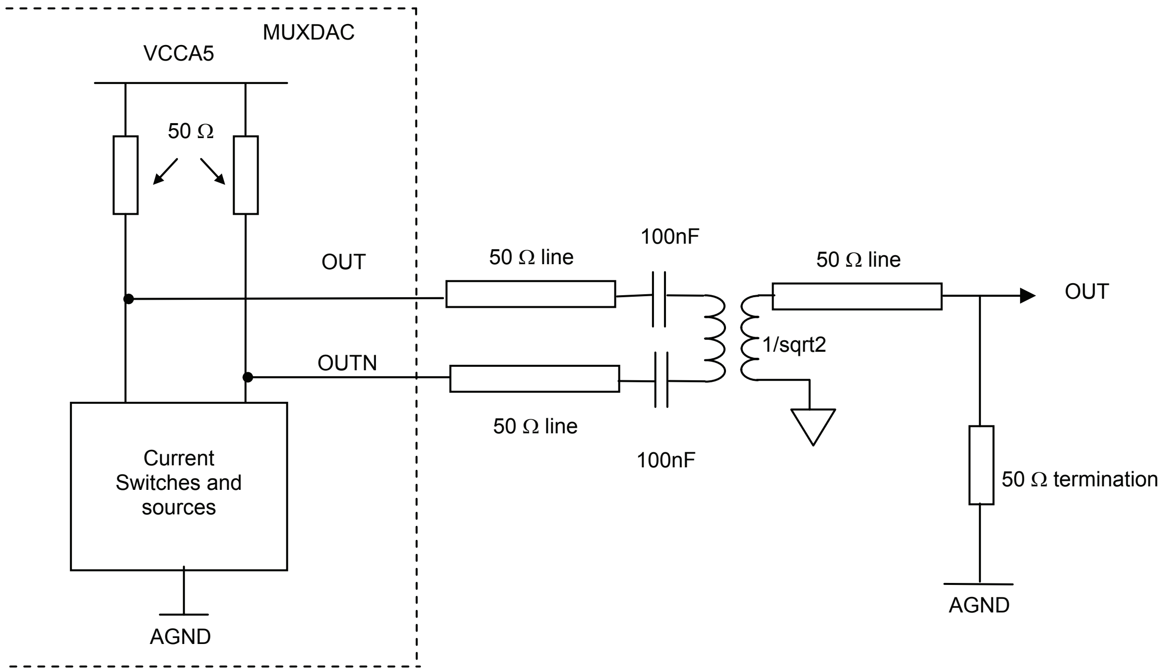


Figure 23. Analogue output using a 1/√2 a balun

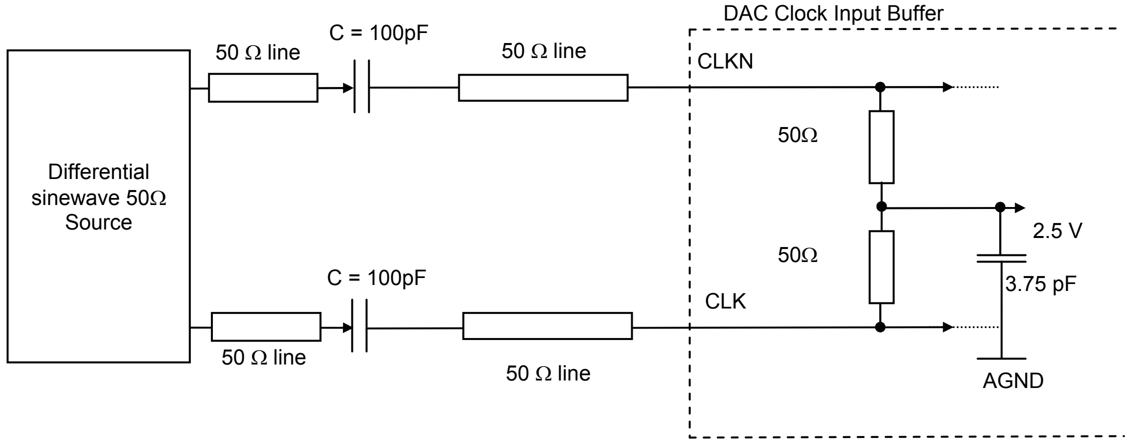


Note: The AC coupling capacitors should be chosen as broadband capacitors with a value depending on the application.

6.2. Clock Input (CLK/CLKN)

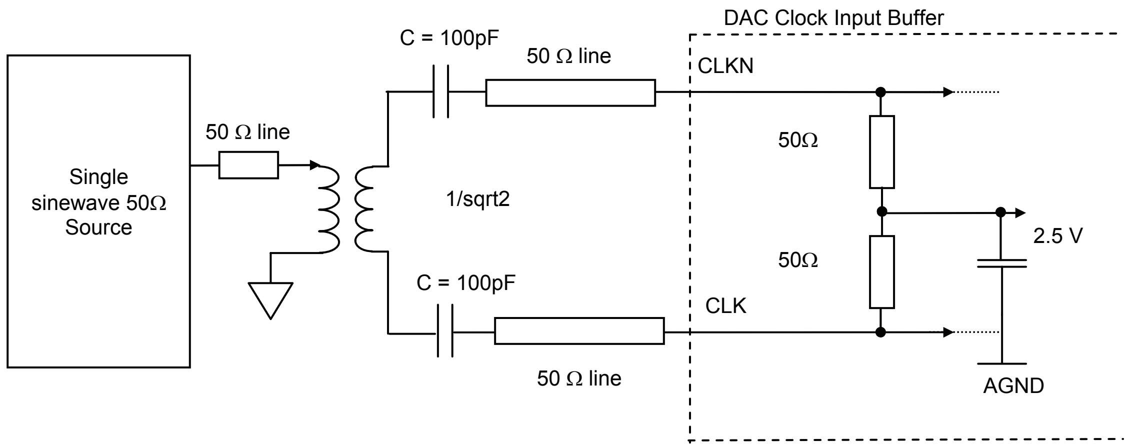
The DAC input clock (sampling clock) should be entered in differential mode as described in Figure 12.

Figure 24. Clock input differential termination



Note: The buffer is internally pre-polarized to 2.5V (buffer between VCC5 and AGND).

Figure 25. Clock input differential with Balun

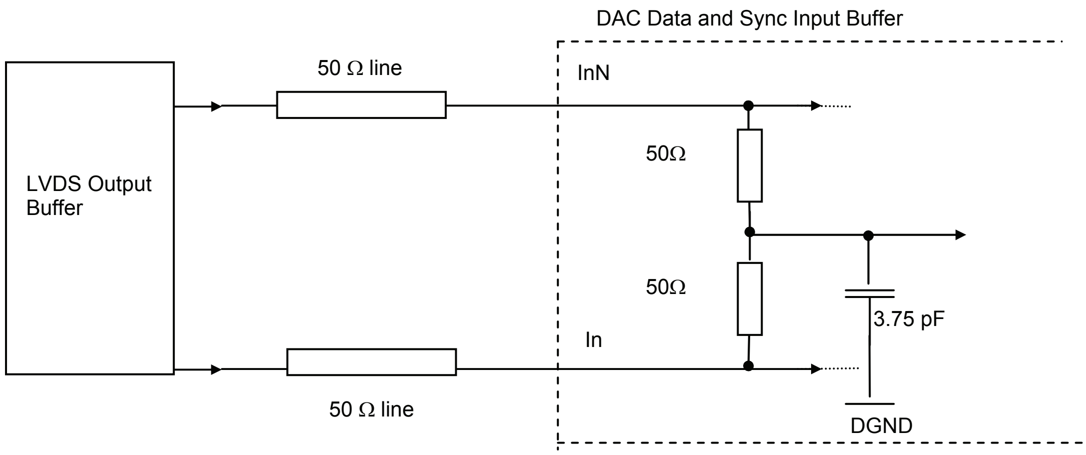


Note: The AC coupling capacitors should be chosen as broadband capacitors with a value depending on the application.

6.3. Digital Data, SYNC and IDC Inputs

LVDS buffers are used for the digital input data, the reset signal (active low) and IDC signal.
They are all internally terminated by 2 x 50Ω to ground via a 3.75 pF capacitor.

Figure 26. Digital data, Reset and IDC input differential termination

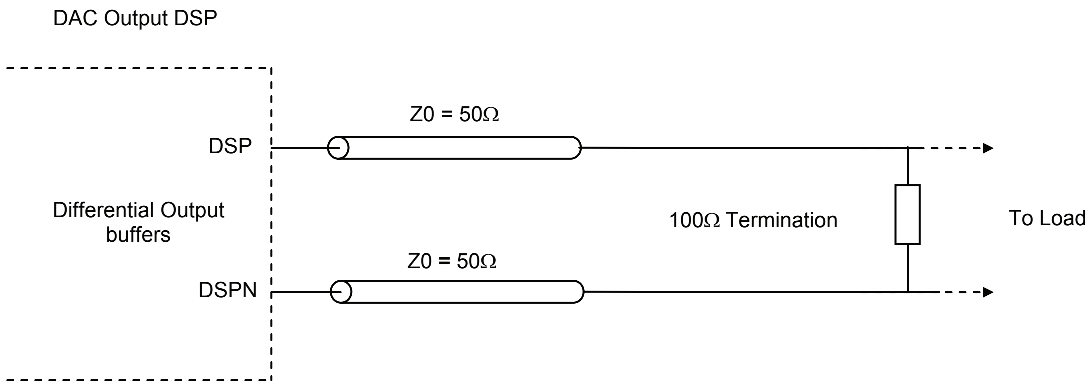


Notes: 1. In the case when only two ports are used (2:1 MUX ratio), then the unused data should be left open (no connect).
2. Data and IDC signals should be routed on board with the same layout rules and the same length.

6.4. DSP clock

The DSP, DSPN output clock signals are LVDS compatible.
They have to be terminated via a differential 100 Ω termination as described in Figure 14.

Figure 27. DSP output differential termination

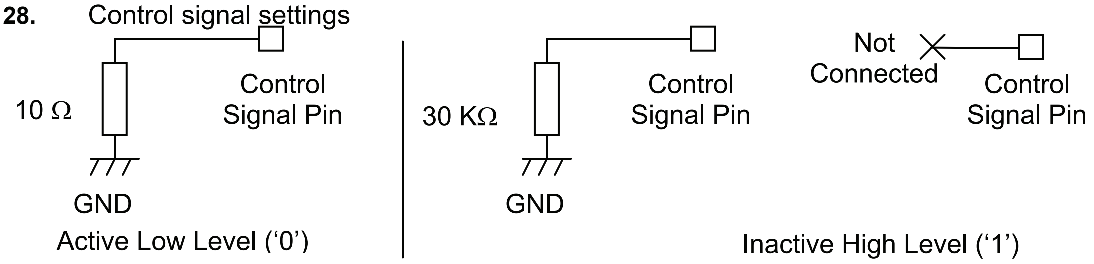


6.5. Control signal settings

The MUX, MODE, PSS and OCDS control signals use the same static input buffer.

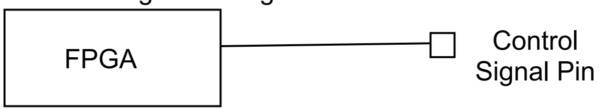
Logic "1" = 30 KΩ to Ground, or tied to V_{CCD} = 3.3V or left open
Logic "0" = 10 Ω to Ground or Grounded

Figure 28. Control signal settings



The control signal could be driven by FPGA.

Figure 29. Control signal settings with FPGA

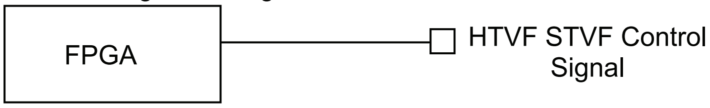


Logic "1" > VIH or VCCD = 3.3V
Logic "0" < VIL or 0V

6.6. HTVF and STVF Control signal

The HTVF and STVF control signals is a output 3.3V CMOS buffer.
These signals could be acquite by FPGA.

Figure 30. Control signal settings with FPGA

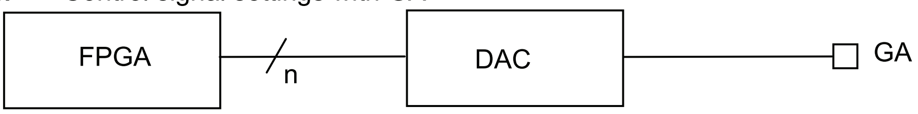


6.7. GA function Signal

This function allows you to adjust the internal gain of the DAC
The gain of the DAC can be tuning with applied analog voltage by ±0.5V around $V_{CCA3}/2$

This analog input signal could be generated by a DAC control by FPGA or microcontroller.

Figure 31. Control signal settings with GA

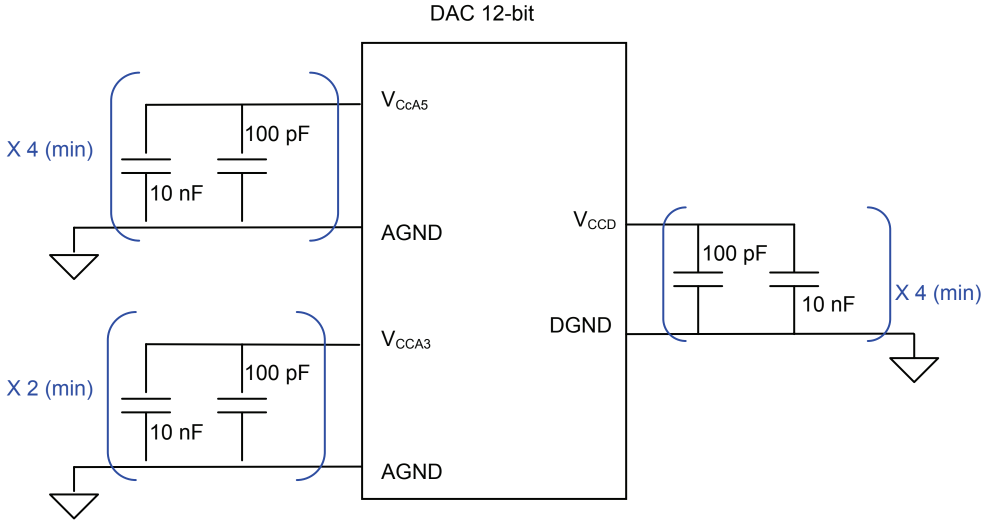


6.8. Power supplies decoupling and bypassing

The DAC requires 3 distinct power supplies:
V_{CCA5} = 5V (for the analogue core)
V_{CCA3} = 3.3V (for the analogue part)
V_{CCD} = 3.3V (for the digital part)

It is recommended to decouple all power supplies to ground as close as possible to the device balls with 100 pF in parallel to 10nF capacitors. The minimum number of decoupling pairs of capacitors can be calculated as the minimum number of groups of neighboring pins.
4 pairs of 100pF in parallel to 10 nF capacitors are required for the decoupling of V_{CCA5}. 4 pairs for the V_{CCA3} is the minimum required and finally, 10 pairs are necessary for V_{CCD}.

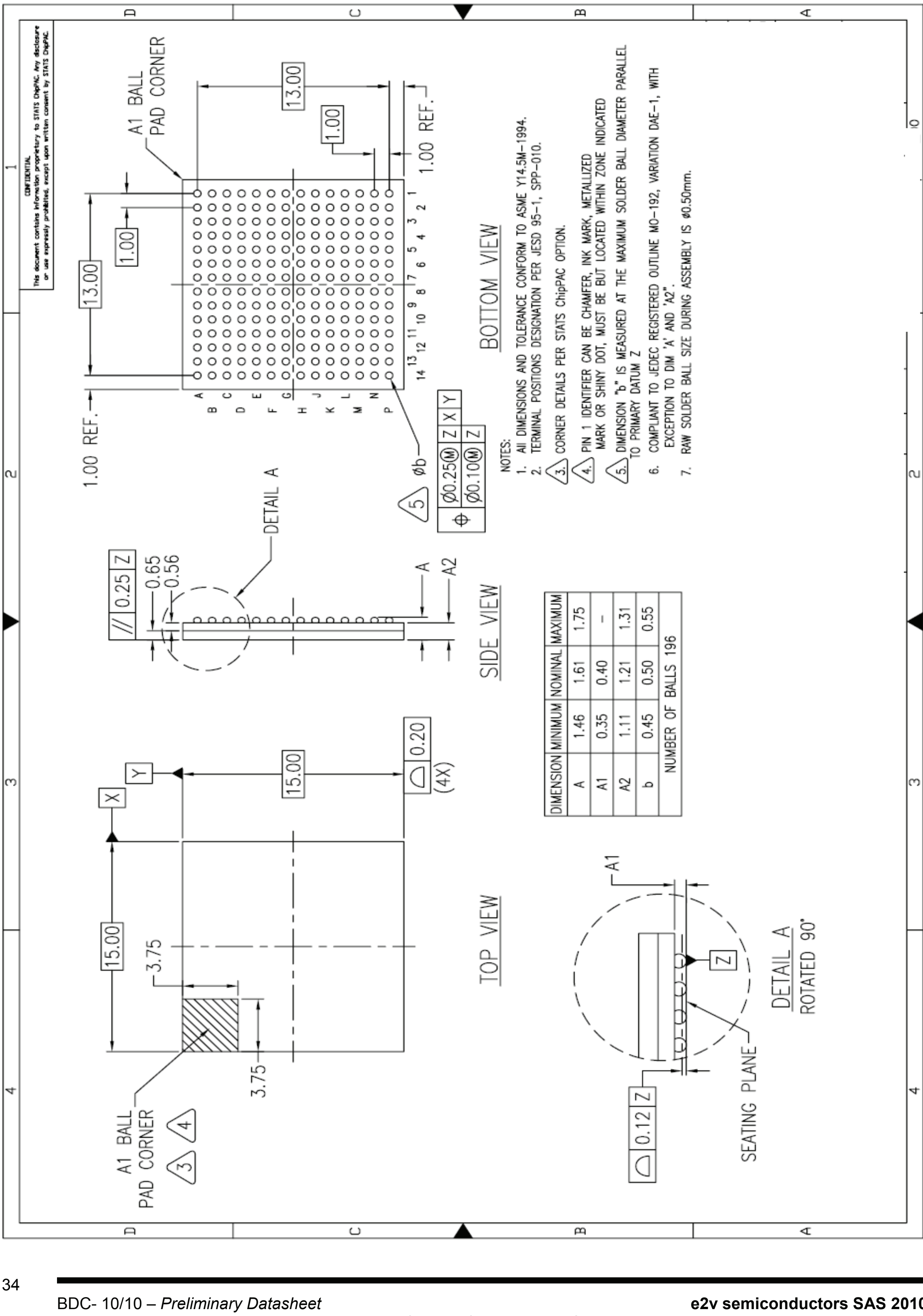
Figure 32. Power supplies decoupling scheme



Each power supply has to be bypassed as close as possible to its source or access by 100 nF in parallel to 22µF capacitors (value depending of DC/DC regulators).

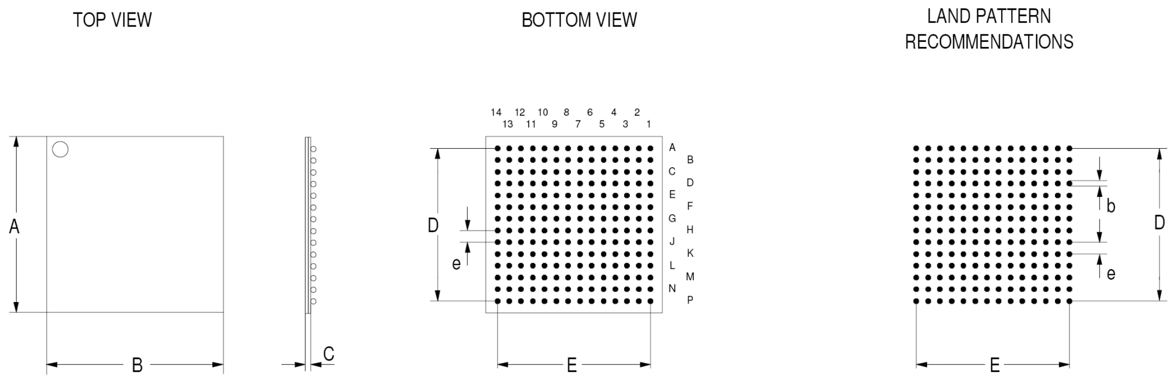
7. PACKAGE INFORMATION

7.1. fpBGA 196 outline



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	1.46	1.61	1.75
A1	0.35	0.40	-
A2	1.11	1.21	1.31
b	0.45	0.50	0.55
NUMBER OF BALLS 196			

7.2. Land Pattern Recommendation



A	B	C	D	E	e	b
15.00	15.00	1.21	13.00	13.00	1.00	0.45

7.3. Thermal characteristics fpBGA196

7.3.1. Thermal resistance

Assumptions:

Still air
Pure conduction
No radiation
Heating zone = 5% of die surface

Rth Junction -bottom of Balls = 13.6°C/W
Rth Junction - board (JEDEC JESD-51-8) = 18.4°C/W
Rth Junction -top of case = 17.0°C/W

Assumptions:

Heating zone = 5% of die surface
Still air, Jedec condition

Rth Junction - ambient (JEDEC) = 32.3 °C/W

7.3.2. Hot spots

Max hot spot above average is # 8°C either in condition Tref = 0°C at bottom of ball or Tref =Tair = 0°C when mounted on a JEDEC board.

Max hot spot is located in DAC_element_MSB.

Diode will measure a temperature that is 3°C lower than this value.

- For an air temperature of 85°C in industrial range (still air), maximum temperature on chip will be T = 85°C + 35.02°C # 120 °C, that is below the 125 °C maximum allowable for the chip.

- For an air temperature of 90°C (still air), maximum temperature on chip will be T = 90°C + 35.02°C # 125 °C which is maximum allowable for the chip.

- For an air temperature > 90°C an air flow must be applied, or an external heatsink must be used.

8. ORDERING INFORMATION

Table 15. Ordering information

Part Number	Package	Temperature Range	Screening Level	Comments
EVX12DS130AZPY	fpBGA196 RoHS	Ambient	Prototype	
EV12DS130ACZPY	fpBGA196 RoHS	0°C <Tc, Tj< 90°C	Commercial « C » Grade	
EV12DS130AVZPY	fpBGA196 RoHS	-40°C <Tc, Tj < 110°C	Industrial « V » Grade	
EV12DS130AZPY-EB	fpBGA196 RoHS	Ambient	Prototype	Evaluation board

Table Of Contents