EV12DS130AGS
Low Power 12-bit 3 GSps DAC with 4/2:1 MUX

Datasheet

Main Features

- **12-bit Resolution**
- **3 GSps Guaranteed Conversion Rate**
- **6 GHz Analog Output Bandwidth**
- **60 ps Full Scale Rise Time**
- **4:1 or 2:1 integrated Parallel MUX (Selectable)**
- **Selectable Output Modes :**
  Return to Zero, Non Return to Zero, Narrow Return to Zero, RF
- **Low Latency Time: 3.5 Clock Cycle.**
- **1.3 Watt Power Dissipation**
- **Functions**
  - **Selectable MUX Ratio 4:1 (Full Speed), 2:1 (Half Speed)**
  - **Triple Majority Voting**
  - **User-friendly Functions:**
    - **Gain Adjustment**
    - **Input Data Check Bit (IDC_P, IDC_N) for Timing with FPGA Check**
    - **Setup Time and Hold Time Violation Flags (STVF, HTVF)**
    - **Clock Phase Shift Select for Synchronization with DSP (PSS[2:0])**
    - **Output Clock Division Selection (Possibility to Change the Division Ratio of the DSP Clock)**
    - **Input Under Clocking Mode**
    - **Diode for Die junction Temperature Monitoring**
- **LVDS Differential Data input and DSP Clock Output**
- **Analog Output Swing: 1Vpp Differential (100Ω Differential Impedance)**
- **Power up Reset**
- **External Reset for Synchronization of Multiple MuxDACs**
- **Power Supplies : 3.3 V (Digital), 3.3V & 5V (Analogue)**
- **Ci-CGA255 Package (21 x 21 mm Body Size, 1.27 mm Pitch)**

Performances

Broadband: NPR at –14 dB Loading Factor, (See Section 6.2.7 "NPR Performances" on page 65)

1st Nyquist (NRTZ):	**NPR = 50.2 dB**	**9.9 Bit equivalent at Fs = 3 GSps**
1st Nyquist (NRTZ):	**NPR = 55.7 dB**	**10.8 Bit equivalent at Fs = 1.5 GSps**
2nd Nyquist (NRTZ or RTZ):	**NPR = 44.0 dB**	**8.8 Bit equivalent at Fs = 3 GSps**
3rd Nyquist (RF):	**NPR = 42.0 dB**	**8.5 Bit Equivalent at Fs = 3 GSps**

Single Tone: (see Section 4. "Functional Description" on page 14)

- **Performances Characterized for Fout from 100 MHz to 4500 MHz and from 2 GSps to 3.2 GSps.**
- **Performance Industrially Screened Over 3 Nyquist Zones at 3 GSps for Selected Fout.**

Step Response

- **Full Scale Rise /Fall Time < 60 ps**

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Applications

- **Direct Digital Synthesis for Broadband Applications (L-S and Lower C Band)**
- **Automatic Test Equipment (ATE)**
- **Arbitrary Waveform Generators**
- **Satellite up-conversion Sub-systems**
- **Radar Waveform Signal Synthesis**
- **DOCSIS V3.0 Systems**

1. Block Diagram

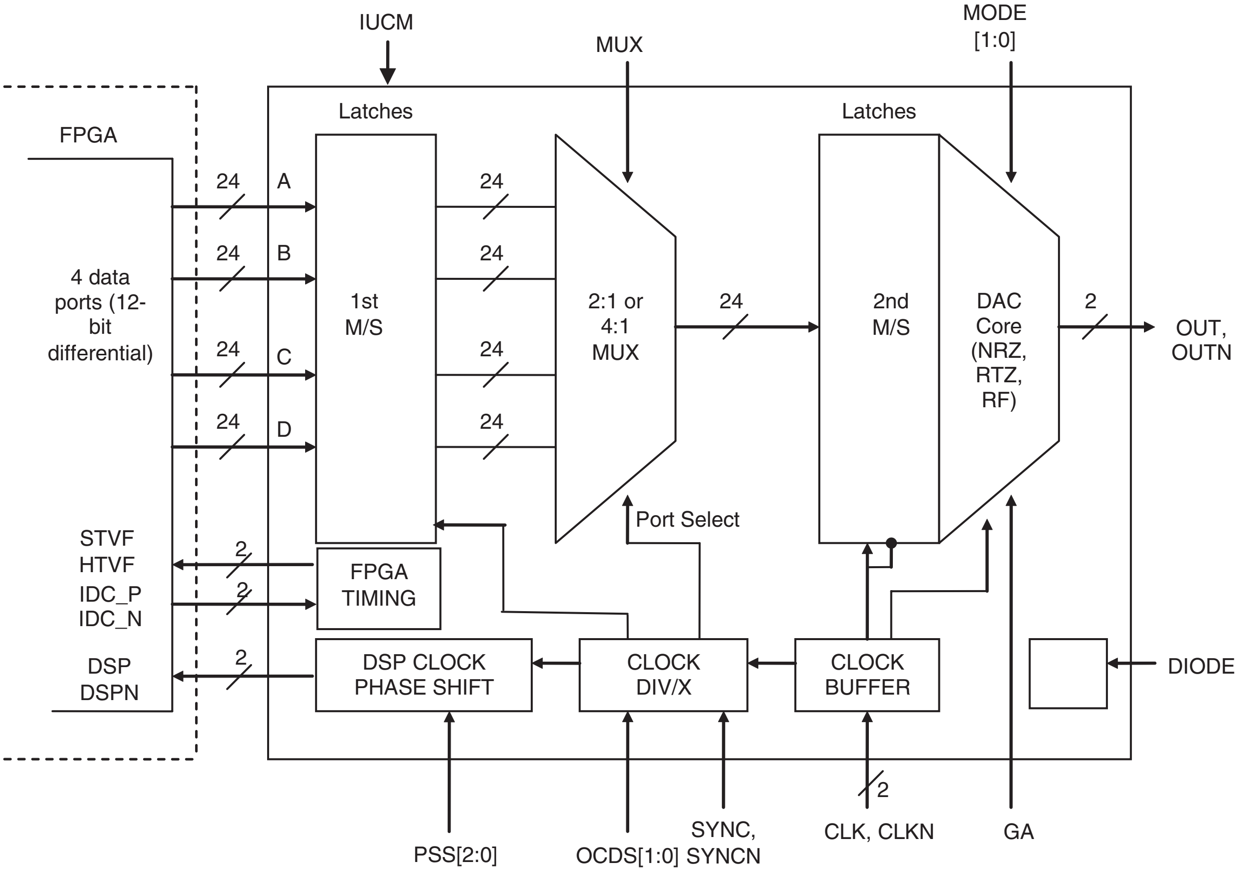


Figure 1-1. Simplified Block Diagram

2. Description

The EV12DS130A is a 12-bit 3 GSps DAC with an integrated 4:1 or 2:1 multiplexer, allowing easy interface with standard LVDS FPGAs thanks to user friendly features as OCDS, PSS.

It embeds different output modes (RTZ, NRZ, narrow RTZ, RF) that allows performances optimizations depending on the working Nyquist zone.

The Noise Power Ratio (NPR) performance, which is 9.7 Bit equivalent at 3 GSps, over more than 900 MHz instantaneous bandwidth, and the 70 dB linearity (SFDR, IMD) over full 1st Nyquist zone at 3 GSps (NRZ feature), makes this product well suited for in high-end applications such as arbitrary waveform generators and broadband DDS systems.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Positive Analogue supply voltage	V_{CCA5}	6	V
Positive Analogue supply voltage	V_{CCA3}	3.6	V
Positive Digital supply voltage	V_{CCD}	3.6	V
Digital inputs (on each single-ended input) and IDC, SYNC, SYNCN, signal Port P = A, B, C, D V_{IL} V_{IH} Swing	[P0..P11], [P0N…P11N] IDC_P, IDC_N	0.8 1.625 800	V V mV
Master clock input V_{IL} V_{IH} Swing	CLK, CLKN	1.5 3.5 2.45	V V Vpp
Master clock input power level (single-ended mode)	P_{CLK}	12	dBm
Control functions inputs V_{IL} V_{IH}	MUX, IUCM, MODE[0..1], PSS[0..2], OCDS[0..1]	–0.4V V_{CCD} + 0.4	V V
Gain Adjustment function	GA	–0.3V, V_{CCA3} +0.3	V
Junction Temperature	Tj	150°C	°C
Storage Temperature	Tstg	–65 to 150	°C

Notes:
1. Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
2. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.
3. Maximum ratings enable active inputs with DAC powered off.
4. Maximum ratings enable floating inputs with DAC powered on.
5. DSP clock and STVF, HTVF output buffers must not be shorted to ground nor positive power supply.

3.2 Recommended Conditions of Use

Table 3-2. **Recommended Conditions of Use**

Parameter	Symbol	Comments	Recommended Value	Unit	Note
Positive analogue supply voltage	V_{CCA5}		5.0	V	(2)
Positive analogue supply voltage	V_{CCA3}		3.3	V	(1)(2)
Positive digital supply voltage	V_{CCD}		3.3	V	(2)
Digital inputs (on each single-ended input) and IDC, SYNC signals V_{IL} V_{IH} Swing	A0..A11, A0N..A11N B0..B11, B0N..B11N C0..C11, C0N..C11N D0..D11, D0N..D11N IDC_P, IDC_N		 1.075 1.425 350		
Master clock input	CLK, CLKN		1.2	Vpp	
Master clock input power level Differential mode	P_{CLK}		3	dBm	
Control functions inputs	IUCM, MUX, OCDS, PSS, MODE, PSS	V_{IL} V_{IH}	0 V_{CCD}	V V	
Gain Adjustment function	GA	Range	0 V_{CCA3}	V	
Operating Temperature Range	Tc = Tcase Tj = T junction	Military "M" & space grade	–55°C < Tc, Tj < 125°C –55°C < Tc, Tj < 125°C	°C	

Notes:
1. For low temperature it is recommended to operate at maximum analog supplies (V_{CCA3}) level
2. Power up sequencing: In order to optimize the performance, it is recommended to follow the power up sequence with a wait of 10 ms in between : V_{CCD} => V_{CCA3} => V_{CCA5}.

Analog output is in differential. Single-ended operation is not recommended. Optimum performance is only in differential configuration.

3.3 Electrical Characteristics

Values in the tables below are based on our conditions of measurement and valid over temperature range respectively for M, and Space quality level and for typical power supplies (V_{CCA5} = 5V, V_{CCA3} = 3.3V, V_{CCD} = 3.3V), typical swing, unless specified and in MUX4:1 mode.

Table 3-3. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test Level(2)
RESOLUTION		12			bit		1,6
ESD CLASSIFICATION			Class 1B				
POWER REQUIREMENTS							
Power Supply voltage							
- Analogue	V_{CCA5}	4.75	5	5.25	V		1,6
- Analogue	V_{CCA3}	3.15	3.3	3.45	V		
- Digital	V_{CCD}	3.15	3.3	3.45			
Power Supply current (4:1 MUX)							
- Analogue	I_{CCA5}		84	92	mA		1,6
- Analogue	I_{CCA3}		106	125	mA		
- Digital	I_{CCD}		187	210	mA		
Power Supply current (2:1 MUX)							
- Analogue	I_{CCA5}		84	92	mA		1,6
- Analogue	I_{CCA3}		106	125	mA		
- Digital	I_{CCD}		160	180	mA		
Power dissipation (4:1 MUX)	PD		1.4	1.6	W		1,6
Power dissipation (2:1 DMUX)	PD		1.3	1.5	W		1,6
DIGITAL DATA INPUTS, SYNC and IDC INPUTS							
Logic compatibility		LVDS					
Digital input voltages:							
- Differential input voltage	V_{ID}	100	350	500	mVpp		1,6
- Common mode	V_{ICM}		1.25		V		1,6
Input capacitance from each single input to ground				2	pF		5
Differential Input resistance		80	100	120	Ω		1,6
CLOCK INPUTS							
Input voltages (Differential operation swing)		0.56	1	2.24	Vpp		4
Power level (Differential operation)		–4	1	8	dBm		4
Common mode		2.4	2.49	2.6	V		
Input capacitance from each single input to ground (at die level)				2	pF		5
Differential Input resistance:		80	100	120	Ω		1,6
DSP CLOCK OUTPUT							
Logic compatibility		LVDS					
Digital output voltages:							

Table 3-3. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test Level[2]
- Differential output voltage - Common mode	V_{OD} V_{OCM}	240	350 1.30	450	mV V		1,6
ANALOG OUTPUT							
Full-scale Differential output voltage (100Ω differentially terminated)		0.92	1	1.08	Vpp		1,6
Full-scale output power (differential output)		0.25	1	1.6	dBm		1,6
Single-ended mid-scale output voltage (50Ω terminated)			V_{CCA5} – 0.43		V	(4)	
Output capacitance				1.5	pF		5
Output internal differential resistance		90	100	110	Ω		5
Output VSWR (using e2v evaluation board) 1.5 GHz 3 GHz 4.5 GHz			1.17 1.54 1.64				4
Output bandwidth		5.74	6		GHz		4
FUNCTIONS							
Digital functions: MODE, OCDS, PSS, MUX - Logic 0 - Logic 1	V_{IL} V_{IH}	 1.6	0 V_{CCD}	0.8	V V		
Gain Adjustment function	GA		0 V_{CCA3}				1,6
Digital output function (HTVF, STVF) Logic 0 Logic 1	V_{OL} V_{OH}	– 2.1	– –	0.8	V V	(5)	1,6
DC ACCURACY							
Differential Non-Linearity	DNL+		0.5	0.95	LSB		1,6
Differential Non-Linearity	DNL-	–0.95	–0.5		LSB		1,6
Integral Non-Linearity	INL+		1	3	LSB		1,6
Integral Non-Linearity	INL-	–3	–1		LSB		1,6
DC gain: - Initial gain error - DC gain adjustment - DC gain sensitivity to power supplies - DC gain drift over temperature			0 ±11 ±2 ±2		%FS %FS %FS %FS	(3)	1,6 1,6 1,6 4

Notes:
1. For use in higher nyquist zone, it is recommended to use higher power clock within the limit.
2. See Section 3.7 on page 13 for explanation of test levels.
3. Initial gain error corresponds to the deviation of the DC gain center value from unity gain. The gain can be set to 1 thanks to the GA function. DC gain dispersion excludes initial gain error.
4. Single-ended operation is not recommended, this line is given for better understanding of what is output by the DAC.
5. In order to modify the Vol/Voh value, pull up and pull down resistances of 10KΩ could be used.

3.4 AC Electrical Characteristics

Figures in tables herafter are derived from industrial screening without any correction to take in account the balun effect, but for practical reasons (necessity to cover also 2nd and 3rd Nyquist Zones) the balun used for industrial test is not optimum for first Nyquist performances, and results when Fout or folded low order hamonics are between DC to 400 MHz are very pessimistic. For further details please refer to Section 6.2.3 on page 49 for effect of the balun on performances.

Table 3-4. AC Electrical Characteristics NRZ Mode (First Nyquist Zone)

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**	**Test level**(2)
Single-tone Spurious Free Dynamic Range First Nyquist							
Fs = 3 GSps @ Fout = 100 MHz 0 dBFS	ISFDRI	57	68		dBc	(1)	1,6
Fs = 3 GSps @ Fout = 400 MHz 0 dBFS			63				4
Fs = 3 GSps @ Fout = 100 MHz –3 dBFS		59	70				1,6
Highest spur level First Nyquist							
Fs = 3 GSps @ Fout = 100 MHz 0 dBFS			–68	–56			1,6
Fs = 3 GSps @ Fout = 400 MHz 0 dBFS			–61		dBm		4
Fs = 3 GSps @ Fout = 100 MHz –3 dBFS			–72	–60			1,6
SFDR sensitivity & high spur level variation over power supplies			±2		dB		4
Signal independent Spur (clock-related spur)							
Fc/2			–82		dBm		4
Fc/4			<–85		dBm		4
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 3 GSps 20 MHz to 900 MHz broadband pattern, 25 MHz notch centered on 450 MHz	NPR	45	49		dB		1,6
Equivalent ENOB Computed from NPR figure	ENOB	9	9.6		Bit	(3)	1,6
Signal to Noise Ratio Computed from NPR figure	SNR	56	58		dB	(3)	1,6
Self Noise Density at code 0 or 4095			–163	–154	dBm/Hz	(3)	1,6

Notes:
1. Ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured.
2. See Section 3.7 on page 13 for explanation of test levels.
3. NPR band limitations are only due to measurement equipment limitations not to the component itself. Typical values are obtained from characterization measurements. Please refer to Section 6.2.7 ”NPR Performances” on page 65 for more details.

Table 3-5. AC Electrical Characteristics NRTZ Mode (First & Second Nyquist Zone)

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test level(2)
Single-tone Spurious Free Dynamic Range	|SFDR|				dBc	(1)	
MUX4:1							
Fs = 3 GSps @ Fout = 100 MHz 0 dBFS		60	68				1,6
Fs = 3 GSps @ Fout = 700 MHz 0 dBFS		54	62				1,6
Fs = 3 GSps @ Fout = 1800 MHz 0 dBFS		52	61				1,6
Fs = 3 GSps @ Fout = 700 MHz –3 dBFS		58	66				1,6
MUX2:1							
Fs = 1.5 GSps @ Fout = 700 MHz 0 dBFS		51	65				1,6
Highest spur level					dBm		
MUX4:1							
Fs = 3 GSps @ Fout = 100 MHz 0 dBFS			–70	–62			1,6
Fs = 3 GSps @ Fout = 700 MHz 0 dBFS			–64	–56			1,6
Fs = 3 GSps @ Fout = 1800 MHz 0 dBFS			–67	–57			1,6
Fs = 3 GSps @ Fout = 700 MHz –3 dBFS			–70	–63			1,6
MUX2:1							
Fs = 1.5 GSps @ Fout = 700 MHz 0 dBFS			–68	–53			1,6
SFDR sensitivity & high spur level variation over power supplies			±2		dB		4
Signal independent Spur (clock-related spur)							
Fc			–29		dBm		4
Fc/2			–80		dBm		4
Fc/4			<-80		dBm		4
Self Noise Density at code 0 or 4095			–149	–143	dBm/Hz		1,6
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 3 GSps 20 MHz to 900 MHz broadband pattern, 25 MHz notch centered on 450 MHz	NPR	45.5	50.2		dB	(3)	1,6
Equivalent ENOB Computed from NPR figure	ENOB	9.1	9.9		Bit	(3)	1,6
Signal to Noise Ratio Computed from NPR figure	SNR	56.5	61.2		dB	(3)	1,6

Table 3-5. AC Electrical Characteristics NRTZ Mode (First & Second Nyquist Zone) (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test level[(2)]
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 1.5 GSps 10 MHz to 450 MHz broadband pattern, 12.5 MHz notch centered on 225 MHz	NPR		55.7		dB	(3)	4
Equivalent ENOB Computed from NPR figure	ENOB		10.8		Bit	(3)	4
Signal to Noise Ratio Computed from NPR figure	SNR		66.7		dB	(3)	4

Notes:
1. Ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured.
2. See Section 3.7 on page 13 for explanation of test levels.
3. NPR band limitations are only due to measurement equipment limitations not to the component itself. Typical values are obtained from characterization measurements. Please refer to Section 6.2.7 ”NPR Performances” on page 65 for more details.

Table 3-6. AC Electrical Characteristics RTZ Mode (Second Nyquist Zone)

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test level[(2)]
Single-tone Spurious Free Dynamic Range							
MUX4:1	|SFDR|				dBc	(1)	
Fs = 3 GSps @ Fout = 1600 MHz 0 dBFS		51	60				1,6
Fs = 3 GSps @ Fout = 2900 MHz 0 dBFS		50	57				1,6
Highest spur level							
MUX4:1					dBm		
Fs = 3 GSps @ Fout =1600 MHz 0 dBFS			–67	–58			1,6
Fs = 3 GSps @ Fout = 2900 MHz 0 dBFS			–66	–60			1,6
SFDR sensitivity & high spur level variation over power supplies			±2		dB		4
Signal independent Spur (clock-related spur)							
Fc			–25		dBm		4
Fc/2			<-80		dBm		4
Fc/4			<-80		dBm		4
Self Noise Density at code 0 or 4095			–143	–140	dBm/Hz		1,6

Table 3-6. AC Electrical Characteristics RTZ Mode (Second Nyquist Zone) (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test level[2]
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 3 GSps 1520 MHz to 2200 MHz broadband pattern, 25 MHz notch centered on 1850 MHz	NPR	39.5	44.0		dB	(3)	1,6
Equivalent ENOB Computed from NPR figure	ENOB	8.1	8.8		Bit	(3)	1,6
Signal to Noise Ratio Computed from NPR figure	SNR	50.5	55.0		dB	(3)	1,6

Notes:
1. Ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured.
2. See Section 3.7 on page 13 for explanation of test levels.
3. NPR band limitations are only due to measurement equipment limitations not to the component itself. Typical values are obtained from characterization measurements. Please refer to Section 6.2.7 ”NPR Performances” on page 65 for more details.

Table 3-7. AC Electrical Characteristics RF Mode (Second and Third Nyquist Zones)

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test level[2]
Single-tone Spurious Free Dynamic Range	|SFDR|				dBc	(1)	
2nd Nyquist							
Fs = 3 GSps @ Fout = 1600 MHz 0 dBFS		44	52				1,6
Fs = 3 GSps @ Fout = 2900 MHz 0 dBFS			60				4
3rd Nyquist							
Fs = 3 GSps @ Fout = 3800 MHz 0 dBFS		45	53			(3)	1,6
Fs = 3 GSps @ Fout = 4400 MHz 0 dBFS		45	54				1,6
Highest spur level					dBm		
2nd Nyquist							
Fs = 3 GSps @ Fout = 1600 MHz 0 dBFS			–58	–50			1,6
Fs = 3 GSps @ Fout = 2900 MHz 0 dBFS			–58				4
3rd Nyquist							
Fs = 3 GSps @ Fout = 3800 MHz 0 dBFS			–60	–52			1,6
Fs = 3 GSps @ Fout = 4400 MHz 0 dBFS			–62	–55			1,6
SFDR sensitivity & high spur level variation over power supplies			±2		dB		4
Signal independent Spur (clock-related spur)							
Fc			–28		dBm		4
Fc/2			<-80		dBm		4
Fc/4			<-80		dBm		4

Table 3-7. AC Electrical Characteristics RF Mode (Second and Third Nyquist Zones) (Continued)

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**	**Test level**(2)
Self Noise Density at code 0 or 4095			–141	–138	dBm/Hz		1,6
Noise Power Ratio (2^{nd} Nyquist) –14 dBFS peak to rms loading factor Fs = 3 GSps 1520 MHz to 2200 MHz broadband pattern, 25 MHz notch centered on 1850 MHz	NPR	38	42		dB	(4)	1,6
Equivalent ENOB Computed from NPR figure	ENOB	7.8	8.5		Bit	(4)	1,6
Signal to Noise Ratio Computed from NPR figure	SNR	49	53		dB	(4)	1,6
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 3 GSps 2200 MHz to 2880 MHz broadband pattern, 25 MHz notch centered on 2550 MHz	NPR	38	42		dB	(4)	1,6
Equivalent ENOB Computed from NPR figure	ENOB	7.8	8.5		Bit	(4)	1,6
Signal to Noise Ratio Computed from NPR figure	SNR	49	53		dB	(4)	1,6
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 3 GSps 3050 MHz to 3700 MHz broadband pattern, 25 MHz notch centered on 3375 MHz	NPR	38	40		dB	(4)	1,6
Equivalent ENOB Computed from NPR figure	ENOB	7.8	8.2		Bit	(4)	1,6
Signal to Noise Ratio Computed from NPR figure	SNR	49	51		dB	(4)	1,6

Notes:
1. Ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured.
2. See Section 3.7 on page 13 for explanation of test levels.
3. Ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured over the third Nyquist frequency band (Fs to 3Fs/2).
4. NPR band limitations are only due to measurement equipment limitations not to the component itself. Typical values are obtained from characterization measurements. Please refer to Section 6.2.7 ”NPR Performances” on page 65 for more details.

3.5 Timing Characteristics and Switching Performances

Table 3-8. Timing Characteristics and Switching Performances

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test level(2)
SWITCHING PERFORMANCE AND CHARACTERISTICS							
Maximum operating clock frequency 4:1 MUX mode 2:1 MUX mode		3 1.5			GHz		1,6
Minimum operating clock frequency				300	MHz	(1)	4
TIMING CHARACTERISTICS							
Analog output rise/fall time	Tor Tof			60	ps	(3)	4
Tsetup (Fc = 3 GSps)		250			ps	(4)	4
Thold (Fc = 3 GSps)		100			ps	(4)	4
Input data rate (Mux 4:1)			750		MSps		4
Input data rate (Mux 2:1)			750		MSps		4
Master clock input jitter				100	fs rms	(5)	4
DSP clock phase tuning range		0		+3.5	Clock Cycle		5
DSP clock phase tuning steps			0.5		Clock cycle		5
Master clock to DSP, DSPN delay	TDSP		1.6		ns		4
SYNC to DSP, DSPN MUX 2:1 MUX4:1			880 1600		ps		4
Pipeline delay MUX4:1 MUX2:1	TDP			3.5 3.5	Clock cycles		4
Output delay	TOD		160		ps		4

Notes:
1. Minimum operating clock frequency can be DC. It depends on the clock input AC coupling capacitor used in the final application and limitation to the environment as circuit itself displays no lower clock frequency limitation. Refer to Section 6.2 on page 40.
   Minimum analogue output frequency depends on the AC coupling scheme used on the differential analogue output signal and on the DAC mode selected (refer to Section 4.2 "MODE Function" on page 16, to Figure 7-1 on page 78 and Figure 7-2 on page 79).
2. See Section 3.7 on page 13 for explanation of the test level.
3. Digital input data rise/fall time defined between 20% to 80%.
4. Exclusive of period (pp) jitter on Data. Setup and hold time for DATA at input relative to DSP clock at output.
5. Master clock input jitter defined over 5 GHz bandwidth.

3.6 Timing Information

Figure 3-1. Timing Diagram for 4:1 MUX Principle of Operation OCDS[00], IUCM Disabled

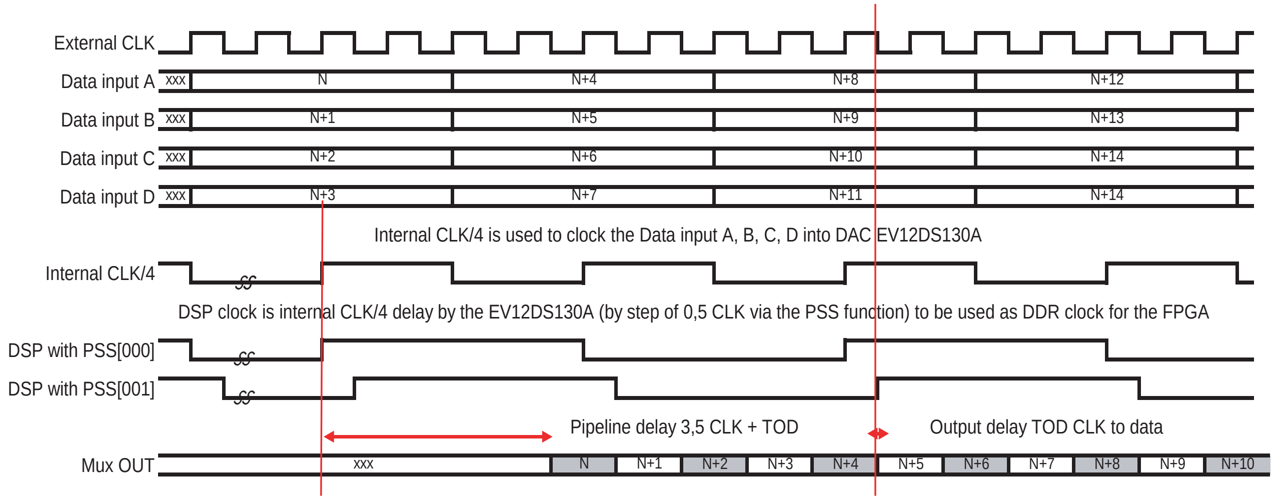
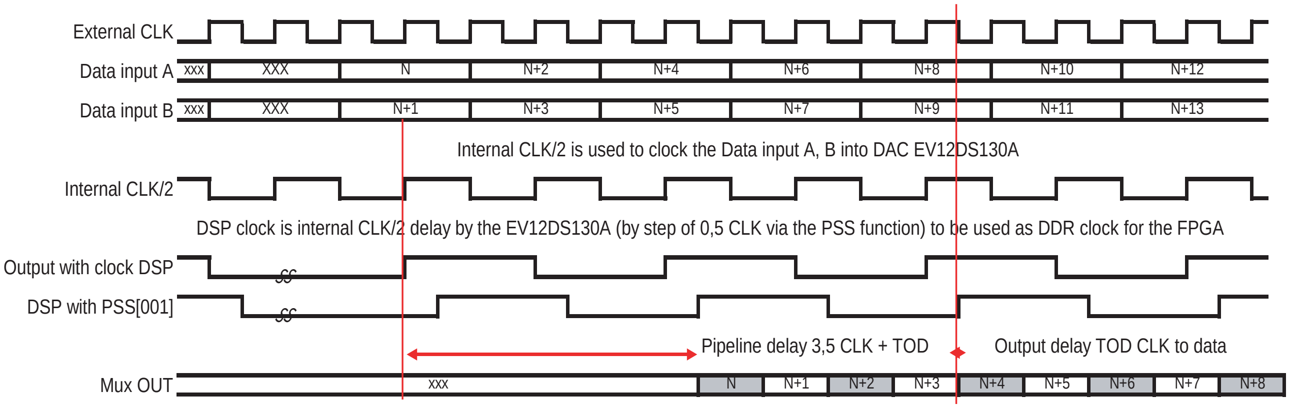


Figure 3-2. Timing Diagram for 2:1 MUX Principle of Operation OCDS[00], IUCM Disabled



3.7 Explanation of Test Levels

1	100% production tested at +25°C(1).
2	100% production tested at +25°C(1), and sample tested at specified temperatures.
3	Sample tested only at specified temperatures
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter is a typical value only guaranteed by design only
6	100% production tested over specified temperature range (for Space/Mil grade(2)).

Only MIN and MAX values are guaranteed (typical values are issuing from characterization results).

Notes:
1. Unless otherwise specified.
2. If applicable, please refer to “Ordering Information”

3.8 Digital Input Coding Table

Table 3-9. Coding Table

Digital output msb……….lsb	Differential analog output
000000000000	–500 mV
010000000000	–250 mV
011000000000	–125 mV
100000000000	0 mV
101000000000	+125 mV
110000000000	+250 mV
111111111111	+500 mV

4. Functional Description

Figure 4-1. DAC Functional Diagram

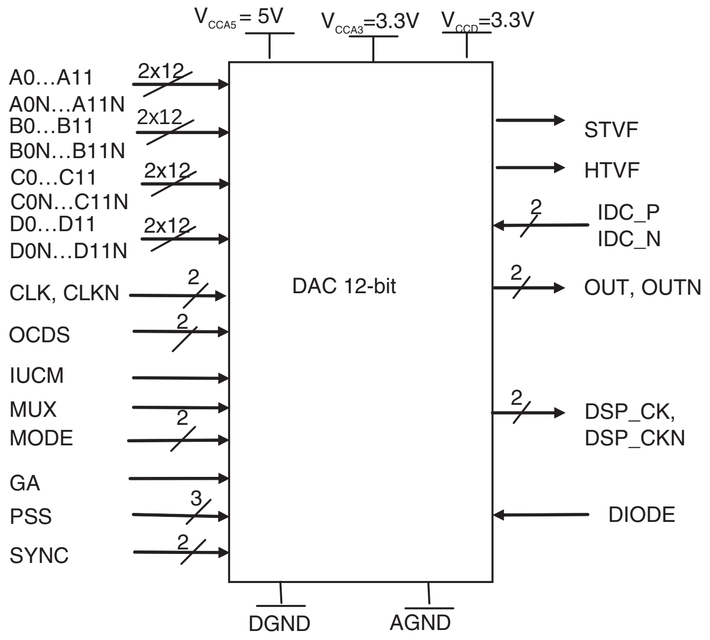


Table 4-1. Functions Description

Name	Function	Name	Function
V_{CCD}	3.3V Digital Power Supply	CLK	In-phase Master clock
V_{CCA5}	5V Analog Power Supply	CLKN	Inverted phase Master clock
V_{CCA3}	3.3V Analog Power Supply	DSP_CK	In-phase Output clock
DGND	Digital Ground	DSP_CKN	Inverted phase Output clock
AGND	Analog ground (for analog supply reference)	PSS[0..2]	Phase shift select
A[11…0]	In-phase digital input Port A	GA	Gain Adjust
A[11..0]N	Inverted phase digital input Port A	MUX	MUX Selection
B[11…0]	In-phase digital input Port B	MODE[0..1]	DAC Mode: NRZ, RTZ, NRTZ, RF
B[11..0]N	Inverted phase digital input Port B	STVF	Setup time Violation flag
C[11…0]	In-phase digital input Port C	HTVF	Hold time Violation flag
C[11..0]N	Inverted phase digital input Port C	IDC_P, IDC_N	Input data check
D[11…0]	In-phase digital input Port D	OCDS[0..1]	Output Clock Division factor Selection (by 4, 8, 16 or 32)
D[11..0]N	Inverted phase digital input Port D	Diode	Diode for temperature monitoring
OUT	In-phase analog output	SYNC/ SYNCN	Synchronization signal (Active High)
OUTN	Inverted phase analog output	IUCM	Input underclocking mode

4.1 MUX

Two modes for the MUX ratio are allowed:

- 4:1, which allows operation at full sampling rate (ie. 3 GHz);
- 2:1, which can only be used up to 1.5 GHz sampling rate.

Label	Value	Description	Comments
MUX	0	4:1 mode	Refer to Timing Information
	1	2:1 mode	Refer to Timing Information

In 2:1 MUX ratio, the unused data ports (ports C and D) can be left open.

4.2 MODE Function

Label	Value	Description	Default Setting (Not Connected)
MODE[1:0]	00	NRZ mode	11 RF mode
	01	Narrow RTZ (a.k.a. NRTZ) mode	
	10	RTZ Mode (50%)	
	11	RF mode	

The MODE function allows choosing between NRZ, NRTZ, RTZ and RF functions. NRZ and narrow RTZ should be chosen for use in 1st Nyquist zone while RTZ should be chosen for use in 2nd and RF for 3rd Nyquist zones.

Theory of operation: see following subsections for time domain waveform of the different modes.

Ideal equations describing max available Pout for frequency domain in the four modes are given hereafter, with X = normalised output frequency (that is Fout/Fclock, edges of Nyquist zones are then at X = 0 1/2 1 3/2 2 …)

In fact due to limited bandwidth, an extra term must be added to take in account a first order LPF.

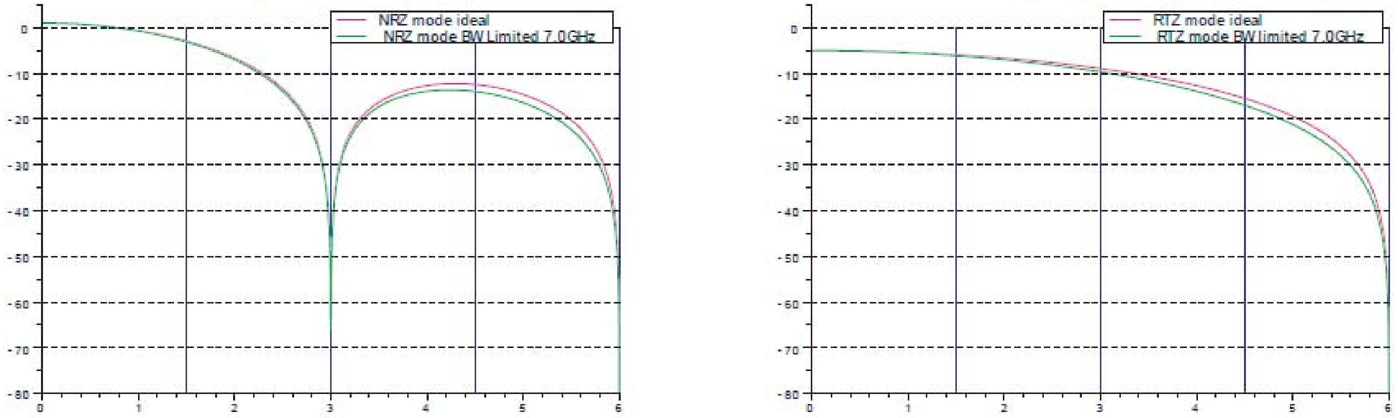
- NRZ mode: $Pout(X) = 20*\log_{10}(k*\text{sinc}(k*\pi*X)|/0.893)$
  where $\text{sinc}(x) = \sin(x)/x$, and $k = 1$
- NRTZ mode: $Pout(X) = 20*\log_{10}(k*\text{sinc}(k*\pi*X)|/0.893)$
  where $k = (Fclock-T\tau)/Fclock$ and $T\tau$ is width of reshaping pulse, $T\tau$ is about 75ps.
- RTZ mode: $Pout(X)= 20*\log_{10}(k*\text{sinc}(k*\pi*X)|/0.893)$
  where k is the duty cycle of the clock presented at the DAC input, please note that due to phase mismatch in balun used to convert single ended clock to differential clock the first zero may move around the limit of the 4th and the 5th Nyquist zones. Ideally k = 1/2.
- RF mode:$Pout(x) = 20*\log_{10}(k*|\text{sinc}(k*\pi*X/2)/\sin(k*\pi*X/2)|/0.893)$
  where k is as per in NRTZ mode.

As a consequence:

- NRZ mode offers max power for 1st Nyquist operation
- RTZ mode offers slow roll off for 2nd Nyquist or 3rd Nyquist operation
- RF mode offers maximum power over 2nd and 3rd Nyquist operation
- NRTZ mode offers optimum power over full 1st and first half of 2nd Nyquist zones. This is the most relevant in term of performance for operation over 1st and beginning of 2nd Nyquist zone, depending on the sampling rate the zero of transmission moves in the 3rd Nyquist zone from begin to end when sampling rate increases.

Note in the two following figures: Pink line is ideal equation's result, and green line includes a first order 6GHz cut-off LPF to take in account finite bandwidth effect due to die and package.

Figure 4-2. Max available Pout[dBm] at nominal gain vs Fout[GHz] in the four output modes at 3 GSps, over four Nyquist zones, computed for Tτ = 75 ps.



NRZ mode: Max Pout [dBm] vs Fout [GHz] at3.0Gsps

RTZ mode: Max Pout [dBm] vs Fout [GHz] at3.0Gsps

NRTZ mode rpw 75ps :
Max Pout [dBm] vs Fout [GHz] at3.0Gsps

RF mode rpw 75ps :
Max Pout [dBm] vs Fout [GHz] at3.0Gsps

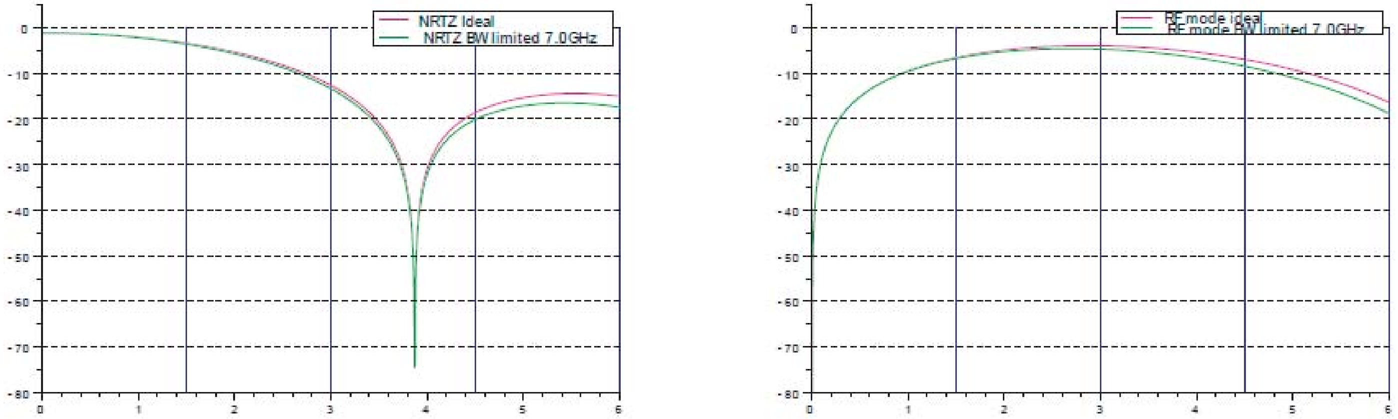
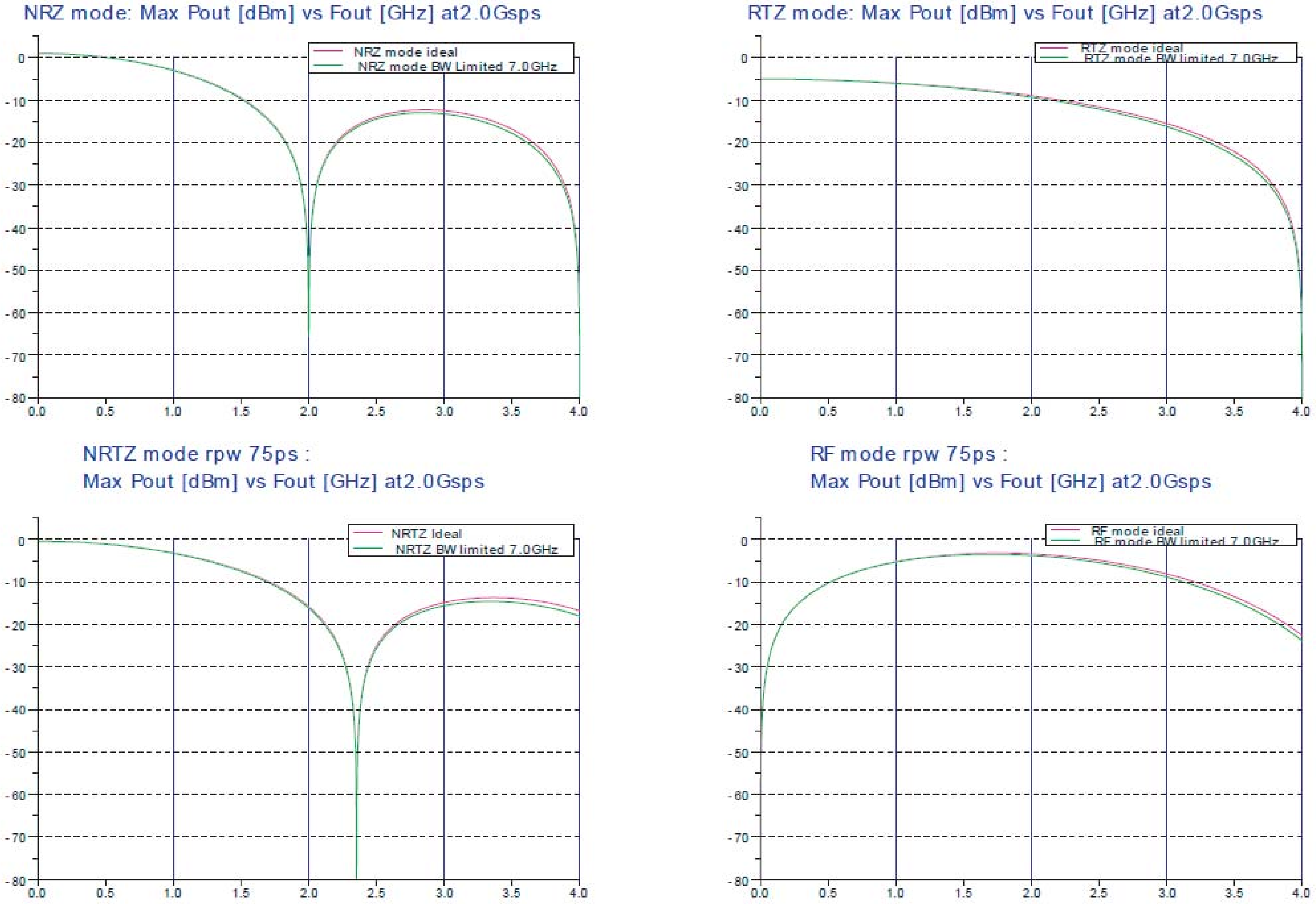


Figure 4-3. Max available Pout[dBm] at nominal gain vs Fout[GHz] in the four output modes at 2 GSps, over four Nyquist zones, computed for $T\tau = 75$ ps



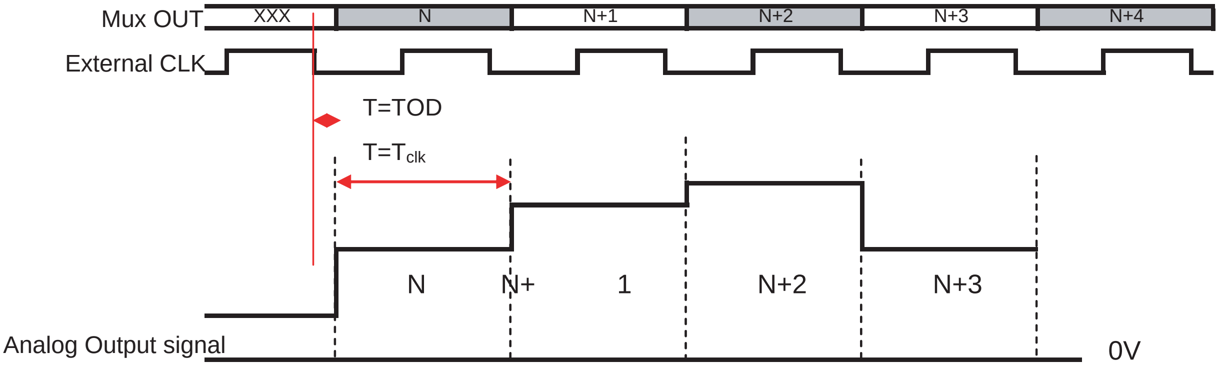
- NRZ mode offers max power for 1st Nyquist operation
- RTZ mode offers slow roll off for 2nd Nyquist operation
- RF mode offers maximum power over 2nd and 3rd Nyquist operation
- NRTZ mode offers optimum power over full 1st and first half of 2nd Nyquist zones. This is the most relevant in term of performance for operation over 1st and beginning of 2nd Nyquist zone

4.2.1 NRZ Output Mode

This mode does not allow for operation in the 2nd Nyquist zone because of the Sinx/x notch.

The advantage is that it gives good results at the beginning of the 1st Nyquist zone (less attenuation than in RTZ architecture), it removes the parasitic spur at the clock frequency (in differential).

Figure 4-4. NRZ Timing Diagram

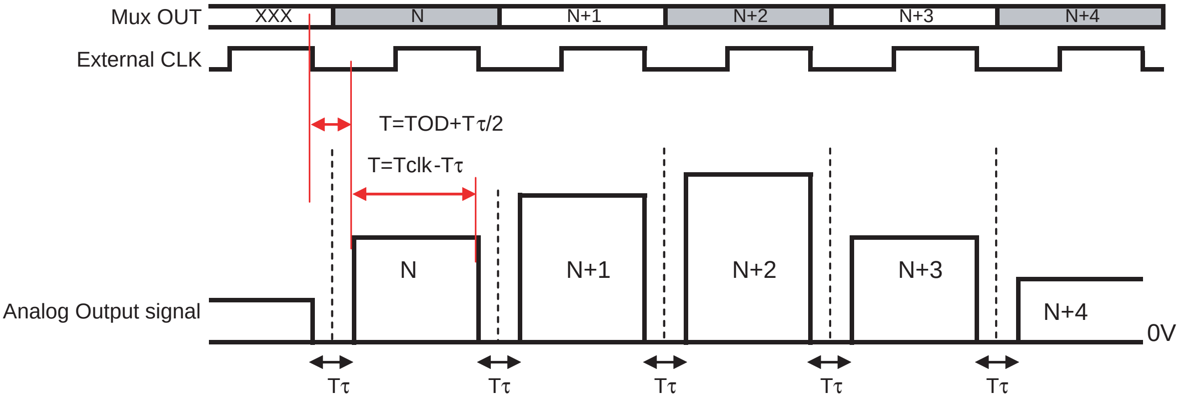


4.2.2 Narrow RTZ Mode

This mode has the following advantages:

- Optimized power in 1st Nyquist zone
- Extended dynamic through elimination of noise on transition edges
- Improved spectral purity (see Section 6.2.3 on page 49)
- Trade off between NRZ and RTZ

Figure 4-5. Narrow RTZ Timing Diagram



Note: Tτ is independant of Fclock.

4.2.3 RTZ Mode

The advantage of the RTZ mode is to enable the operation in the 2nd zone but the drawback is clearly to attenuate more the signal in the first Nyquist zone.

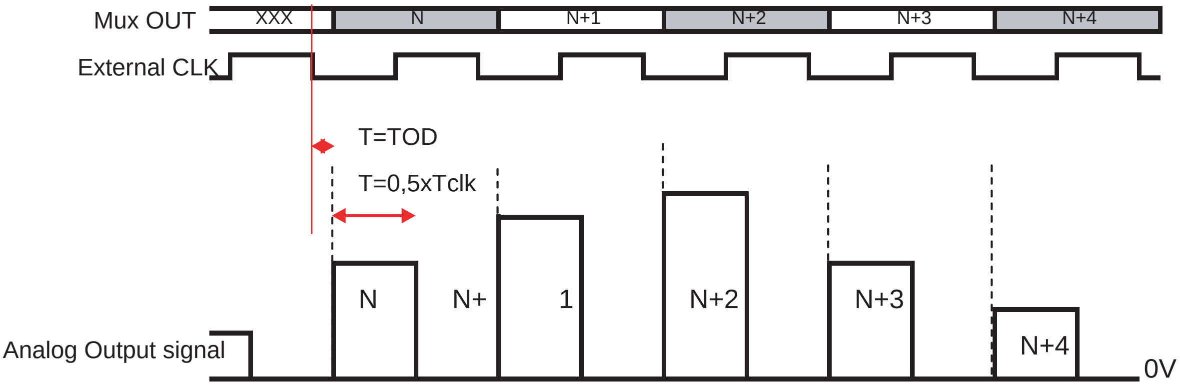
Advantages:

- Extended roll off of sinc
- Extended dynamic through elimination of hazardous transitions

Weakness:

- By construction clock spur at Fs.

Figure 4-6. RTZ Timing Diagram



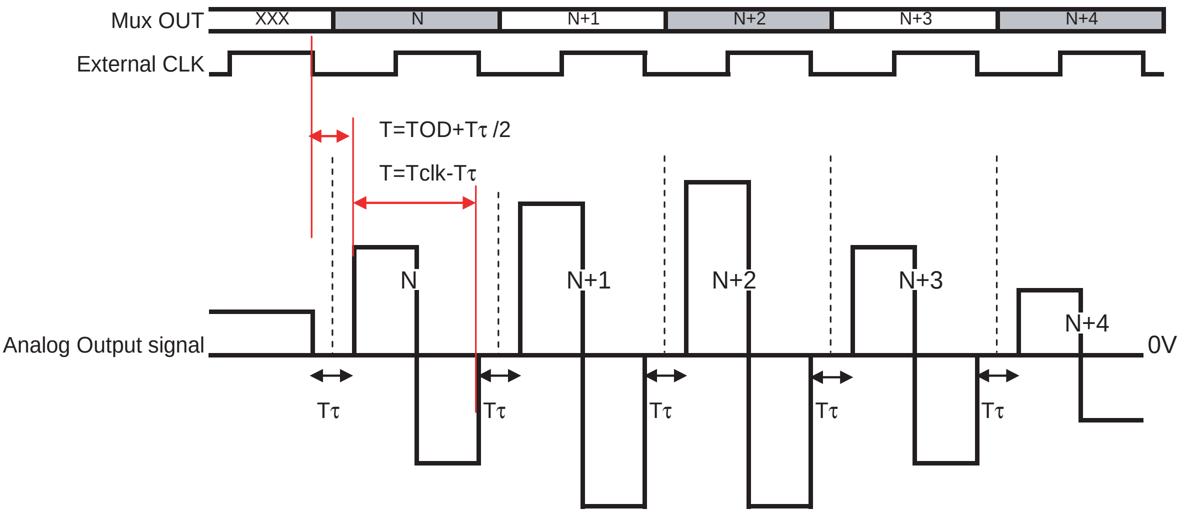
4.2.4 RF Mode

RF mode is optimal for operation at high input frequency, since the decay with frequency occurs at higher frequency than for RTZ. Unlike NRZ or RTZ modes, RF modes presents notch DC and 2N*Fs, and minimum attenuation for Fout = Fs.

Advantages:

- Optimized for 2nd and 3rd Nyquist operation
- Extended dynamic range through elimination of hazardous transitions.
- Clock spur pushed to 2.Fs

Figure 4-7. RF Timing Diagram



Note: The central transition is not hazardous but its elimination allows to push clock spur to 2.Fs
Tτ is independant of Fclock.

4.3 PSS (Phase Shift Select Function)

It is possible to adjust the timings between the sampling clock and the DSP output clock (which frequency is given by the following formula: Sampling clock / 2NX where N is the MUX ratio, X the output clock division factor).

The DSP clock output phase can be tuned over a range of 3.5 input clock cycles (7 steps of half a clock cycle) in addition to the intrinsic propagation delay between the DSP clock (DSP, DSPN) and the sampling clock (CLK, CLKN).

Three bits are provided for the phase shift function: PSS[2:0].

By setting these 3 bits to 0 or 1, one can add a delay on the DSP clock in order to properly synchronize the input data of the DAC and the sampling clock (the DSP clock should be applied to the FPGA and should be used to clock the DAC digital input data).

Table 4-2. PSS Coding Table

Label	Value	Description
PSS[2:0]	000	No additional delay on DSP clock
	001	0.5 input clock cycle delay on DSP clock
	010	1 input clock cycle delay on DSP clock
	011	1.5 input clock cycle delay on DSP clock
	100	2 input clock cycle delay on DSP clock
	101	2.5 input clock cycle delay on DSP clock
	110	3 input clock cycle delay on DSP clock
	111	3.5 input clock cycle delay on DSP clock

In order to determine how much delay needs to be added on the DSP clock to ensure the synchronization between the input data and the sampling clock within the DAC, the HTVF and STVF bits should be monitored. Refer to Section 4.6 on page 27.

Note: In MUX 4:1 mode the 8 settings are relevant, in MUX 2:1 only the four first settings are relevant since the four last setting will yield exactly the same results.

Figure 4-8. PSS Timing Diagram for 4:1 MUX, IUCM Disabled, OCDS[00]

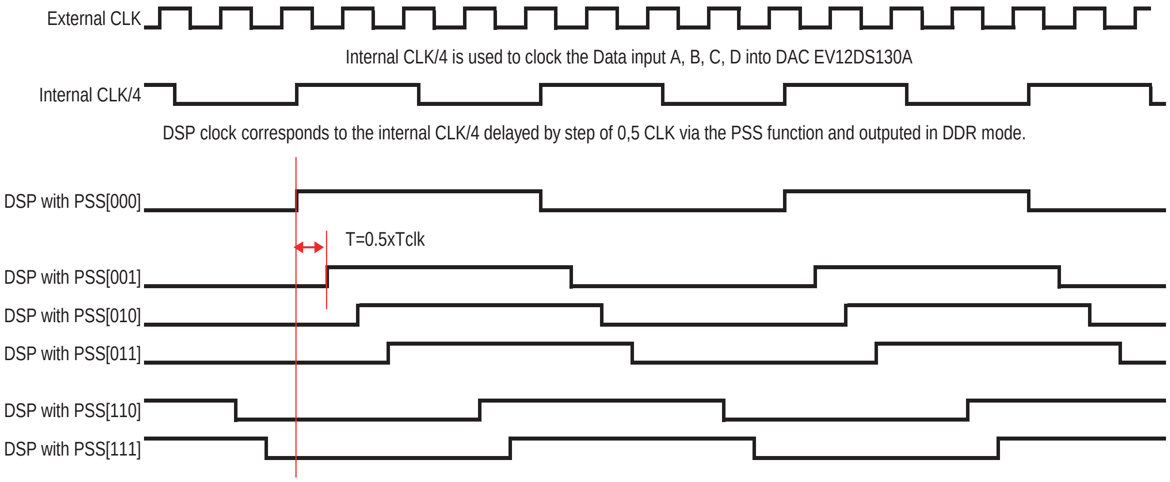
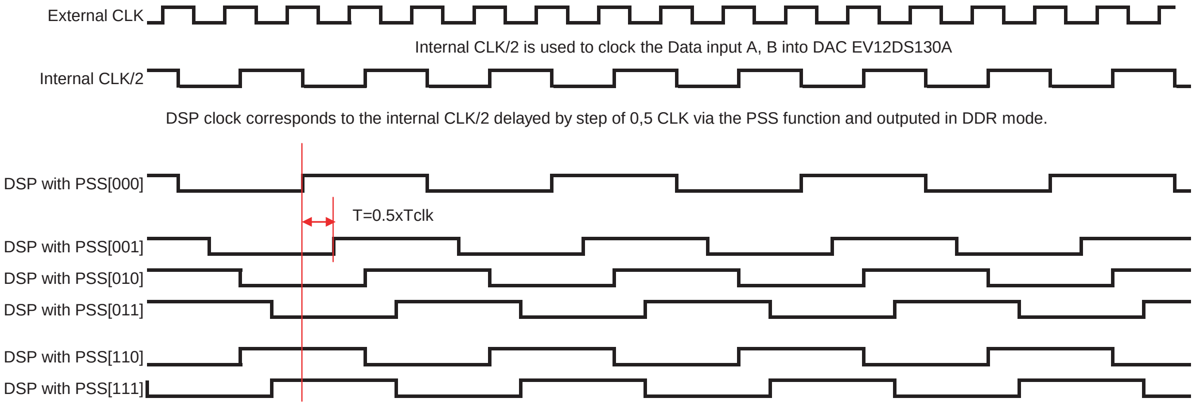


Figure 4-9. PSS Timing Diagram for 2:1 MUX



4.4 Output Clock Division Select Function OCDS[1:0]

It is possible to change the DSP clock internal division factor from 1 to 2, 4 and 8 with respect to the sampling clock/2N where N is the MUX ratio. This is possible via the OCDS "Output Clock Division Select" bits.

OCDS is used to obtain a synchronisation clock for the FPGA slow enough to allow the FPGA to operate with no further internal division of this clock, thus its internal phase is determined by the DSP clock phase. This is useful in a system with multiple DACs and multiple FPGAs to guarantee deterministic phase relationship between the FPGAs after a synchronisation of all the DACs.

Table 4-3. OCDS[1:0] Coding Table

Label	Value	Description
OCDS [1:0]	00	DSP clock frequency is equal to the sampling clock divided by 2N
	01	DSP clock frequency is equal to the sampling clock divided by 2N*2
	10	DSP clock frequency is equal to the sampling clock divided by 2N*4
	11	DSP clock frequency is equal to the sampling clock divided by 2N*8

Figure 4-10. OCDS Timing Diagram for 4:1 MUX

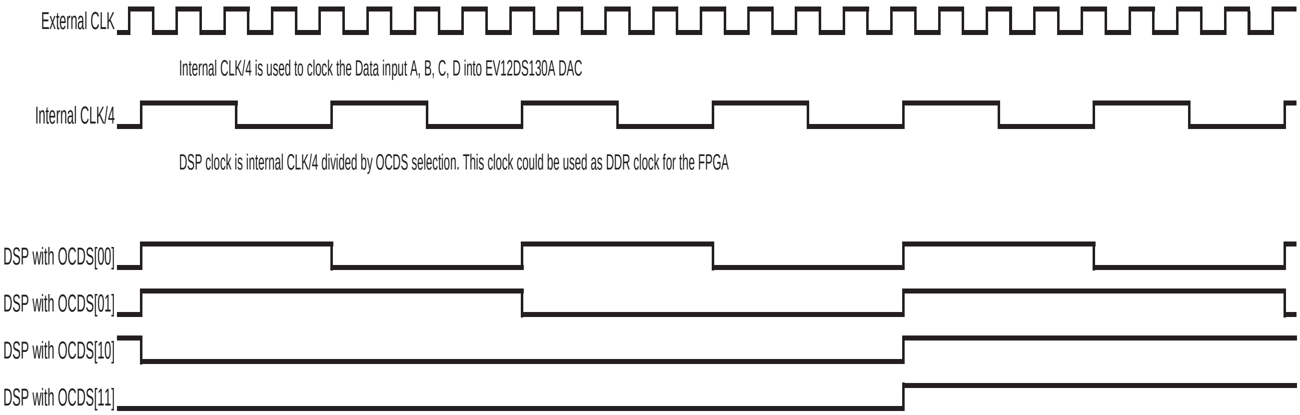
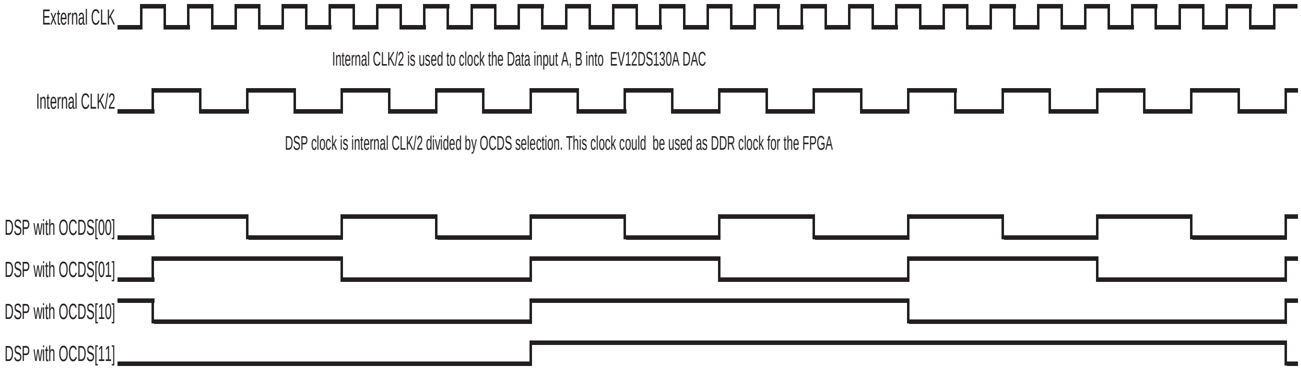


Figure 4-11. OCDS Timing Diagram for 2:1 MUX



4.5 Input Under Clocking Mode (IUCM), Principle and Spectral Response

An Input Under Clocking Mode has been added to the DAC in order to allow for a specific use where the input data are applied to the DAC at half the nominal rate with respect of the DAC sampling rate. This mode is available for 4:1 MUX mode. It should also work in 2:1 MUX mode but has no specific interest.

To disable this mode, the IUCM pin must be connected to GND.

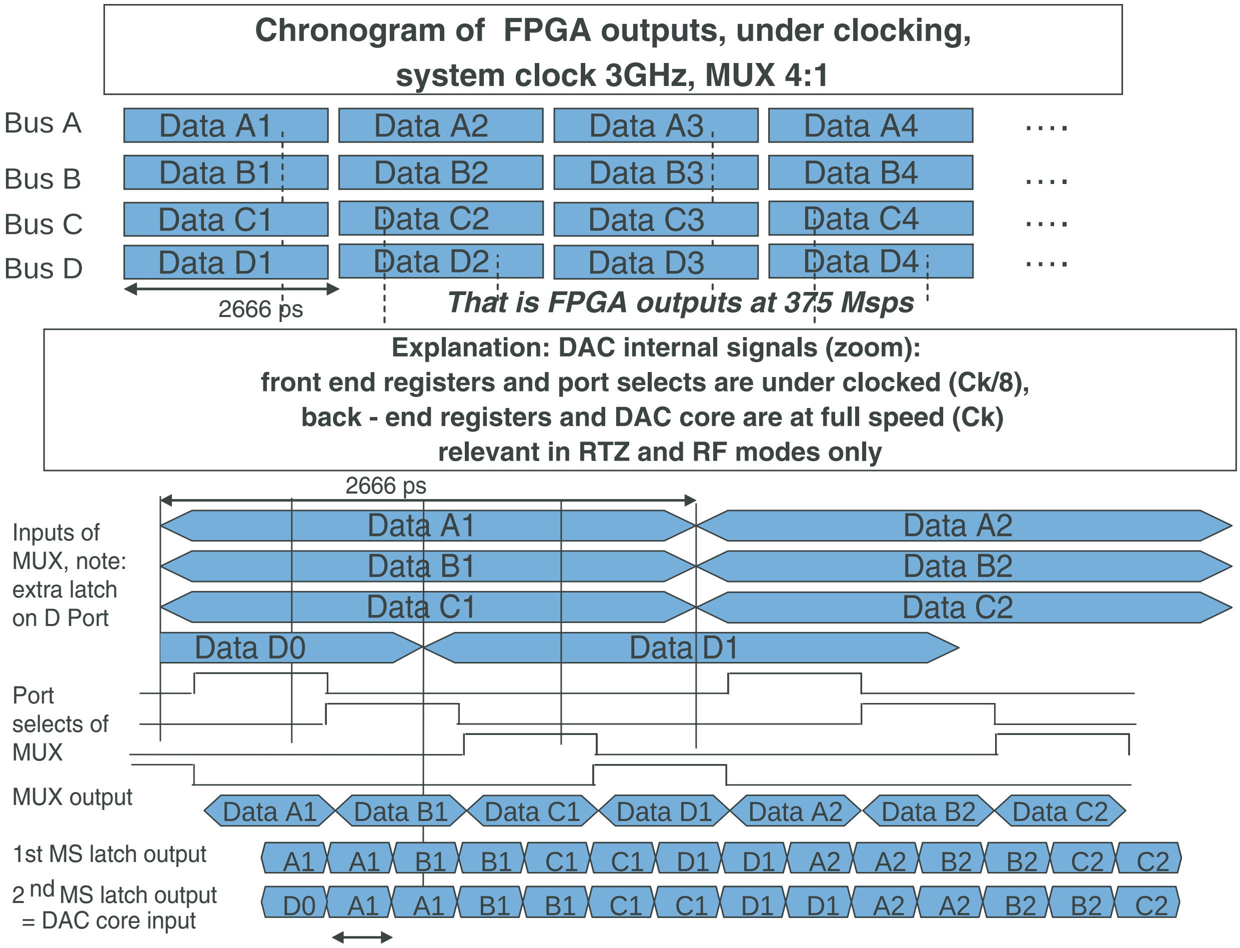
To enable this mode, IUCM must be connected to V_{CCD} or left unconnected

When the under clocking mode is activated, the DAC expects data at half the nominal rate: if the DAC works at Fs sampling rate, then in 4:1 MUX mode, the input data rate should be Fs/4 and the DSP clock should be Fs/(2N*OCDS), with N = MUX ratio and OCDS = 1, 2, 4 or 8.

When the IUCM is active, the input data rate can be Fs/8 and the DSP clock frequency is Fs/(2N*OCDS*2), with N = MUX ratio and OCDS = 1, 2, 4 or 8. This means that in input under clocking mode, the DAC is capable to treat data at half the nominal rate. In this case, the DSP clock is also half its nominal speed.

Label	Logic Value	Description
IUCM	0	Input Under Clocking Mode inactive
	1	Input Under Clocking Mode active

Figure 4-12. Input Under Clocking Mode Timing Diagram (MUX 4:1 "0", IUCM ON, OCDS "00", MODE RTZ or RF)



The IUCM mode affects spectral response of the different modes.

The first effect is that Nyquist zone edges are not anymore at n*Fclock/2 but at n*/Fclock/4 (direct consequence of the division by 2 of the data rate).

The second effect is the modification of the equations ruling the spectral responses in the different modes.

Ideal equations describing max available Pout for frequency domain in the four output modes when IUCM mode is activated are given hereafter, with X = normalised output frequency (that is Fout/Fclock, edges of Nyquist Zones are then at X = 0 1/4 1/2 3/4 1 …)

In fact due to limited bandwidth, an extra term must be added to take in account a first order LPF with a 6 Ghz cut-off frequency.

- NRZ mode: $Pout(X) = 20*\log_{10}(|k*sinc(k*\pi*X)*\cos(\pi*X)|/0.893)$
  where $sinc(x) = \sin(x)/x$, and $k = 1$
- NRTZ mode: $Pout(X) = 20*\log_{10}(|k*sinc(k*\pi*X)*\cos(\pi*X)|/0.893)$
  where k = (Fclock-T)/Fclock and T is width of reshaping pulse, T is about 75ps.
- RTZ mode: $Pout(X) = 20*\log_{10}(|k*sinc(k*\pi*X)*\cos(\pi*X)|/0.893)$
  where k is the duty cycle of the clock presented at the DAC input, please note that due to phase mismatch in balun used to convert single ended clock to differential clock the third zero may move around the limit of the 8th and the 9th Nyquist zones. Ideally $k = 1/2$.
- RF mode: $Pout(x) = 20*\log_{10}(|k*sinc(k*\pi*X/2)*\sin(k*\pi*X/2)*\cos(\pi*X)|/0.893)$
  where k is as per in NRTZ mode.

Figure 4-13. Max Available Pout[dBm] at Nominal Gain vs Fout[GHz] in the Four Output Modes at 3 GSps, Combined with IUCM, Over Four Nyquist Zones, Computed for Tτ =75 ps.

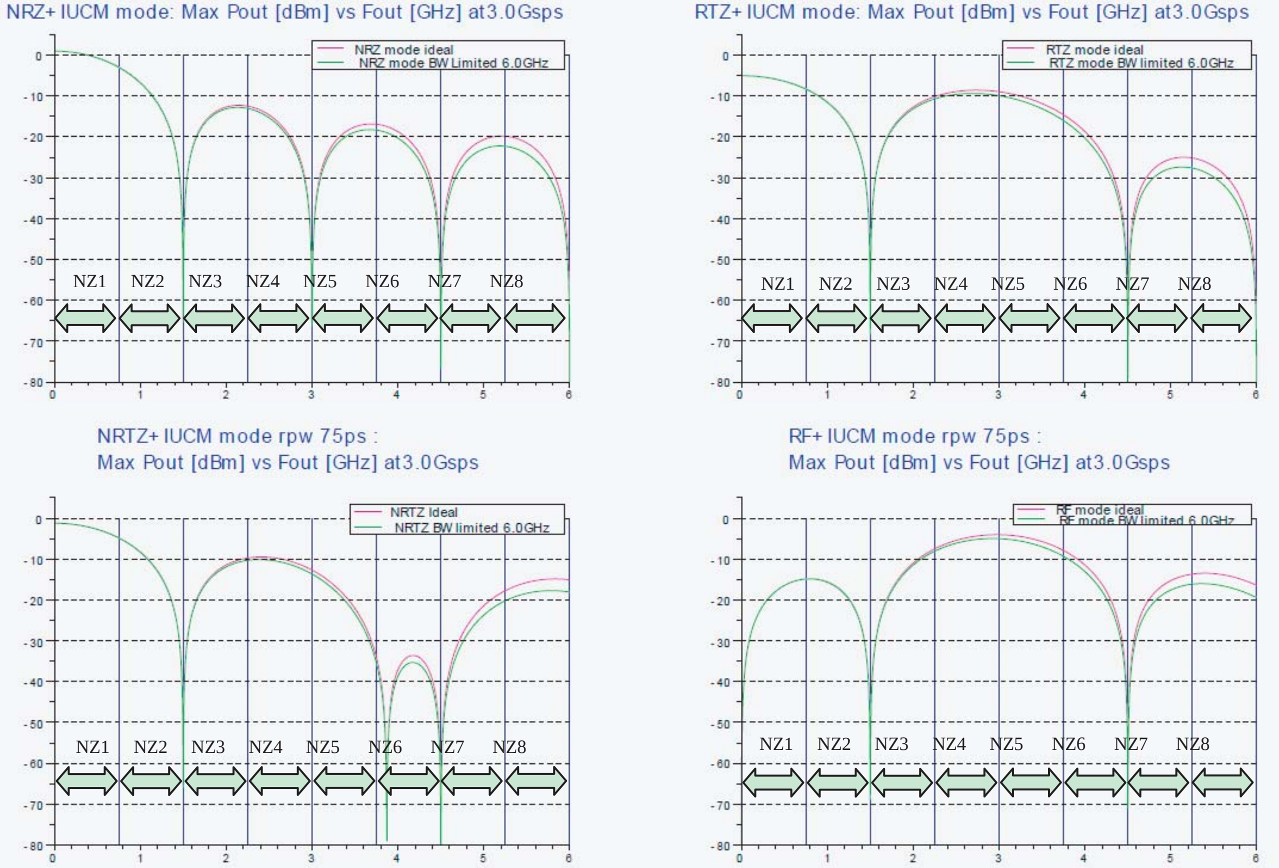
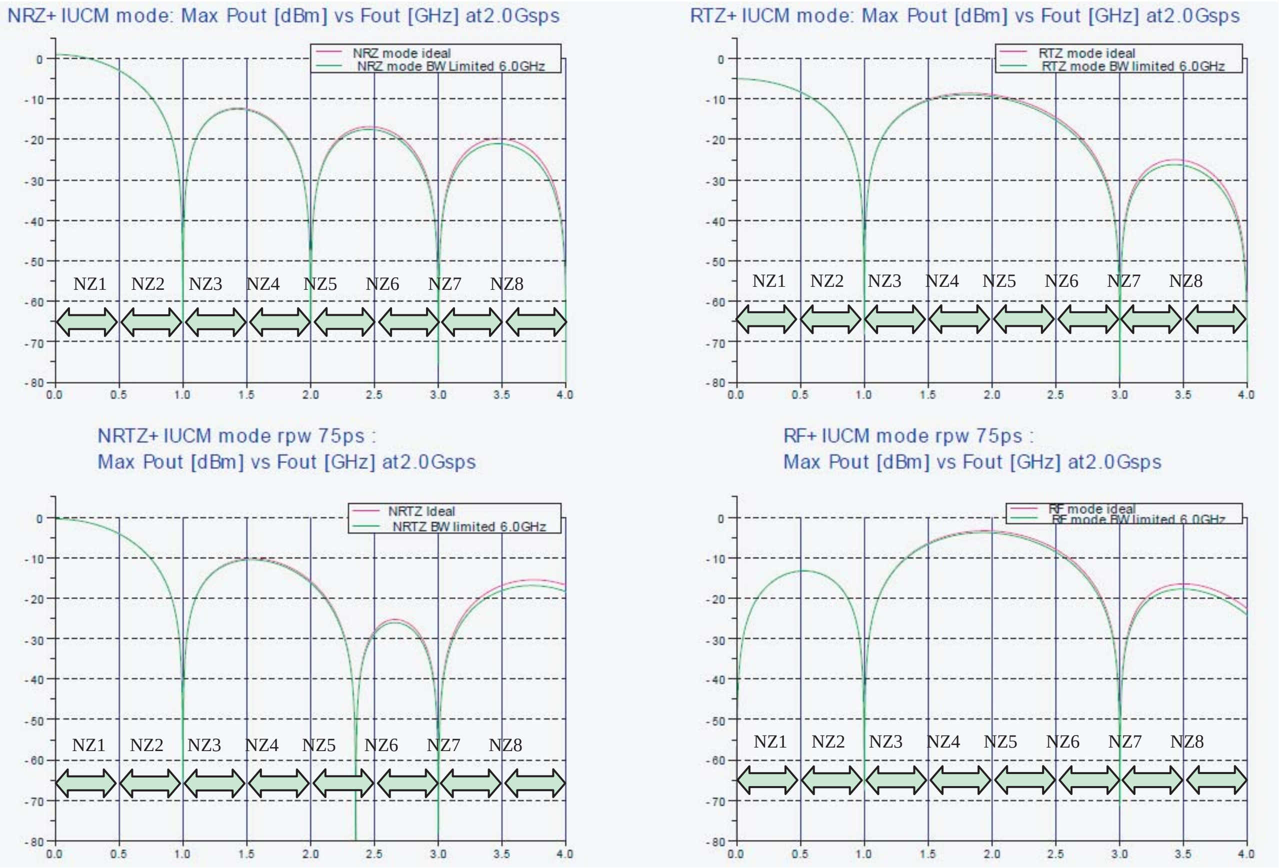


Figure 4-14. Max Available Pout[dBm] at Nominal Gain vs Fout[GHz] in the Four Output Modes at 3 GSps, Combined with IUCM, Over Four Nyquist Zones, Computed for Tτ = 75 ps



4.6 Synchronization FPGA-DAC: IDC_P, IDC_N, HTVF and STVF Functions

IDC_P, IDC_N: Input Data check function (LVDS signal).
HTVF: Hold Time Violation Flag.
STVF: Setup Time Violation Flag.

The IDC_P, IDC_N signal are an LVDS signals. This signal is toggling at each cycle synchronously with other data bits.

This signal should be generated by the FPGA so that the DAC can check in real-time if the timings between the FPGA and the DAC are correct. The information on the timings is then given by HTVF, STVF signals.

When used, it should be routed as the data signals (same layout rules and same length).

It should be driven to an LVDS low or high level if not used.

Figure 4-15. IDC Timing vs Data Input

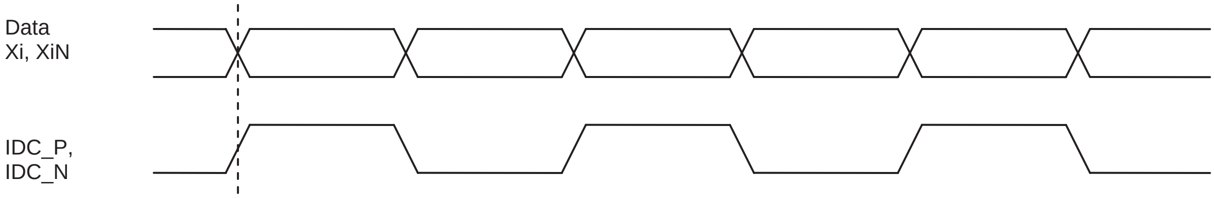
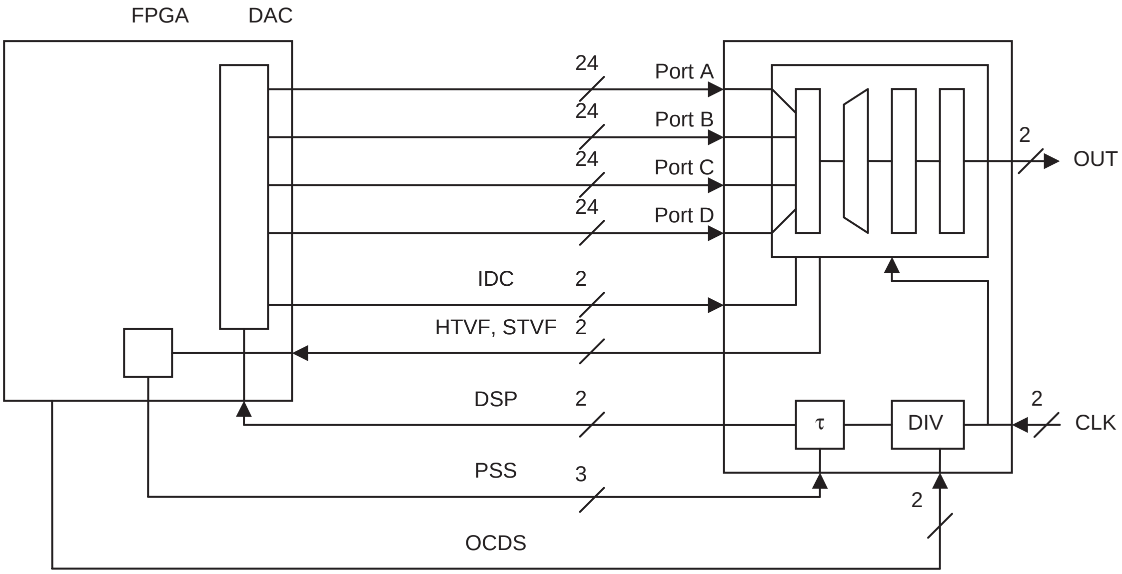


Figure 4-16. FPGA to DAC Synoptic



HTVF and STVF are CMOS 3.3V output signals, these signals indicate if the DAC and the FPGA are synchronised.

Table 4-4. HTVF, STVF Coding Table

Label	Value	Description
HTVF	0	SYNCHRO OK
	1	Data Hold time violation detected
STVF	0	SYNCHRO OK
	1	Data Setup time violation detected

Note: During Monitoring STVF indicates setup time of data violation (Low -> OK, High -> Violation), HTVF indicates hold time of data violation (Low -> OK, High -> Violation).

Principle of Operation:

The Input Data Check pair (IDC_P, IDC_N) will be sampled three times with half a master clock period shift (the second sample being synchronous with all the data sampling instant), these three samples will be compared, and depending on the results of the comparison a violation may be signalled.

- Violation of setup time -> STVF is high level
- Violation of hold time -> HTVF is high level

In case of violation of timing (setup or hold) the user has two solutions:

- Shift phase in the FPGA PLL (if this functionality is available in FPGA) for changing the internal timing of DATA and Data Check signal inside FPGA.
- Shift the DSP clock timing (Output clock of the DAC which can be used for FPGA synchronization – refer to Section 4.3 on page 21), in this case this shift also shift the internal timing of FPGA clock.

4.7 DSP Output Clock

The DSP output clock DSP, DSPN is an LVDS signal which is used to synchronize the FPGA generating the digital patterns with the DAC sampling clock.

The DSP clock frequency is a fraction of the sampling clock frequency. The division factor depends on OCDS settings. The DSP clock frequency is equal to (sampling frequency / [2N*X]) where N is the MUX ratio and X is the output clock division factor, determined by OCDS[0..1] bits.

For example, in a 4:1 MUX ratio application with a sampling clock of 3 GHz and OCDS set to “00” (ie. Factor of 1), the input data rate is 750 MSps and the DSP clock frequency is 375 MHz.

This DSP clock is used in the FPGA to control the digital data sequencing. Its phase can be adjusted thanks to the PSS[2:0] bits (refer to Section 4.3 on page 21) in order to ensure a proper synchronization between the data coming to the DAC and the sampling clock.

The HTVF and STVF bits should be used to check whether the timing between the FPGA and the DAC is correct. HTVF and STVF bits will indicate whether the DAC and FPGA are aligned or not. PSS bits should then be used to shift the DSP clock and thus the input data of the DAC, so that a correct timing is achieved between the FPGA and the DAC.

4.8 OCDS, IUCM, MUX Combinations Summary

Table 4-5. OCDS, IUCM, MUX, PSS Combinations Summary

MUX		IUCM		OCDS		PSS range	Data rate	Comments
0	4:1	1	ON	00	DSP clock division factor 16	0 to 7/(2Fs) by 1/(2Fs) steps	Fs/8	Refer to Figure 4-12 on page 25
0		1		01	DSP clock division factor 32			
0		1		10	DSP clock division factor 64			
0		1		11	DSP clock division factor 128			
0		0	OFF, normal mode	00	DSP clock division factor 8	0 to 7/(2Fs) by 1/(2Fs) steps	Fs/4	Refer to Figure 4-10 on page 23
0		0		01	DSP clock division factor 16			
0		0		10	DSP clock division factor 32			
0		0		11	DSP clock division factor 64			

Table 4-5. OCDS, IUCM, MUX, PSS Combinations Summary (Continued)

MUX		IUCM		OCDS		PSS range	Data rate	Comments
1	2:1	1	ON	00	DSP clock division factor 8	0 to 7/(2Fs) by 1/(2Fs) steps	Fs/4	Not recommended mode, not guaranteed
1		1		01	DSP clock division factor 16			
1		1		10	DSP clock division factor 32			
1		1		11	DSP clock division factor 64			
1		0	OFF, normal mode	00	DSP clock division factor 4	0 to 7/(2Fs) by 1/(2Fs) steps	Fs/2	Refer to Figure 4-10 on page 23
1		0		01	DSP clock division factor 8			
1		0		10	DSP clock division factor 16			
1		0		11	DSP clock division factor 32			

Note: Behaviour according to MUX, OCDS and PSS combination is independent of output mode (MODE).

4.9 Synchronization Functions

There are two reset functions integrated in this DAC :

- a power up reset, which is triggered by the power supplies;
- Reset (SYNC, SYNCN), which is an external reset and which should ensure the synchronization of multiple DACs.

The external reset is LVDS compatible (same buffer as for the digital input data).
It is active high.

Important note: The SYNC signal must be synchronised on system clock. The pulse duration will depend on factors such as OCDS and PSS and should last at least 3 clock cycles. See application note (reference 1087A Application note EV12DS130A: 3GSps MUXDAC) for further details.

Figure 4-17. Reset Timing Diagram (4:1 MUX)

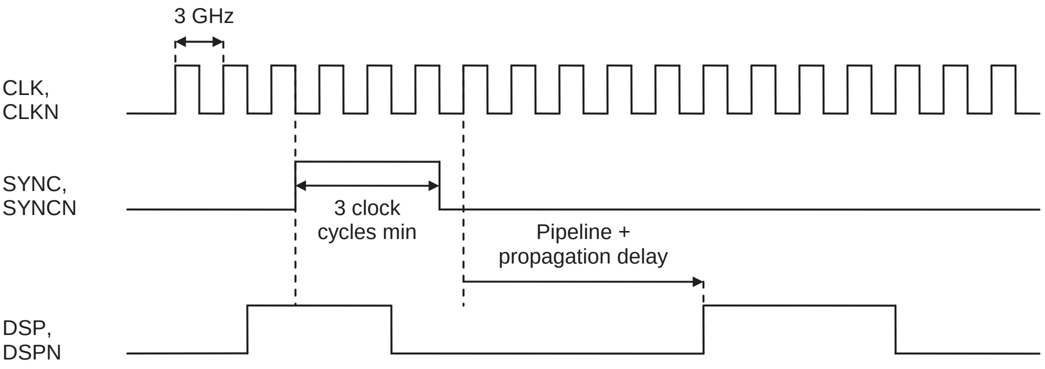
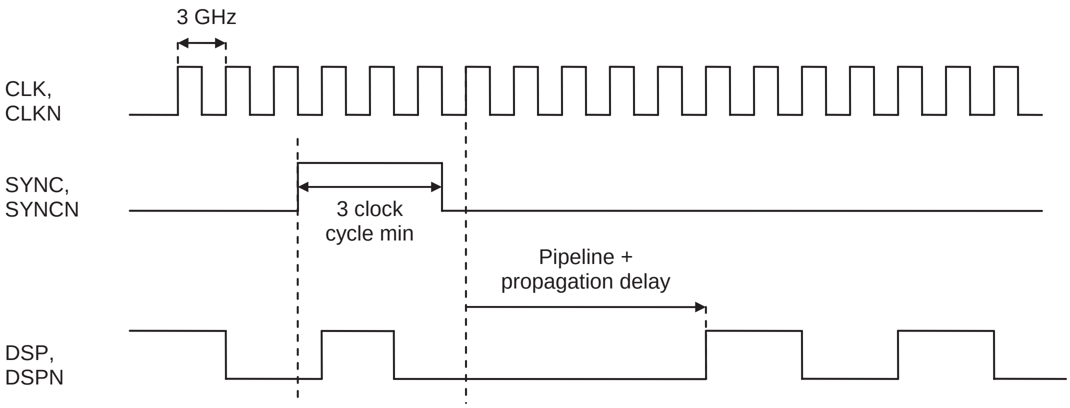


Figure 4-18. Reset Timing Diagram (2:1 MUX)



4.10 Gain Adjust GA Function

This function allows you to adjust the internal gain of the DAC so that it can be always equal to unity gain.

The gain of the DAC can be adjusted by ±11% by tuning the voltage applied on GA by varying GA potential from 0 to $V_{CCA3.}$

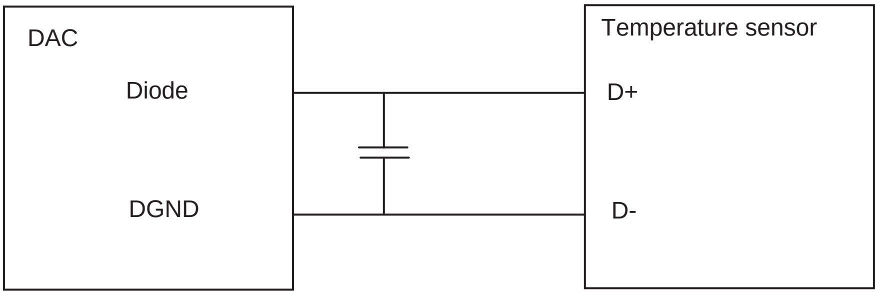
GA max is given for GA = 0 and GA min for GA = V_{CCA3}

4.11 Diode Function

A diode for die junction temperature monitoring is available in this DAC. It is constituted by an ESD diode. In order to monitor the die junction temperature of the DAC.

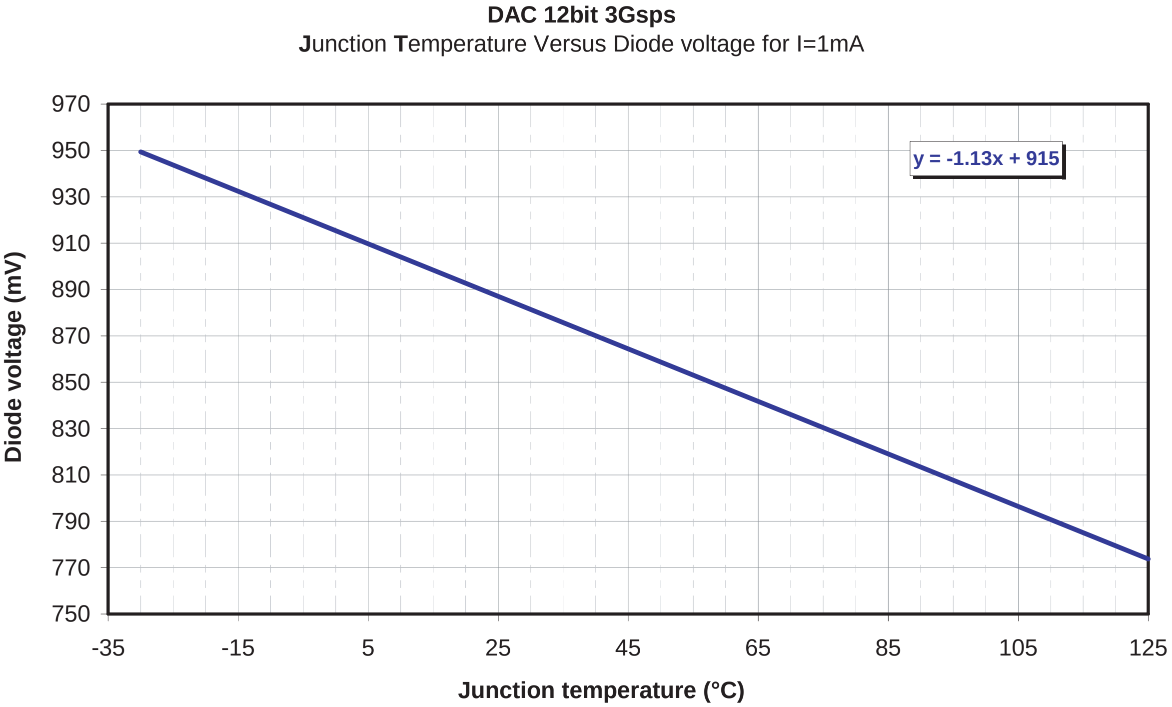
For the measurement of die junction temperature, you could use a temperature sensor (such as ADM1032).

Figure 4-19. Temperature DIODE Implementation



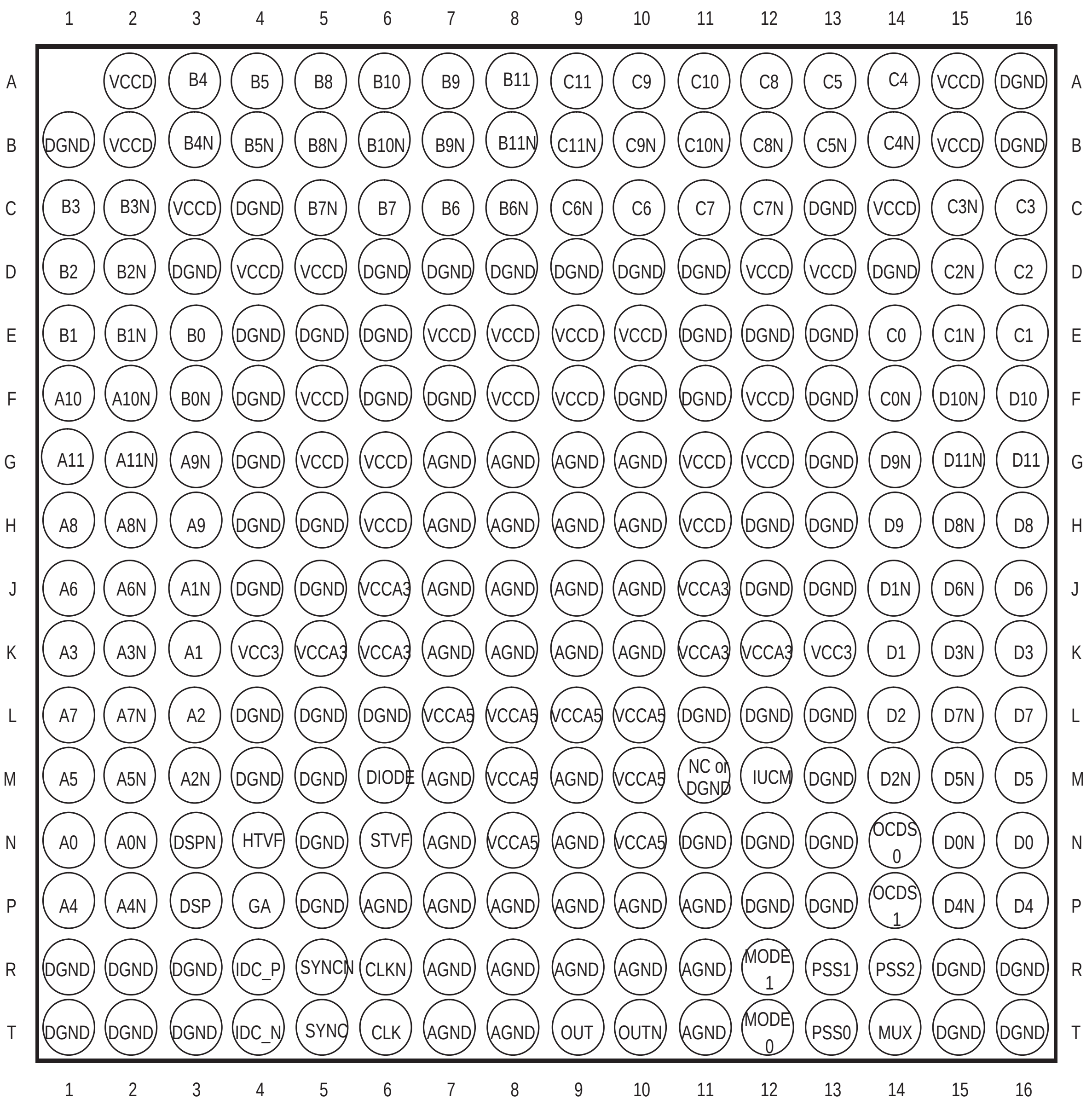
In characterization a current of 1mA has to be applied on the DIODE pin. The voltage across the DIODE pin and the DGND pin provides the junction temperature of the die thanks to the intrinsic diode characteristics provided in Figure 4-18 on page 31.

Figure 4-20. Diode Characteristics for Die Junction Monitoring



5. PIN Description

Figure 5-1. Pinout View fpBGA196 (Top View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		VCCD	B4	B5	B8	B10	B9	B11	C11	C9	C10	C8	C5	C4	VCCD	DGND	A
B	DGND	VCCD	B4N	B5N	B8N	B10N	B9N	B11N	C11N	C9N	C10N	C8N	C5N	C4N	VCCD	DGND	B
C	B3	B3N	VCCD	DGND	B7N	B7	B6	B6N	C6N	C6	C7	C7N	DGND	VCCD	C3N	C3	C
D	B2	B2N	DGND	VCCD	VCCD	DGND	DGND	DGND	DGND	DGND	DGND	VCCD	VCCD	DGND	C2N	C2	D
E	B1	B1N	B0	DGND	DGND	DGND	VCCD	VCCD	VCCD	VCCD	DGND	DGND	DGND	C0	C1N	C1	E
F	A10	A10N	B0N	DGND	VCCD	DGND	DGND	VCCD	VCCD	DGND	DGND	VCCD	DGND	C0N	D10N	D10	F
G	A11	A11N	A9N	DGND	VCCD	VCCD	AGND	AGND	AGND	AGND	VCCD	VCCD	DGND	D9N	D11N	D11	G
H	A8	A8N	A9	DGND	DGND	VCCD	AGND	AGND	AGND	AGND	VCCD	DGND	DGND	D9	D8N	D8	H
J	A6	A6N	A1N	DGND	DGND	VCCA3	AGND	AGND	AGND	AGND	VCCA3	DGND	DGND	D1N	D6N	D6	J
K	A3	A3N	A1	VCC3	VCCA3	VCCA3	AGND	AGND	AGND	AGND	VCCA3	VCCA3	VCC3	D1	D3N	D3	K
L	A7	A7N	A2	DGND	DGND	DGND	VCCA5	VCCA5	VCCA5	VCCA5	DGND	DGND	DGND	D2	D7N	D7	L
M	A5	A5N	A2N	DGND	DGND	DIODE	AGND	VCCA5	AGND	VCCA5	NC or DGND	IUCM	DGND	D2N	D5N	D5	M
N	A0	A0N	DSPN	HTVF	DGND	STVF	AGND	VCCA5	AGND	VCCA5	DGND	DGND	DGND	OCDS0	D0N	D0	N
P	A4	A4N	DSP	GA	DGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	DGND	OCDS1	D4N	D4	P
R	DGND	DGND	DGND	IDC_P	SYNCN	CLKN	AGND	AGND	AGND	AGND	AGND	MODE1	PSS1	PSS2	DGND	DGND	R
T	DGND	DGND	DGND	IDC_N	SYNC	CLK	AGND	AGND	OUT	OUTN	AGND	MODE0	PSS0	MUX	DGND	DGND	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Table 5-1. Pinout Table CLGA255

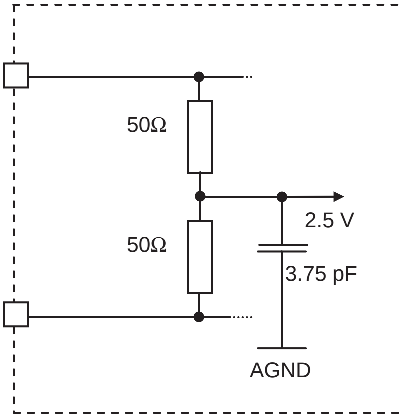
Signal Name	Pin number	Description	Dir	Equivalent simplified schematics
Power supplies				
VCCA5	L7, L8, L9, L10, M8, M10, N8, N10	5V analogue power supplies Referenced to AGND	NA	
VCCA3	J6, J11, K4, K5, K6, K11, K12, K13	3.3V analogue power supply Referenced to AGND	NA	
VCCD	A2, A15, B2, B15, C3, C14, D4, D5, D12, D13, E7, E8, E9, E10, F5, F8, F9, F12, G5, G6, G11, G12, H6, H11	3.3V digital power supply Referenced to DGND	NA	
AGND	G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M7, M9, N7, N9, P6, P7, P8, P9, P10, P11, R7, R8, R9, R10, R11, T7, T8, T11,	Analogue Ground AGND plane should be separated from DGND on the board (the two planes can be connected by 0 ohm resistors)	NA	
DGND	A16, B1, B16, C4, C13, D3, D6, D7, D8, D9, D10, D11, D14, E4, E5, E6, E11, E12, E13, F4, F6, F7, F10, F11, F13, G4, G13, H4, H5, H12, H13, J4, J5, J12, J13, L4, L5, L6, L11, L12, L13, M4, M5, M13, N5, N11, N12, N13, P5, P12, P13, R1, R2, R3, R15, R16, T1, T2, T3, T15, T16	Digital Ground AGND plane should be separated from DGND on the board (the two planes can be connected by 0 ohm resistors)	NA	
Clock signals				
CLK, CLKN	T6, R6	Sampling clock signal input (In-phase and inverted phase)	I	
DSP, DSPN	P3, N3	Output clock (in-phase and inverted phase	O	

Table 5-1. Pinout Table CLGA255 (Continued)

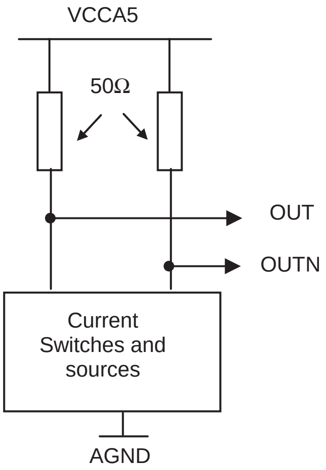
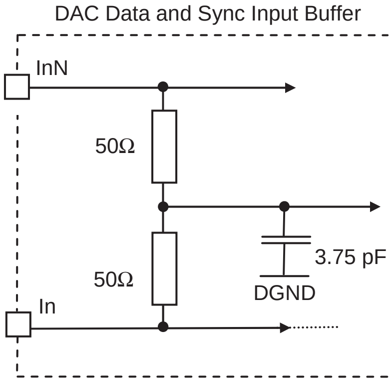
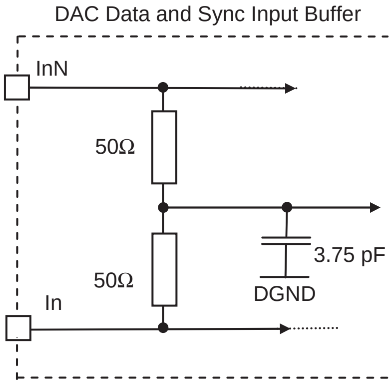
Signal Name	Pin number	Description	Dir	Equivalent simplified schematics
Analog Output Signal				
OUT, OUTN	T9, T10	In phase and inverted phase analogue output signal (differential termination required)	O	
Digital Input Signals				
A0, A0N A1, A1N A2, A2N A3, A3N A4, A4N A5, A5N A6, A6N A7, A7N A8, A8N A9, A9N A10, A10N A11, A11N	N1, N2 K3, J3 L3, M3 K1, K2 P1, P2 M1, M2 J1, J2 L1, L2 H1, H2 H3, G3 F1, F2 G1, G2	Differential digital inputs Port A Data A0, A0N is the LSB Data A11, A11N is the MSB	I	
B0, B0N B1, B1N B2, B2N B3, B3N B4, B4N B5, B5N B6, B6N B7, B7N B8, B8N B9, B9N B10, B10N B11, B11N	E3, F3 E1, E2 D1, D2 C1, C2 A3, B3 A4, B4 C7, C8 C6, C5 A5, B5 A7, B7 A6, B6 A8, B8	Differential digital inputs Port B Data B0, B0N is the LSB Data B11, B11N is the MSB	I	

Table 5-1. Pinout Table CLGA255 (Continued)

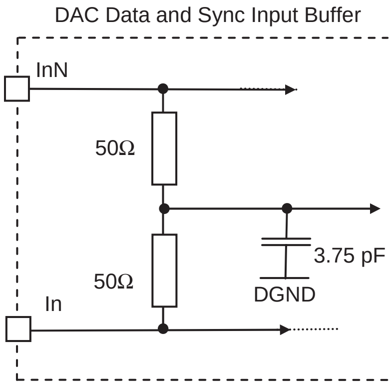
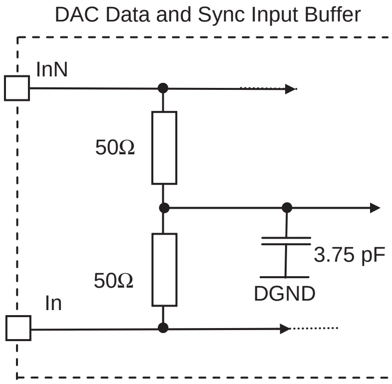
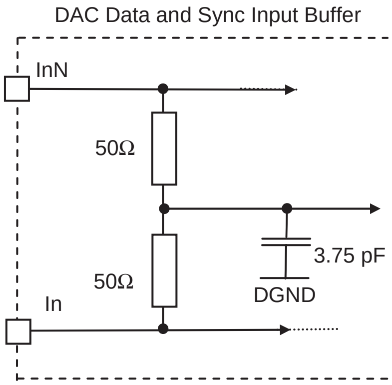
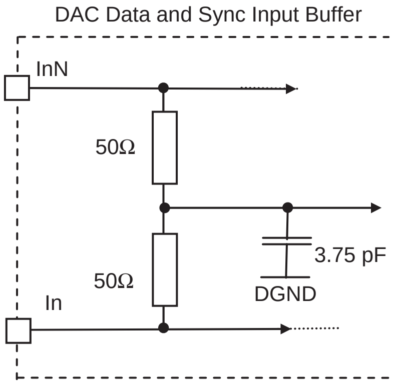
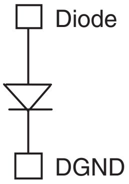
Signal Name	Pin number	Description	Dir	Equivalent simplified schematics
C0, C0N C1, C1N C2, C2N C3, C3N C4, C4N C5, C5N C6, C6N C7, C7N C8, C8N C9, C9N C10, C10N C11, C11N	E14, F14 E16, E15 D16, D15 C16, C15 A14, B14 A13, B13 C10, C9 C11, C12 A12, B12 A10, B10 A11, B11 A9, B9	Differential digital inputs Port C Data C0, C0N is the LSB Data C11, C11N is the MSB	I	
D0, D0N D1, D1N D2, D2N D3, D3N D4, D4N D5, D5N D6, D6N D7, D7N D8, D8N D9, D9N D10, D10N D11, D11N	N16, N15 K14, J14 L14, M14 K16, K15 P16, P15 M16, M15 J16, J15 L16, L15 H16, H15 H14, G14 F16, F15 G16, G15	Differential digital inputs Port D Data D0, D0N is the LSB Data D11, D11N is the MSB	I	
Control Signals				
HTVF	N4	Setup time violation flag	O	
STVF	N6	Hold time violation flag	O	
IDC_P IDC_N	R4 T4	Input data check	I	
PSS0 PSS1 PSS2	T13 R13 R14	Phase Shift Select (PSS2 is the MSB)	I	

Table 5-1. Pinout Table CLGA255 (Continued)

Signal Name	Pin number	Description	Dir	Equivalent simplified schematics
MODE0 MODE1	T12 R12	DAC Mode selection bits: - RTZ - NRZ - Narrow RTZ - RF	I	
OCDS0 OCDS1	N14 P14	Output Clock Division Select = these bits allow to select the clock division factor applied on the DSP, DSPN signal. - By 2N (OCDS0 = 0, OCDS1 = 0) - By 2N*2 (OCDS0 = 1, OCDS1 = 0) - By 2N*4 (OCDS0 = 1, OCDS1 = 0) - By 2N*8 (OCDS0 = 1, OCDS1 = 1) With N = MUX ratio	I	
SYNC, SYNCN	T5, R5	In phase and Inverted phase reset signal	I	 DAC Data and Sync Input Buffer
GA	P4	Gain adjust	I	
MUX	T14	MUX selection:	I	
IUCM	M12	Input underclocking mode	I	
Diode	M6	Diode for die junction temperature monitoring function	I	
NC	M11	No connected pin		

6. Characterization Results

Unless otherwise specified results are given at room temperature (Tj ~ 60°C), nominal power supply, in 4:1 MUX mode, gain at nominal setting.

6.1 Static Performances

6.1.1 DC Gain Characterization

Figure 6-1. DAC DC Gain vs Gain Adjust (Measured in NRZ Mode)

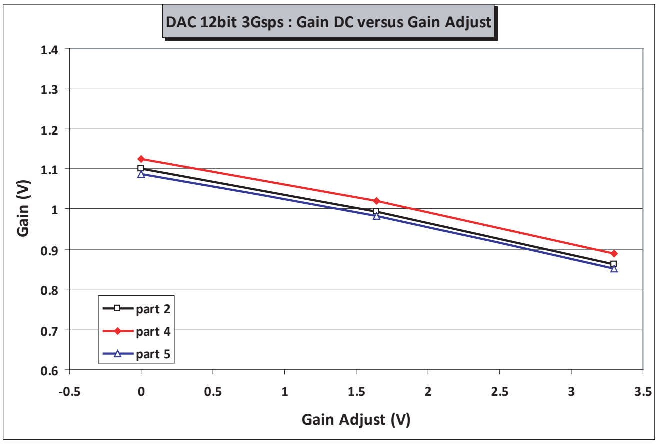


Figure 6-2. DAC DC Gain Drift from Unity Gain vs Temperature (Measured in NRZ Mode)

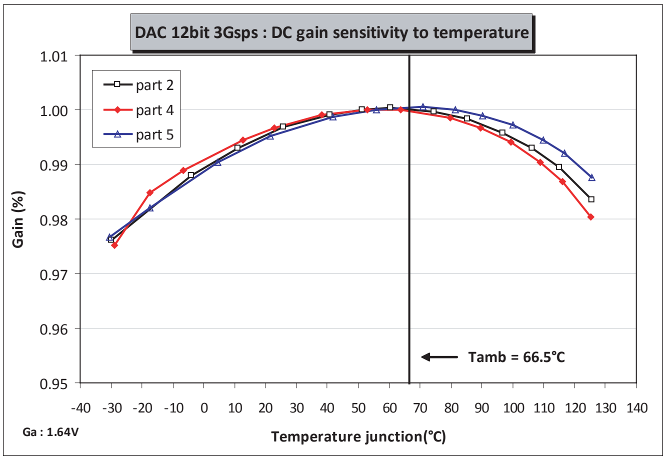
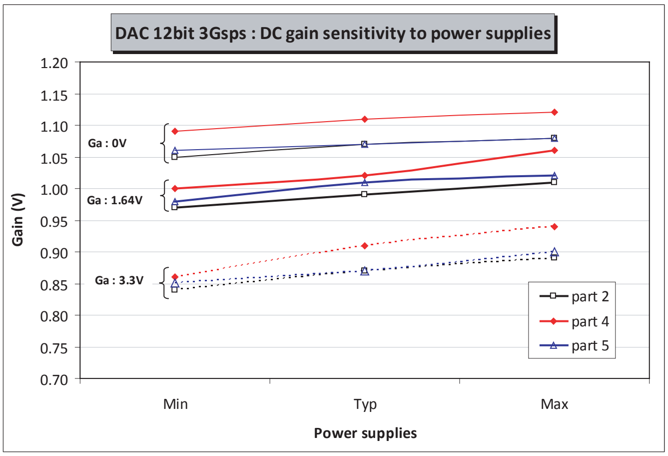


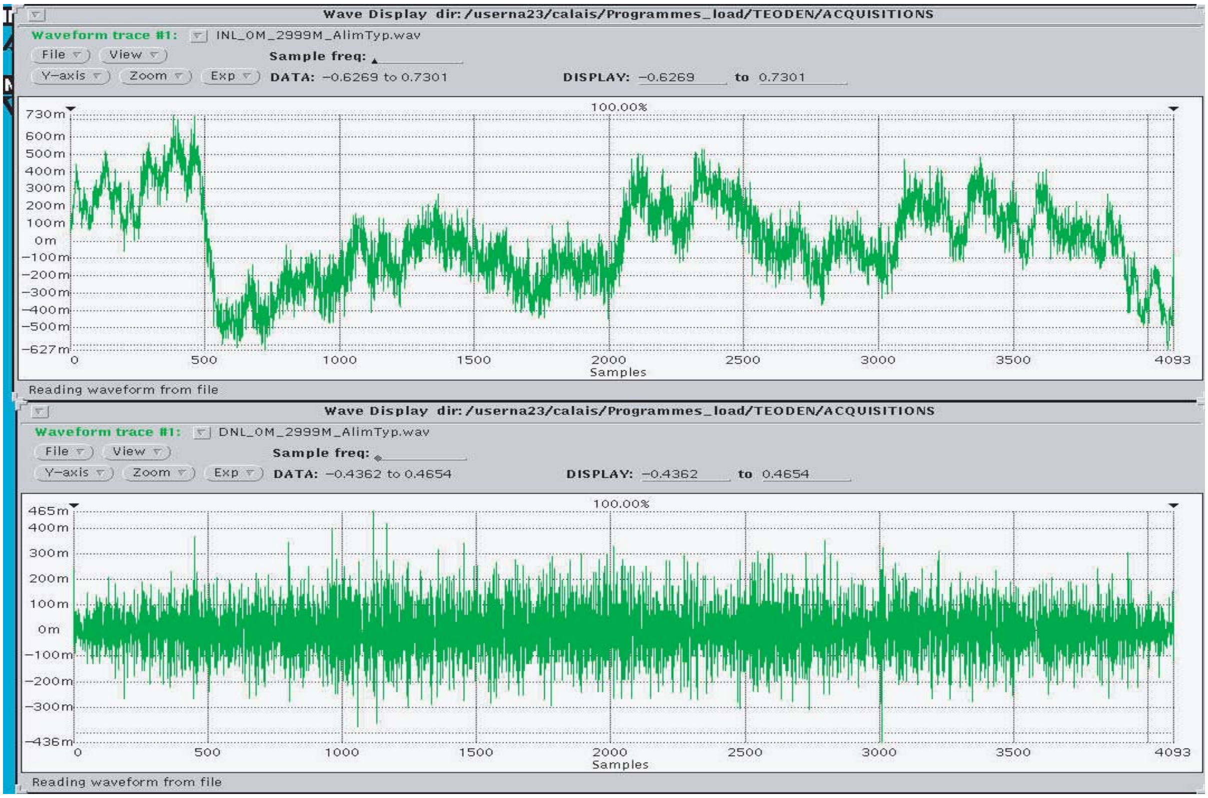
Figure 6-3. DC Gain Sensitivity to Power Supply (Measured in NRZ Output Mode)



Conditions: room temperature, supply levels:
- Min: VCCA: 4.75V // VCCA3 = VCCD = 3.15V
- Typ: VCCA: 5V // VCCA3 = VCCD = 3.3V
- Max: VCCA: 5.25V // VCCA3 = VCCD = 3.45V

6.1.2 Static Leariy

Figure 6-4. INL/DNL Measurement at Fout = 100 kHz and 3 GSps



Wave Display dir: /userna23/calais/Programmes_load/TEODEN/ACQUISITIONS

Waveform trace #1: INL_0M_2999M_AlimTyp.wav

Sample freq:

DATA: −0.6269 to 0.7301

DISPLAY: −0.6269 to 0.7301

Reading waveform from file

Wave Display dir: /userna23/calais/Programmes_load/TEODEN/ACQUISITIONS

Waveform trace #1: DNL_0M_2999M_AlimTyp.wav

Sample freq:

DATA: −0.4362 to 0.4654

DISPLAY: −0.4362 to 0.4654

Reading waveform from file

INL reflects at true 12 bit DAC.

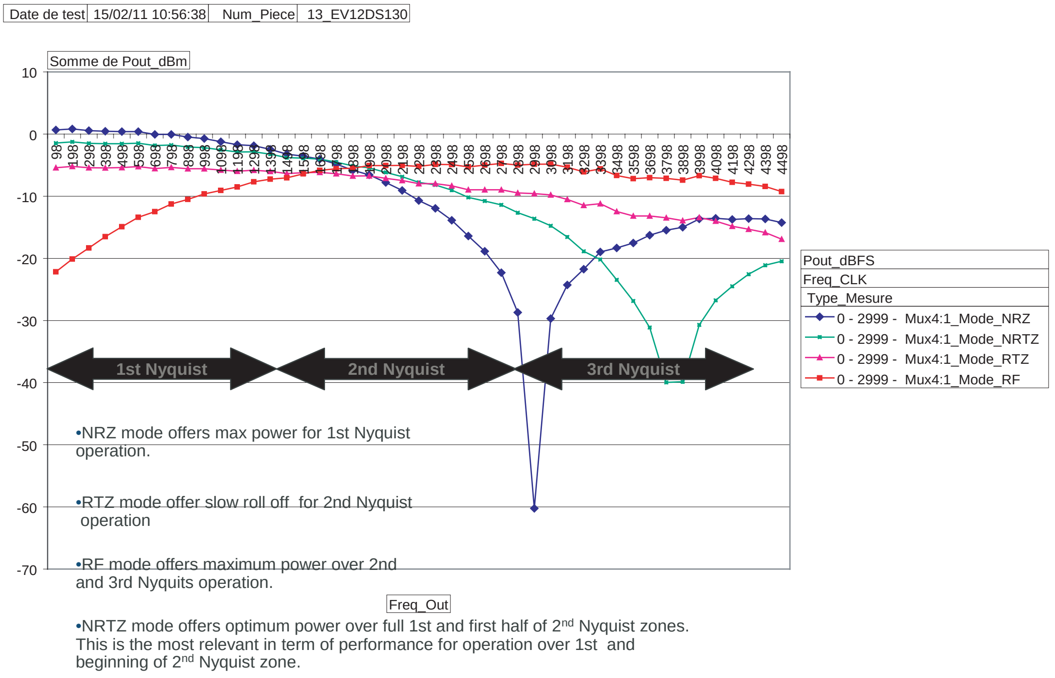
Low DNL values reflect a strickly monotonous 12 bit DAC.

6.2 AC Performances

6.2.1 Available Output Power vs Fout.

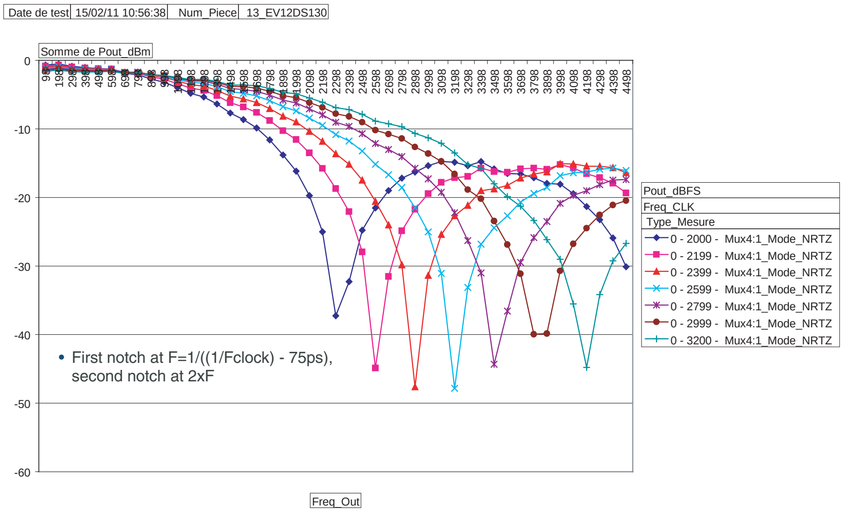
The following plots summarize characterization of one device on industrial tester, for a Fout sweep from 98 MHz to 4498 MHz (step 100 MHz).

Figure 6-5. Available Pout vs Fout from 98 MHz to 4498 MHz in the 4 Output Modes at 3 GSps



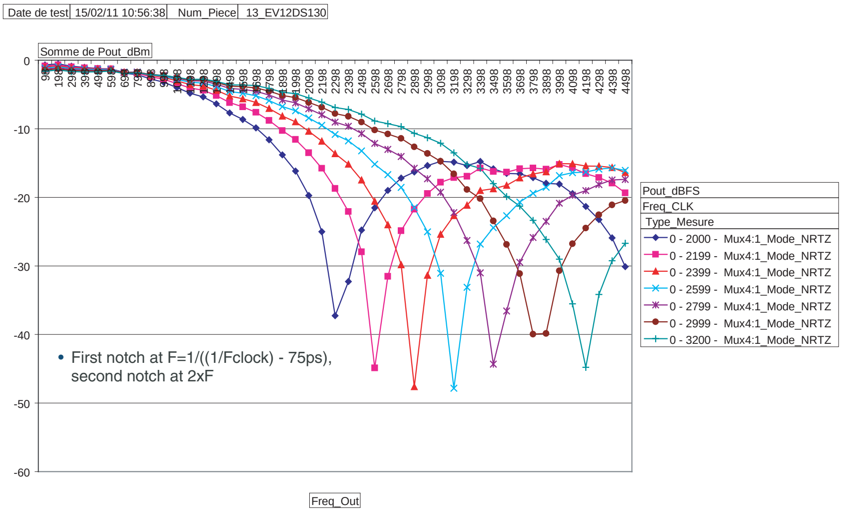
- NRZ mode offers max power for 1st Nyquist operation.
- RTZ mode offer slow roll off for 2nd Nyquist operation
- RF mode offers maximum power over 2nd and 3rd Nyquits operation.
- NRTZ mode offers optimum power over full 1st and first half of 2nd Nyquist zones. This is the most relevant in term of performance for operation over 1st and beginning of 2nd Nyquist zone.

Figure 6-6. Available Pout vs Fout from 98 MHz to 4498 MHz and from 2 GSps to 3.2 GSps in NRZ Mode



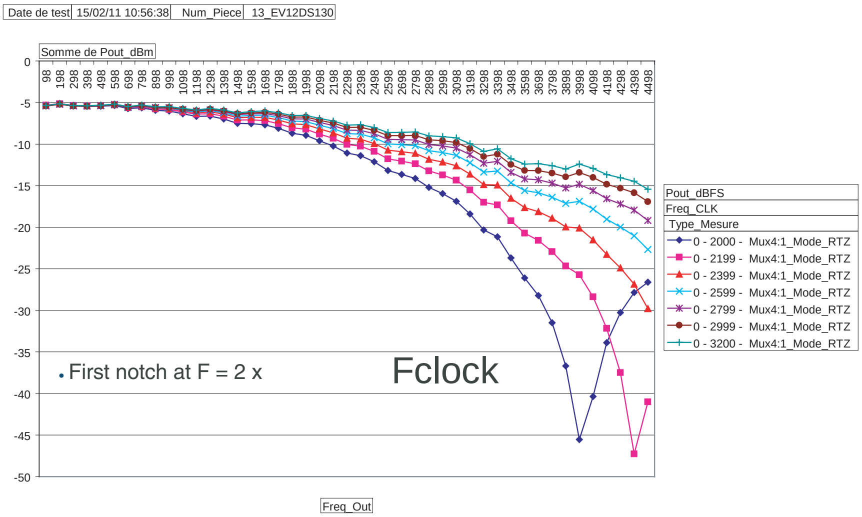
- First notch at F=1/((1/Fclock) - 75ps), second notch at 2xF

Figure 6-7. Available Pout vs Fout from 98 MHz to 4498 MHz and from 2 GSps to 3.2 GSps in NRTZ Mode



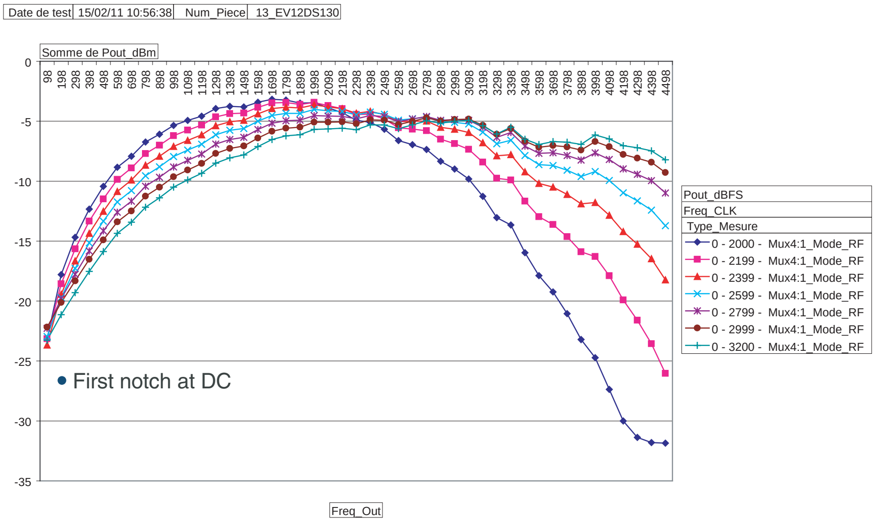
- First notch at F=1/((1/Fclock) - 75ps), second notch at 2xF

Figure 6-8. Available Pout vs Fout from 98 MHz to 4498 MHz and from 2 GSps to 3.2 GSps in RTZ Mode



- First notch at F = 2 x Fclock

Figure 6-9. Available Pout vs Fout from 98 MHz to 4498 MHz and from 2 GSps to 3.2 GSps in RF Mode



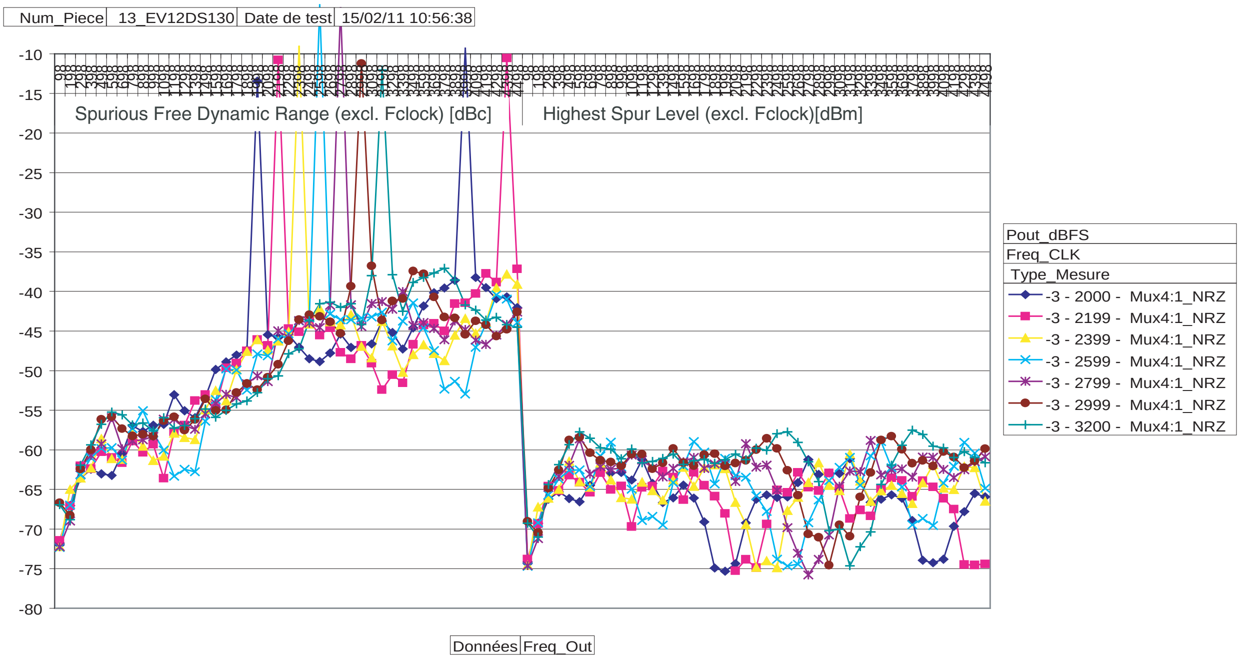
- First notch at DC

6.2.2 Single Tone Measurements

The following plots summarize characterization of one device on industrial tester in MUX4:1 mode, for an Fout sweep from 98 MHz to 4498 MHz (step 100 MHz).

The left side of the plot gives SFDR expressed in dBc and the right side gives HSL (Highest Spur Level excluding Fclock spur) expressed in dBm.

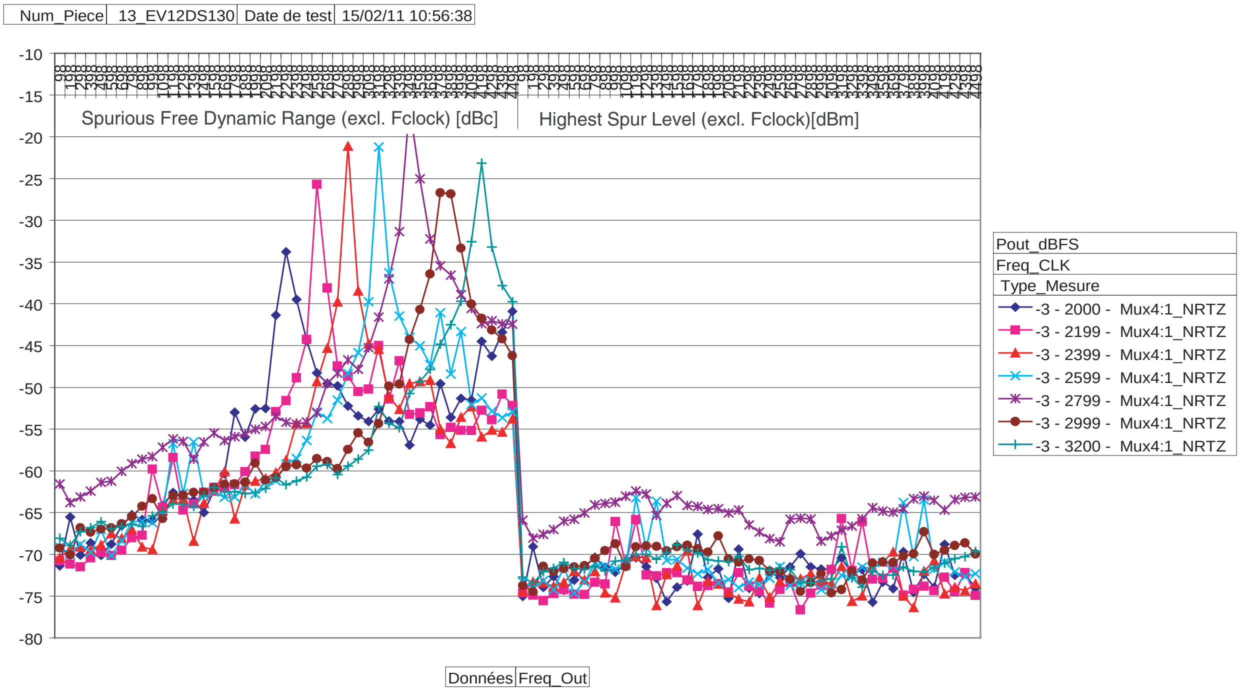
Figure 6-10. SFDR and HSL in NRZ mode at –3 dBFS for sampling rate from 2000 MSps to 3200 MSps



NRZ mode is only relevant for Fout below 400 MHz.

The spikes in the SFDR are caused by normalization artifacts due to the Sinc(x) null.

Figure 6-11. SFDR and HSL in NRTZ mode at –3 dBFS for sampling rate from 2000 MSps to 3200 MSps

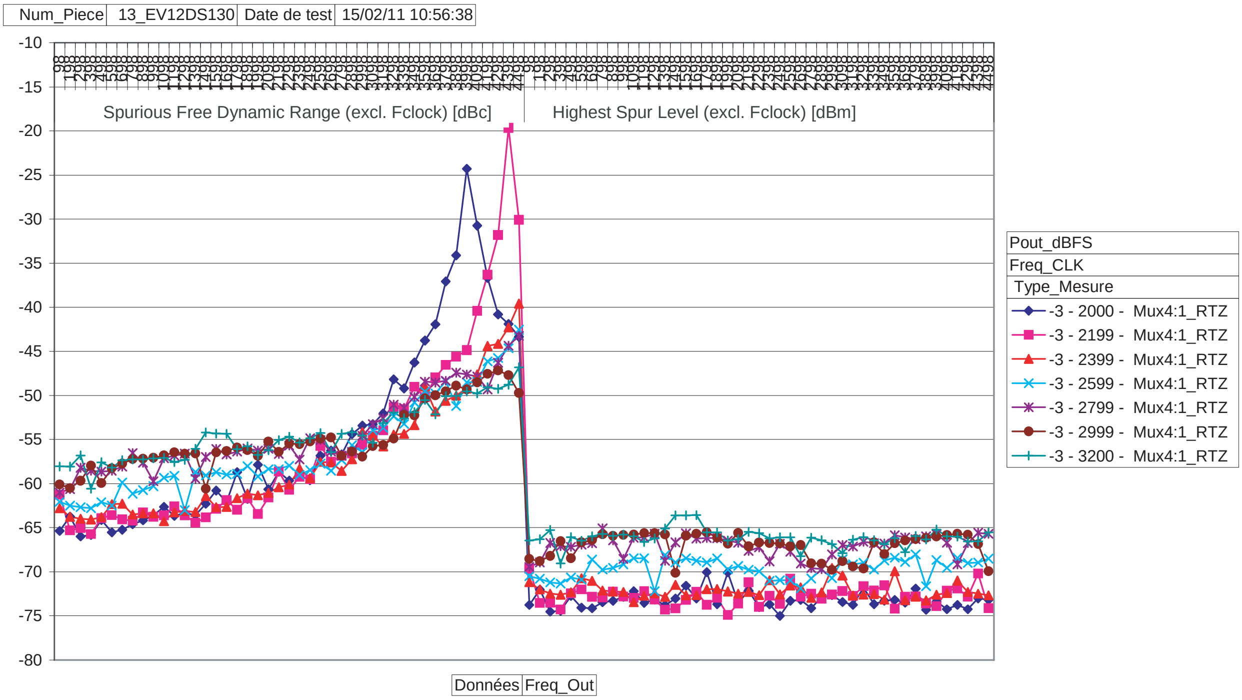


N

NRTZ mode brings significant improvement regarding NRZ mode. This mode concentrates the benefits of both NRZ mode (high power available) and RTZ mode (extended available dynamic range).

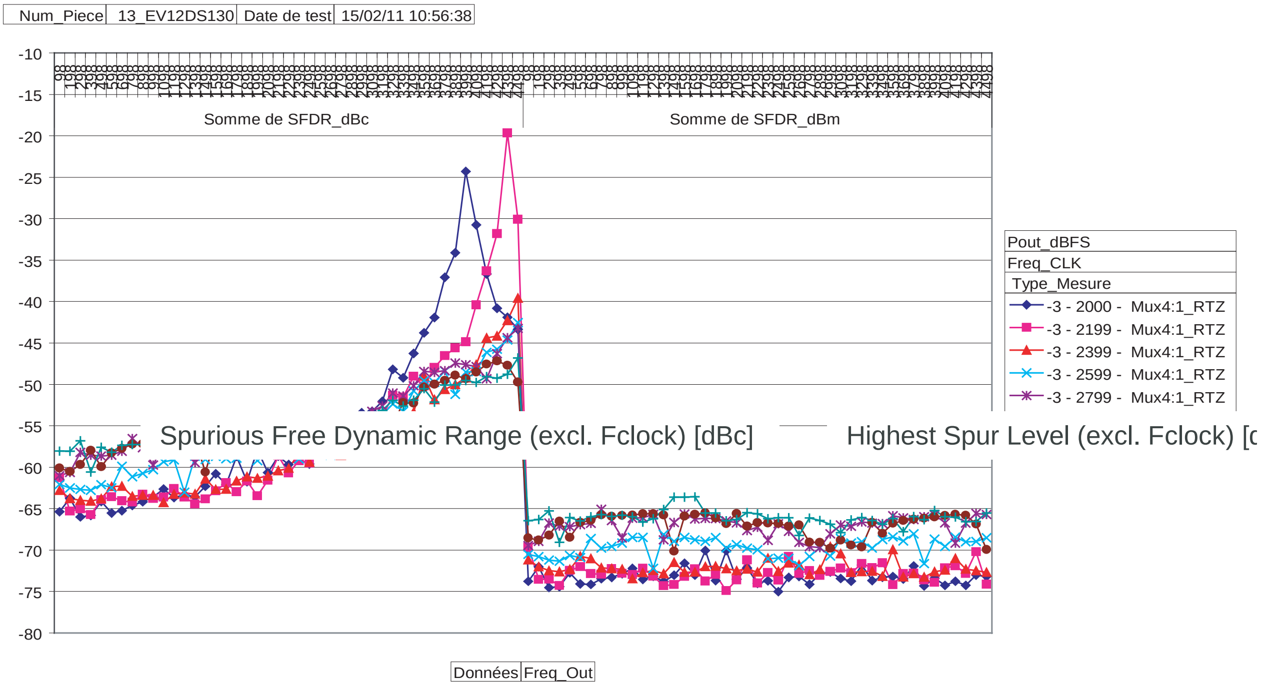
The spikes in the SFDR are caused by normalization artifacts due to the Sinc(x) null.

Figure 6-12. SFDR and HSL in RTZ Mode at –3 dBFS for Sampling Rate from 2000 MSps to 3200 MSps



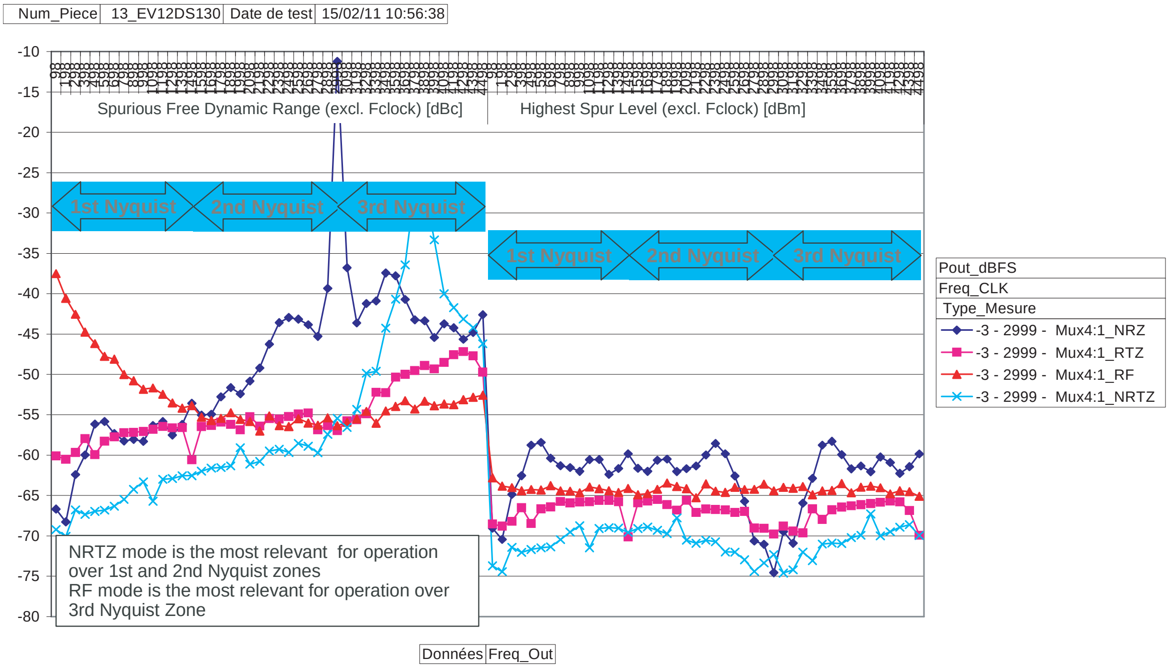
RTZ mode allows for operation over the 3 first Nyquist zones.
In first and beginning of second Nyquist zone NRTZ mode is mode relevant. The spikes in the SFDR are caused by normalization artifacts due to the Sinc(x) null.

Figure 6-13. SFDR and HSL in RF Mode at –3 dBFS for Sampling Rate from 2000 MSps to 3200 MSps



RF mode allows for operation over 3^{rd} Nyquist zones. Performances are not sensitive to output level.
Performance roll off occurs beyond 3000 MSps.

Figure 6-14. Comparison of the 4 Output Modes at 2999 MSps and at –3 dBFS: SFDR and HSL



NRZ is interesting only at the very beginning of the first Nyquist zone.

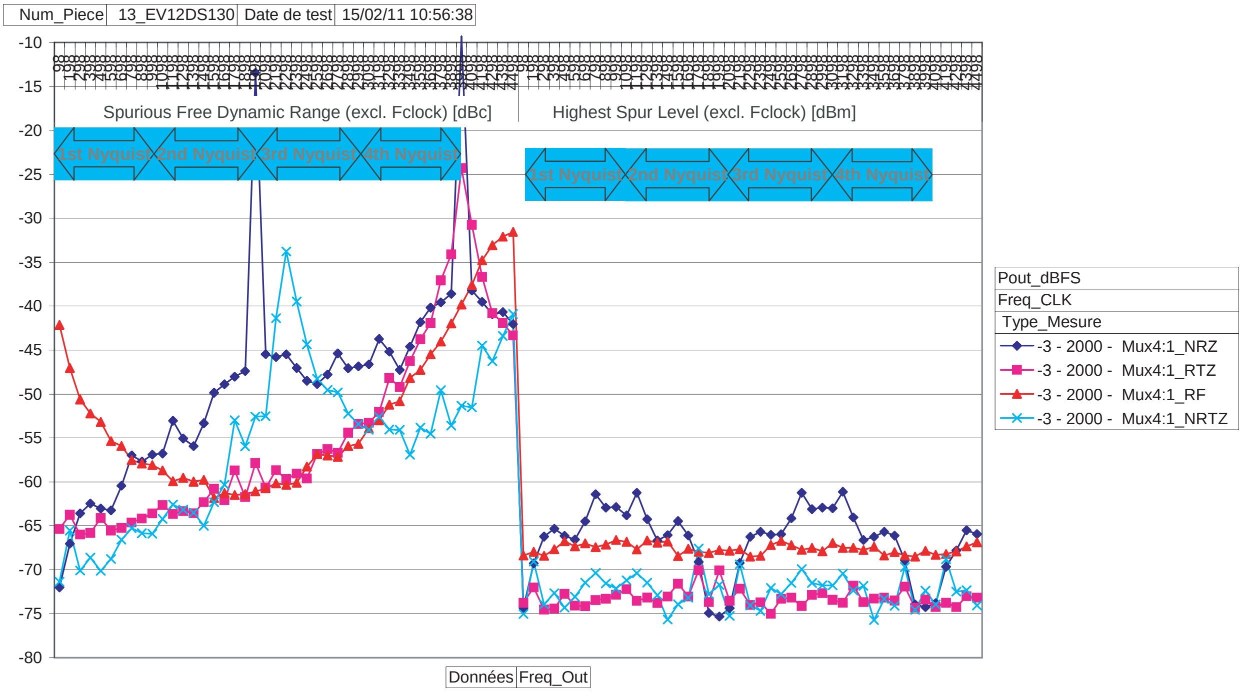
NRTZ is relevant over 1st 2nd and 4th Nyquist zones.

RTZ is relevant over 2nd and 3rd Nyquist zones.

RF mode displays a good behavior over 2nd and 3rd Nyquist Zones.

The spikes in the SFDR are caused by normalization artifacts due to te Sinc(x) null

Figure 6-15. Comparison of the 4 Output Modes at 2000 MSps and –3 dBFS: SFDR and HSL



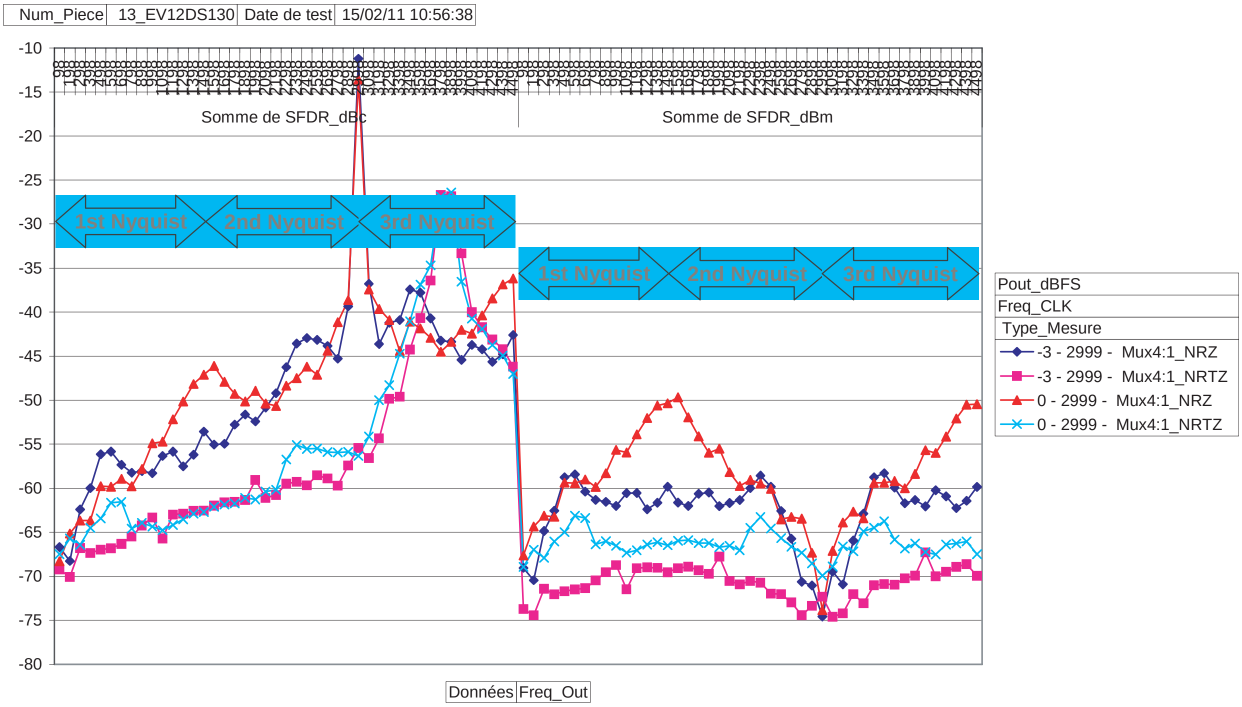
NRTZ is the most relevant over 1st Nyquist zone, 1st half of 2nd Nyquits zone and 4th Nyquist zone.

RF mode is the best choice for 2nd half of 2nd Nyquist Zone and 3rd Nyquist zone.

RTZ gives relevant performances over the three first Nyquist zones.

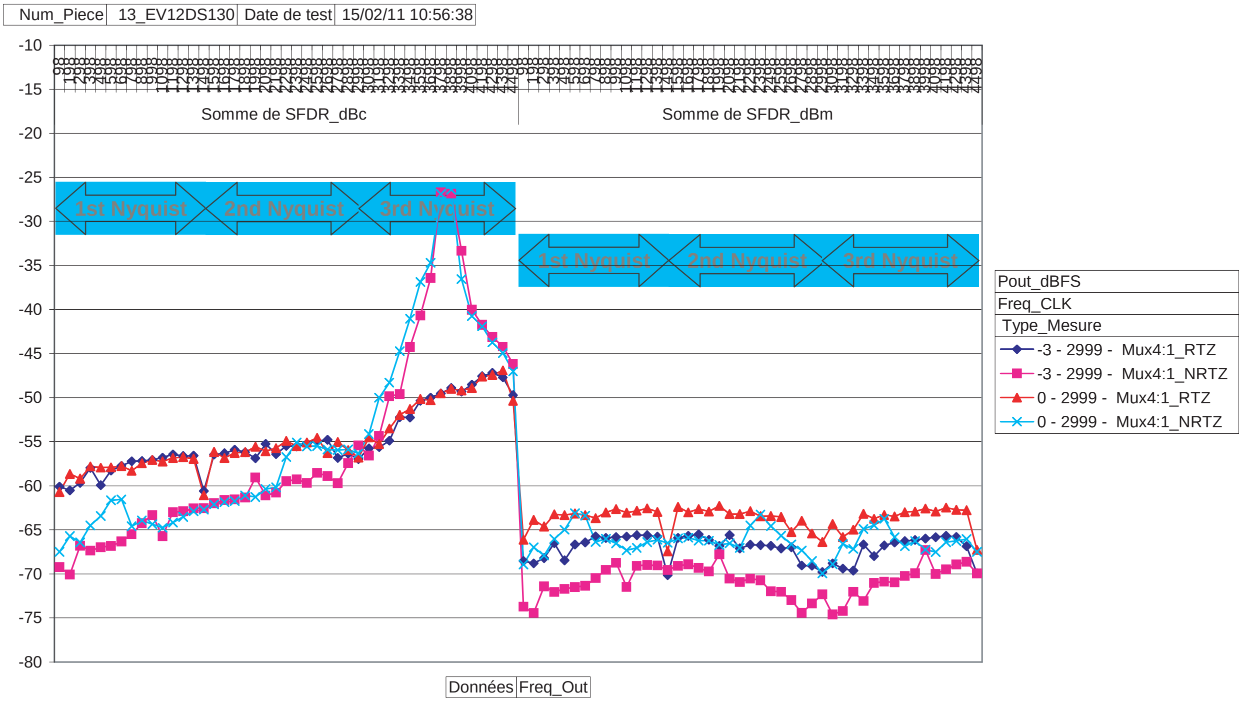
The spikes in the SFDR are caused by normalization artifacts due to the Sinc(x) null

Figure 6-16. Comparison of NRZ and NRTZ Modes at Full Scale and –3 dBFS at 2999 MSps: SFDR and HSL (Excluding Fclock)



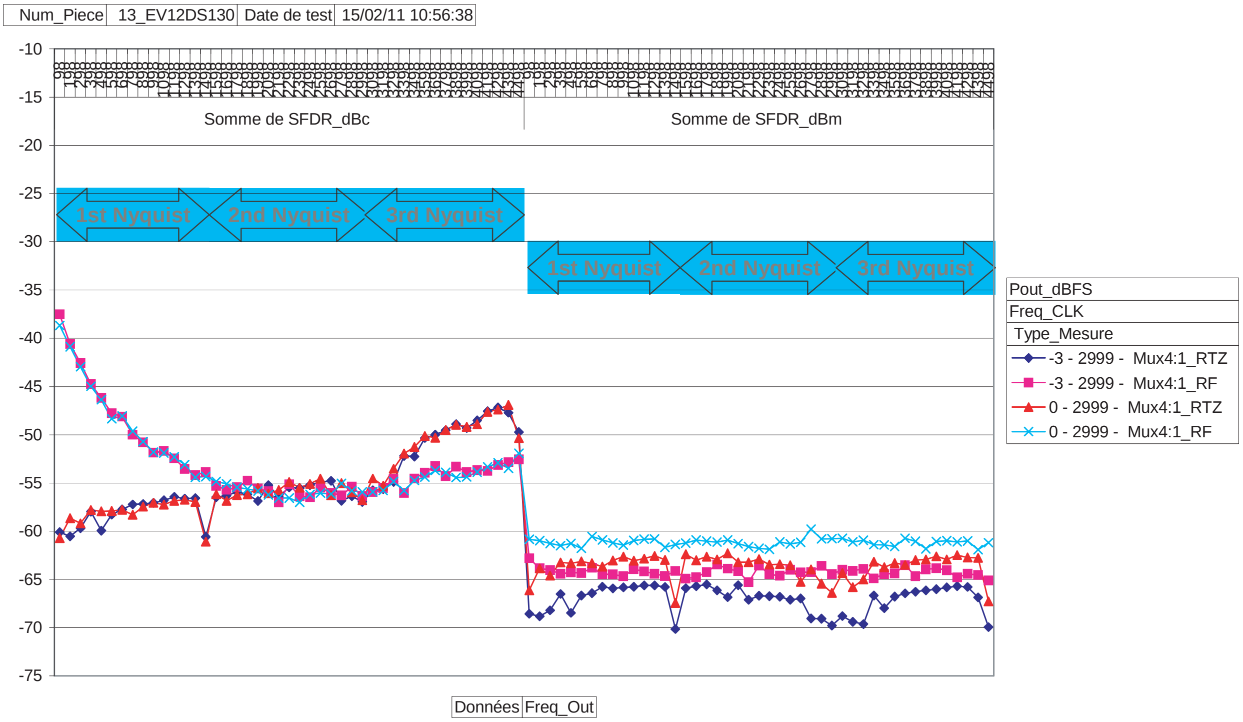
NRTZ gives better performances over 1st and 2nd Nyquist zone, and is much less sensitive to output level.

Figure 6-17. Comparison of NRTZ and RTZ Modes at Full Scale and –3 dBFS at 2999 MSps: SFDR and HSL



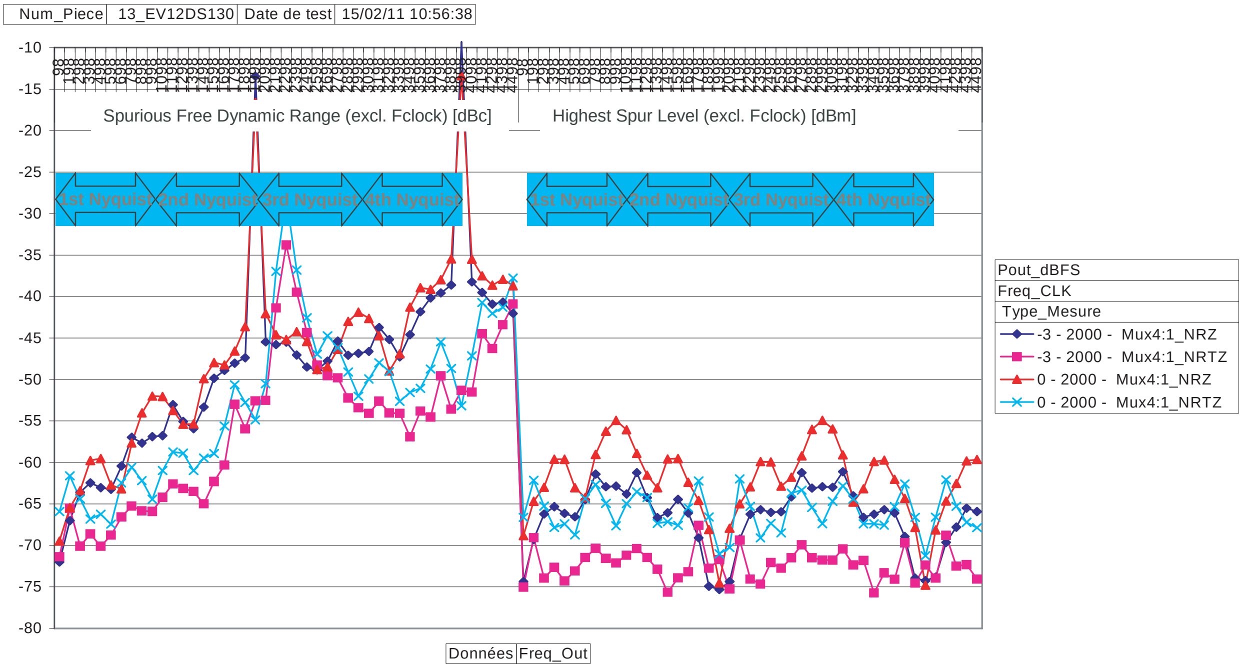
NRTZ is more relevant for 1st Nyquist zone and 1st half of 2nd Nyquist zone. Beyond middle of second Nyquist zone RTZ mode is more relevant.

Figure 6-18. Comparison of RTZ and RF Modes at Full Scale and –3 dBFS at 2999 MSps: SFDR and HSL



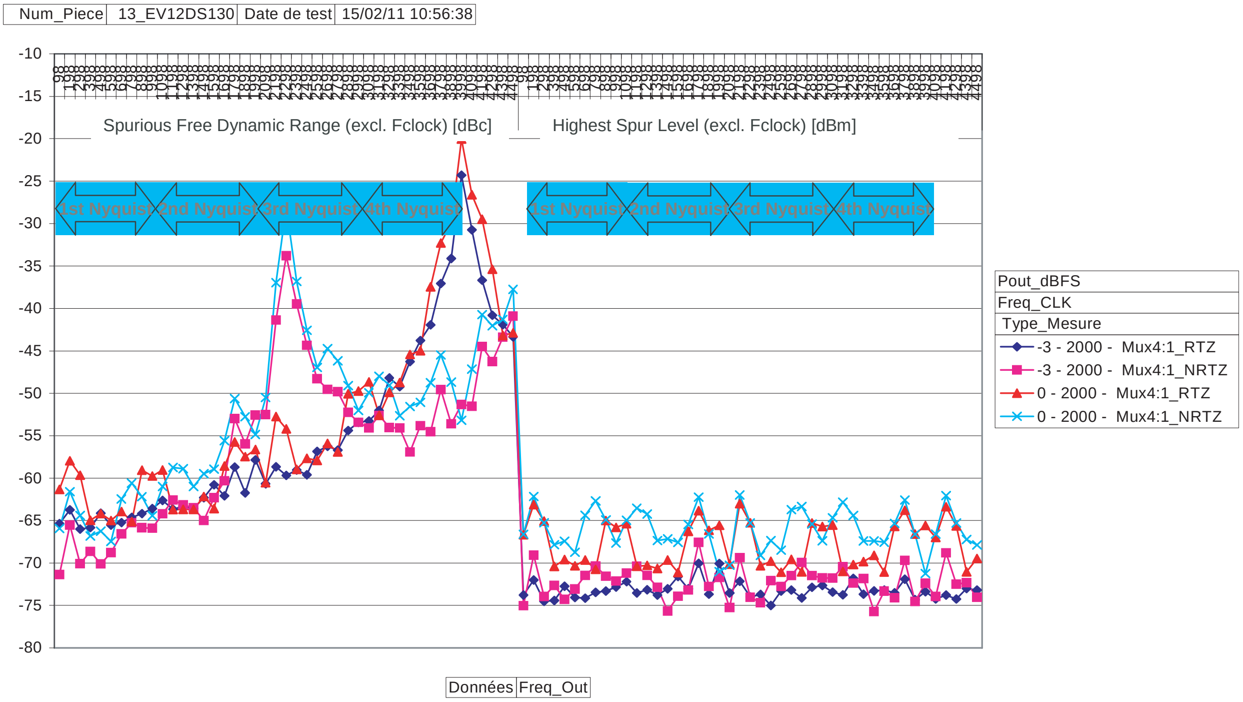
RF mode gives better performance over 3rd Nyquist zone.

Figure 6-19. Comparison of NRZ and NRTZ Modes at Full Scale and –3 dBFS at 2000 MSps: SFDR and HSL (Excluding Fclock)



NRTZ linearity is slightly improved reducing the sampling rate to 2000 MSps, possibility of operation over the 4th Nyquist zone is demonstrated.

Figure 6-20. Comparison of NTRZ and RTZ Modes at Full Scale and –3 dBFS at 2000 MSps: SFDR and HSL (Excluding Fclock)



NRTZ mode is relevant in 1st, 2nd Nyquist zones and is still usable over 4th Nyquist zone with SFDR in excess of 50 dBc.

6.2.3 Single Tone Measurements: Spectrum of a 1482 MHz Pattern Generated at 3 GSps

Measurements hereafter have been performed on an EV12DS130AZPY device, with FSU8 spectrum analyzer, using a 0.5 GHz-7 GHz balun on the analog output, generating a single tone at –3 dBFS.

Figure 6-21. Observation of the 1st and 2nd Nyquist Zones in Output Mode NRZ

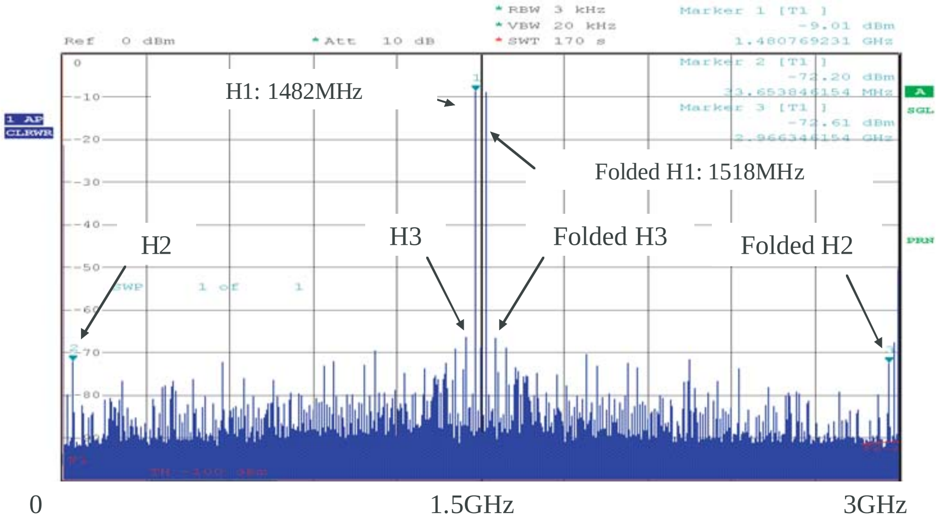


Figure 6-22. Observation of the 1st and 2nd Nyquist Zones in Output Mode NRTZ

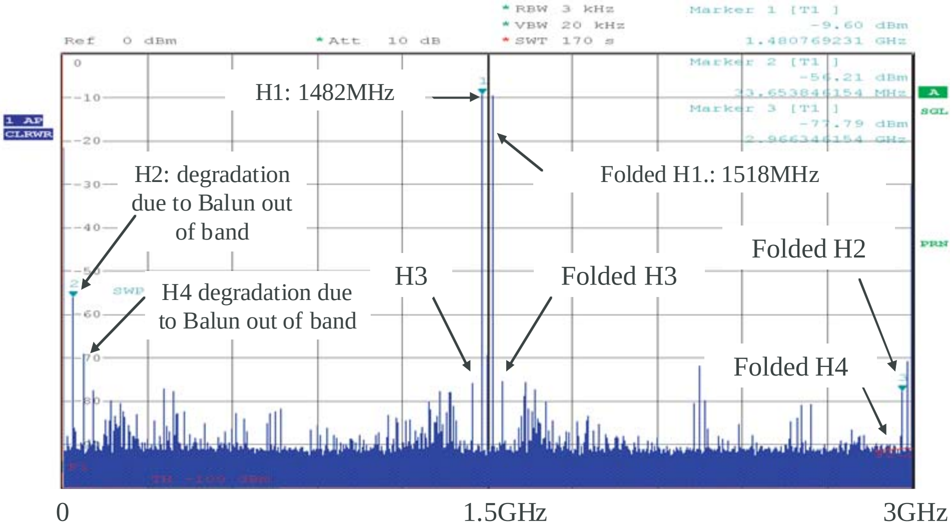
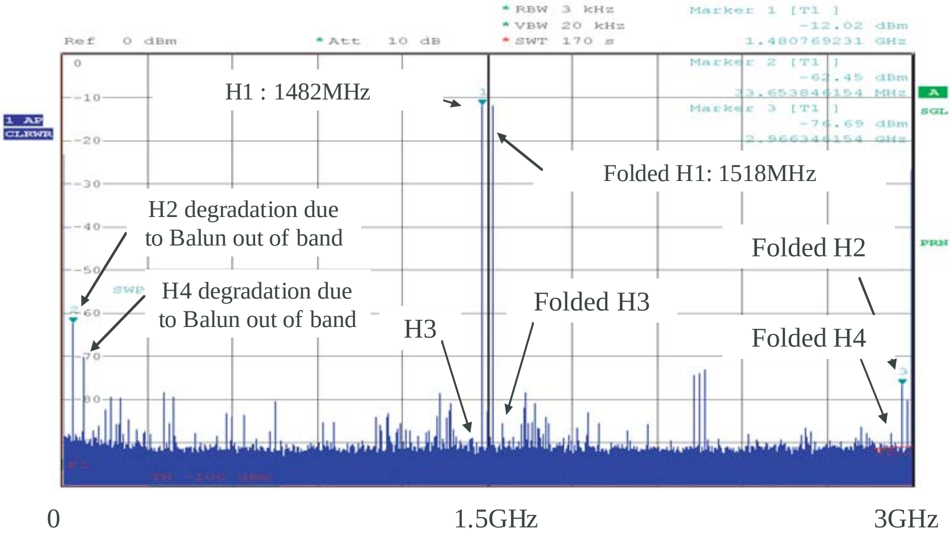


Figure 6-23. Observation of the 1st and 2nd Nyquist Zones in Output Mode RTZ



These three plots show clearly the benefit of NRTZ or RTZ modes over NRZ mode in term of spectral purity for tones generated beyond the 1st quarter of the first Nyquist zone. Further more it illustrates the dramatic degradations induced by an inappropriate Balun choice (part of the band of interest out of the specified domain of the Balun).

Following figures illustrate the possible improvement when using a more appropriate Balun.

The measurement are now performed in RTZ mode (which offers the best spectral purity), with FSEB spectrum analyzer, for a –3 dBFS tone generated at the same frequencies for Fclock and Fout, with different Baluns to perform the Differential to single conversion before spectrum analyzer.

Figure 6-24. Spectrum of the 1st Nyquist Zone, Output Mode RTZ, with a 0.5GHz to 7GHz Bandwidth Balun

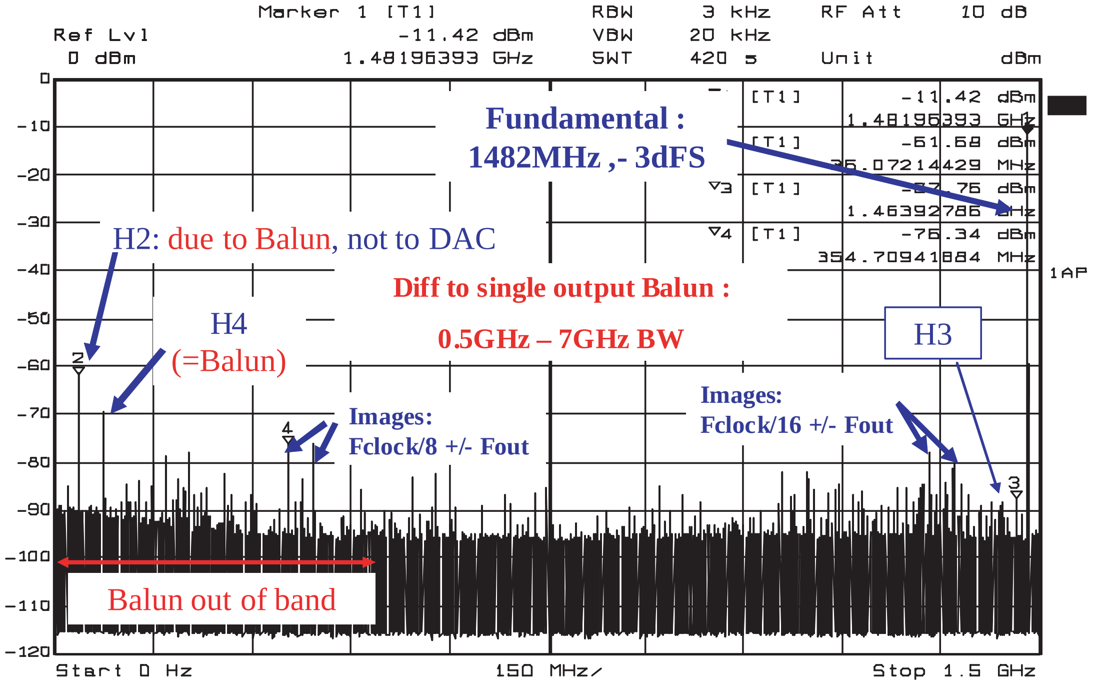


Figure 6-25. Spectrum of the 1st Nyquist zone, Output Mode RTZ, with a 0.5 MHz to 1.5 GHz Bandwidth Balun

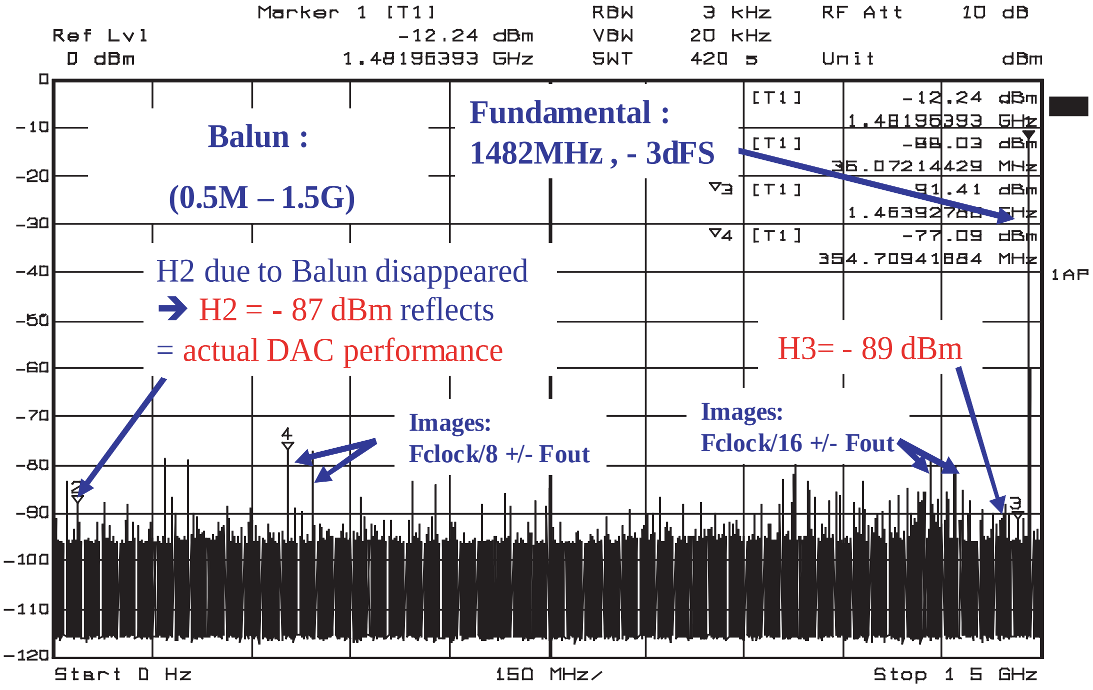
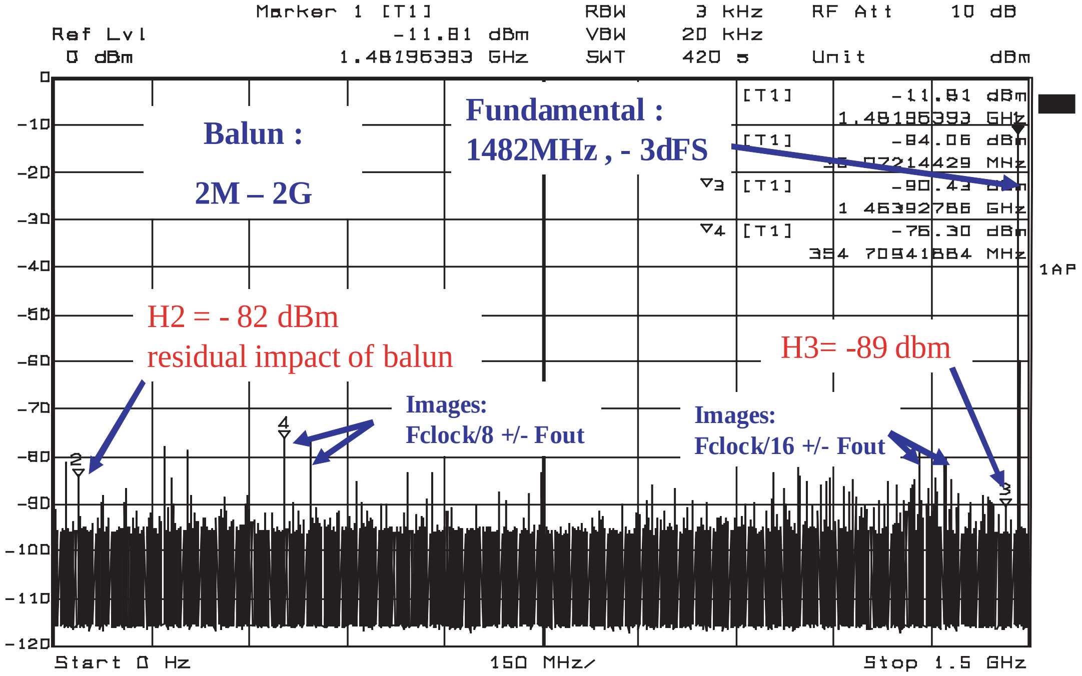


Figure 6-26. Spectrum of the 1st Nyquist Zone, Output Mode RTZ with a 2 MHz to 2GHz Bandwidth Balun



The impact of the output Balun choice on performance in 1st Nyquist Zone is confirmed.

As a consequence the board designer must be aware that optimum performance can be reached only when using a Balun optimal for the band of interest of the application. For operation in the first Nyquist zone it is recommended to select a Balun which is specified from less than 2 MHz to at least 1.5GHz. For operation in the 2nd or the 3rd Nyquits zone it is recommended to use a Balun specified from 0.5GHz to 7GHz.

For practical reason the industrial test is done with a 0.5GHz to 7GHz Balun, whatever the Nyquist zone observed, and therefore all specified values in single tone for the 1st Nyquist zone are pessimistic regarding the performance which can actually be reached using an optimal Balun.

Figures hereafter give spectrum obtained in 1st Nyquist zone in NRZ and NRTZ mode using an optimal Balun, on the same device with the same frequency couples, and indeed they display significant improvement.

Figure 6-27. Spectrum of the 1st Nyquist Zone, Output Mode NRZ, with a 0.5 MHz to 1.5GHz Bandwidth Balun

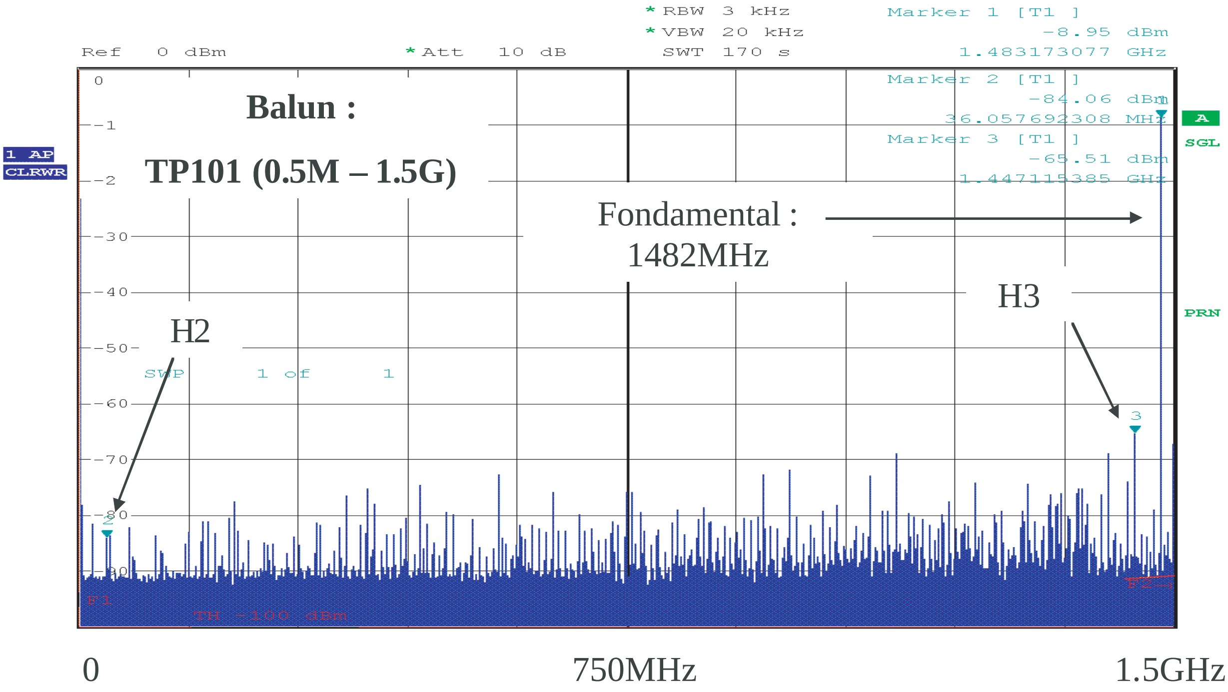
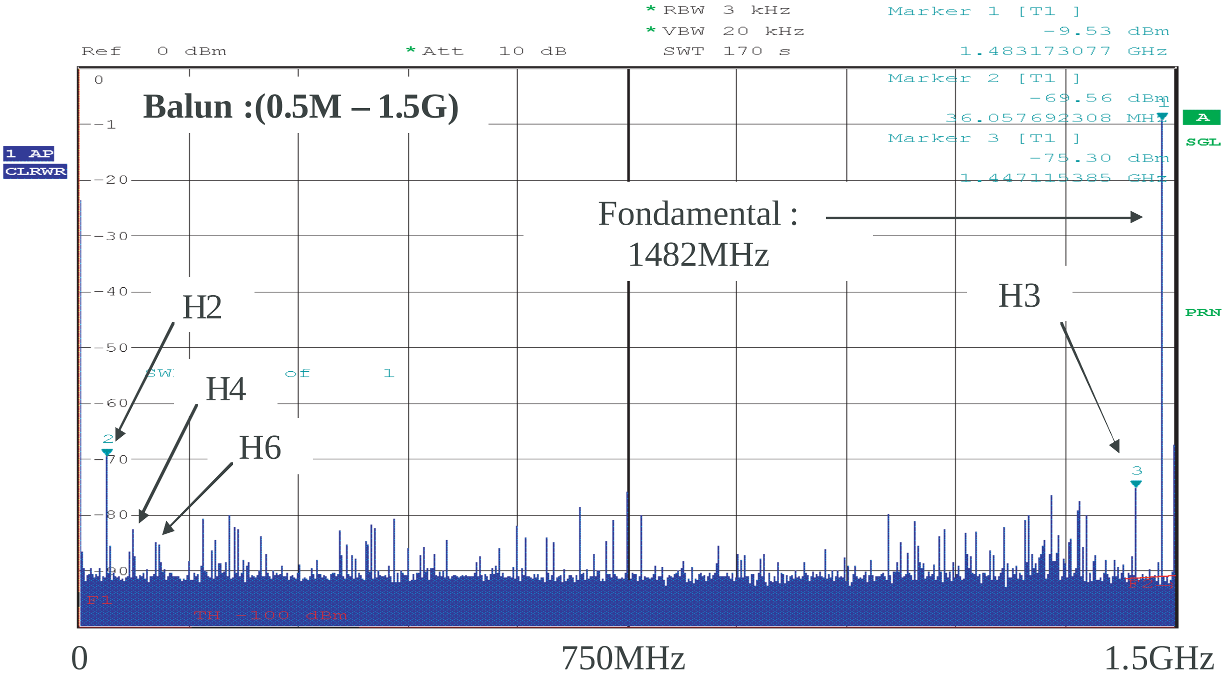


Figure 6-28. Spectrum of the 1st Nyquist Zone, Output Mode NRTZ, with a 0.5 MHz to 1.5 GHz Bandwidth Balun

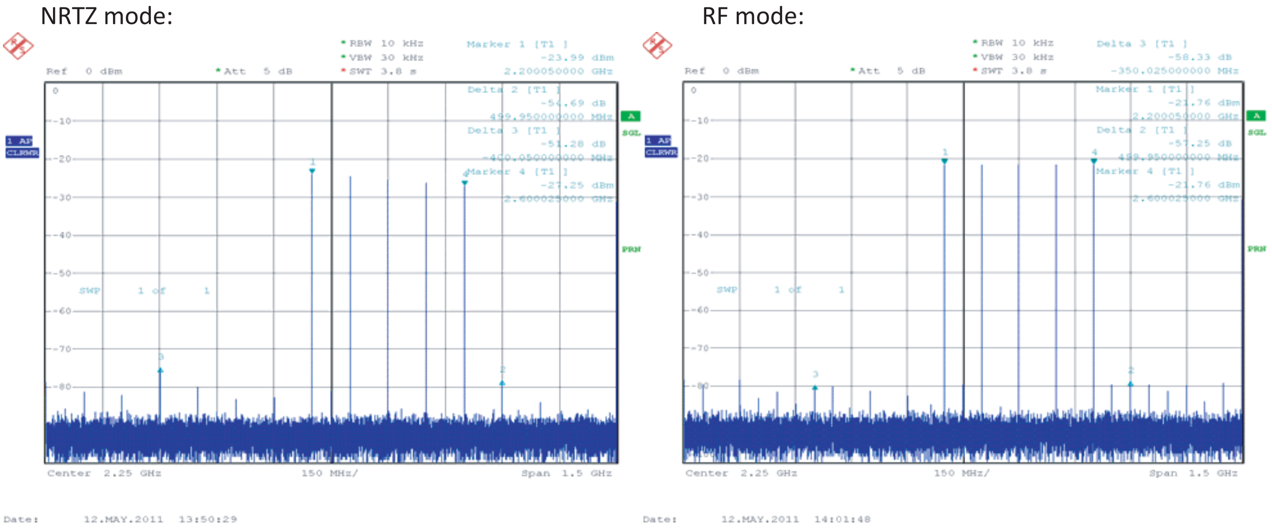


6.2.4 Multi Tone Measurements

A five tones pattern (400 MHz, 500 MHz, 600 MHz, 700 MHz and 800 MHz) is applied to the DAC operating at 3 GSps and results are observed in the 2nd, 3rd, 4th and 5th Nyquist zones.

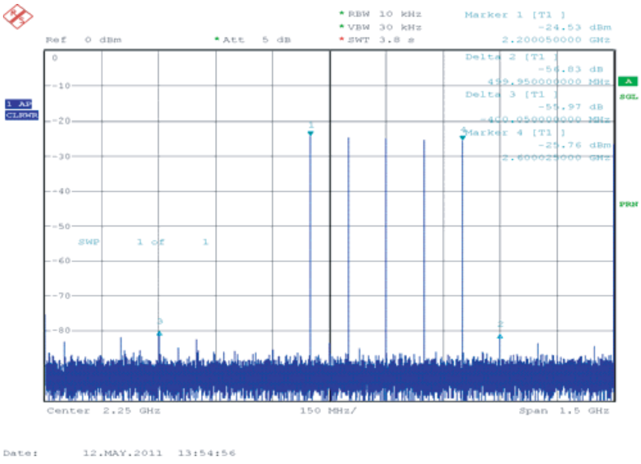
Results are given in the most relevant mode considering the Nyquist zone observed.

Figure 6-29. Observation of the 2nd Nyquist Zone (Tones are pushed from 2.2 GHz to 2.6 GHz): NRTZ, RF and RTZ Modes


NRTZ mode:

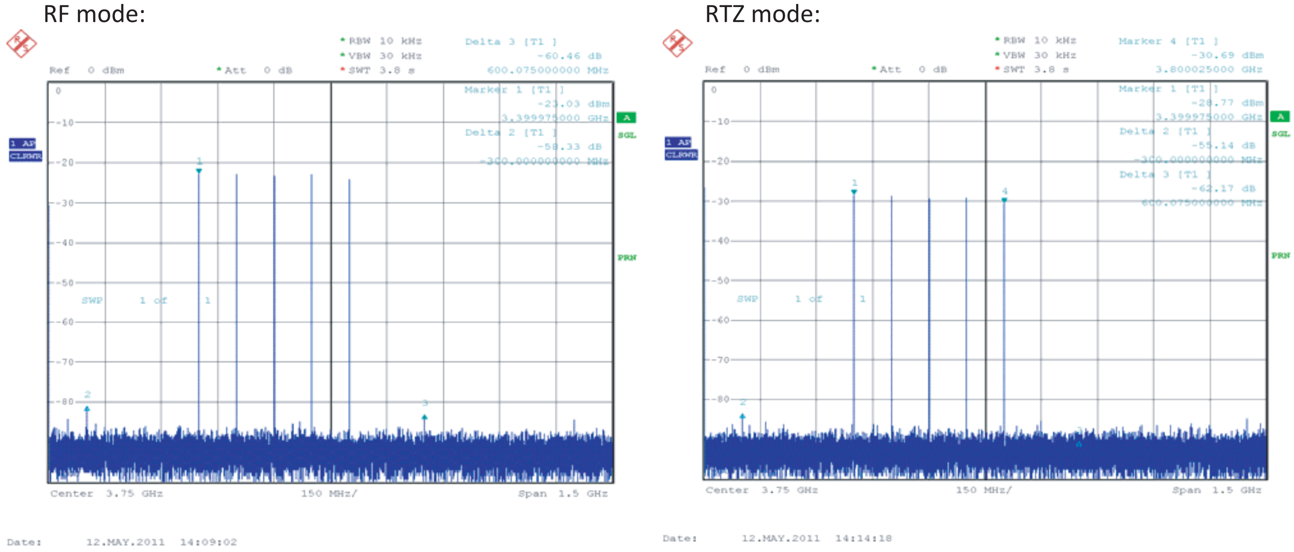
RF mode:

RTZ mode:



	Fout (MHz)	Pout (dBm)	SFDR (freq)	SFDR (dBc)
NRTZ	2200	-23,99	1800	-51,28
RTZ	2200	-24,53	1800	-55,97
RF	2200	-21,76	2700	-57,25

Figure 6-30. Observation of the 3rd Nyquist Zone (Tones are pushed from 3.4GHz to 3.8GHz): RF and RTZ Modes



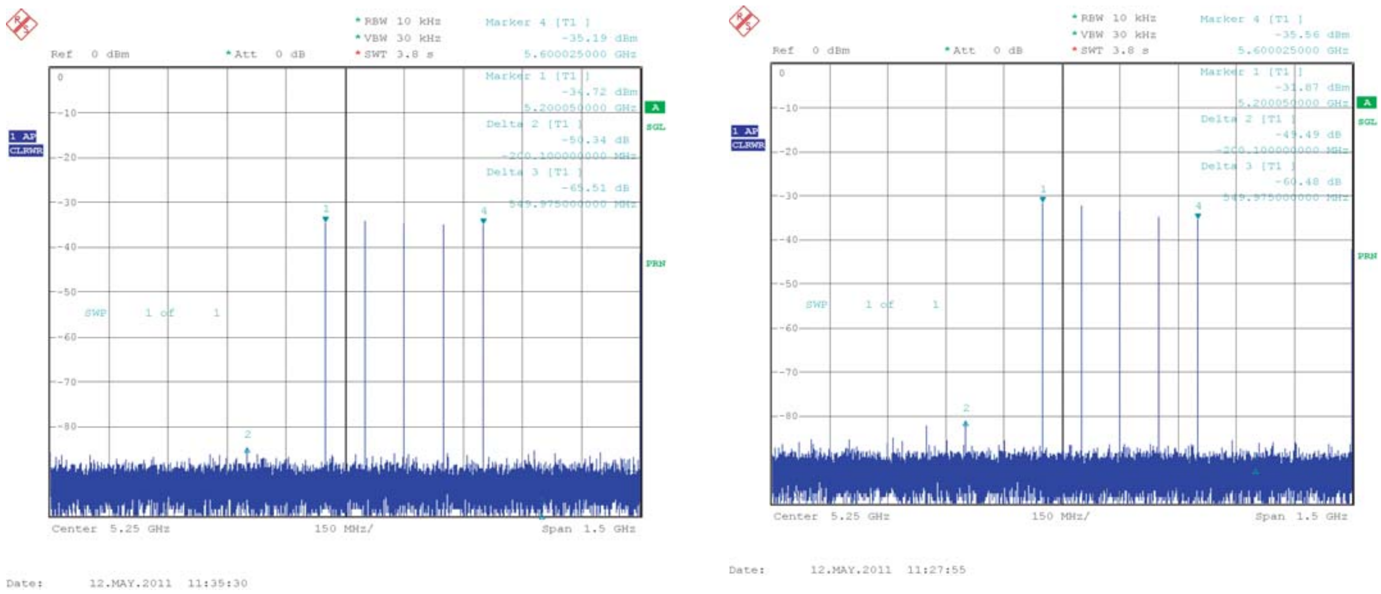
RF mode:

RTZ mode:

	Fout (MHz)	Pout (dBm)	SFDR (freq)	SFDR (dBc)
N RTZ	3400	–39.43	4000	–44.48
RTZ	3400	–28.77	3100	–55.14
RF	3400	–23.03	3100	–58.33

NRTZ performances are degraded because of the sinc attenuation (first notch in the first half of the 3rd Nyquist zone).

Figure 6-31. Observation of the 4th Nyquist Zone (Tones are pushed from 5.2GHz to 5.6 GHz): NRTZ and RF Modes



NRTZ mode

RF mode

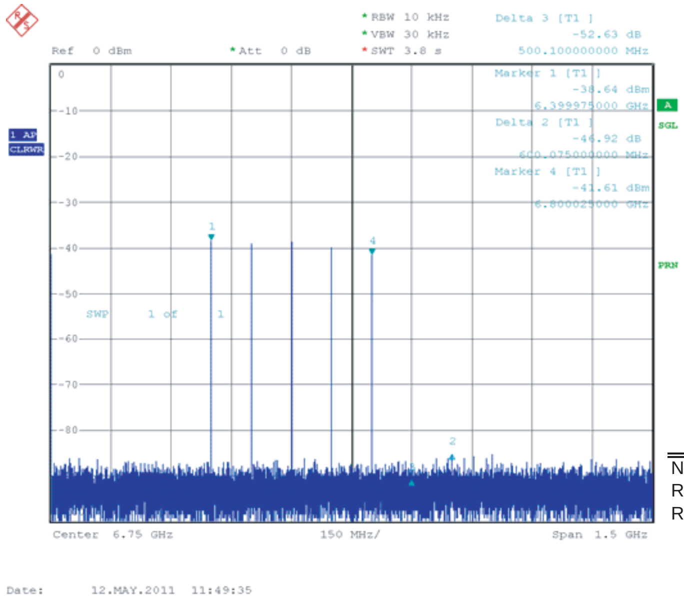
	Fout (MHz)	Pout (dBm)	SFDR (freq)	SFDR (dBc)
N RTZ	5200	–34.72	5000	–50.34
RTZ	5200	–40.37	4700	–45
RF	5200	–31.87	4700	–49.49

RTZ mode is degraded because of the sinc attenuation (first notch at the end of the 4th Nyquist zone).

RF mode offers significantly more power than RTZ mode, this is why we still have acceptable performances.

NRTZ operation is possible because the 4th Nyquist zone is fully included in the secondary spectral lobe.

Figure 6-32. Observation of the 5th Nyquist Zone (Tones are pushed from 6.4GHz to 6.8GHz): NRTZ Mode



	Fout (MHz)	Pout (dBm)	SFDR (freq)	SFDR (dBc)
N RTZ	6400	-38,64	7000	-46,92
RTZ	6800	-46,69	7000	-39,25
RF	6400	-46,89	7000	-38,01

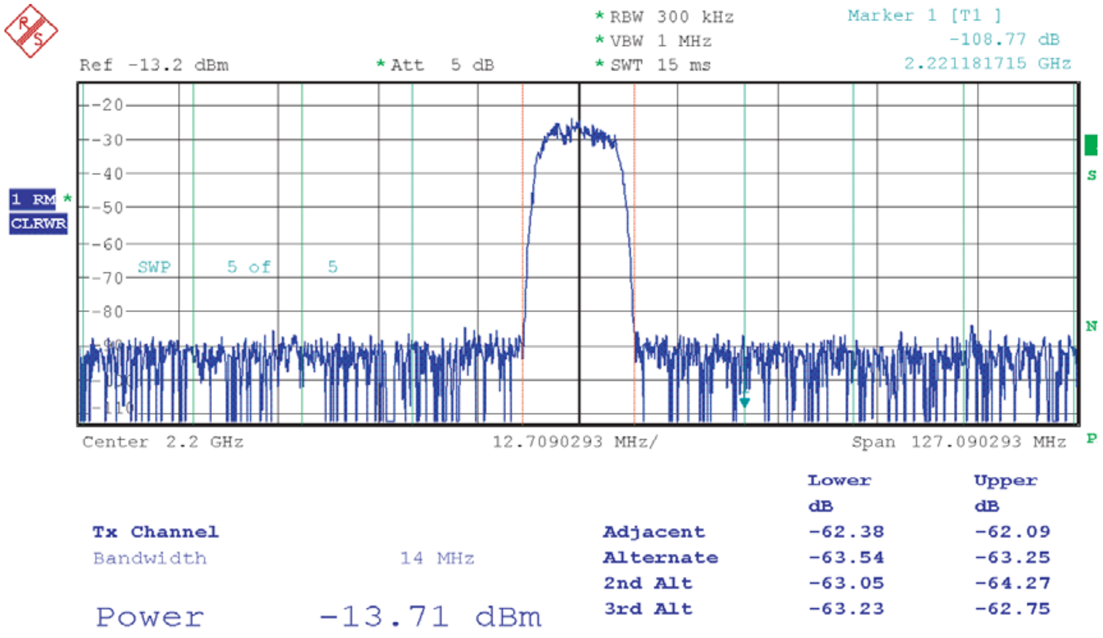
NRTZ mode is still usable in the 5th Nyquist zone (SFDR in excess of 46 dB).

6.2.5 DMWS (Direct Micro Wave Synthesis) Capability Measurements: ACPR

Measurements given here after are performed on the DAC at 3 GSps with a 10 MHz wide QPSK pattern centred on 800 MHz.

Results are observed in 2nd, 3rd, 4th and 5th Nyquist zones and are given only for the most relevant modes (that is RF and/or NRTZ modes).

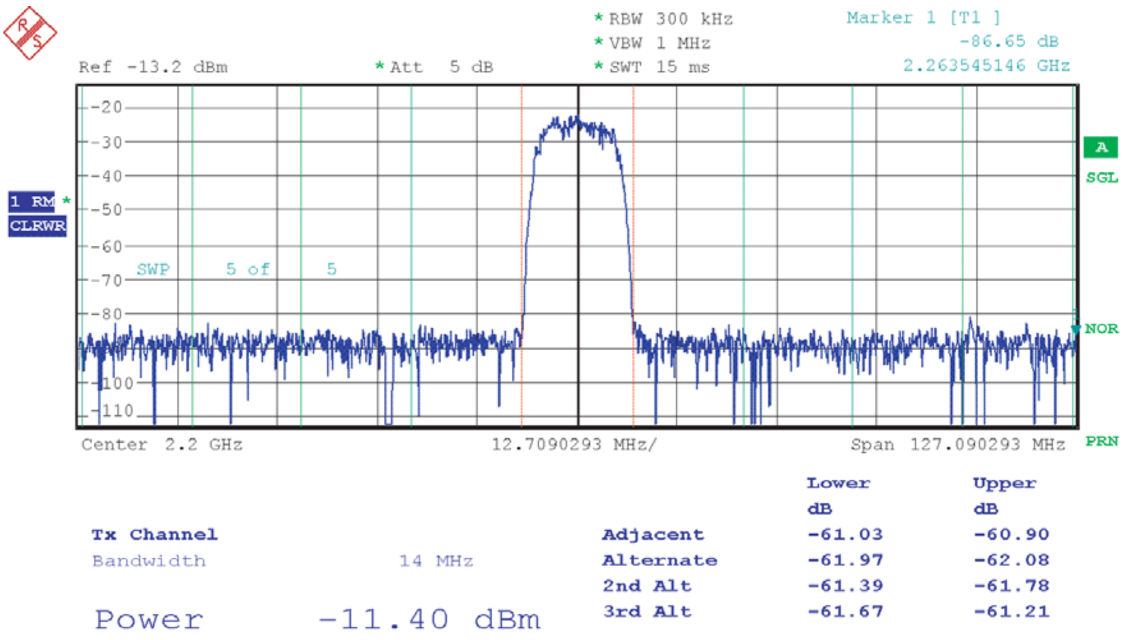
Figure 6-33. NRTZ Mode, 2nd Nyquist: Center Frequency is pushed to 3 GHz – 800 MHz = 2.2 GHz



Tx Channel			Lower dB	Upper dB
Bandwidth	14 MHz	Adjacent	-62.38	-62.09
		Alternate	-63.54	-63.25
		2nd Alt	-63.05	-64.27
Power	-13.71 dBm	3rd Alt	-63.23	-62.75

ACPR is in excess of 62 dB. DMWS capability is proven for second Nyquist in NRTZ mode.

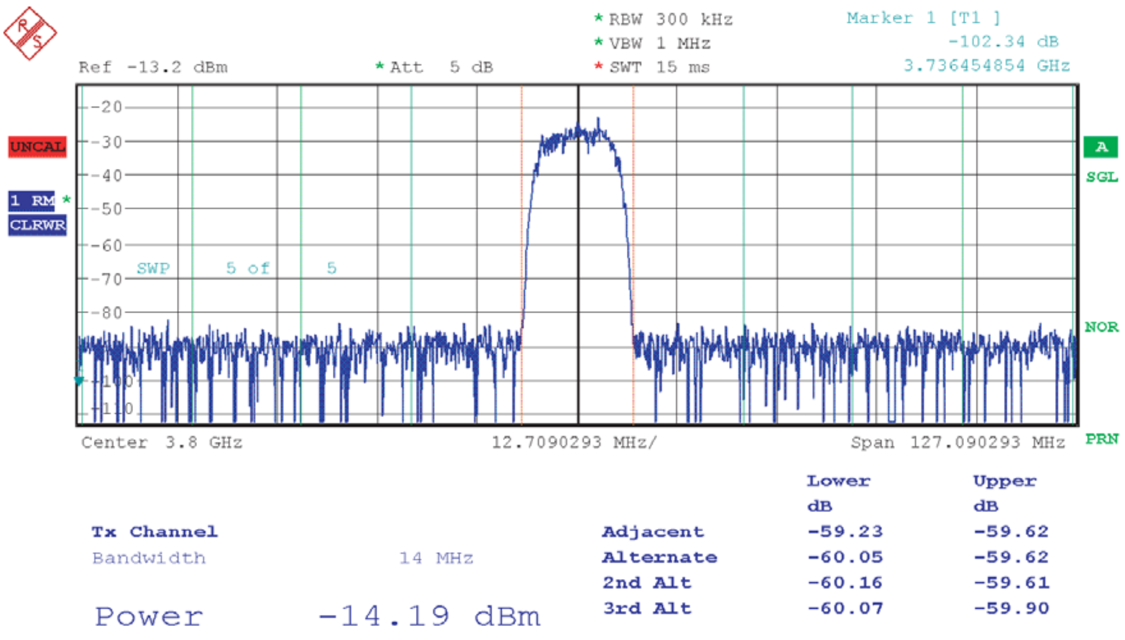
Figure 6-34. RF Mode, 2nd Nyquist: Center Frequency is pushed to 3 GHz – 800 MHz = 2.2 GHz



```
                                             *RBW 300 kHz         Marker 1 [T1 ]
                                             *VBW 1 MHz                -86.65 dB
Ref -13.2 dBm              *Att  5 dB        *SWT 15 ms           2.263545146 GHz

SWP      5 of      5

Center  2.2 GHz             12.7090293 MHz/           Span 127.090293 MHz

                                                     Lower        Upper
                                                     dB           dB
Tx Channel                              Adjacent     -61.03       -60.90
Bandwidth          14 MHz               Alternate    -61.97       -62.08
                                        2nd Alt      -61.39       -61.78
Power        -11.40 dBm                 3rd Alt      -61.67       -61.21
```

ACPR is in excess of 60 dB. DMWS capability is proven for the second Nyquist zone in RF mode with slightly reduced dynamic range regarding NRTZ mode but with increased output power.

Figure 6-35. RF Mode, 3rd Nyquist Zone: Center Frequency is pushed to 3 GHz+ 800 MHz = 3.8 GHz

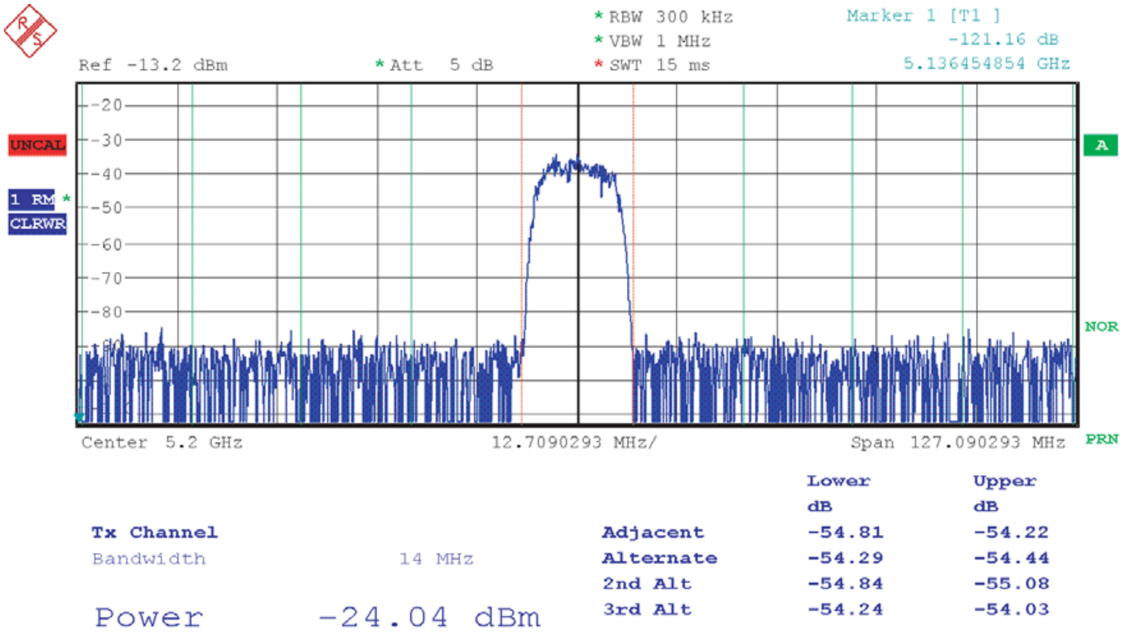


```
                                             *RBW 300 kHz         Marker 1 [T1 ]
                                             *VBW 1 MHz               -102.34 dB
Ref -13.2 dBm              *Att  5 dB        *SWT 15 ms           3.736454854 GHz

SWP      5 of      5

Center  3.8 GHz             12.7090293 MHz/           Span 127.090293 MHz

                                                     Lower        Upper
                                                     dB           dB
Tx Channel                              Adjacent     -59.23       -59.62
Bandwidth          14 MHz               Alternate    -60.05       -59.62
                                        2nd Alt      -60.16       -59.61
Power        -14.19 dBm                 3rd Alt      -60.07       -59.90
```

ACPR is in excess of 59 dB. DMWS capability is proven for the third Nyquist zone in RF mode.

Note: due the notch of available Pout near the middle of the third Nyquist zone, the NRTZ mode is not relevant for DMWS in the third Nyquist zone.

Figure 6-36. NRTZ Mode, 4th Nyquist Zone: Center Frequency is pushed to 6 GHz – 800 MHz = 5.2 GHz



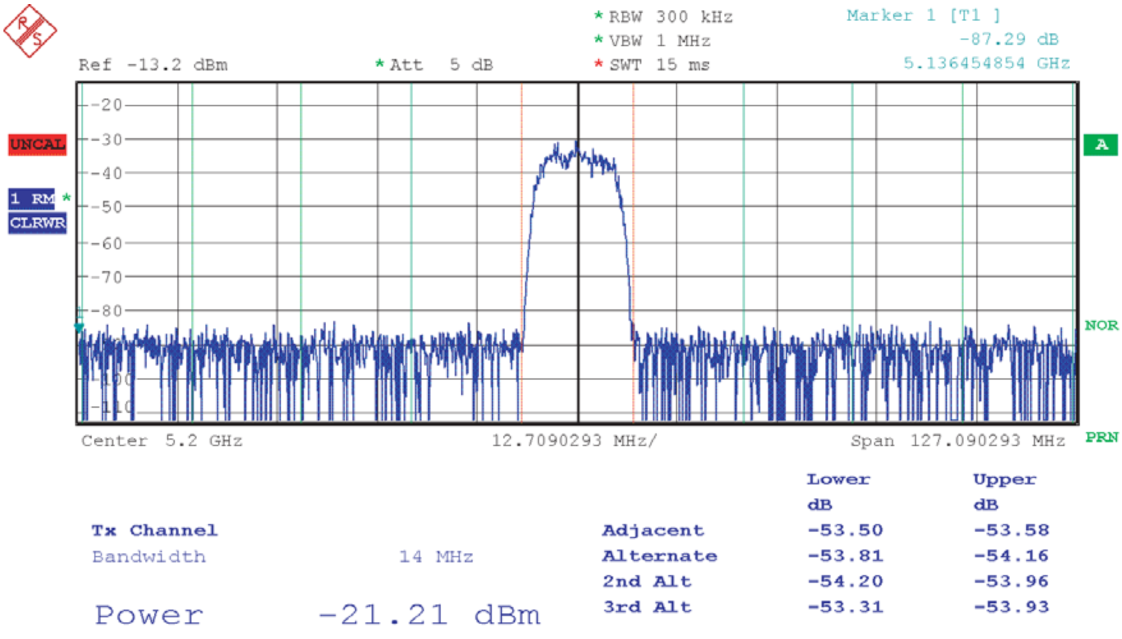
*RBW 300 kHz
*VBW 1 MHz
Ref -13.2 dBm *Att 5 dB *SWT 15 ms
Marker 1 [T1]
-121.16 dB
5.136454854 GHz

Center 5.2 GHz 12.7090293 MHz/ Span 127.090293 MHz

			Lower dB	Upper dB
Tx Channel		**Adjacent**	-54.81	-54.22
Bandwidth	14 MHz	**Alternate**	-54.29	-54.44
		2nd Alt	-54.84	-55.08
Power	-24.04 dBm	**3rd Alt**	-54.24	-54.03

ACPR is in excess of 54 dB. DMWS capability is proven for the fourth Nyquist zone in NRTZ mode.

Figure 6-37. RF Mode, 4th Nyquist Zone: Center Frequency is pushed to 6 GHz – 800 MHz = 5.2 GHz



*RBW 300 kHz
*VBW 1 MHz
Ref -13.2 dBm *Att 5 dB *SWT 15 ms
Marker 1 [T1]
-87.29 dB
5.136454854 GHz

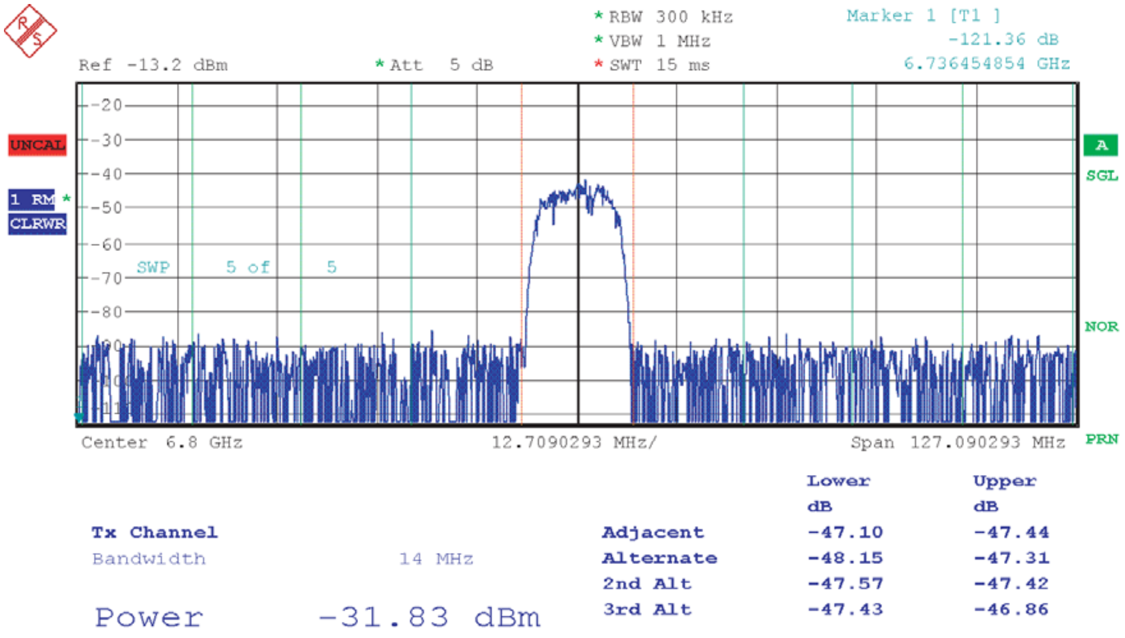
Center 5.2 GHz 12.7090293 MHz/ Span 127.090293 MHz

			Lower dB	Upper dB
Tx Channel		**Adjacent**	-53.50	-53.58
Bandwidth	14 MHz	**Alternate**	-53.81	-54.16
		2nd Alt	-54.20	-53.96
Power	-21.21 dBm	**3rd Alt**	-53.31	-53.93

ACPR is in excess of 53 dB. DMWS capability is proven for the fourth Nyquist zone in RF mode.

Note due to a notch of available Pout near the end of the 4th Nyquist zone in RF output mode, for DMWS beyond middle of 4th Nyquist zone it is recommended to use the NRTZ output mode instead of the RF output mode.

Figure 6-38. NRTZ Mode, 5th Nyquist Zone: Center Frequency is pushed to 6 GHz + 800 MHz = 6.8 GHz



Ref -13.2 dBm

*Att 5 dB

*RBW 300 kHz

*VBW 1 MHz

*SWT 15 ms

Marker 1 [T1]

-121.36 dB

6.736454854 GHz

Center 6.8 GHz

12.7090293 MHz/

Span 127.090293 MHz

Tx Channel

Bandwidth 14 MHz

Power -31.83 dBm

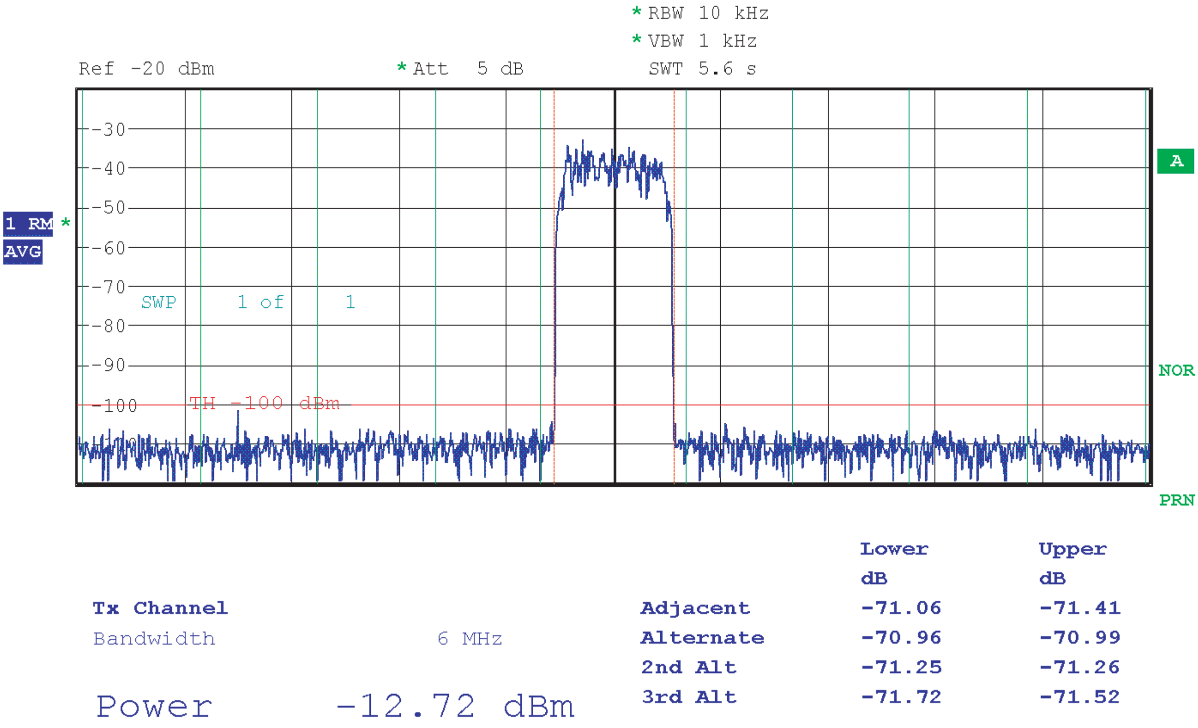
	Lower dB	Upper dB
Adjacent	-47.10	-47.44
Alternate	-48.15	-47.31
2nd Alt	-47.57	-47.42
3rd Alt	-47.43	-46.86

ACPR is still in excess of 47 dB. DMWS capability if proven for the fifth Nyquist zone in NRTZ mode with reduced available dynamic range.

6.2.6 DOCSIS v3.0 Capability Measurements

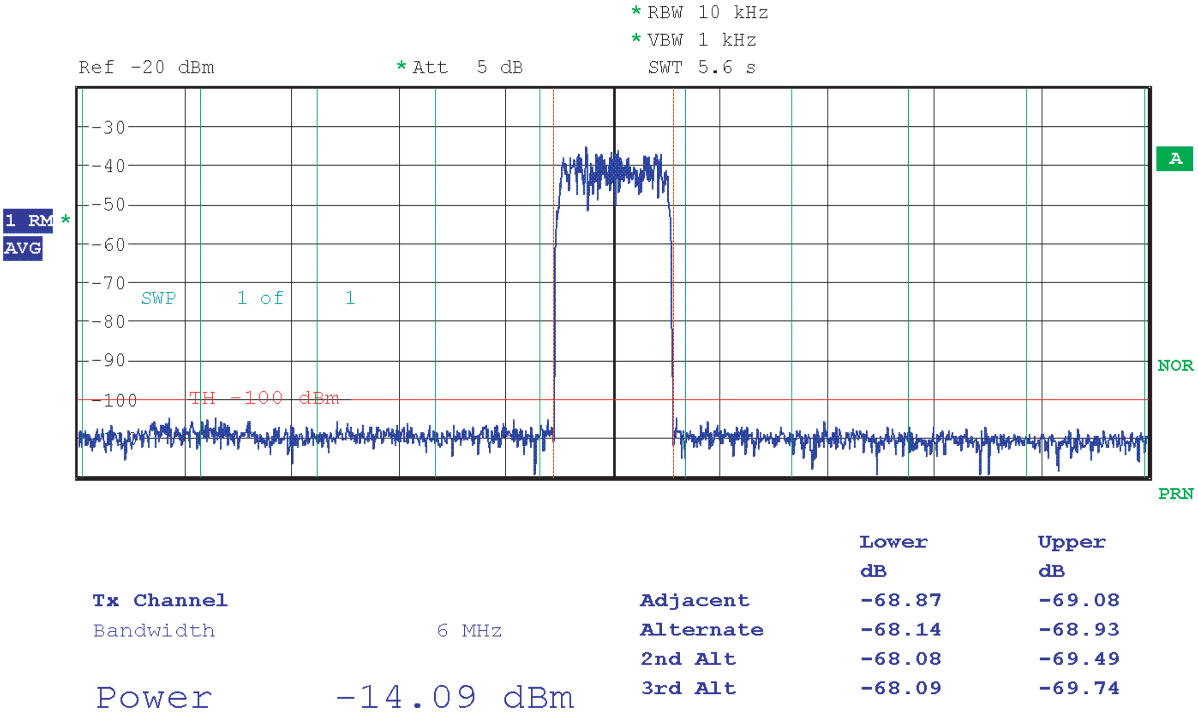
Measurements here after have been carried out on a soldered device EV12DS130AZPY (fPBGA 196), in NRTZ mode.

Figure 6-39. ACPR 1 Channel Centred on 300 MHz, Output Mode NRTZ



			Lower dB	Upper dB
Tx Channel		**Adjacent**	**-71.06**	**-71.41**
Bandwidth	6 MHz	**Alternate**	**-70.96**	**-70.99**
		2nd Alt	**-71.25**	**-71.26**
Power	-12.72 dBm	**3rd Alt**	**-71.72**	**-71.52**

Figure 6-40. ACPR 1 Channel Centred on 900 MHz, Output Mode NRTZ



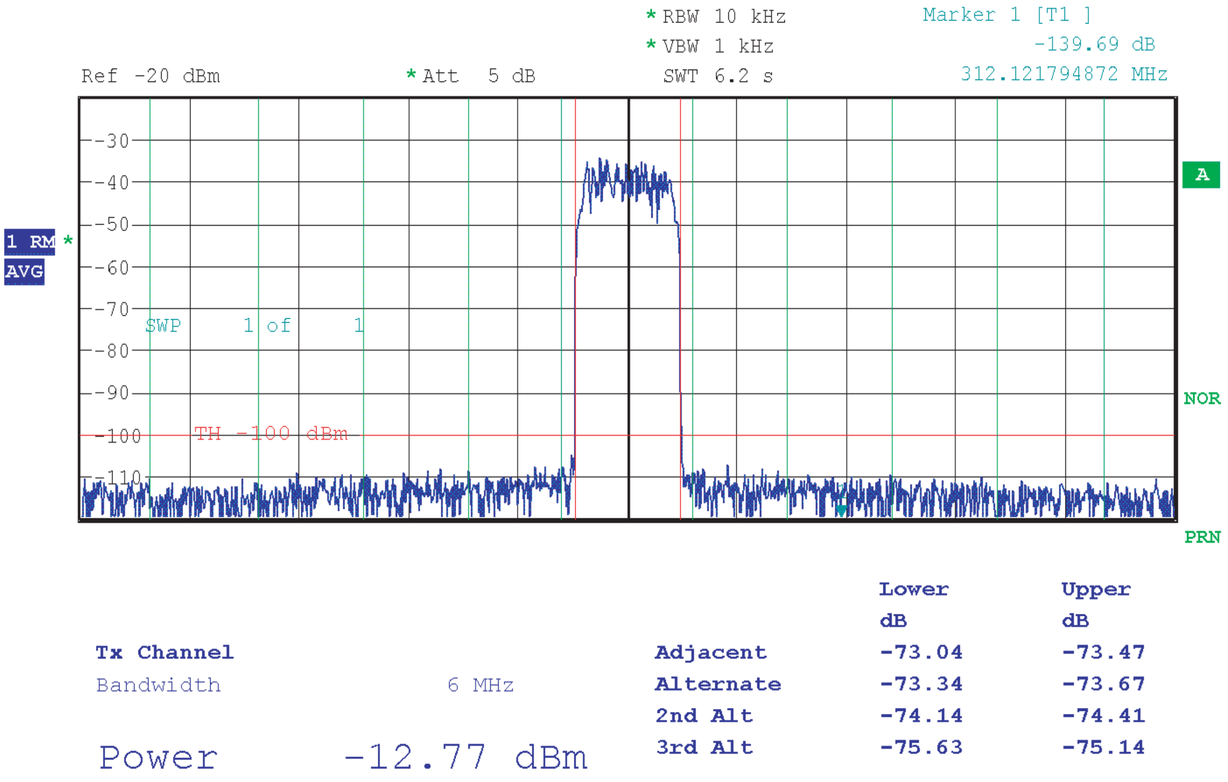
Tx Channel
Bandwidth 6 MHz

Power -14.09 dBm

	Lower dB	Upper dB
Adjacent	-68.87	-69.08
Alternate	-68.14	-68.93
2nd Alt	-68.08	-69.49
3rd Alt	-68.09	-69.74

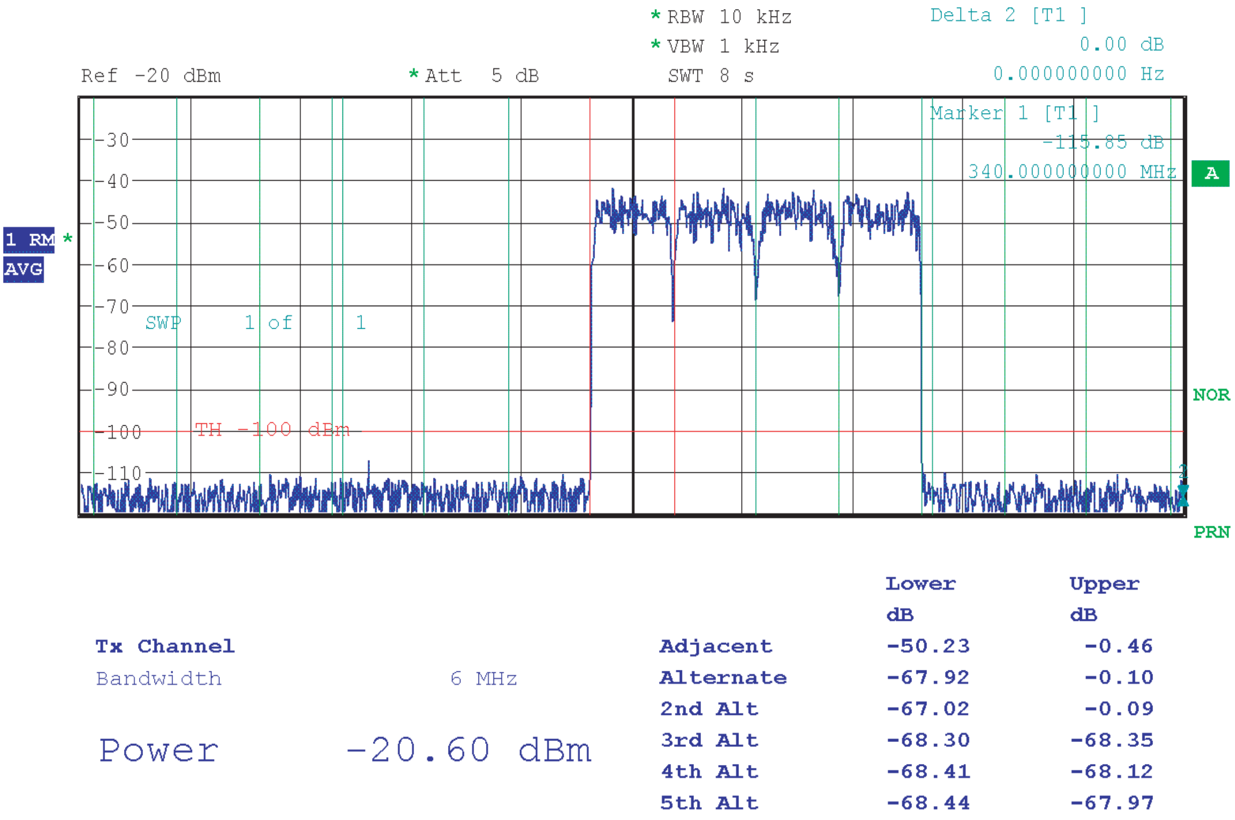
Measurements here after have been carried out on a soldered device EV12DS130AGS (CI-CGA 255), in NRTZ mode.

Figure 6-41. ACPR 1 channel centred on 300 MHz, Output Mode NRTZ, CI-CGA255



```
                                        *RBW 10 kHz        Marker 1 [T1 ]
                                        *VBW 1 kHz              -139.69 dB
Ref -20 dBm               *Att   5 dB    SWT 6.2 s         312.121794872 MHz

                                                      Lower       Upper
                                                      dB          dB
Tx Channel                              Adjacent      -73.04      -73.47
Bandwidth                 6 MHz         Alternate     -73.34      -73.67
                                        2nd Alt       -74.14      -74.41
Power          -12.77 dBm               3rd Alt       -75.63      -75.14
```

Figure 6-42. ACPR 4 Channels Centred on 300 MHz, Output Mode NRTZ, CI-CGA255



Ref -20 dBm

*Att 5 dB

*RBW 10 kHz
*VBW 1 kHz
SWT 8 s

Delta 2 [T1]
0.00 dB
0.000000000 Hz

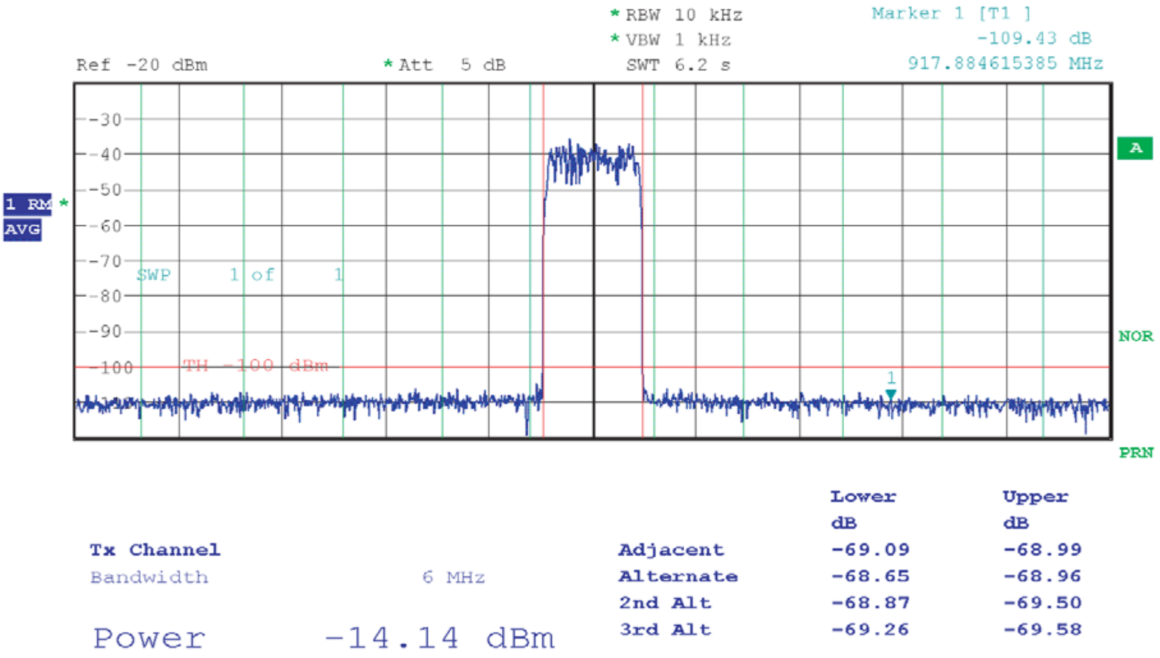
Marker 1 [T1]
-115.85 dB
340.000000000 MHz

Tx Channel
Bandwidth 6 MHz

Power -20.60 dBm

	Lower dB	Upper dB
Adjacent	-50.23	-0.46
Alternate	-67.92	-0.10
2nd Alt	-67.02	-0.09
3rd Alt	-68.30	-68.35
4th Alt	-68.41	-68.12
5th Alt	-68.44	-67.97

Figure 6-43. ACPR 1 Channel Centred on 900 MHz, Output Mode NRTZ, CI-CGA255



Ref -20 dBm

*Att 5 dB

*RBW 10 kHz
*VBW 1 kHz
SWT 6.2 s

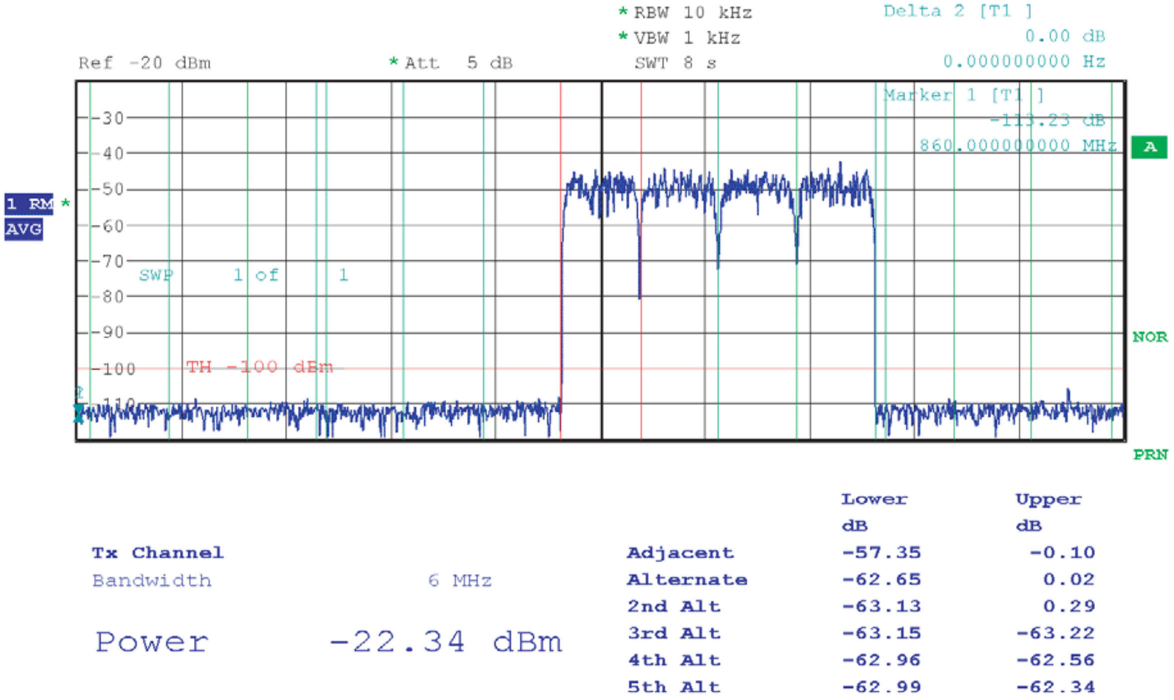
Marker 1 [T1]
-109.43 dB
917.884615385 MHz

Tx Channel
Bandwidth 6 MHz

Power -14.14 dBm

	Lower dB	Upper dB
Adjacent	-69.09	-68.99
Alternate	-68.65	-68.96
2nd Alt	-68.87	-69.50
3rd Alt	-69.26	-69.58

Figure 6-44. ACPR 4 channels centred on 900 MHz, Output Mode NRTZ, CI-CGA255



Tx Channel			Lower dB	Upper dB
Bandwidth	6 MHz	Adjacent	-57.35	-0.10
		Alternate	-62.65	0.02
		2nd Alt	-63.13	0.29
Power	-22.34 dBm	3rd Alt	-63.15	-63.22
		4th Alt	-62.96	-62.56
		5th Alt	-62.99	-62.34

6.2.7 NPR Performances

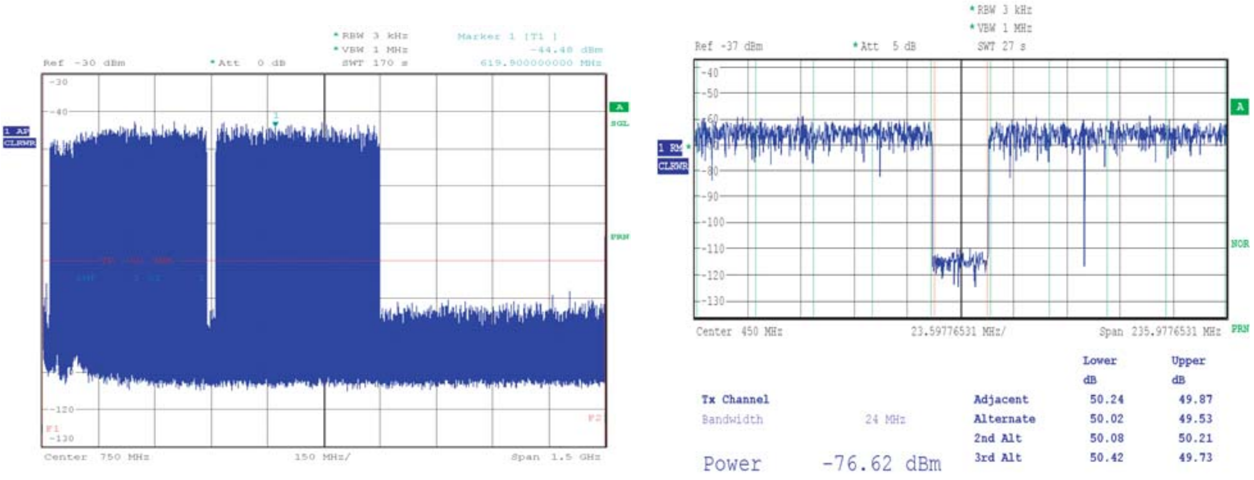
NPR measurements have been carried out at optimum loading factor for a 12 bit DAC, that is –14 dB loading factor (LF), with the DAC operating at 3 GSps.

SNR can be computed from SNR measurement with the formula: $SNR_{[dB]} = NPR_{[dB]} + |LF_{[dB]}| - 3$.

ENOB can be computed with the formula: $ENOB = (SNR_{[dB]} - 1.76) / 6.02$.

Note: Results illustrated hereafter (spectrum and zoom on notch) come for measurement on a EV12DS130AGS device (CI-CGA255 package). Measurements have been carried out using the ACP treatment of the spectrum analyzer Rhode & Schwarz FSU8, in RMS detection mode.

Figure 6-45. NPR in first Nyquist Zone, 20 MHz to 900 MHz noise pattern with a 25 MHz notch centred on 450 MHz, NRZ mode

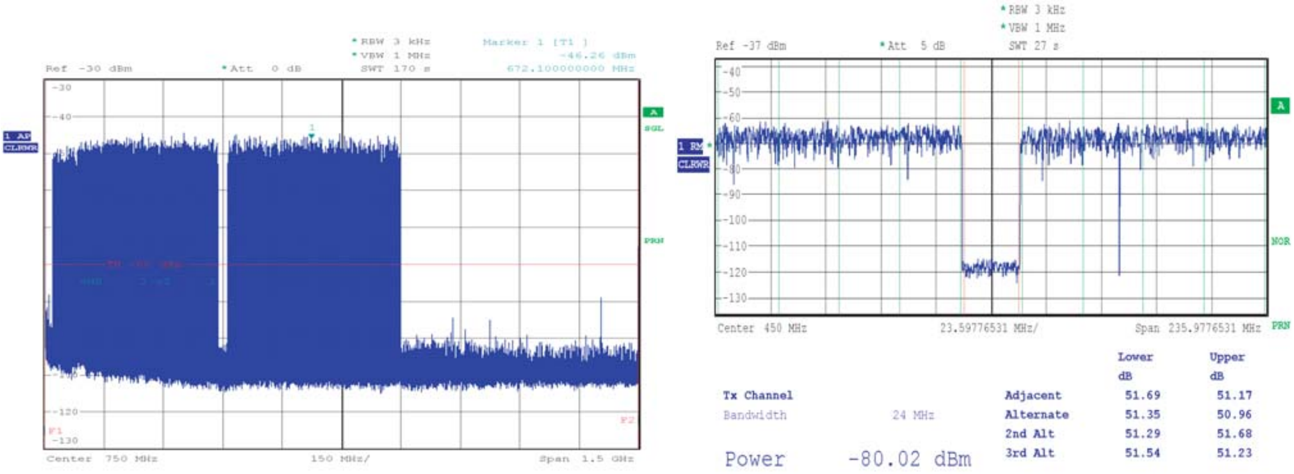


```
                                          Lower     Upper
                                          dB        dB
Tx Channel                    Adjacent    50.24     49.87
Bandwidth          24 MHz     Alternate   50.02     49.53
                              2nd Alt     50.08     50.21
Power       -76.62 dBm        3rd Alt     50.42     49.73
```

Measured average NPR: 50.02 dB, therefore SNR = 61.02 dB and ENOB = 9.84 bit

Effects at low frequency are due to balun and pattern.

Figure 6-46. NPR in first Nyquist Zone, 20 MHz to 900 MHz noise pattern with a 25 MHz notch centred on 450 MHz, NRTZ mode

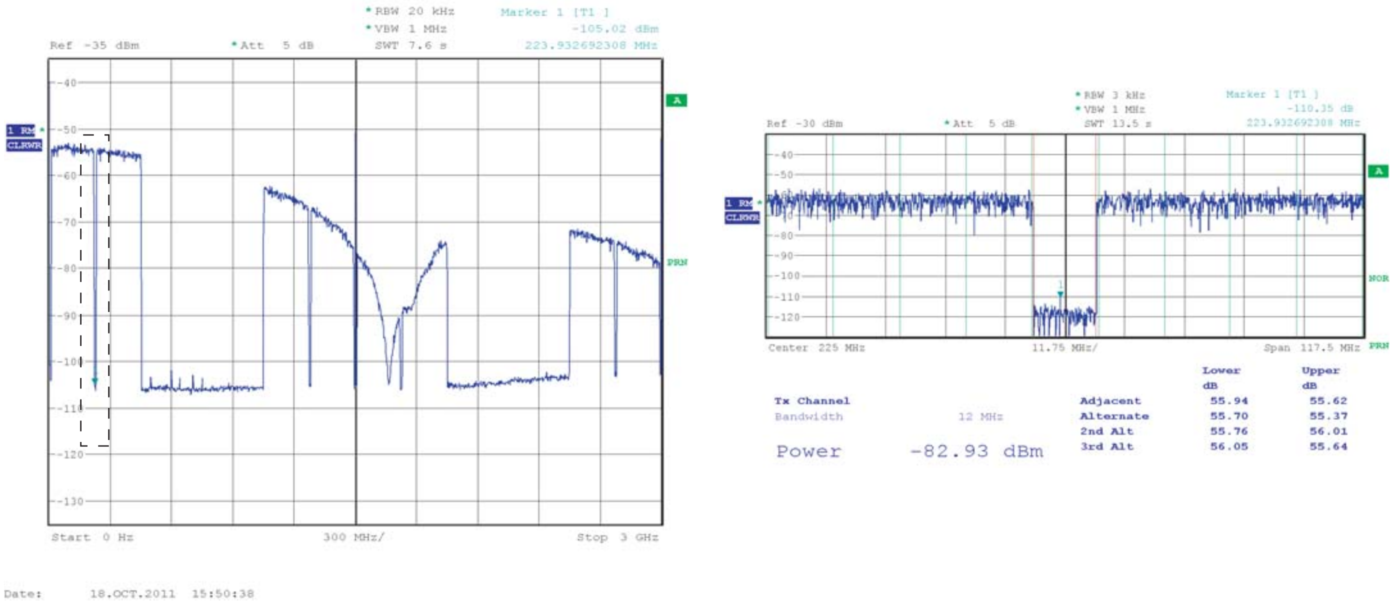


```
                                          Lower     Upper
                                          dB        dB
Tx Channel                    Adjacent    51.69     51.17
Bandwidth          24 MHz     Alternate   51.35     50.96
                              2nd Alt     51.29     51.68
Power       -80.02 dBm        3rd Alt     51.54     51.23
```

Measured average NPR: 51.36 dB, therefore SNR = 62.36 dB and ENOB = 10.07 bit.

Effects at low frequency are due to balun and pattern.

Figure 6-47. NPR in First Nyquist Zone, 10 MHz to 450 MHz Noise Pattern with a 12.5 MHz Notch Centred on 225 MHz, NRTZ Mode at Fs = 1.5 GSpS



RBW 20 kHz
VBW 1 MHz
SWT 7.6 s
Marker 1 [T1]
-105.02 dBm
223.932692308 MHz
Ref -35 dBm
Att 5 dB
Start 0 Hz
300 MHz/
Stop 3 GHz

Date: 18.OCT.2011 15:50:38

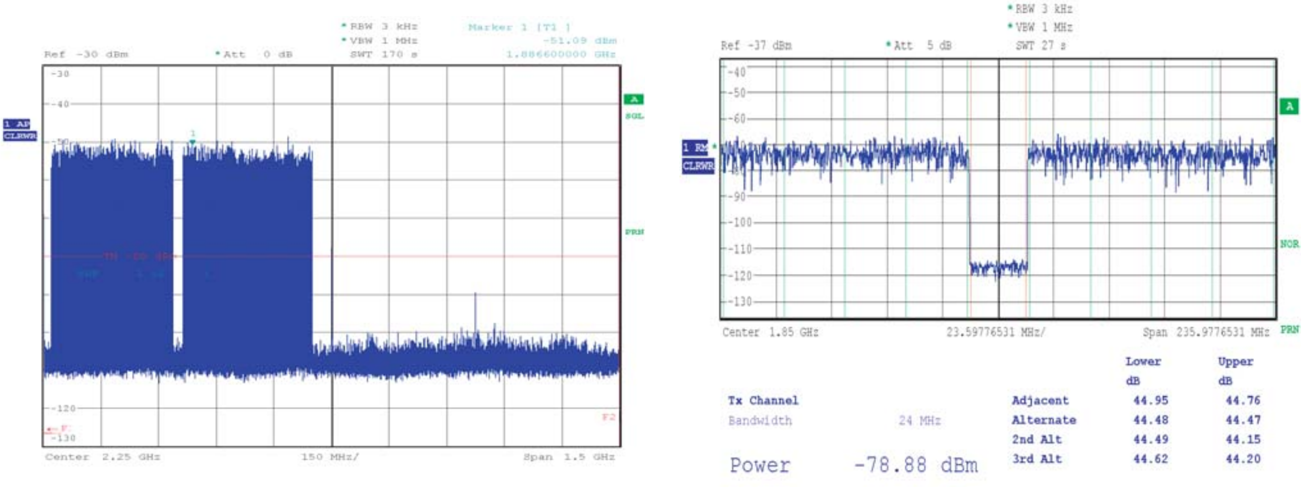
RBW 3 kHz
VBW 1 MHz
SWT 13.5 s
Marker 1 [T1]
-110.35 dB
223.932692308 MHz
Ref -30 dBm
Att 5 dB
Center 225 MHz
11.75 MHz/
Span 117.5 MHz

			Lower dB	Upper dB
Tx Channel		Adjacent	55.94	55.62
Bandwidth	12 MHz	Alternate	55.70	55.37
		2nd Alt	55.76	56.01
Power	-82.93 dBm	3rd Alt	56.05	55.64

Measured average NPR: 55.7 dB, therefore SNR = 66.7 dB and ENOB = 10.8 bit.

Effects at low frequency are due to balun and pattern.

Figure 6-48. NPR in second Nyquist Zone, 1520 MHz to 2200 MHz Noise Pattern with a 25 MHz Notch Centred on 1850 MHz, RTZ mode



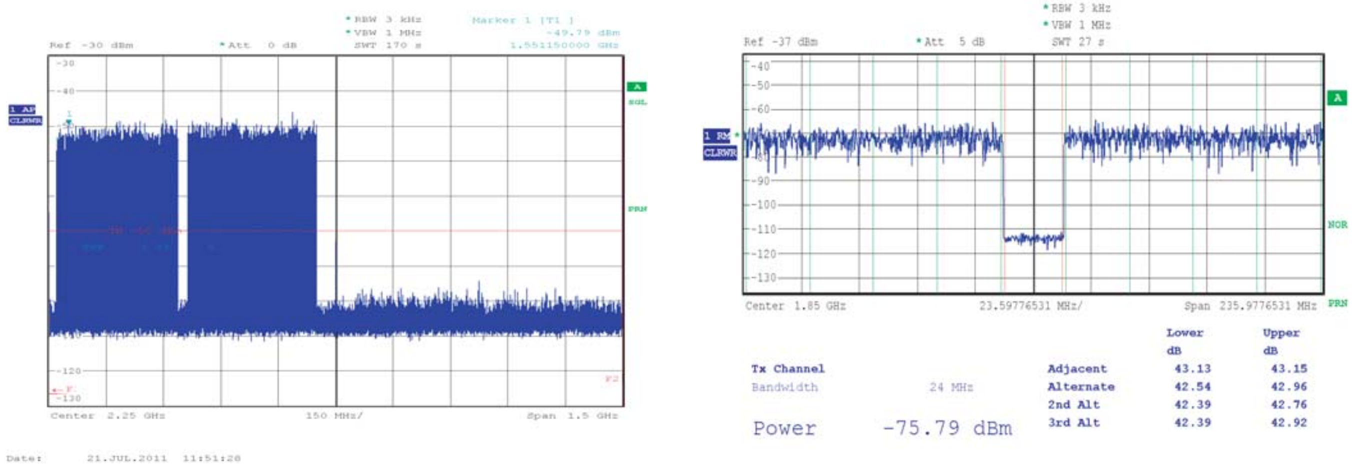
RBW 3 kHz
VBW 1 MHz
SWT 170 s
Marker 1 [T1]
-51.09 dBm
1.886600000 GHz
Ref -30 dBm
Att 0 dB
Center 2.25 GHz
150 MHz/
Span 1.5 GHz

RBW 3 kHz
VBW 1 MHz
SWT 27 s
Ref -37 dBm
Att 5 dB
Center 1.85 GHz
23.59776531 MHz/
Span 235.9776531 MHz

			Lower dB	Upper dB
Tx Channel		Adjacent	44.95	44.76
Bandwidth	24 MHz	Alternate	44.48	44.47
		2nd Alt	44.49	44.15
Power	-78.88 dBm	3rd Alt	44.62	44.20

Measured average NPR: 44.6 dB, therefore SNR = 55.6 dB and ENOB = 8.94 bit

Figure 6-49. NPR in second Nyquist Zone, 1520 MHz to 2200 MHz noise pattern with a 25 MHz notch centred on 1850 MHz, RF Mode



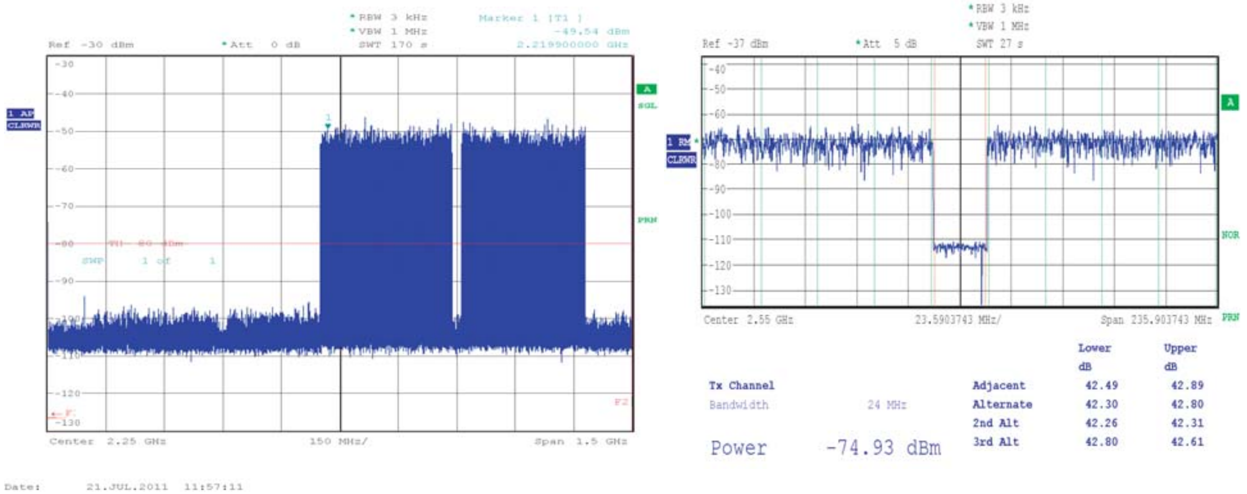
Tx Channel
Bandwidth 24 MHz
Power -75.79 dBm

	Lower dB	Upper dB
Adjacent	43.13	43.15
Alternate	42.54	42.96
2nd Alt	42.39	42.76
3rd Alt	42.39	42.92

Measured average NPR: 42.78 dB, therefore SNR = 53.78 dB and ENOB = 8.64 bit

Effects at low frequency are due to balun and pattern.

Figure 6-50. NPR in second Nyquist Zone, 2200 MHz to 2880 MHz Noise Pattern with a 25 MHz Notch Centred on 2550 MHz, RF Mode



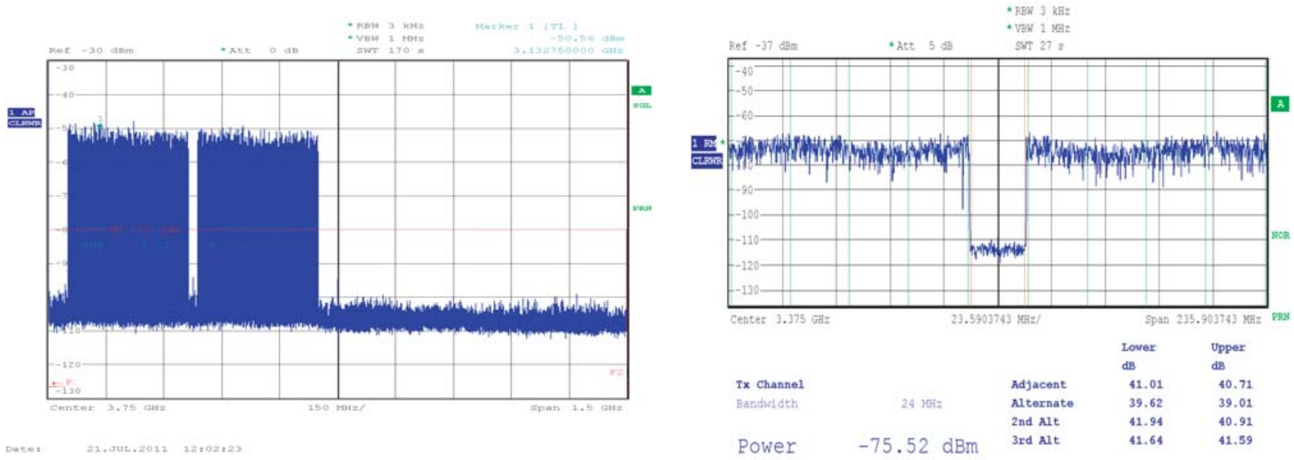
Tx Channel
Bandwidth 24 MHz
Power -74.93 dBm

	Lower dB	Upper dB
Adjacent	42.49	42.89
Alternate	42.30	42.80
2nd Alt	42.26	42.31
3rd Alt	42.80	42.61

Measured average NPR: 42.56 dB, therefore SNR = 53.56 dB and ENOB = 8.6 bit.

Effects at low frequency are due to balun and pattern.

Figure 6-51. NPR in third Nyquist Zone, 3050 MHz to 3700 MHz Noise Pattern with a 25 MHz Notch Centred on 3375 MHz, RF Mode



Tx Channel			Lower dB	Upper dB
Bandwidth	24 MHz	Adjacent	41.01	40.71
		Alternate	39.62	39.01
Power	-75.52 dBm	2nd Alt	41.94	40.91
		3rd Alt	41.64	41.59

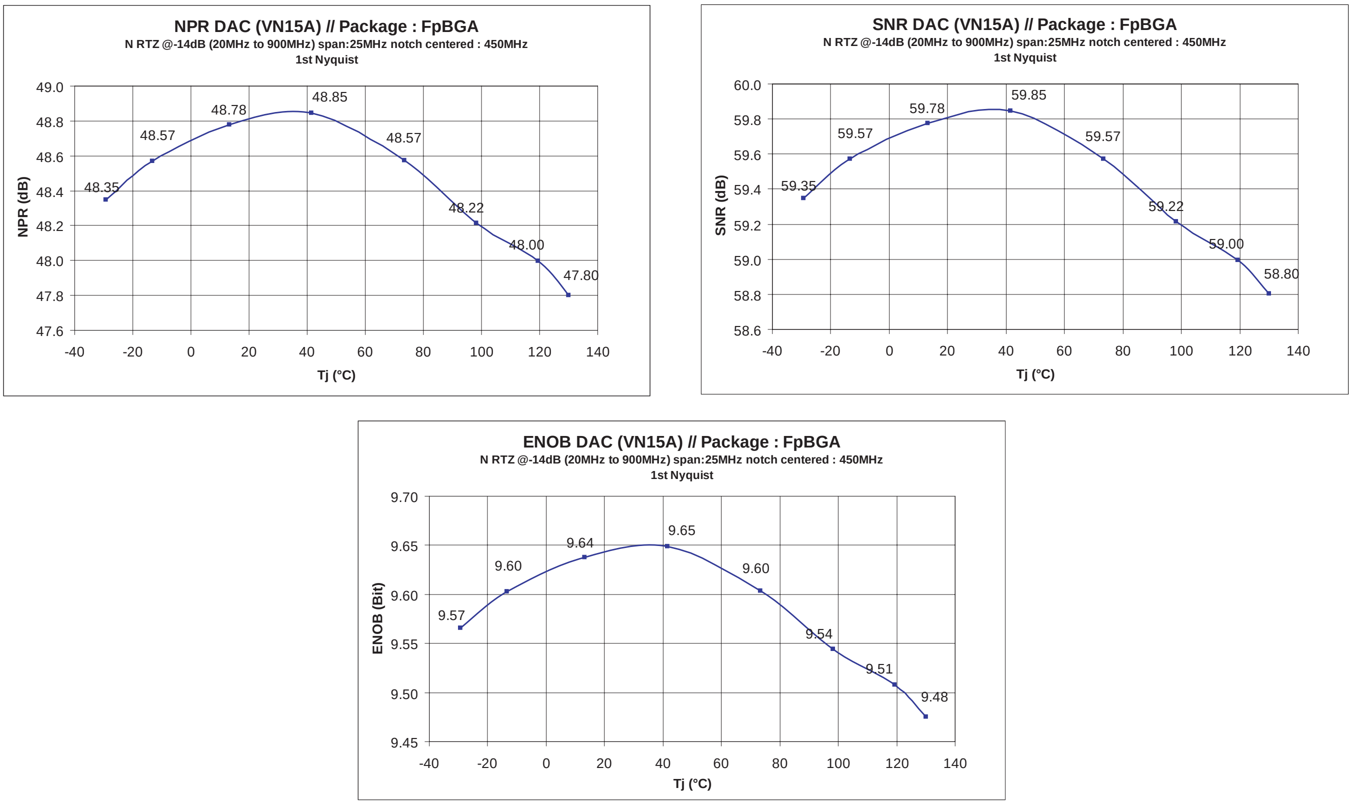
Measured average NPR: 40.08 dB, therefore SNR = 51.08 dB and ENOB = 8.19 bit

Effects at low frequency are due to balun and pattern.

The following figure reflects the stability of NPR in first Nyquist in NRTZ mode (and therefore SNR and ENOB) against temperature.

Measurements have been carried out at nominal power supply on an EV12DS130AZPY, at 3 GSps, with the FSU8 spectrum analyzer in RMS detection mode.

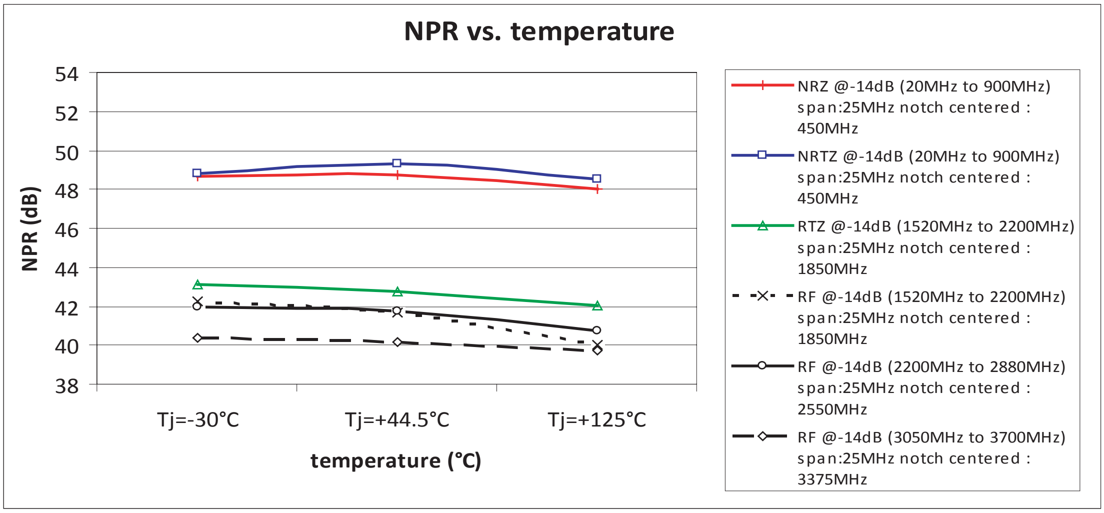
Figure 6-52. Drift of NPR and Associated SNR and ENOB in First Nyquist in NRTZ Mode from Tj = –30°C to Tj = 125°C



Optimum is at Tj = 40°C, degradation over temp is within 1 dB (or 0.15 effective bit).

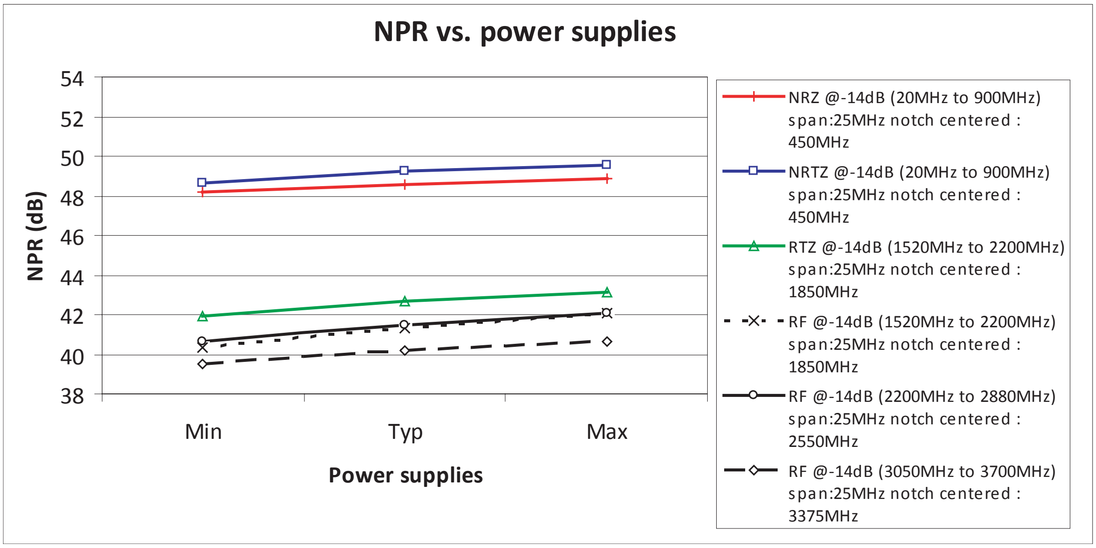
Measurements hereafter have been carried out on an EV12AS130AGS device at 3 GSps, with the FSU8 spectrum analyzer in RMS detection mode.

Figure 6-53. Drift of NPR vs temp in the 4 Output Modes at Nominal Supply



Conclusion: performances are stable in the four output modes against temperature.

Figure 6-54. NPR vs Power Supply Level in the 4 Output Modes at Room Temperature



Conditions: Typical, excepted: power supplies

Min: V_{CCA}: 4.75V // $V_{CCA3} = V_{CCD} = 3.15V$

Typ: V_{CCA}: 5V // $V_{CCA3} = V_{CCD} = 3.3V$

Max: V_{CCA}: 5.25V // $V_{CCA3} = V_{CCD} = 3.45V$.

Conclusion: performances are fairly stable against power supply.

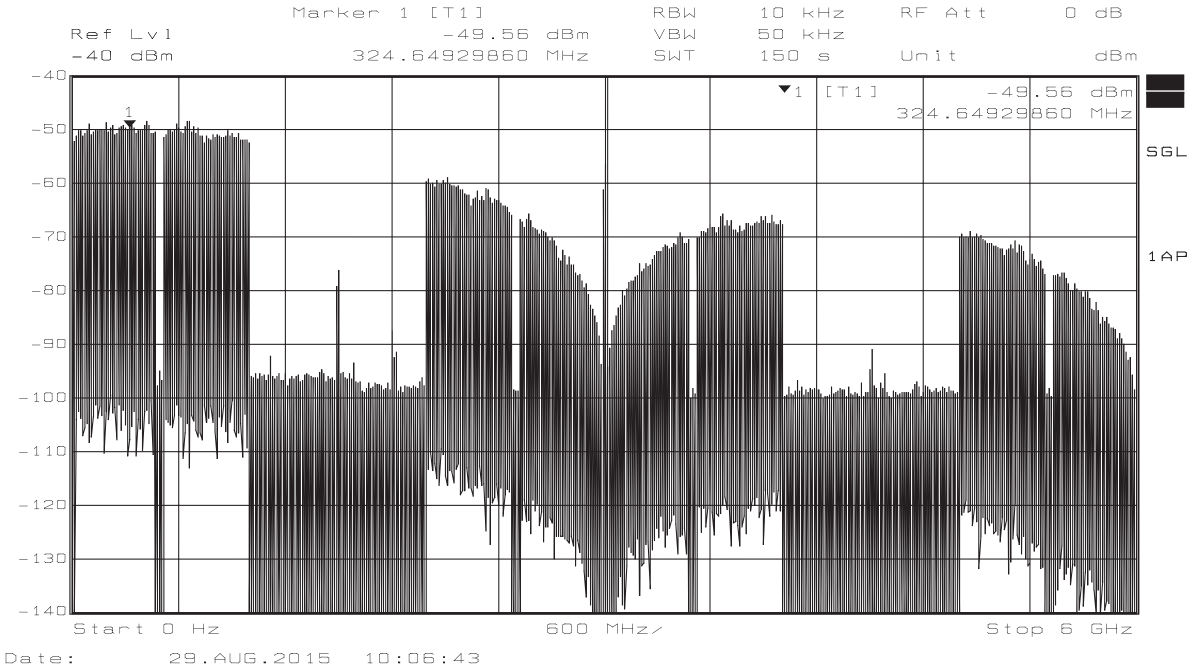
6.2.8 Spectrum over 4 Nyquist Zones in the four Output Modes (IUCM = 0)

Observation of a 1GHz broadband pattern with a 25 MHz notch centred on 500 MHz spectrum over 4 Nyquist zones at 3 GSps (that is from DC to 6 GHz), measurements performed on an EV12DS130AGS device (CI-CGA 255 package, with an overall 6 GHz bandwidth limitation).

By periodisation of a sampled system each tone F_i of the pattern in the 1st Nyquist zone is duplicated as follows:

- 2nd Nyquist Zone: tone at Fclock - F_i.
- 3rd Nyquist Zone: tone at Fclock + F_i.
- 4th Nyquist Zone: tone at 2*Fclock - F_i.

Figure 6-55. Spectrum over 4 Nyquist Zones at 3 GSps in NRZ Output Mode, IUCM off



First Zero of the sinc() function is at Fclock.

Figure 6-56. Spectrum over 4 Nyquist Zones at 3 GSps in NRTZ Output Mode, IUCM off

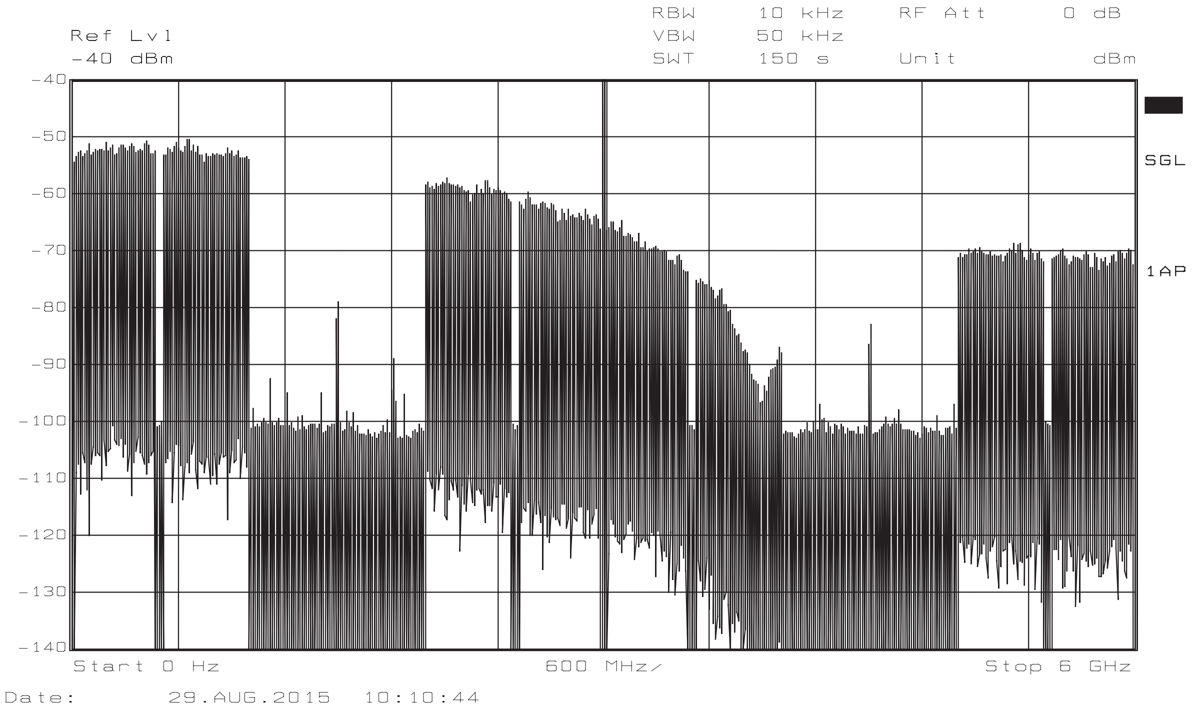
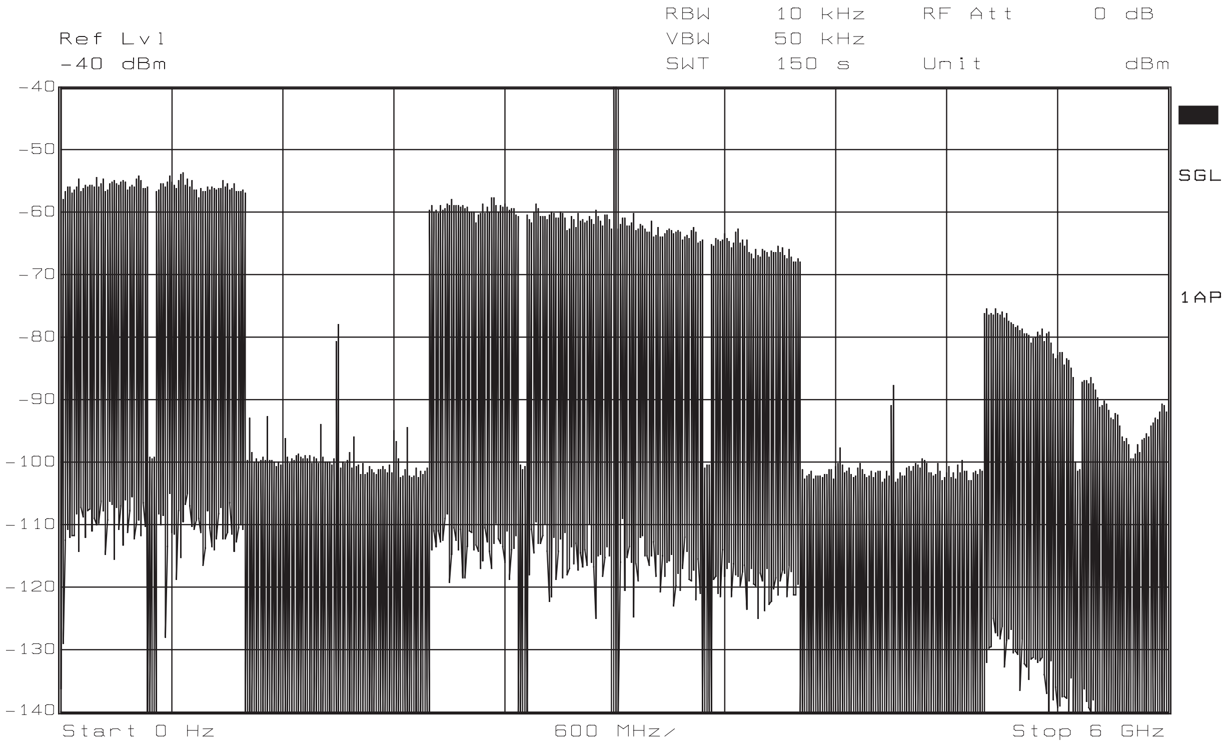
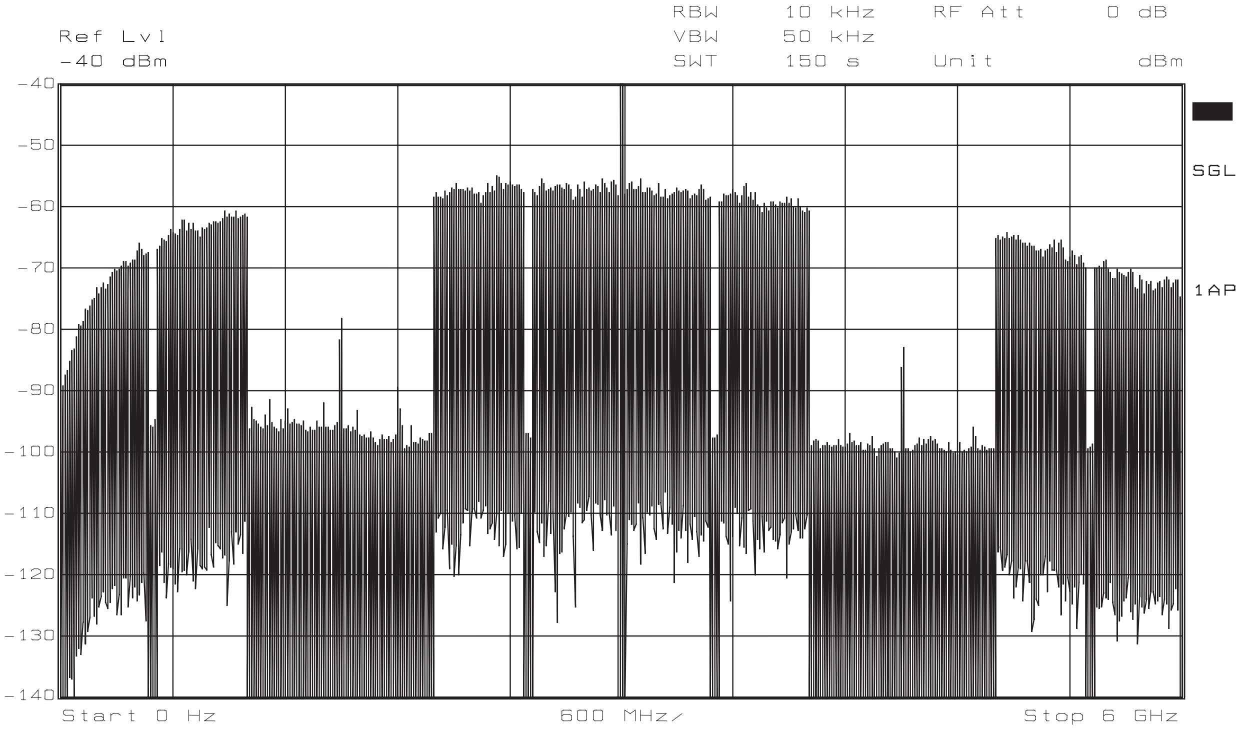


Figure 6-57. Spectrum over 4 Nyquist Zones at 3 GSps in RTZ Output Mode, IUCM off



First Zero of the sinc() function is slightly before 2*Fclock which indicates that the duty cycle of RTZ function is a little bit more than 50%, this is due to the balun which introduced some phase error beyond the 180 degrees between CLK and CLKN thus creating a duty cycle on the clock actually seen by the DAC.

Figure 6-58. Spectrum over 4 Nyquist Zones at 3 GSps in RF Output Mode, IUCM off



Measurements are showing a pretty good fit with theory, see Section 4.2 on page 16.

6.2.9 Spectrum over 8 Nyquist Zones in the Four Output Modes (IUCM = 1)

Observation of a 500 MHz broadband pattern with a 12.5 MHz notch centred on 250 MHz spectrum over 8 Nyquist zones at 3 GSps (that is from DC to 6 GHz), measurements performed on an EV12DS130AGS device (CI-CGA 255 package, with an overall 6GHz bandwidth limitation).

In IUCM mode with a 3GHz clock, the actual data rate is 1.5 GSps, and therefore each Nyquist zone is only 750 MHz wide.

Zeroes at 1.5GHz and 4.5GHz are zeroes of the cos(x) function, see Section 4.5 on page 24 for theory.

The other Zeroes depending on the output mode are exactly the same as per in non IUMC mode.

Figure 6-59. Spectrum over 8 Nyquist zones at 3 GSps in NRZ output mode, IUCM on

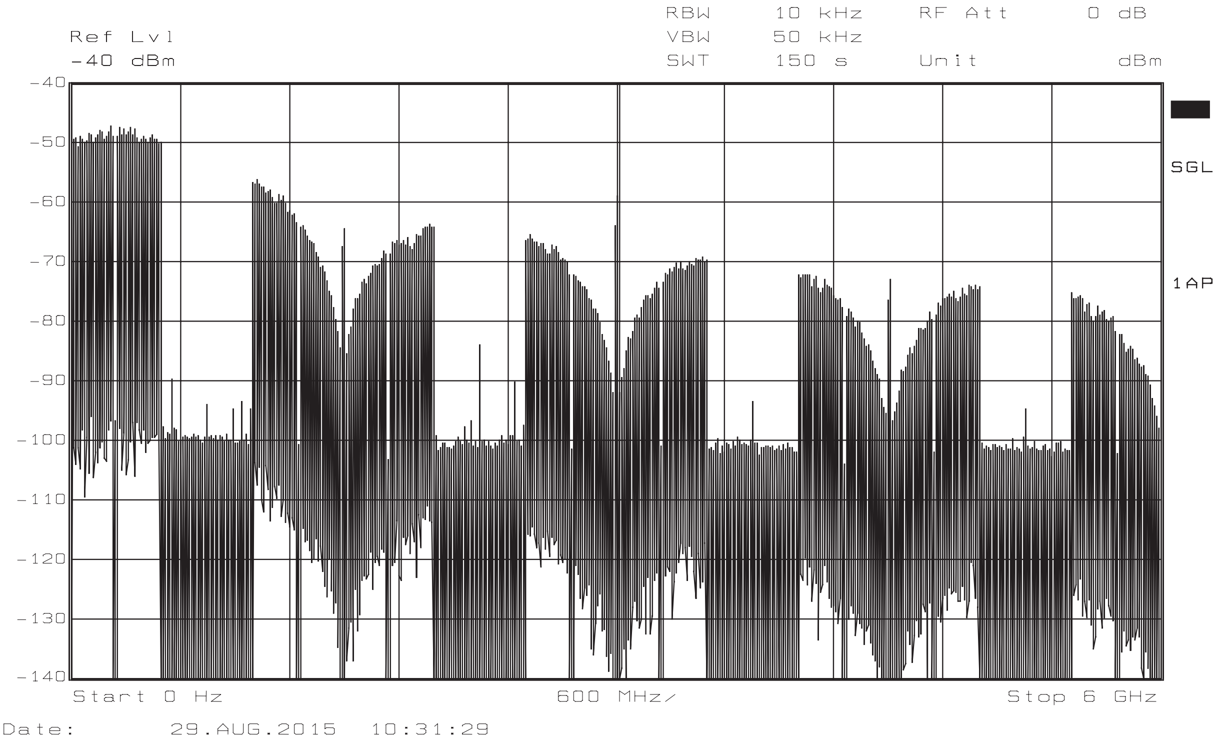


Figure 6-60. Spectrum over 8 Nyquist zones at 3 GSps in NRTZ output mode, IUCM on

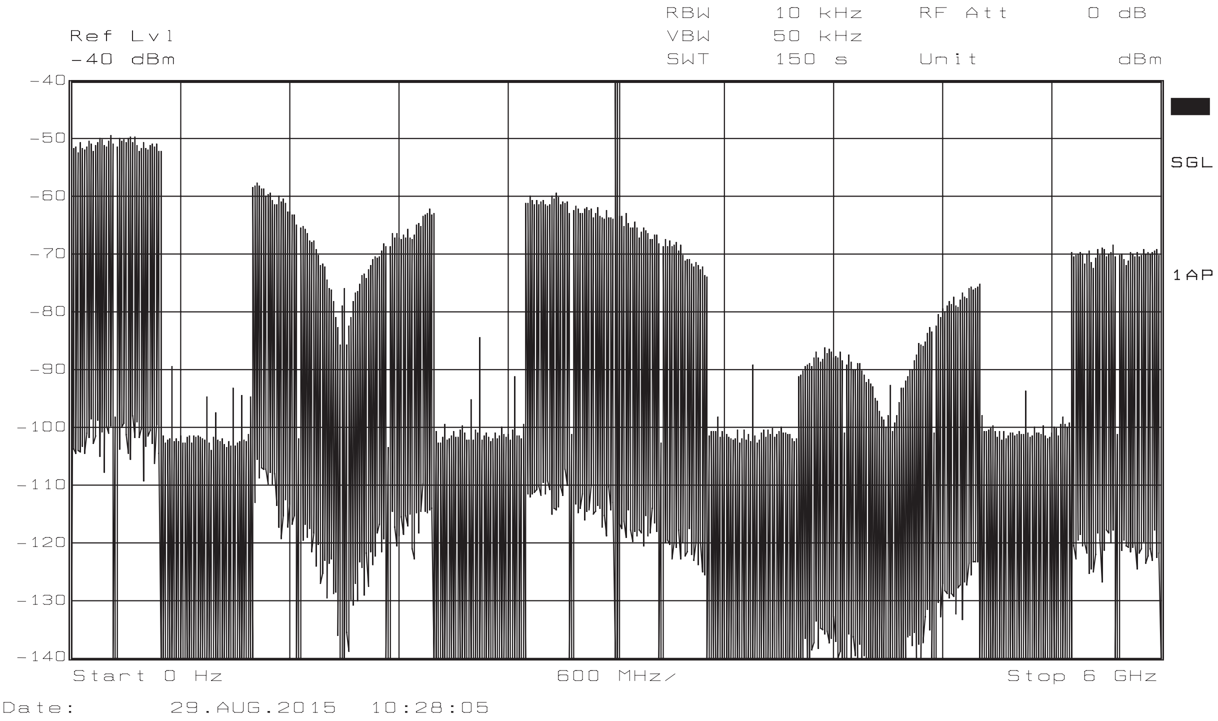


Figure 6-61. Spectrum over 8 Nyquist zones at 3 GSps in RTZ output mode, IUCM on

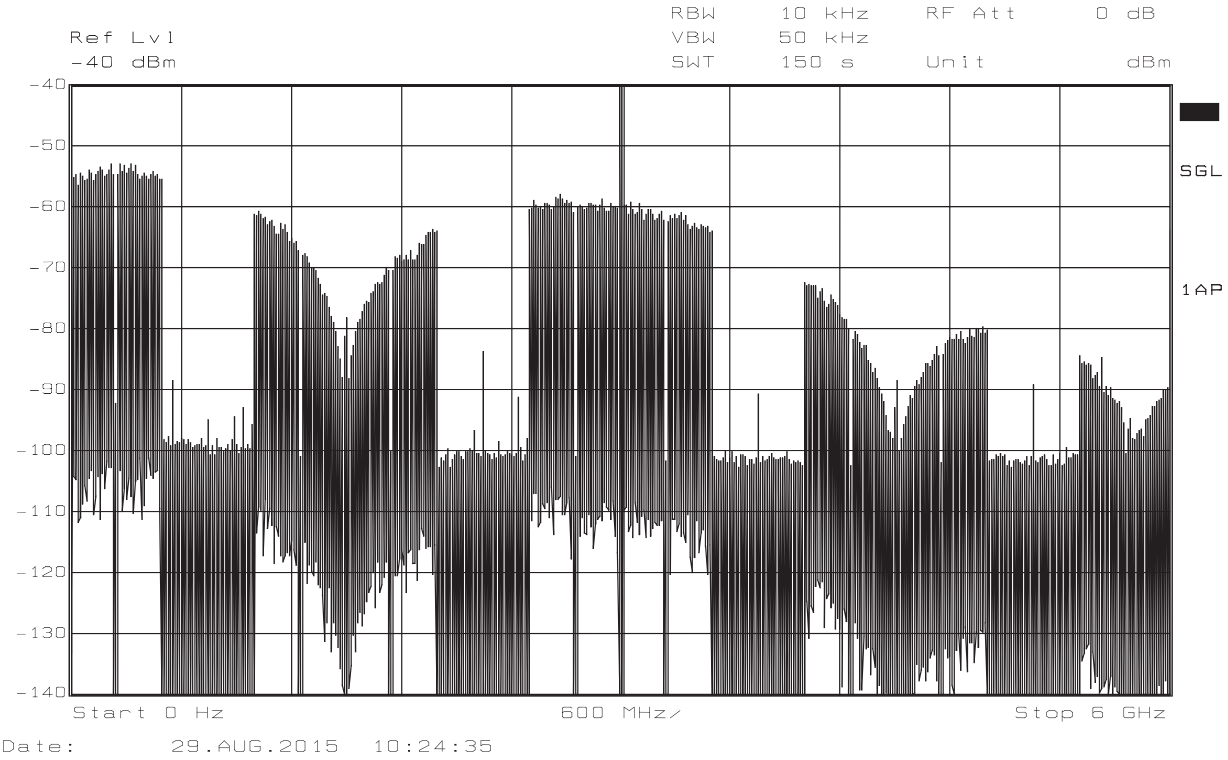
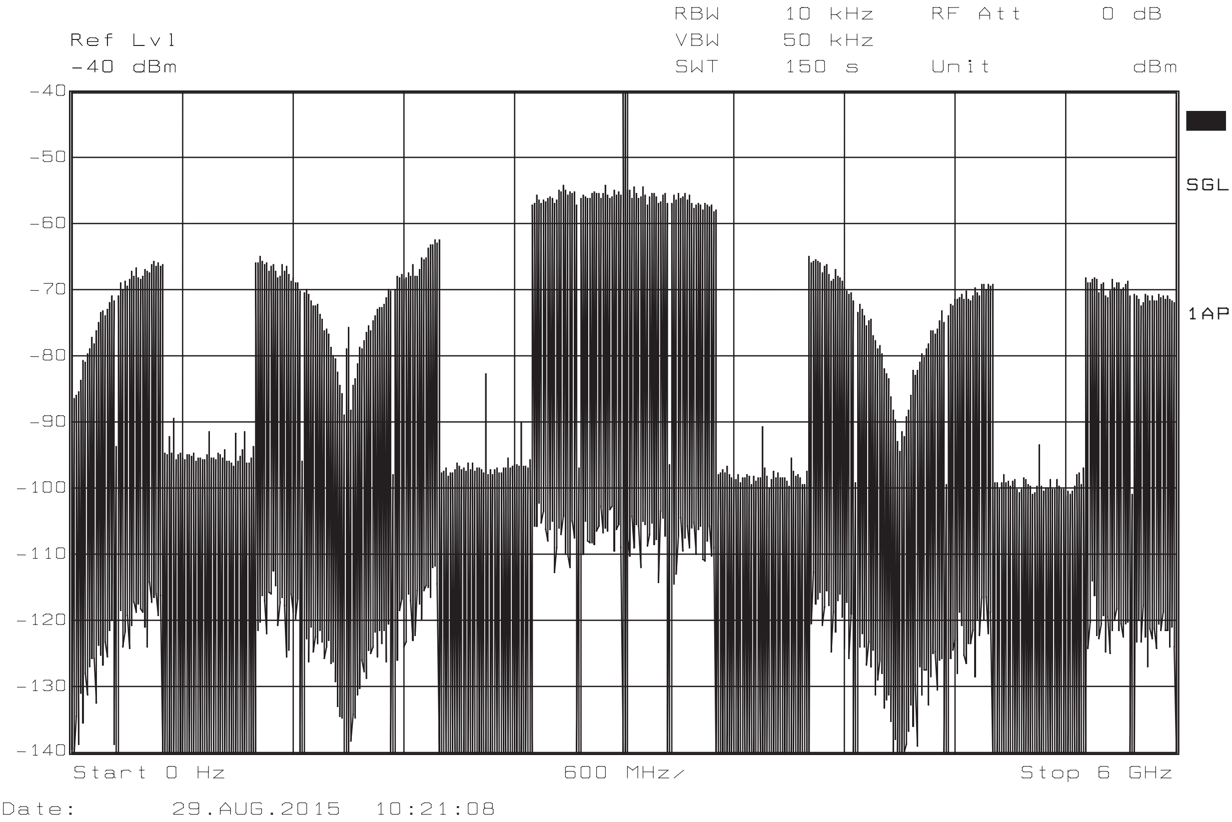


Figure 6-62. Spectrum over 8 Nyquist zones at 3 GSps in RF output mode, IUCM = 1



Measurements show a good fit with theory, see Section 4.5 on page 24.

7. Application Information

7.1 Analogue Output (OUT/OUTN)

The analogue output should be used in differential way as described in the figures below.

If the application requires a single-ended analogue output, then a balun is necessary to generate a single-ended signal from the differential output of the DAC.

Figure 7-1. Analogue Output Differential Termination

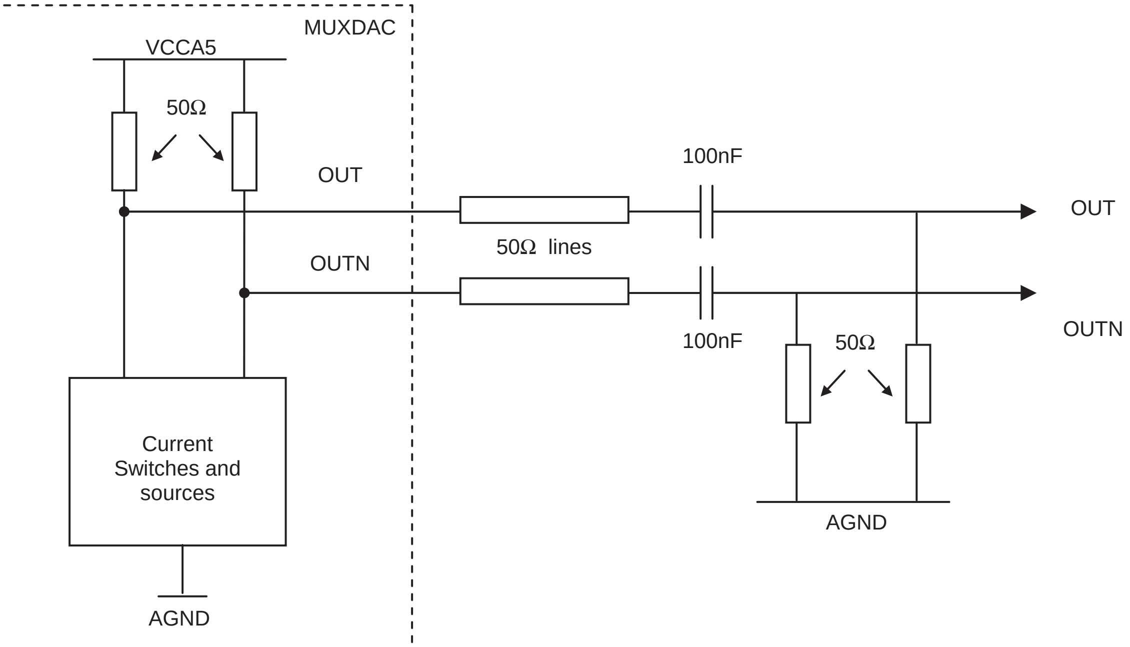
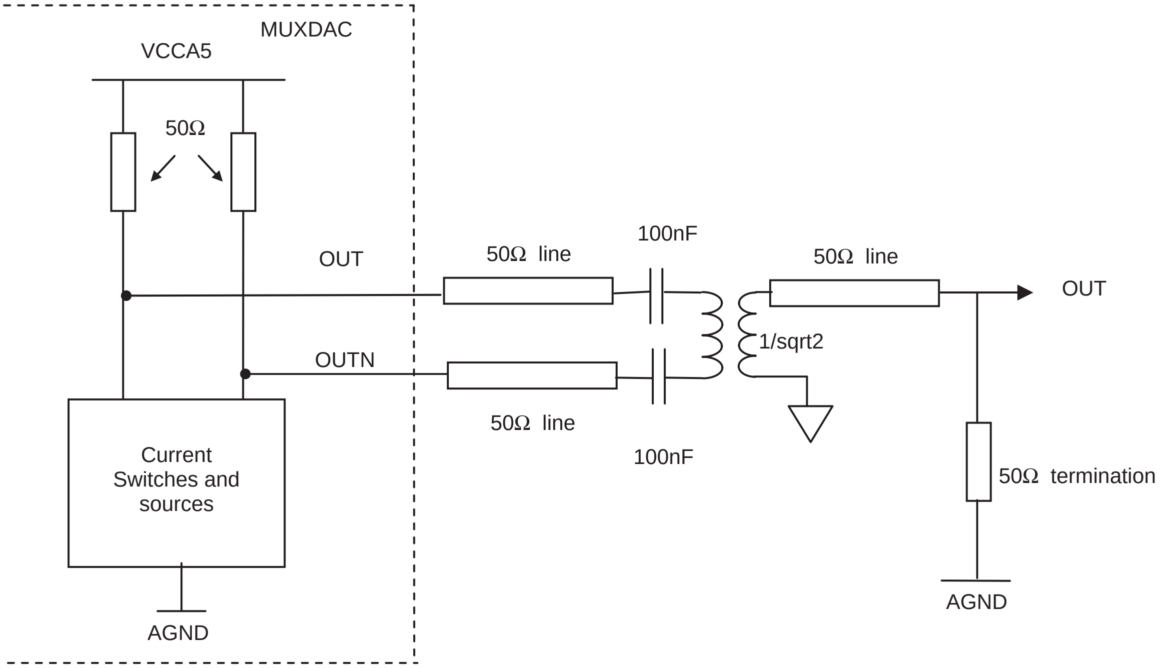


Figure 7-2. Analogue Output Using a 1/ √2 Balun

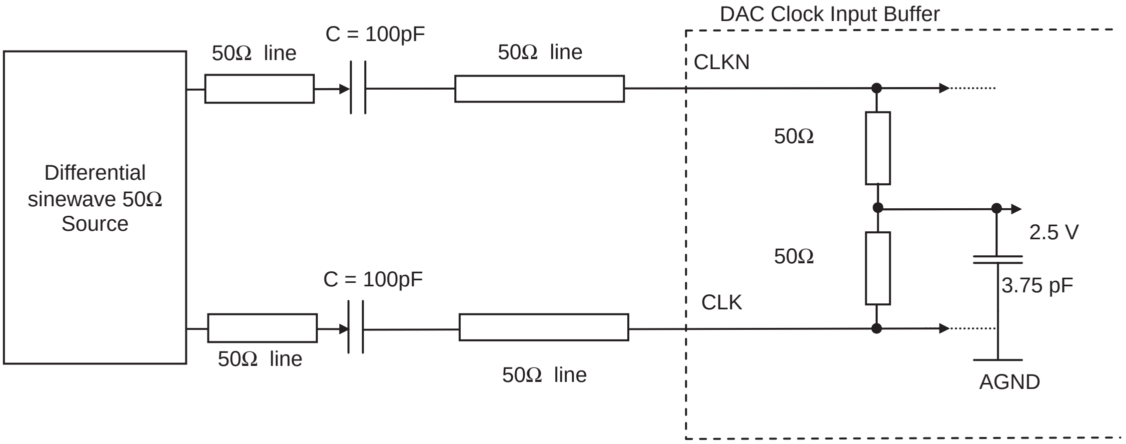


Note: The AC coupling capacitors should be chosen as broadband capacitors with a value depending on the application.

7.2 Clock Input (CLK/CLKN)

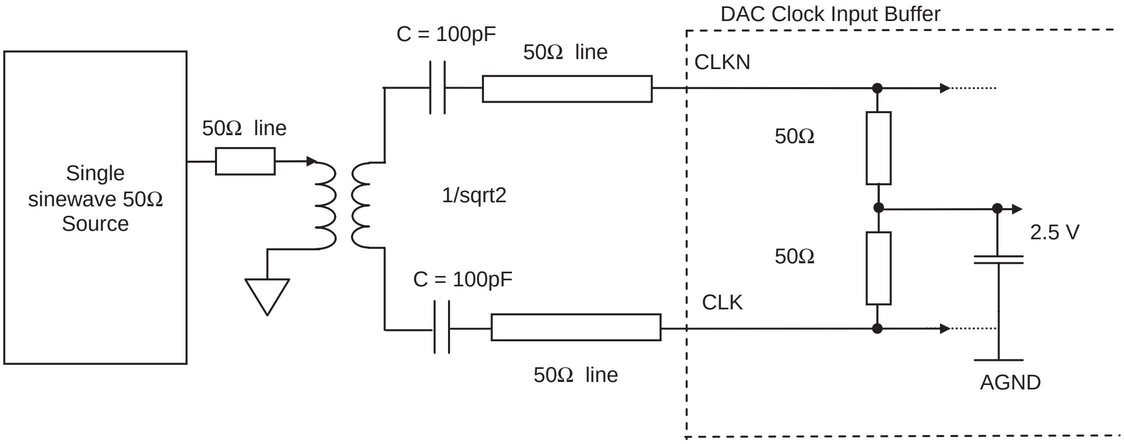
The DAC input clock (sampling clock) should be entered in differential mode as described in Figure 4-9 on page 22.

Figure 7-3. Clock Input Differential Termination



Note: The buffer is internally pre-polarized to 2.5V (buffer between V_{CC5} and AGND).

Figure 7-4. Clock Input Differential with Balun



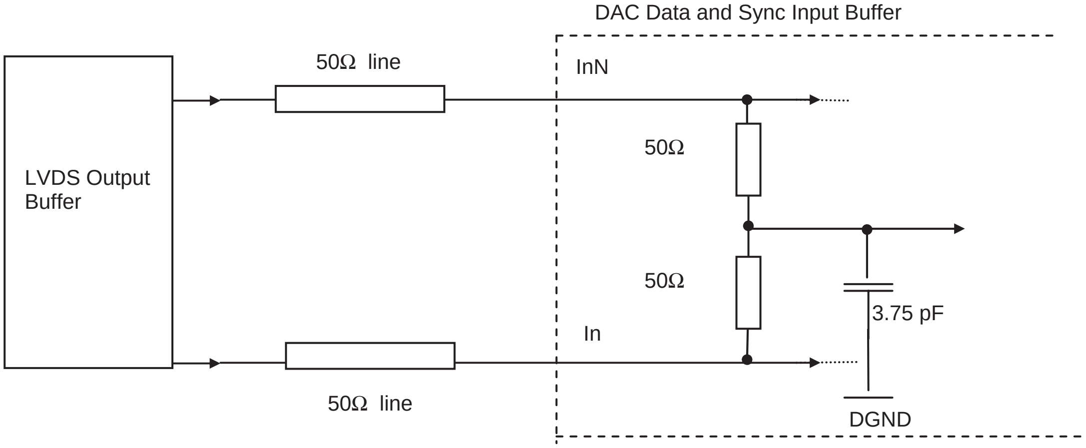
Note: The AC coupling capacitors should be chosen as broadband capacitors with a value depending on the application.

7.3 Digital Data, SYNC and IDC Inputs

LVDS buffers are used for the digital input data, the reset signal (active low) and IDC signal.

They are all internally terminated by 2 × 50Ω to ground via a 3.75 pF capacitor.

Figure 7-5. Digital Data, Reset and IDC Input Differential Termination



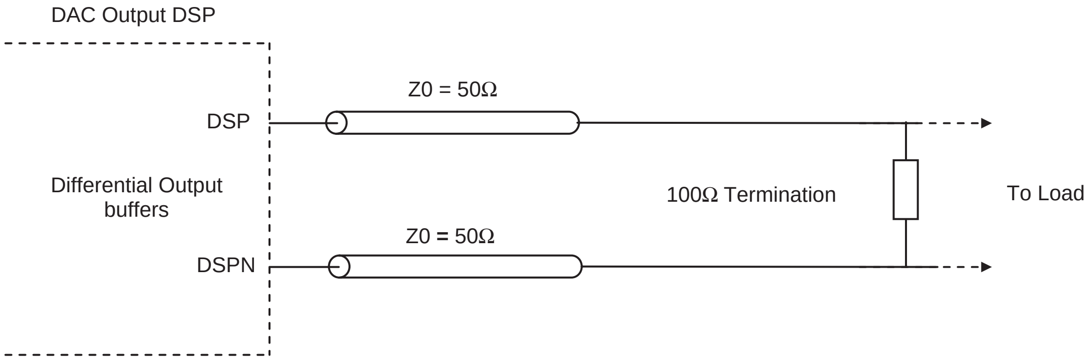
Notes:
1. In the case when only two ports are used (2:1 MUX ratio), then the unused data should be left open (no connect).
2. Data and IDC signals should be routed on board with the same layout rules and the same length.

7.4 DSP Clock

The DSP, DSPN output clock signals are LVDS compatible.

They have to be terminated via a differential 100Ω termination as described in Figure 4-11 on page 23.

Figure 7-6. DSP Output Differential Termination



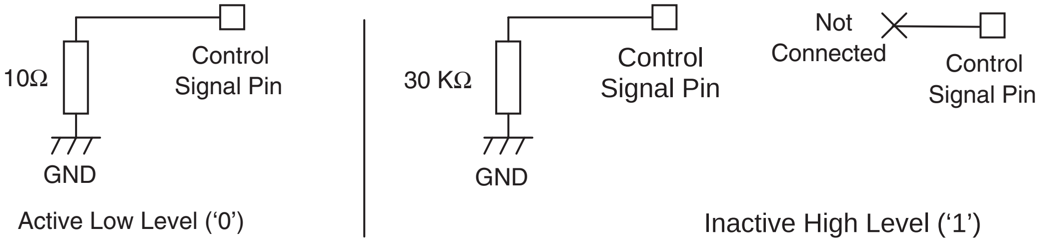
7.5 Control Signal Settings

The MUX, MODE, PSS and OCDS control signals use the same static input buffer.

Logic “1” = 30 KΩ to Ground, or tied to V_{CCD} = 3.3V or left open

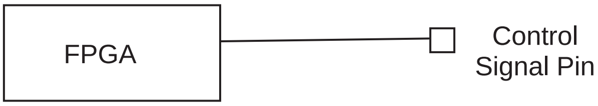
Logic “0” = 10Ω to Ground or Grounded

Figure 7-7. Control Signal Settings



The control signal can be driven by FPGA.

Figure 7-8. Control Signal Settings with FPGA



Logic “1” > V_{IH} or V_{CCD} = 3.3V

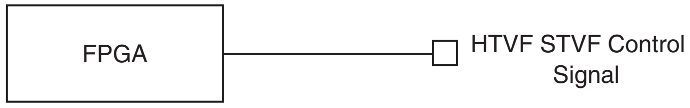
Logic “0” < V_{IL} or 0V

7.6 HTVF and STVF Control Signal

The HTVF and STVF control signals is a output 3.3V CMOS buffer.

These signals could be acquired by FPGA.

Figure 7-9. Control Signal Settings with FPGA



In order to modify the Vol/Voh value, pull up and pull down resistances of 10KΩ could be used

7.7 GA Function Signal

This function allows you to adjust the internal gain of the DAC.

The gain of the DAC can be tuning with applied analog voltage from 0 to V_{CCA3}

This analog input signal could be generated by a DAC control by FPGA or microcontroller.

Figure 7-10. Control Signal Settings with GA

7.8 Power Supplies Decoupling and Bypassing

The DAC requires 3 distinct power supplies:

V_{CCA5} = 5V (for the analogue core)

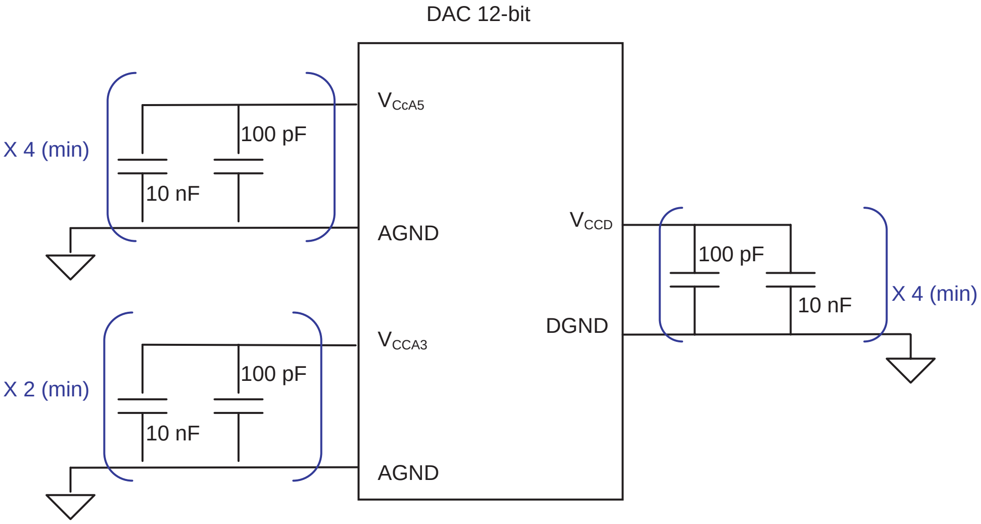
V_{CCA3} = 3.3V (for the analogue part)

V_{CCD} = 3.3V (for the digital part)

It is recommended to decouple all power supplies to ground as close as possible to the device balls with 100 pF in parallel to 10nF capacitors. The minimum number of decoupling pairs of capacitors can be calculated as the minimum number of groups of neighbouring pins.

4 pairs of 100pF in parallel to 10 nF capacitors are required for the decoupling of V_{CCA5}. 4 pairs for the V_{CCA3} is the minimum required and finally, 10 pairs are necessary for V_{CCD}.

Figure 7-11. Power Supplies Decoupling Scheme



Each power supply has to be bypassed as close as possible to its source or access by 100 nF in parallel to 22 µF capacitors (value depending of DC/DC regulators).

7.9 Power Up sequencing

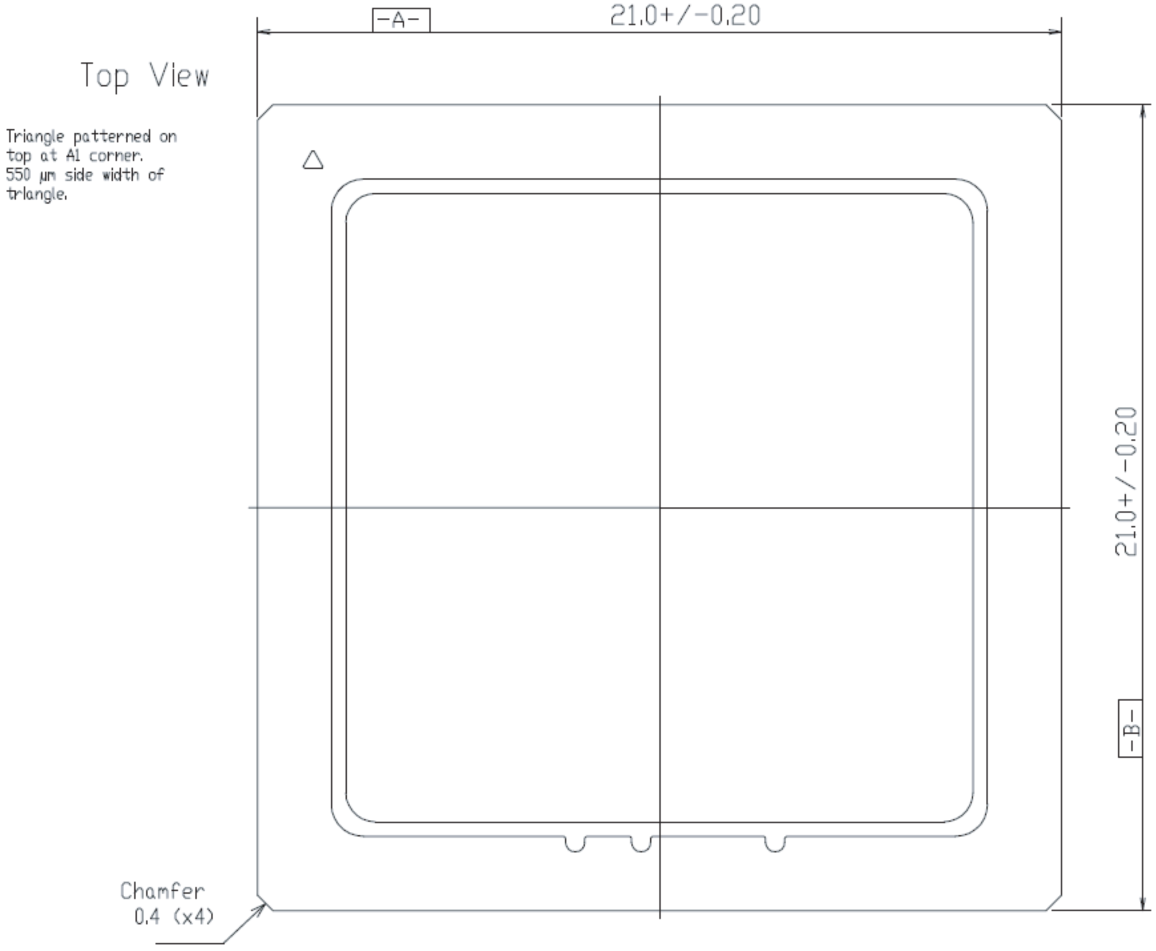
In order to optimize the performance, it is recommended to follow the power up sequence:
V_{CCD} => V_{CCA3} => V_{CCA5}

8. Package Information

8.1 CLGA255 Outline

8.1.1 Top View

Figure 8-1. Ci-CGA255 Top View

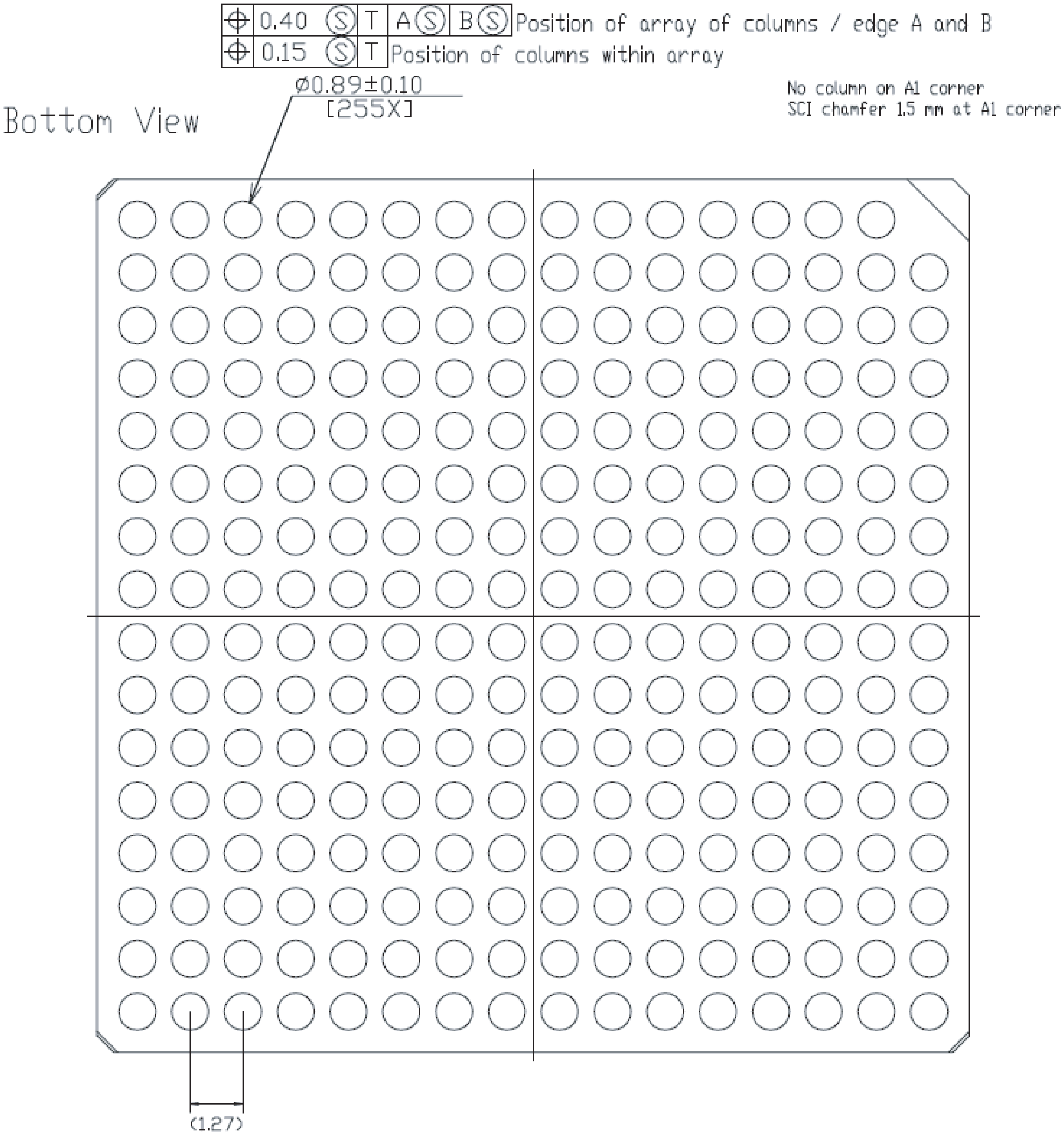


All units in mm

Seal ring is connected to AGND

8.1.2 Bottom View

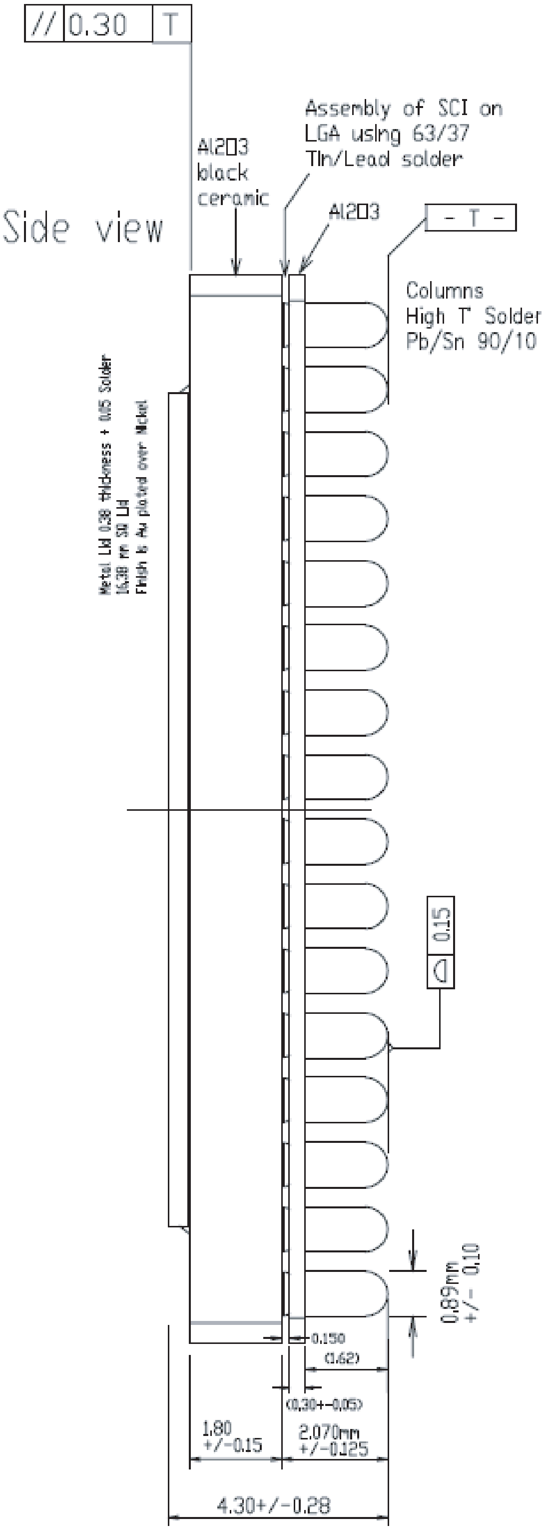
Figure 8-2. Ci-CGA255 Bottom View



All units in mm.

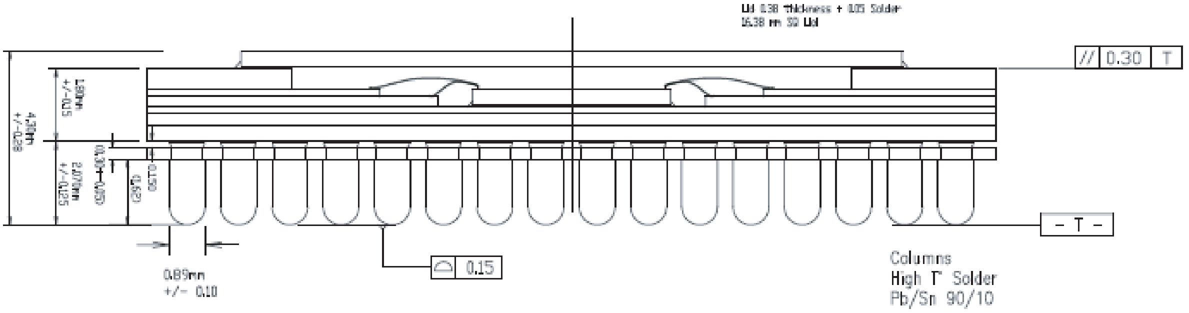
8.1.3 Side View

Figure 8-3. Ci-CGA255 Side View



8.1.4 Cross Section

Figure 8-4. Ci-CGA255 Cross Section



All units in mm.

Die backplane is connected to AGND

8.2 Thermal Characteristics CI-CGA255

Assumptions:

- Die thickness = 300µm
- No convection
- Pure conduction
- No radiation
  - Rth Junction -bottom of columns (NTK SCI – 0.89 mm diameter) = 13.8°C/W
  - Rthj-top of lid = 19.3°C/W
  - Rthj-board (JEDEC JESD51-8) = 17°C/W (board size = 39 x 39 mm, 1.6 mm thickness)

Assumptions:

- Convection according to JEDEC
- Still air
- Horizontal 2s2p board
  - Rth-j-a (JEDEC) = 29.5°C/W (board size 114.3 x 76.2 mm, 1.6 mm thickness)

Assumptions:

- Convection according to JEDEC, except larger board dimensions and one additional copper plane
- Still air
- Horizontal 2s3p board
  - Rth-j-a (JEDEC) = 18.9°C/W (board size 260 x 220 mm, 1.6 mm thickness)

9. Ordering Information

Table 9-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EVX12DS130AGS	CI-CGA255	Ambient	Prototype	
EV12DS130AMGSD/T	CI-CGA255	–55°C< Tc,Tj<125°C	D/T Grade	
EV12DS130AMGS9NB1	CI-CGA255	–55°C < Tc,Tj <125°C	Space Grade	
EV12DS130AGS-EB	CI-CGA255	Ambient	Prototype	Evaluation board

Table of Contents

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