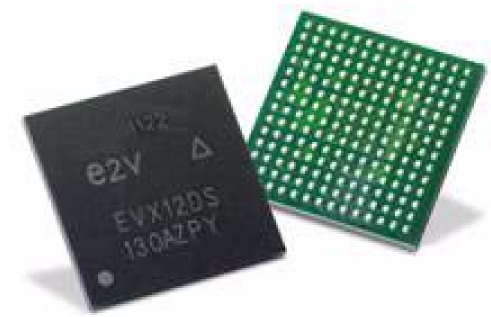
EV12DS130AZP
Low Power 12-bit 3 Gsps Digital to Analog Converter with 4/2:1 Multiplexer

Datasheet



Main Features

- 12-bit Resolution
- 3 GSps Guaranteed Conversion Rate
- 7 GHz Analog Output Bandwidth
- 4:1 or 2:1 integrated Parallel MUX (Selectable)
- Selectable Output Modes:
  Return to Zero, Non Return to Zero, Narrow Return to Zero, RF
- Low Latency Time: 3.5 Clock Cycles
- 1.4 Watt Power Dissipation in MUX 4:1 Mode
- Functions
  - Selectable MUX Ratio 4:1 (Full Speed), 2:1 (Half Speed)
  - Triple Majority Voting
  - User-friendly Functions:
    - Gain Adjustment
    - Input Data Check Bit (FPGA Timing Check)
    - Setup Time and Hold Time Violation Flags (STVF, HTVF)
    - Clock Phase Shift Select for Synchronization with DSP (PSS[2:0])
    - Output Clock Division Selection (Possibility to Change the Division Ratio of the DSP Clock)
    - Input Under Clocking Mode
    - Diode for Die junction Temperature Monitoring
- LVDS Differential Data input and DSP Clock Output
- Analog Output Swing: $1V_{pp}$ Differential (100Ω Differential Impedance)
- External Reset for Synchronization of Multiple MuxDACs
- Power Supplies: 3.3 V (Digital), 3.3V & 5.0V (Analog)
- FpBGA Package (15 × 15 mm Body Size, 1 mm Pitch)

Performances

Broadband: NPR at –14 dB Loading Factor, (See Section 7.2.7 "NPR Performance" on page 59)

- 1st Nyquist (NRTZ): NPR = 51.3 dB 10.0 Bit Equivalent at Fs = 3 GSps
- 1st Nyquist (NRTZ): NPR = 55.7 dB 10.8 Bit Equivalent at Fs = 1.5 GSps
- 2nd Nyquist (NRTZ or RTZ): NPR = 44.6 dB 8.9 Bit Equivalent at Fs = 3 GSps
- 3rd Nyquist (RF): NPR = 42.5 dB 8.6 Bit Equivalent at Fs = 3 GSps

Single Tone: (see Section 5. "Functional Description" on page 15)

- Performances Characterized for Fout from 100 MHz to 4500 MHz and from 2 GSps to 3.2 GSps.
- Performance Industrially Screened Over 3 Nyquist Zones at 3 GSps for Selected Fout.

Step Response

- Full Scale Rise /Fall Time 50 ps

Visit our website: www.e2v.com
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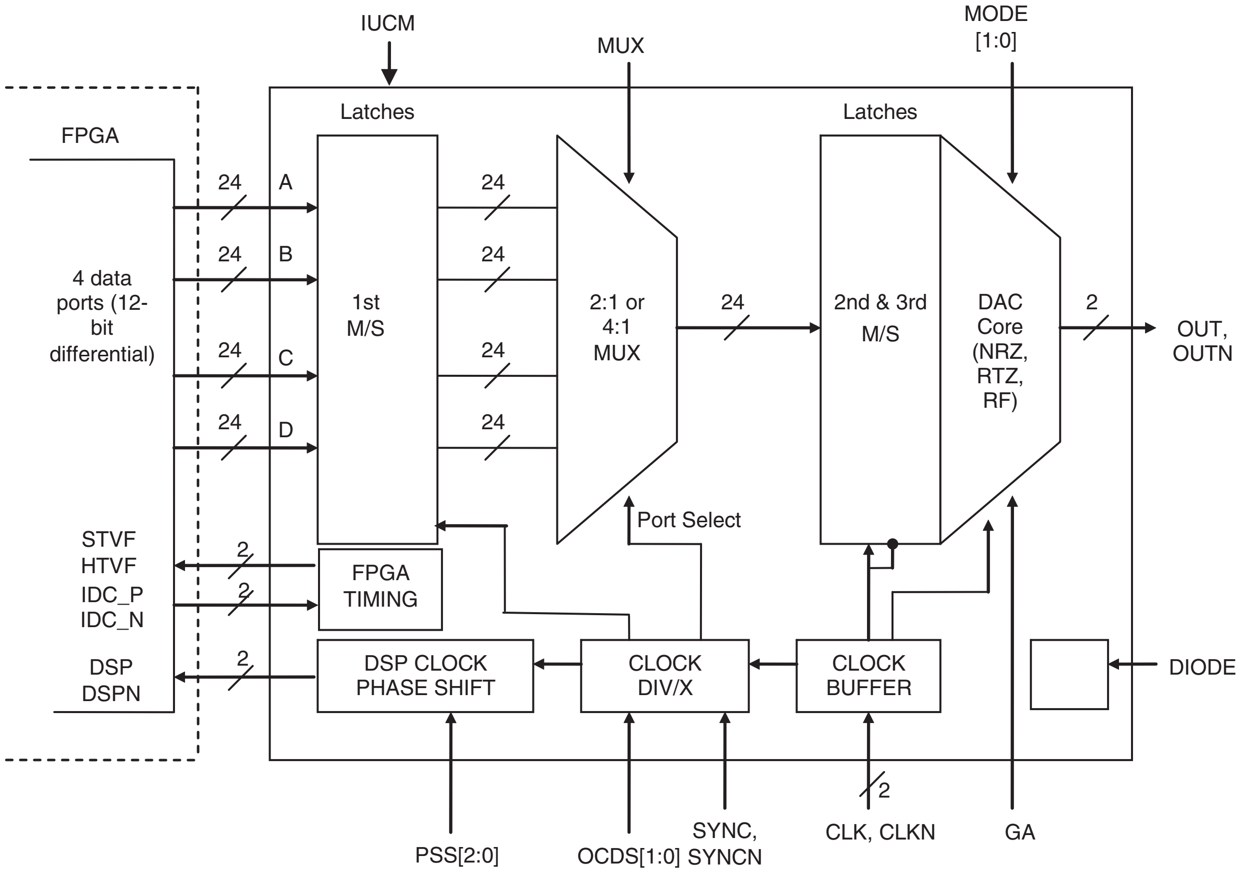
1077E–BDC–12/13

Applications

- **Direct Digital Synthesis for Broadband Applications (L-S and Lower C Band)**
- **Automatic Test Equipment (ATE)**
- **Arbitrary Waveform Generators**
- **Radar Waveform Signal Synthesis**
- **DOCSIS V3.0 Systems**

1. Block Diagram

Figure 1-1. Simplified Block Diagram



2. Description

The EV12DS130A is a 12-bit 3 GSps DAC with an integrated 4:1 or 2:1 multiplexer, allowing easy interface with standard LVDS FPGAs thanks to user friendly features as OCDS, PSS.

It embeds different output modes (RTZ, NRZ, narrow RTZ, RF) that allows performance optimizations depending on the working Nyquist zone.

The Noise Power Ratio (NPR) performance, over more than 900 MHz instantaneous bandwidth, and the high linearity (SFDR, IMD) over full 1^{st} Nyquist zone at 3 GSps (NRZ feature), make this product well suited for high-end applications such as arbitrary waveform generators and broadband DDS systems.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Positive Analog supply voltage	V_{CCA5}	6.0	V
Positive Analog supply voltage	V_{CCA3}	4.0	V
Positive Digital supply voltage	V_{CCD}	4.0	V
Digital inputs (on each single-ended input) and IDC, SYNC, signal Port P = A, B, C, D V_{IL} V_{IH} Digital Input maximum Differential mode swing	[P0..P11], [P0N.. P11N] IDC_P, IDC_N SYNC, SYNCN	GND–0.3 V_{CCA3} 2.0	V V V_{pp}
Master clock input (on each single-ended input) V_{IL} V_{IH} Master Clock Maximum Differential mode swing	CLK, CLKN	1.5 3.5 2.5	V V V_{pp}
Control functions inputs V_{IL} V_{IH}	MUX, MODE[0..1], PSS[0..2], OCDS[0..1]	–0.4V V_{CCD} + 0.4	V V
Gain Adjustment function	GA	–0.3V, V_{CCA3} + 0.3	V
Maximum Junction Temperature	Tj	170	°C
Storage Temperature	Tstg	–65 to 150	°C
Electrostatic discharge immunity ESD Classification	ESD HBM	1000 Class 1B	V

Notes:
1. Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
2. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.
3. Maximum ratings enable active inputs with DAC powered off.
4. Maximum ratings enable floating inputs with DAC powered on.
5. DSP clock and STVF, HTVF output buffers must not be shorted to ground nor positive power supply.

3.2 Recommended Conditions of Use

Table 3-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Recommended Value	Unit	Note
Positive analog supply voltage	V_{CCA5}		5.0	V	(2)(4)
Positive analog supply voltage	V_{CCA3}		3.3	V	(1)(2)(4)
Positive digital supply voltage	V_{CCD}		3.3	V	(2)(4)
Digital inputs (on each single-ended input) and IDC, SYNC, signal Port P = A, B, C, D V_{IL} V_{IH} Differential mode swing	[P0..P11], [P0N.. P11N] IDC_P, IDC_N SYNC, SYNCN		 1.075 1.425 700	 V V mV_{pp}	(3)
Master clock input power level (Differential mode)	P_{CLK}		3	dBm	(3)
Control functions inputs	MUX, OCDS, PSS, MODE, PSS	V_{IL} V_{IH}	0 V_{CCD}	V V	
Gain Adjustment function	GA	Range	0 V_{CCA3}	V	
Operating Temperature Range	T_c T_j	Commercial "C" grade Industrial "V" grade	$T_c > 0°C$ / $T_j < 90°C$ $T_c > -40°C$ / $T_j < 110°C$	°C	

Notes:
1. For low temperature it is recommended to operate at maximum analog supplies (V_{CCA3}) level.
2. In order to obtain the guaranteed performances and functionality the following rules shall be followed when powering the device: (see Section 8.9 "Power Up Sequencing" on page 72)

   Power-up sequence:
   It is necessary to raise V_{CCA5} power supply within the range 5.20V up to a recommended maximum of 5.60V during at least 1ms at power up. Then the supply voltage has to settle within 500 ms to a steady nominal supply voltage within a range of 4.75V up to 5.25V.
   A power-up sequence on V_{CCA5} that does not comply with the above recommendation will not compromise the functional operation of the device. Only the noise floor will be affected.

   The rise time for any of the power supplies (V_{CCD}, V_{CCA5} and V_{CCA3}) shall be ≤ 10 ms.

   At power-up a SYNC pulse is internally and automatically generated when the following sequence is satisfied: V_{CCD}, V_{CCA3} and V_{CCA5}. To cancel the SYNC pulse at power-up, it is necessary to apply the sequence: V_{CCA5}, V_{CCA3}, V_{CCD}. (V_{CCA3} can not reach 0.5V until V_{CCA5} is greater than 4.5V. V_{CCD} can not reach 0.5V until V_{CCA3} is greater than 3.0V). Any other sequence may not have a deterministic SYNC behaviour.

   Relationship between power supplies:
   Within the applicable power supplies range, the following relationship shall always be satisfied $V_{CCA3} \geq V_{CCD}$, taking into account AGND and DGND planes are merged and power supplies accuracy. See erratasheet (ref 1125) for SYNC condition of use.
3. Analog output is in differential. Single-ended operation is not recommended. Guaranteed performance is only in differential configuration.
4. No power-down sequencing is required.

3.3 Electrical Characteristics

Values in the tables below are based on our conditions of measurement in room temperature for typical power supply (V_{CCA5} = 5.0V, V_{CCA3} = 3.3V, V_{CCD} = 3.3V), typical swing and in MUX4:1 otherwise specified.

Table 3-3. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test Level[(2)]
RESOLUTION			12		bit		
POWER REQUIREMENTS							
Power Supply voltage - Analog - Analog - Digital	 V_{CCA5} V_{CCA3} V_{CCD}	 4.75 3.15 3.15	 5 3.3 3.3	 5.25 3.45 3.45	V V	(7)(8)	1
Power Supply current (4:1 MUX) - Analog - Analog - Digital	 I_{CCA5} I_{CCA3} I_{CCD}		 84 106 187	 90 122 202	 mA mA mA		1
Power Supply current (2:1 MUX) - Analog - Analog - Digital	 I_{CCA5} I_{CCA3} I_{CCD}		 84 106 160	 90 122 172	 mA mA mA		1
Power dissipation (4:1 MUX)	P_D		1.4	1.6	W		1
Power dissipation (2:1 DMUX)	P_D		1.3	1.5	W		1
DIGITAL DATA INPUTS, SYNC and IDC INPUTS							
Logic compatibility			LVDS				
Digital input voltages: - Differential input voltage - Common mode	 V_{ID} V_{ICM}	 100	 350 1.25	 500	 mV_p V		 1 1
Input capacitance from each single input to ground				2	pF		5
Differential Input resistance		80	100	120	Ω		1
CLOCK INPUTS							
Input voltages (Differential operation swing)		0.56	1	2.24	V_{pp}		4
Power level (Differential operation)		–4	1	8	dBm		4
Common mode		2.4	2.5	2.6	V		
Input capacitance from each single input to ground (at die level)				2	pF		5
Differential Input resistance:		80	100	120	Ω		1
DSP CLOCK OUTPUT							
Logic compatibility			LVDS				
Digital output voltages:							
- Differential output voltage - Common mode	V_{OD} V_{OCM}	240	350 1.3	450	mV_p V		1

Table 3-3. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test Level[(2)]
ANALOG OUTPUT							
Full-scale Differential output voltage (100Ω differentially terminated)		0.92	1	1.08	V_{pp}		1
Full-scale output power (differential output)		0.25	1	1.64	dBm		1
Single-ended mid-scale output voltage (50Ω terminated)			$V_{CCA5} – 0.43$		V	(4)	
Output capacitance			1.5		pF		5
Output internal differential resistance		90	100	110	Ω		1
Output VSWR (using e2v evaluation board) 1.5 GHz 3 GHz 4.5 GHz			 1.17 1.54 1.64				4
Output bandwidth			7		GHz		4
FUNCTIONS							
Digital functions: MODE, OCDS, PSS, MUX - Logic 0 - Logic 1	 V_{IL} V_{IH} I_{IN}	 1.6	 0 V_{CCD}	 0.8 150	 V V µA	 (6)	1
Gain Adjustment function	GA		0 V_{CCA3}				1
Digital output function (HTVF, STVF) Logic 0 Logic 1	 V_{OL} V_{OH} I_O	 – 2.3	 – –	 0.8 80	 V V µA	 (5) (6)	1
DC ACCURACY							
Differential Non-Linearity	DNL+		0.5	0.95	LSB		1
Differential Non-Linearity	DNL-	–0.95	–0.5		LSB		1
Integral Non-Linearity	INL+		1	3	LSB		1
Integral Non-Linearity	INL-	–3	–0.8		LSB		1
DC gain: - Initial gain error - DC gain adjustment - DC gain sensitivity to power supplies - DC gain drift over temperature		 –8	 0 ±11 ±2	 +8 +6	 % % % %	(3)	 1 1 1 4

Notes:
1. For use in higher Nyquist zone, it is recommended to use higher power clock within the limit.
2. See Section 3.6 on page 13 for explanation of test levels.
3. Initial gain error corresponds to the deviation of the DC gain center value from unity gain. The DC gain adjustment (GA function) ensures that the initial gain deviation can be cancelled.
   The DC gain sensitivity to power supplies is given according the rule:
   GainSensVsSupply = |Gain@VccMin – Gain@VccMax| / Gain@Vccnom
4. Single-ended operation is not recommended, this line is given for better understanding of what is output by the DAC.
5. In order to modify the V_{OL}/V_{OH} value, potential divider could be used.
6. Sink or source.

7. Relationship between power supplies:
   Within the applicable power supplies range, the following relationship shall always be satisfied $V_{CCA3} \geq V_{CCD}$, taking into account AGND and DGND planes are merged and power supplies accuracy.
8. Please refer Section 8.9 ”Power Up Sequencing” on page 72.

3.4 AC Electrical Characteristics

Values in the tables below are based on our conditions of measurement in room temperature for typical power supply (V_{CCA5} = 5.0V, V_{CCA3} = 3.3V, V_{CCD} = 3.3V), typical swing and in MUX4:1 otherwise specified.

Table 3-4. AC Electrical Characteristics NRZ Mode (First Nyquist Zone)

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test level(2)
Single-tone Spurious Free Dynamic Range First Nyquist MUX 4:1 Fs = 3 GSps @ Fout = 100 MHz 0 dBFS Fs = 3 GSps @ Fout = 400 MHz 0 dBFS Fs = 3 GSps @ Fout = 100 MHz –3 dBFS	$\lvert SFDR \rvert$	59	68 63 70		dBc	(1)	1 4 4
Highest spur level First Nyquist MUX 4:1 Fs = 3 GSps @ Fout = 100 MHz 0 dBFS Fs = 3 GSps @ Fout = 400 MHz 0 dBFS Fs = 3 GSps @ Fout = 100 MHz –3 dBFS			–68 –59 –72	–58	dBm		1 4 4
SFDR sensitivity & high spur level variation over temperature			±2		dB		4
SFDR sensitivity & high spur level variation over power supplies			±2		dB		4
Signal independent Spur (clock-related spur)							
Fc/2			–82		dBm		4
Fc/4			–85		dBm		4
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 3 GSps 20 MHz to 900 MHz broadband pattern 25 MHz notch centered on 450 MHz	NPR		46		dB	(3)	4
Equivalent ENOB Computed from NPR figure	ENOB		9.2		Bit		4
Signal to Noise Ratio Computed from NPR figure	SNR		57		dB		4
Self Noise Density at code 0 or 4095			–163		dBm/Hz		4

Notes:
1. Ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured.
2. See Section 3.6 on page 13 for explanation of test levels.
3. Figures in tables are derived from industrial screening; for practical reasons (necessity to cover also 2nd and 3rd Nyquist Zones) the balun used for industrial test is not optimum for first Nyquist performances, and results when Fout or folded low order hamonics are between DC to 400 MHz are very pessimistic. For further details please refer to Section 7.2 on page 37 for effect of the balun on performances.

Table 3-5. AC Electrical Characteristics NRTZ Mode (First & Second Nyquist Zone)

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test level[2]
Single-tone Spurious Free Dynamic Range MUX4:1 Fs = 3 GSps @ Fout = 100 MHz 0 dBFS Fs = 3 GSps @ Fout = 700 MHz 0 dBFS Fs = 3 GSps @ Fout = 1800 MHz 0 dBFS Fs = 3 GSps @ Fout = 700 MHz –3 dBFS MUX2:1 Fs = 1.5 GSps @ Fout = 700 MHz 0 dBFS	ISFDRI	 54 53	 68 62 61 66 65		dBc	[1]	 4 4 1 4 1
Highest spur level MUX4:1 Fs = 3 GSps @ Fout = 100 MHz 0 dBFS Fs = 3 GSps @ Fout = 700 MHz 0 dBFS Fs = 3 GSps @ Fout = 1800 MHz 0 dBFS Fs = 3 GSps @ Fout = 700 MHz –3 dBFS MUX2:1 Fs = 1.5 GSps @ Fout = 700 MHz 0 dBFS			 –70 –64 –67 –70 –68	 –59 –55	dBm		 4 4 1 4 1
SFDR sensitivity & high spur level variation over temperature			±2		dB		4
SFDR sensitivity & high spur level variation over power supplies			±2		dB		4
Signal independent Spur (clock-related spur)							
Fc			–29		dBm		4
Fc/2			–80		dBm		4
Fc/4			< –80		dBm		4
Self Noise Density at code 0 or 4095			–149	–144	dBm/Hz		1
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 3 GSps 20 MHz to 900 MHz broadband pattern, 25 MHz notch centered on 450 MHz	NPR	46	50.2		dB	[3]	1
Equivalent ENOB Computed from NPR figure	ENOB	9.2	9.9		Bit	[3]	1
Signal to Noise Ratio Computed from NPR figure	SNR	57	61.2		dB	[3]	1
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 1.5 GSps 10 MHz to 450 MHz broadband pattern, 12.5 MHz notch centered on 225 MHz	NPR		55.7		dB	[3]	4
Equivalent ENOB Computed from NPR figure	ENOB		10.8		Bit	[3]	4
Signal to Noise Ratio Computed from NPR figure	SNR		66.7		dB	[3]	4

Notes: 1. Ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured.
2. See Section 3.6 on page 13 for explanation of test levels.
3. Figures in tables are derived from industrial screening; for practical reasons (necessity to cover also 2nd and 3rd Nyquist Zones) the balun used for industrial test is not optimum for first Nyquist performances, and results when Fout or folded low order hamonics are between DC to 400 MHz are very pessimistic. For further details please refer to Section 7.2 on page 37 for effect of the balun on performances.

Table 3-6. AC Electrical Characteristics RTZ Mode (Second Nyquist Zone)

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test level[2]
Single-tone Spurious Free Dynamic Range MUX4:1 Fs = 3 GSps @ Fout = 1600 MHz 0 dBFS Fs = 3 GSps @ Fout = 2900 MHz 0 dBFS	ISFDRI	50	60 57		dBc	[1]	1 4
Highest spur level MUX4:1 Fs = 3 GSps @ Fout = 1600 MHz 0 dBFS Fs = 3 GSps @ Fout = 2900 MHz 0 dBFS			–67 –66	–58	dBm		1 4
SFDR sensitivity & high spur level variation over temperature			±2		dB		4
SFDR sensitivity & high spur level variation over power supplies			±2		dB		4
Signal independent Spur (clock-related spur)							
Fc			–25		dBm		4
Fc/2			–80		dBm		4
Fc/4			< –80		dBm		4
Self Noise Density at code 0 or 4095			–143		dBm/Hz		4
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 3 GSps 1520 MHz to 2200 MHz broadband pattern, 25 MHz notch centered on 1850 MHz	NPR	40	44.0		dB	[3]	1
Equivalent ENOB Computed from NPR figure	ENOB	8.2	8.8		Bit	[3]	1
Signal to Noise Ratio Computed from NPR figure	SNR	51	55.0		dB	[3]	1

Notes: 1. Ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured.
2. See Section 3.6 on page 13 for explanation of test levels.
3. Please refer to Section 7.2 "AC Performances" on page 37 to have detailed characterization results.

Table 3-7. AC Electrical Characteristics RF Mode (Second and Third Nyquist Zones)

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test level[2]
Single-tone Spurious Free Dynamic Range	|SFDR|				dBc		
2^{nd} Nyquist							
Fs = 3 GSps @ Fout = 1600 MHz 0 dBFS			52			[1]	4
Fs = 3 GSps @ Fout = 2900 MHz 0 dBFS			60				4
3^{rd} Nyquist							
Fs = 3 GSps @ Fout = 3800 MHz 0 dBFS			53			[3]	4
Fs = 3 GSps @ Fout = 4400 MHz 0 dBFS		47	54				1
Highest spur level					dBm		
2^{nd} Nyquist							
Fs = 3 GSps @ Fout =1600 MHz 0 dBFS			–58				4
Fs = 3 GSps @ Fout = 2900 MHz 0 dBFS			–58				4
3^{rd} Nyquist							
Fs = 3 GSps @ Fout = 4400 MHz 0 dBFS			–62	–57			1
SFDR sensitivity & high spur level variation over temperature			±2		dB		4
SFDR sensitivity & high spur level variation over power supplies			±2		dB		4
Signal independent Spur (clock-related spur)							
Fc			–28		dBm		4
Fc/2			–80		dBm		4
Fc/4			< –80		dBm		4
Self Noise Density at code 0 or 4095			–141		dBm/Hz		4
Noise Power Ratio (2^{nd} Nyquist) –14 dBFS peak to rms loading factor Fs = 3 GSps 1520 MHz to 2200 MHz broadband pattern, 25 MHz notch centered on 1850 MHz	NPR		42		dB	[4]	4
Equivalent ENOB Computed from NPR figure	ENOB		8.5		Bit	[4]	4
Signal to Noise Ratio Computed from NPR figure	SNR		53		dB	[4]	4
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 3 GSps 2200 MHz to 2880 MHz broadband pattern, 25 MHz notch centered on 2550 MHz	NPR		42		dB	[4]	4
Equivalent ENOB Computed from NPR figure	ENOB		8.5		Bit	[4]	4
Signal to Noise Ratio Computed from NPR figure	SNR		53		dB	[4]	4

Table 3-7. AC Electrical Characteristics RF Mode (Second and Third Nyquist Zones) (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test level[(2)]
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 3 GSps 3050 MHz to 3700 MHz broadband pattern, 25 MHz notch centered on 3375 MHz	NPR	39	40		dB	(4)	1
Equivalent ENOB Computed from NPR figure	ENOB	8	8.2		Bit	(4)	1
Signal to Noise Ratio Computed from NPR figure	SNR	50	51		dB	(4)	1

Notes:
1. Ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured.
2. See Section 3.6 on page 13 for explanation of test levels.
3. Ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured over the third Nyquist frequency band (Fs to 3Fs/2).
4. Figures in tables herafter are derived from industrial screening without any correction to take in account the balun effect, but for practical reasons (necessity to cover also 2nd and 3rd Nyquist Zones) the balun used for industrial test is not optimum for first Nyquist performances, and results when Fout or folded low order hamonics are between DC to 400 MHz are very pessimistic. For further details please refer to Section 7.2 on page 37 for effect of the balun on performances.

3.5 Timing Characteristics and Switching Performances

Table 3-8. Timing Characteristics and Switching Performances

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test level[(1)]
SWITCHING PERFORMANCE AND CHARACTERISTICS							
Operating clock frequency 4:1 MUX mode 2:1 MUX mode		 300 300		 3000 1500	MHz		4
TIMING CHARACTERISTICS							
Analog output rise/fall time	T_{OR} T_{OF}			60	ps	(2)	4
Data Tsetup (Fc = 3 GSps)		250			ps	(3)	4
Data Thold (Fc = 3 GSps)		100			ps	(3)	4
Max Input data rate (Mux 4:1)			750		MSps		4
Max Input data rate (Mux 2:1)			750		MSps		4
Master clock input jitter				100	fs rms	(4)	4
DSP clock phase tuning range		0		+3.5	Clock Cycle		5
DSP clock phase tuning steps			0.5		Clock cycle		5
Master clock to DSP, DSPN delay	TDSP		1.6		ns		4
SYNC forbidden area lower bound	T_1		$0.5\ T_C$ + 300		ps	(5)	4
SYNC forbidden area upper bound	T_2		$0.5\ T_C$ + 160		ps	(5)	4

Table 3-8. Timing Characteristics and Switching Performances (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test level[1]
SYNC to DSP, DSPN MUX 2:1 MUX4:1			 880 1600		ps		4
Pipeline delay MUX4:1 MUX2:1	TDP			 3.5 3.5	Clock cycles		4
Output delay	TOD		160		ps		4

Notes:
1. See Section 3.6 on page 13 for explanation of the test level.
2. Analog output rise/fall time measured from 20% to 80% of a full scale jump, after probe de-embedding.
3. Exclusive of period (pp) jitter on Data. Setup and hold time for DATA at input relative to DSP clock at output of the component, at PSS = 000; also applicable for IDC signal.
4. Master clock input jitter defined over 5 GHz bandwidth.
5. T_C represents the master clock period. See Figure 3-3 on page 13.

Figure 3-1. Timing Diagram for 4:1 MUX Principle of Operation OCDS[00]

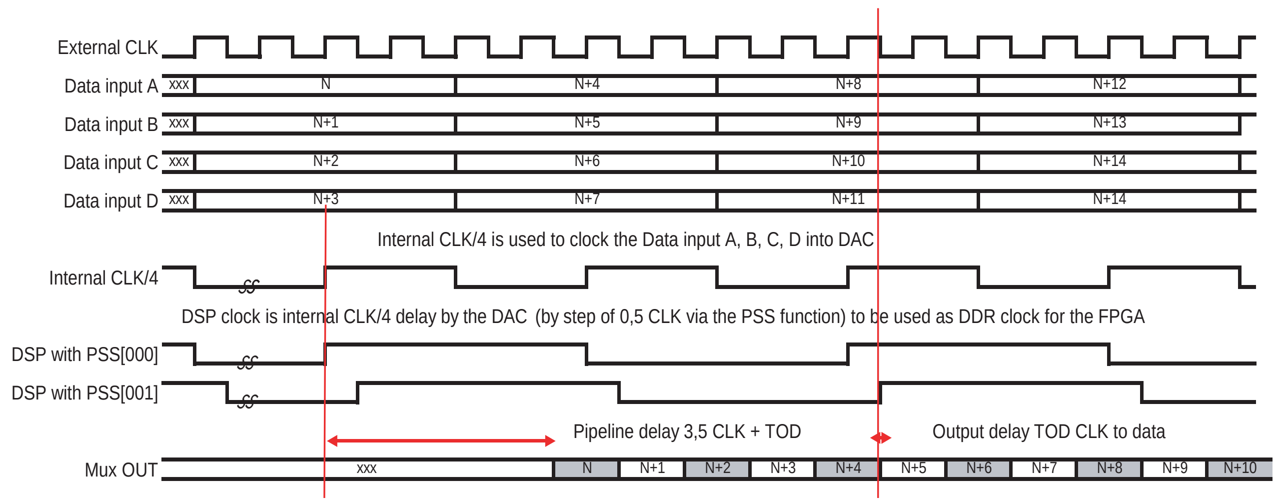


Figure 3-2. Timing Diagram for 2:1 MUX Principle of Operation OCDS[00]

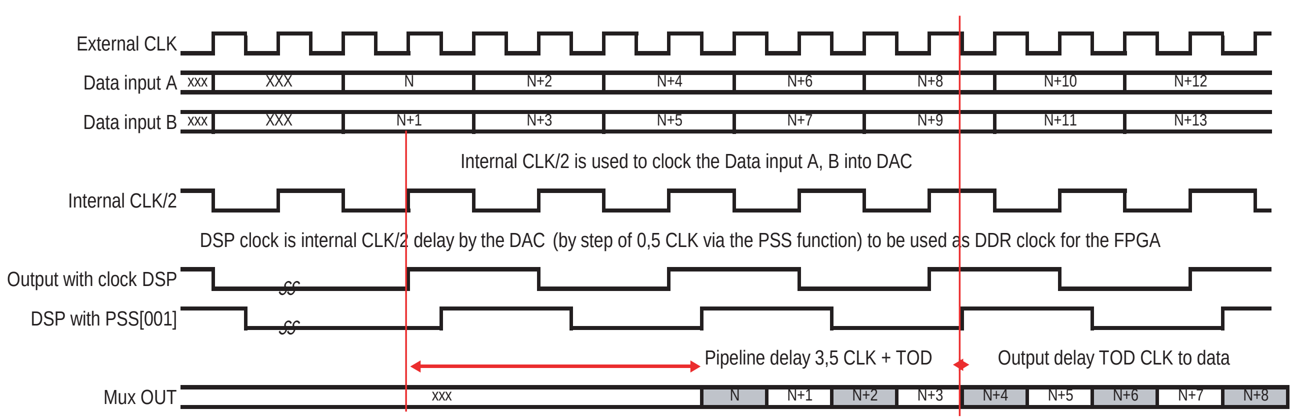
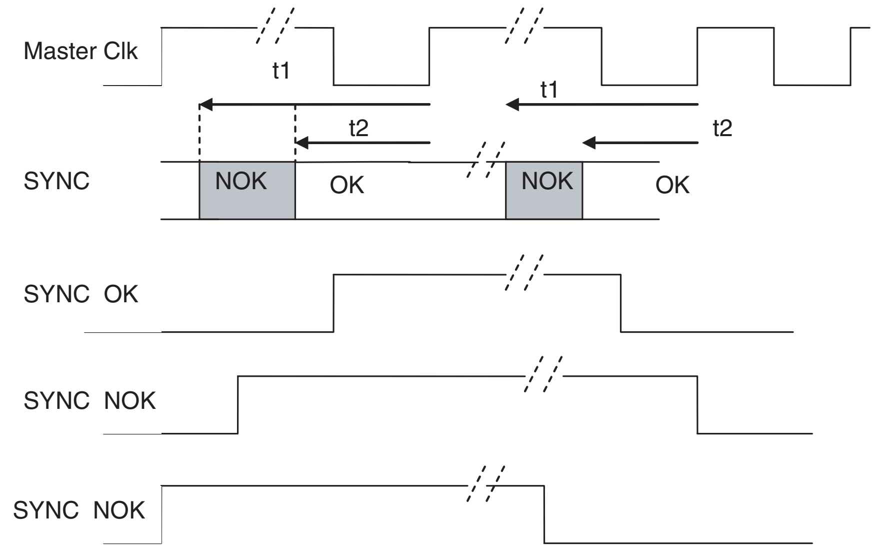


Figure 3-3. SYNC Timing Diagram



Please refer to Section 5.8 "Synchronization functions for multi-DAC operation" on page 25.

3.6 Explanation of Test Levels

1	100% production tested at +25°C[(1)]
2	100% production tested at +25°C[(1)], and sample tested at specified temperatures.
3	Sample tested only at specified temperatures
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter value is only guaranteed by design
6	100% production tested over specified temperature range (for Space/Mil grade[(2)])

Only MIN and MAX values are guaranteed.

Notes: 1. Unless otherwise specified.

2. If applicable, please refer to "Ordering Information"

3.7 Digital Input Coding Table

Table 3-9. Coding Table

Digital output msb..........lsb	Differential analog output
000000000000	–500 mV
010000000000	–250 mV
011000000000	–125 mV
100000000000	0 mV
101000000000	+125 mV
110000000000	+250 mV
111111111111	+500 mV

4. Definition of Terms

Abbreviation	Term	Definition
(Fs max)	*Maximum conversion Frequency*	Maximum conversion frequency
(Fs min)	*Minimum conversion frequency*	Minimum conversion Frequency
(SFDR)	*Spurious free dynamic range*	Ratio expressed in dB of the RMS signal amplitude, set at 1dB below Full Scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dB (i.e., related to converter –1 dB Full Scale), or in dBc (i.e, related to input signal level).
(HSL)	*High Spur Level*	Power of highest spurious spectral component expressed in dBm.
(ENOB)	*Effective Number Of Bits*	ENOB is determinated from NPR measurement with the formula: $ENOB = (SNR_{[dB]} - 1.76) / 6.02$ Where LF “Loading factor” is the ratio between the Gaussian noise standard deviation versus amplitude full scale.
(SNR)	*Signal to noise ratio*	SNR is determinated from NPR measurement with the formula: $SNR_{[dB]} = NPR_{[dB]} + \lvert LF_{[dB]} \rvert - 3$ Where LF “Loading factor” is the ratio between the Gaussian noise standard deviation versus amplitude full scale.
(DNL)	*Differential non linearity*	The Differential Non Linearity for an given code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing point and that the transfer function is monotonic.
(INL)	*Integral non linearity*	The Integral Non Linearity for a given code i is the difference between the measured voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
(TOD)	*Output delay*	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next differential analog output voltage change with specified load.
(NPR)	*Noise Power Ratio*	The NPR is measured to characterize the DAC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise pattern as the input to the DAC under test, the Noise Power Ratio is defined as the ratio of the average noise measured on the shoulder of the notch and inside the notch on the same integration bandwidth.
(VSWR)	*Voltage Standing Wave Ratio*	The VSWR corresponds to the insertion loss linked to power reflection. For example a VSWR of 1:2 corresponds to a 20dB return loss (ie. 99% power transmitted and 1% reflected).
(PSS)	*Phase Shift Select*	The Phase Shift Select function allow to tune the phase of the DSPclock.
(OCDS)	*Output Clock Division Select*	It allows to divide the DSPclock frequency by the OCDS coded value factor
(NRZ)	*Non Return to Zero mode*	Non Return to Zero mode on analog output
(RF)	*Radio Frequency mode*	RF mode on analog output
(RTZ)	*Non return to zero*	Return to zero mode
(NRTZ)	*Narrow Non return to zero*	Narrow return to zero mode

5. Functional Description

Figure 5-1. DAC Functional Diagram

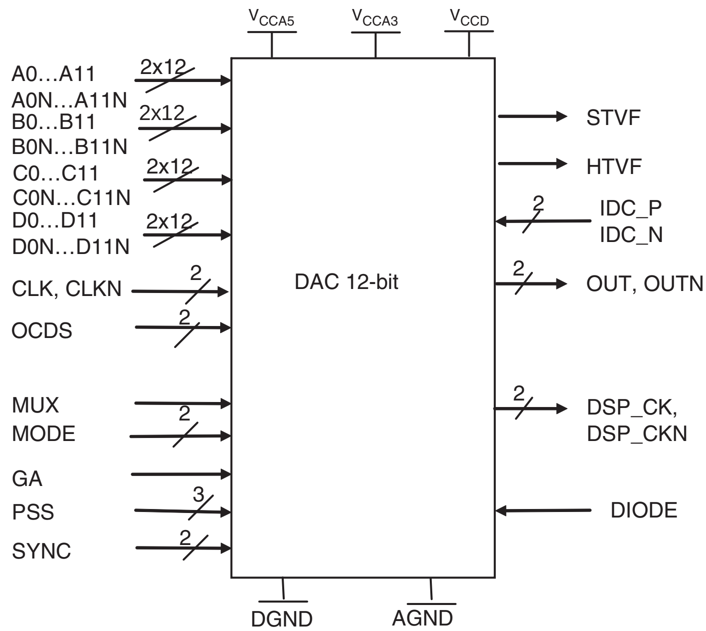


Table 5-1. Functions Description

Name	Function	Name	Function
V_{CCD}	3.3V Digital Power Supply	CLK	In-phase Master clock
V_{CCA5}	5.0V Analog Power Supply	CLKN	Inverted phase Master clock
V_{CCA3}	3.3V Analog Power Supply	DSP_CK	In-phase Output clock
DGND	Digital Ground	DSP_CKN	Inverted phase Output clock
AGND	Analog ground (for analog supply reference)	PSS[0..2]	Phase shift select
A[11…0]	In-phase digital input Port A	GA	Gain Adjust
A[11..0]N	Inverted phase digital input Port A	MUX	MUX Selection
B[11…0]	In-phase digital input Port B	MODE[0..1]	DAC Mode: NRZ, RTZ, NRTZ, RF
B[11..0]N	Inverted phase digital input Port B	STVF	Setup time Violation flag
C[11…0]	In-phase digital input Port C	HTVF	Hold time Violation flag
C[11..0]N	Inverted phase digital input Port C	IDC_P, IDC_N	Input data check
D[11…0]	In-phase digital input Port D	OCDS[0..1]	Output Clock Division factor Selection (by 4 or 8)
D[11..0]N	Inverted phase digital input Port D	Diode	Diode for temperature monitoring
OUT	In-phase analog output	SYNC/SYNCN	Synchronization signal (Active High)
OUTN	Inverted phase analog output		

5.1 Multiplexer

Two multiplexer ratio are allowed:

- 4:1 which allows operation at full sampling rate (ie. 3 GHz)
- 2:1 which can only be used up to 1.5 GHz sampling rate

Label	Value	Description
MUX	0	4:1 mode
	1	2:1 mode

In 2:1 MUX ratio, the unused data ports (ports C and D) can be left open.

5.2 MODE Function

Label	Value	Description	Default Setting (Not Connected)
MODE[1:0]	00	NRZ mode	11 RF mode
	01	Narrow RTZ (a.k.a. NRTZ) mode	
	10	RTZ Mode (50%)	
	11	RF mode	

The MODE function allows choosing between NRZ, NRTZ, RTZ and RF functions. NRZ and narrow RTZ should be chosen for use in 1st Nyquist zone while RTZ should be chosen for use in 2nd and RF for 3rd Nyquist zones.

Theory of operation: see following subsections for time domain waveform of the different modes.

Ideal equations describing max available Pout for frequency domain in the four modes are given hereafter, with X = normalised output frequency (that is Fout/Fclock, edges of Nyquist zones are then at X = 0 1/2 1 3/2 2 …).

Due to limited bandwidth, an extra term must be added to take in account a first order low pass filter.

- NRZ mode: $Pout(X) = 20*\log_{10}(k*sinc(k*\pi*X)|/0.893)$
  where sinc(x) = sin(x)/x, and k = 1
- NRTZ mode: $Pout(X) = 20*\log_{10}(k*sinc(k*\pi*X)|/0.893)$
  where k = (Tclock-Tτ)/Tclock and Tτ is width of reshaping pulse, Tτ is about 75ps.
- RTZ mode: $Pout(X)= 20*\log_{10}(k*sinc(k*\pi*X)|/0.893)$
  where k is the duty cycle of the clock presented at the DAC input, please note that due to phase mismatch in balun used to convert single ended clock to differential clock the first zero may move around the limit of the 4th and the 5th Nyquist zones. Ideally k = 1/2.
- RF mode: $Pout(x) = 20*\log_{10}(k*|sinc(k*\pi*X/2)*\sin(k*\pi*X/2)|/0.893)$
  where k is as per in NRTZ mode.

As a consequence:

- NRZ mode offers max power for 1st Nyquist operation
- RTZ mode offers slow roll off for 2nd Nyquist or 3rd Nyquist operation
- RF mode offers maximum power over 2nd and 3rd Nyquist operation
- NRTZ mode offers optimum power over full 1st and first half of 2nd Nyquist zones. This is the most relevant in term of performance for operation over 1st and beginning of 2nd Nyquist zone, depending on the sampling rate the zero of transmission moves in the 3rd Nyquist zone from begin to end when sampling rate increases.

Note in the two following figures: Pink line is ideal equation’s result, and green line includes a first order 6 GHz cut-off low pass filter to take in account finite bandwidth effect due to die and package.

Figure 5-2. Max Available Pout[dBm] at Nominal Gain vs Fout[GHz] in the Four Output Modes at 3 GSps, over four Nyquist Zones, Computed for $T\tau$ = 75 ps.

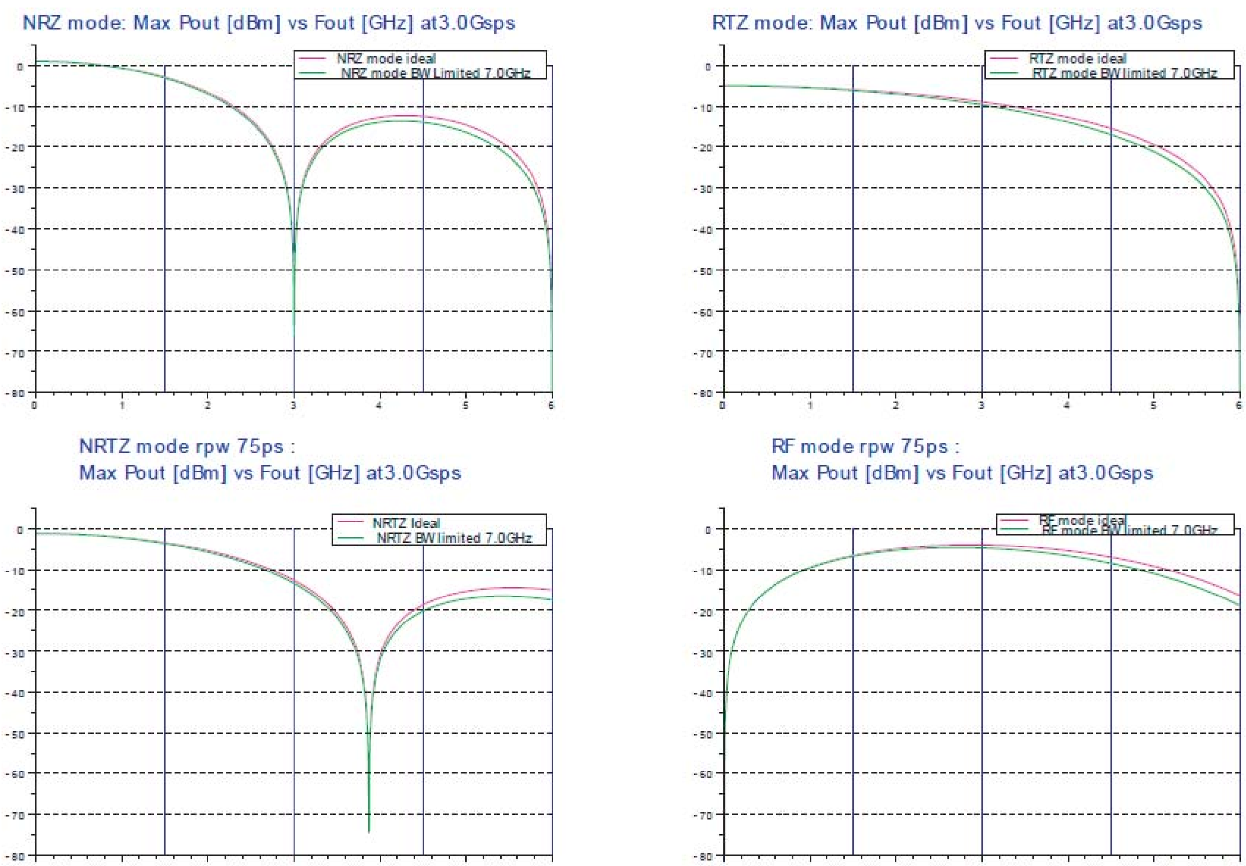
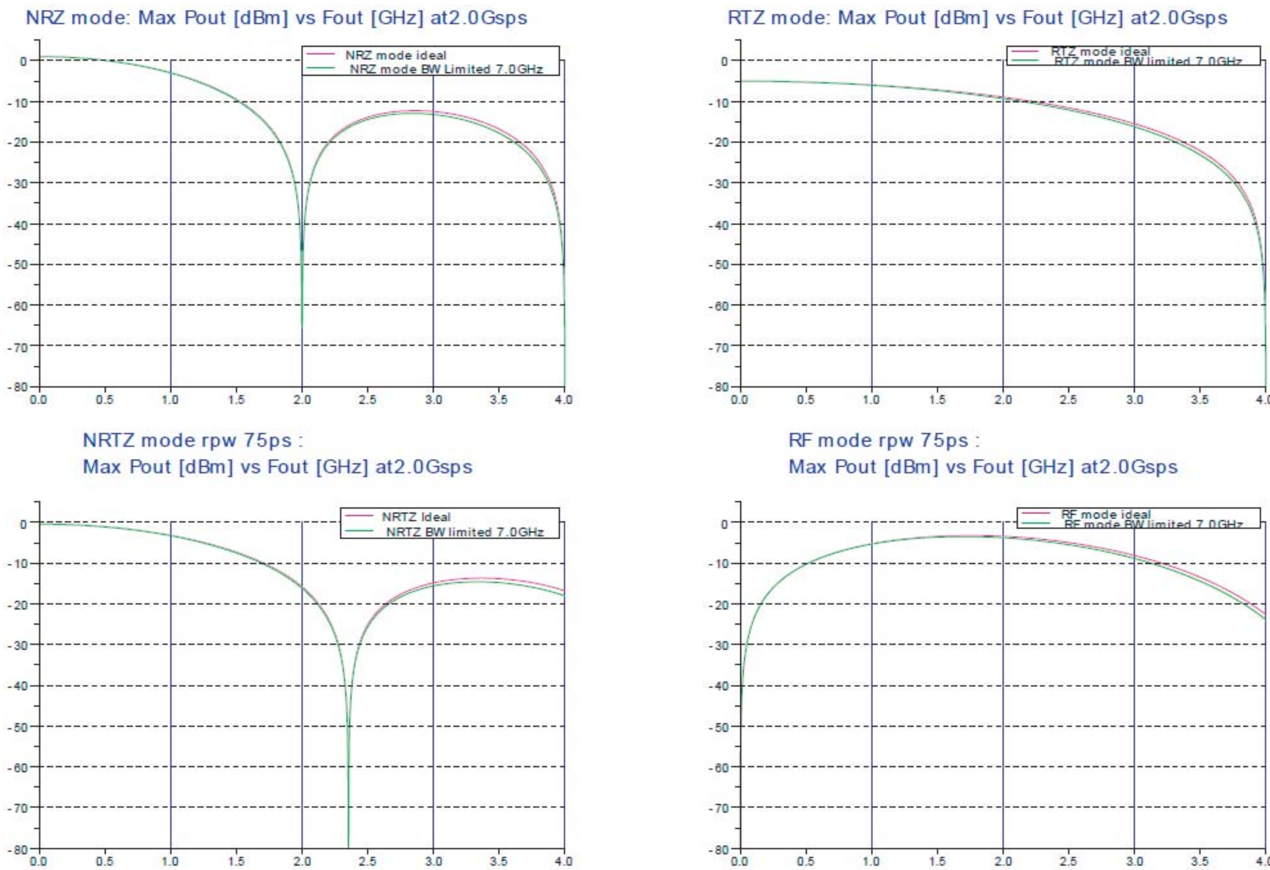


Figure 5-3. Max available Pout[dBm] at Nominal Gain vs Fout[GHz] in the Four Output Modes at 2 GSps, over four Nyquist Zones, Computed for Tτ = 75 ps

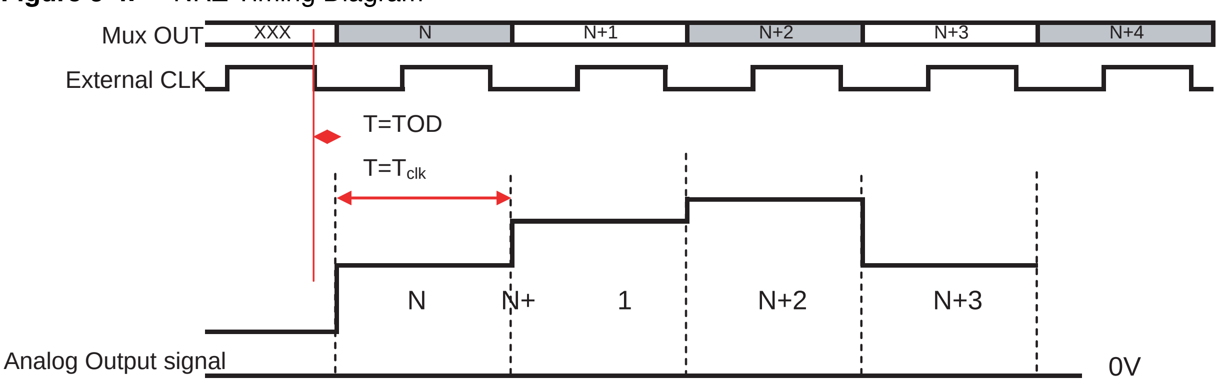


5.2.1 NRZ Output Mode

This mode does not allow for operation in the 2nd Nyquist zone because of the Sinx/x notch.

The advantage is that it gives good results at the beginning of the 1st Nyquist zone (less attenuation than in RTZ architecture), it removes the parasitic spur at the clock frequency (in differential).

Figure 5-4. NRZ Timing Diagram

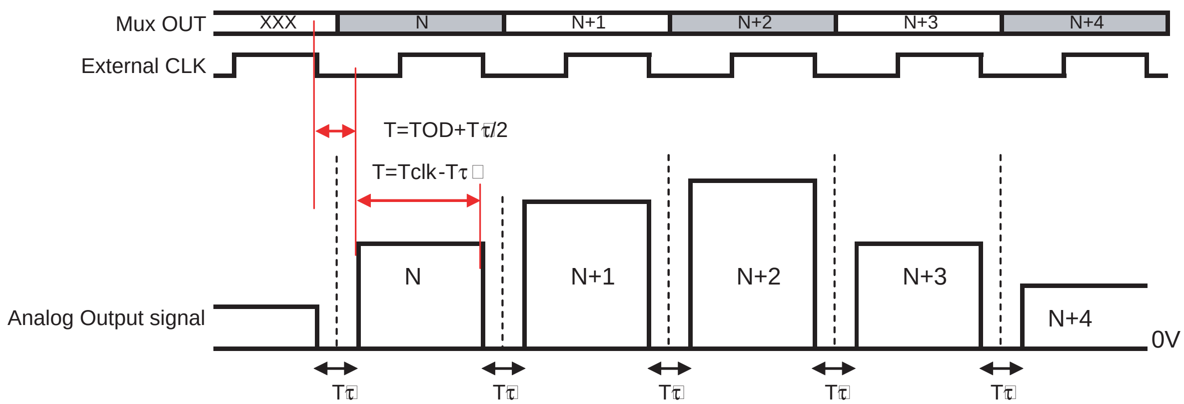


5.2.2 Narrow RTZ Mode

This mode has the following advantages:

- Optimized power in 1st Nyquist zone
- Extended dynamic through elimination of noise on transition edges
- Improved spectral purity (see Section 7.2.3 on page 44)
- Trade off between NRZ and RTZ

Figure 5-5. Narrow RTZ Timing Diagram



Note: Tτ is independant of Fclock.

5.2.3 RTZ Mode

The advantage of the RTZ mode is to enable the operation in the 2nd zone but the drawback is clearly to attenuate more the signal in the first Nyquist zone.

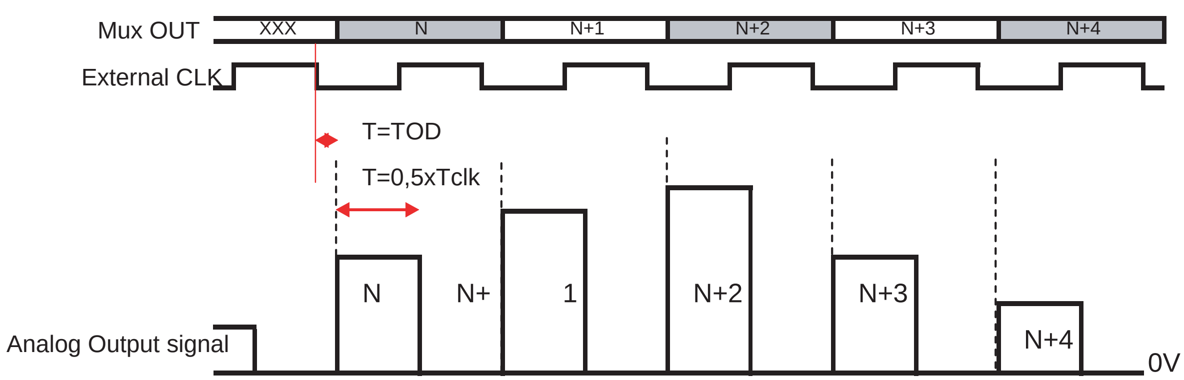
Advantages:

- Extended roll off of sinc
- Extended dynamic through elimination of hazardous transitions

Weakness:

- By construction clock spur at Fs.

Figure 5-6. RTZ Timing Diagram



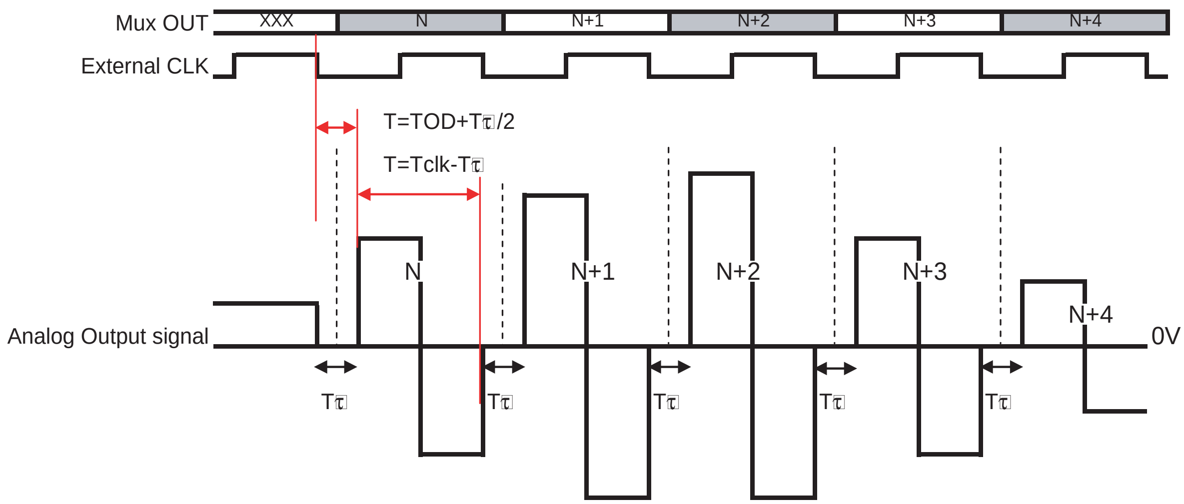
5.2.4 RF Mode

RF mode is optimal for operation at high input frequency, since the decay with frequency occurs at higher frequency than for RTZ. Unlike NRZ or RTZ modes, RF modes presents notch DC and 2N*Fs, and minimum attenuation for Fout = Fs.

Advantages:

- Optimized for 2nd and 3rd Nyquist operation
- Extended dynamic range through elimination of hazardous transitions.
- Clock spur pushed to 2.Fs

Figure 5-7. RF Timing Diagram



Note: The central transition is not hazardous but its elimination allows to push clock spur to 2.Fs
Tτ is independant of Fclock.

5.3 PSS (Phase Shift Select Function)

It is possible to adjust the timings between the sampling clock and the DSP output clock (which frequency is given by the following formula: Sampling clock / 2NX where N is the MUX ratio, X the output clock division factor).

The DSP clock output phase can be tuned over a range of 3.5 input clock cycles (7 steps of half a clock cycle) in addition to the intrinsic propagation delay between the DSP clock (DSP, DSPN) and the sampling clock (CLK, CLKN).

Three bits are provided for the phase shift function: PSS[2:0].

By setting these 3 bits to 0 or 1, one can add a delay on the DSP clock in order to properly synchronize the input data of the DAC and the sampling clock (the DSP clock should be applied to the FPGA and should be used to clock the DAC digital input data).

Table 5-2. PSS Coding Table

Label	Value	Description
PSS[2:0]	000	No additional delay on DSP clock
	001	0.5 input clock cycle delay on DSP clock
	010	1 input clock cycle delay on DSP clock
	011	1.5 input clock cycle delay on DSP clock
	100	2 input clock cycle delay on DSP clock
	101	2.5 input clock cycle delay on DSP clock
	110	3 input clock cycle delay on DSP clock
	111	3.5 input clock cycle delay on DSP clock

In order to determine how much delay needs to be added on the DSP clock to ensure the synchronization between the input data and the sampling clock within the DAC, the HTVF and STVF bits should be monitored. Refer to Section 5.5 on page 23.

Note: In MUX 4:1 mode the 8 settings are relevant, in MUX 2:1 only the four first settings are relevant since the four last setting will yield exactly the same results.

Figure 5-8. PSS Timing Diagram for 4:1 MUX, OCDS[00]

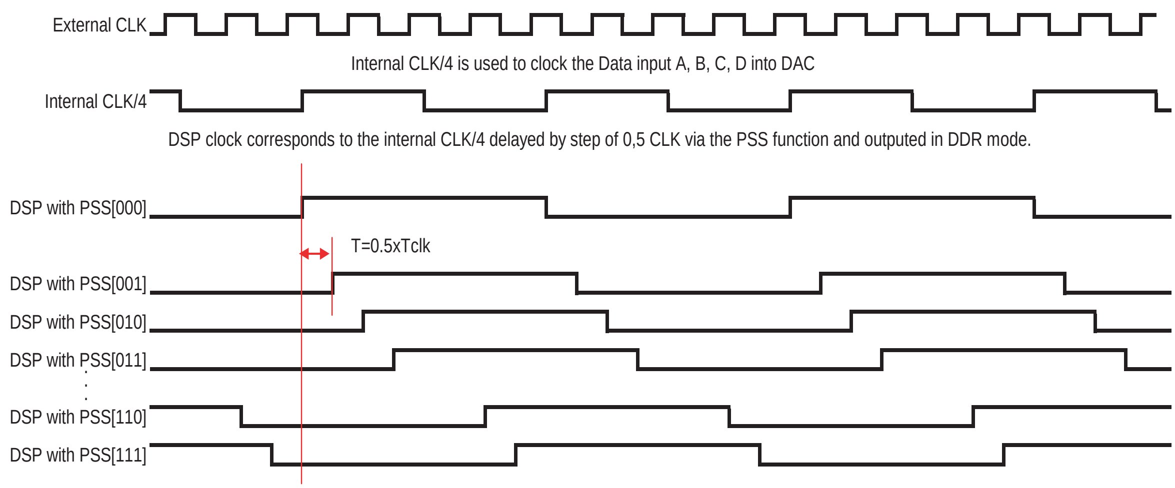
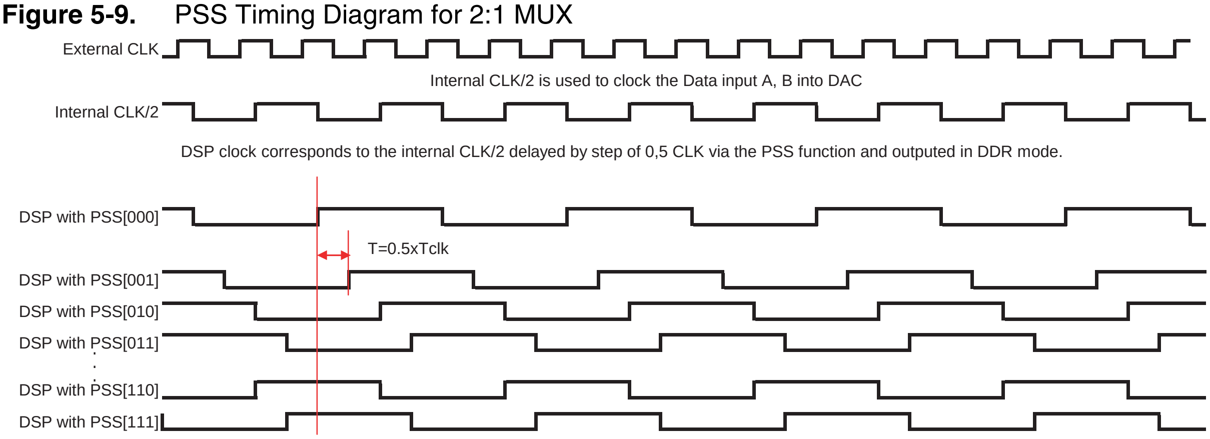


Figure 5-9. PSS Timing Diagram for 2:1 MUX



5.4 Output Clock Division Select Function OCDS[1:0]

It is possible to change the DSP clock internal division factor from 1 to 2 and 4 with respect to the sampling clock/2N where N is the MUX ratio. This is possible via the OCDS "Output Clock Division Select" bits.

OCDS is used to obtain a synchronisation clock for the FPGA slow enough to allow the FPGA to operate with no further internal division of this clock, thus its internal phase is determined by the DSP clock phase. This is useful in a system with multiple DACs and multiple FPGAs to guarantee deterministic phase relationship between the FPGAs after a synchronisation of all the DACs.

Table 5-3. OCDS[1:0] Coding Table

Label	Value	Description
OCDS [1:0]	00	DSP clock frequency is equal to the sampling clock divided by 2N
	01	DSP clock frequency is equal to the sampling clock divided by 2N*2
	10	DSP clock frequency is equal to the sampling clock divided by 2N*4 not recommended for production, before use please contact hotline-bdc@e2v.com
	11	Not allowed

Figure 5-10. OCDS Timing Diagram for 4:1 MUX

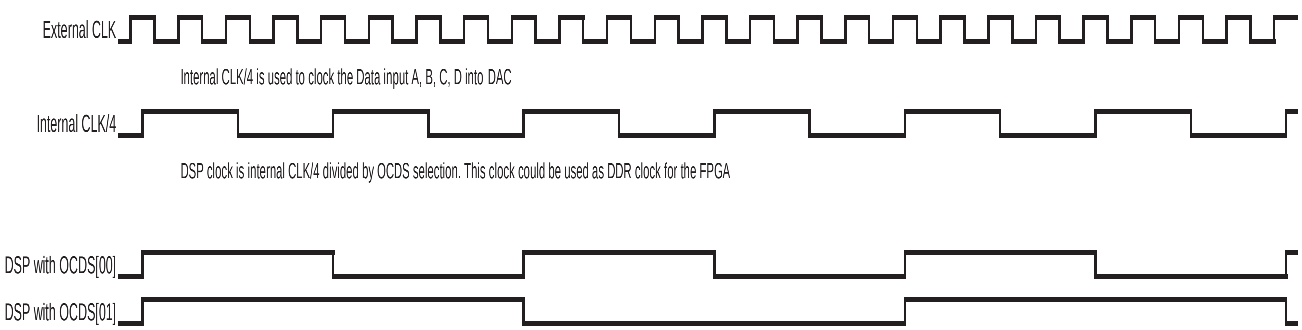
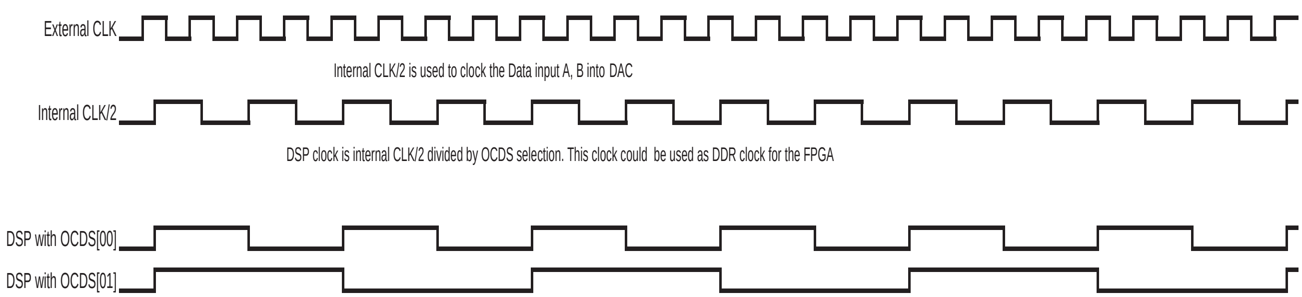


Figure 5-11. OCDS Timing Diagram for 2:1 MUX



5.5 Synchronization FPGA-DAC: IDC_P, IDC_N, HTVF and STVF Functions

IDC_P, IDC_N: Input Data check function (LVDS signal).

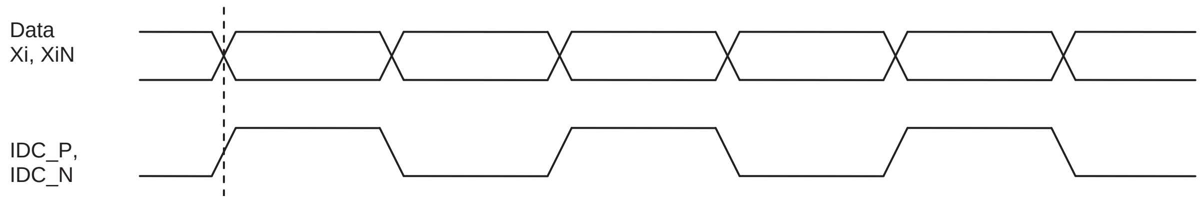
HTVF: Hold Time Violation Flag. (cmos3.3V signal)

STVF: Setup Time Violation Flag. (cmos3.3V signal)

This signal is toggling at each cycle synchronously with other data bits. This signal should be considered as DAC input data that is toggling at each cycle.

This signal should be generated by the FPGA in order the DAC to check in real-time if the timings between the FPGA and the DAC are correct.

Figure 5-12. IDC Timing vs Data Input



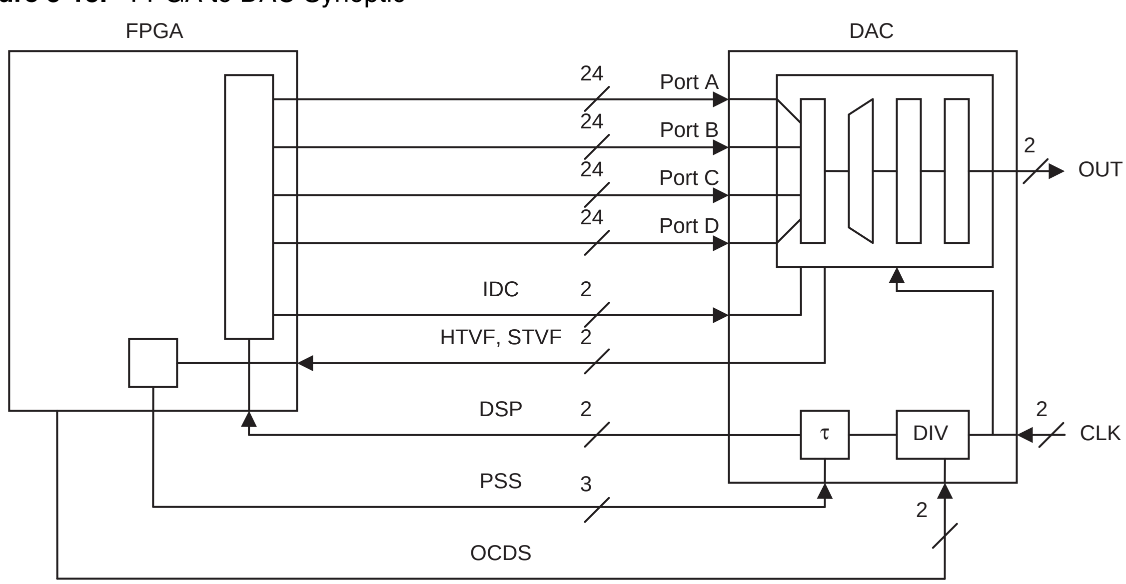
The information on the timings is then given by HTVF, STVF signals (flags).

Table 5-4. HTVF, STVF Coding Table

Label	Value	Description
HTVF	0	SYNCHRO OK
	1	Data Hold time violation detected
STVF	0	SYNCHRO OK
	1	Data Setup time violation detected

During Monitoring STVF indicates setup time of data violation (Low -> OK, High -> Violation), HTVF indicates hold time of data violation (Low -> OK, High -> Violation).

Figure 5-13. FPGA to DAC Synoptic



Principle of Operation:

The Input Data Check pair (IDC_P, IDC_N) will be sampled three times with half a master clock period shift (the second sample being synchronous with all the data sampling instant), these three samples will be compared, and depending on the results of the comparison a violation may be signalled.

- Violation of setup time -> STVF is high level
- Violation of hold time -> HTVF is high level

In case of violation of timing (setup or hold) the user has two solutions:

- Shift phase in the FPGA PLL (if this functionality is available in FPGA) for changing the internal timing of DATA and Data Check signal inside FPGA.
- Shift the DSP clock timing (Output clock of the DAC which can be used for FPGA synchronization – refer to Section 5.3 on page 20), in this case this shift also shift the internal timing of FPGA clock.

Note: When used, it should be routed as the data signals (same layout rules and same length). if not used, it should be driven to an LVDS low or high level.

For further details, refer to application note AN1087.

5.6 DSP Output Clock

The DSP output clock DSP, DSPN is an LVDS signal which is used to synchronize the FPGA generating the digital patterns with the DAC sampling clock.

The DSP clock frequency is a fraction of the sampling clock frequency. The division factor depends on OCDS settings. The DSP clock frequency is equal to (sampling frequency / [2N*X]) where N is the MUX ratio and X is the output clock division factor, determined by OCDS[0..1] bits.

For example, in a 4:1 MUX ratio application with a sampling clock of 3 GHz and OCDS set to “00” (ie. Factor of 1), the input data rate is 750 MSps and the DSP clock frequency is 375 MHz.

This DSP clock is used in the FPGA to control the digital data sequencing. Its phase can be adjusted using the PSS[2:0] bits (refer to Section 5.3 on page 20) in order to ensure a proper synchronization between the data coming to the DAC and the sampling clock.

The HTVF and STVF bits should be used to check whether the timing between the FPGA and the DAC is correct. HTVF and STVF bits will indicate whether the DAC and FPGA are aligned or not. PSS bits should then be used to shift the DSP clock and thus the input data of the DAC, so that a correct timing is achieved between the FPGA and the DAC.

5.7 OCDS, MUX Combinations Summary

Table 5-5. OCDS, MUX, PSS Combinations Summary

MUX		OCDS		PSS Range	Data Rate	Comments
0	4:1	00	DSP clock division factor 8	0 to 7/(2Fs) by 1/(2Fs) steps	Fs/4	Refer to Section 5.4
0		01	DSP clock division factor 16			
0		10	Contact Hotline-BDC			
0		11	Not allowed			
1	2:1	00	DSP clock division factor 4	0 to 7/(2Fs) by 1/(2Fs) steps	Fs/2	Refer to Section 5.4
1		01	DSP clock division factor 8			
1		10	Contact Hotline-BDC			
1		11	Not allowed			

Note: Behaviour according to MUX, OCDS and PSS combination is independent of output mode (MODE).

5.8 Synchronization functions for multi-DAC operation

When the output timing needs to be synchronised, a SYNC operation could be generated.

After the application of the SYNC signal the DSP clock from the DAC will stop for a period and after a constant and known time the DSP clock will start up again.

There are two SYNC functions integrated in this DAC:

- a power up reset, which is triggered by the power supplies if the dedicated power up sequence is applied Vccd => Vcca3 => Vcca5;
- External SYNC pulse applied on (SYNC, SYNCN).

The external SYNC is LVDS compatible (same buffer as for the digital input data). It is active high.

Depending on the settings for OCDS, PSS and also the MUX ratio the width of the SYNC pulse must be greater than a certain number of external clock pulses. It is also necessary that the sync pulse is synchronized with the system clock and is an integer number of clock pulses. See application note (ref 1087) for further details. See erratasheet (ref 1125) for SYNC condition of use.

Figure 5-14. Reset Timing Diagram (4:1 MUX)

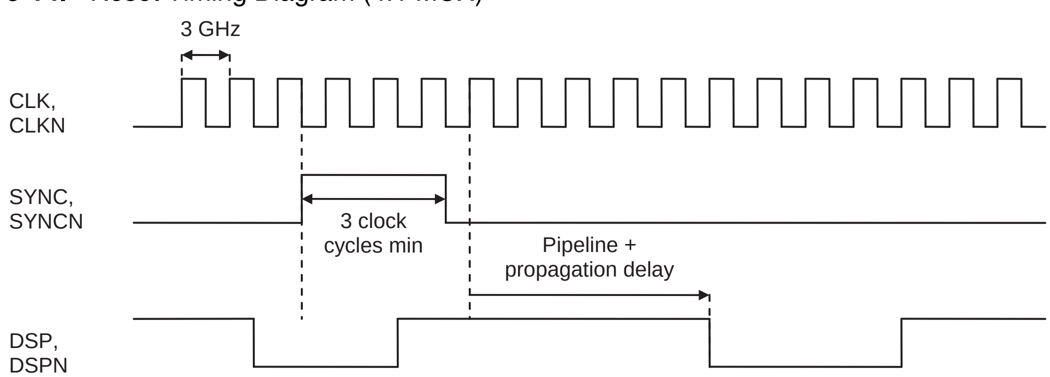
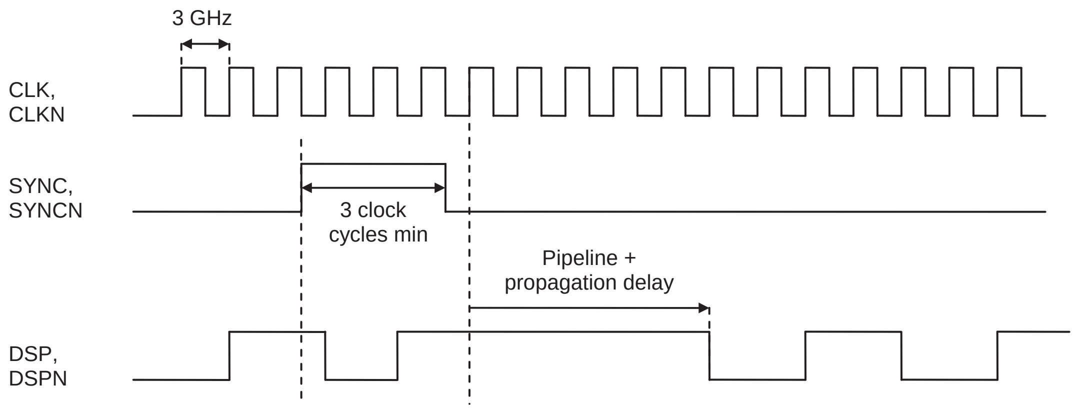


Figure 5-15. Reset Timing Diagram (2:1 MUX)



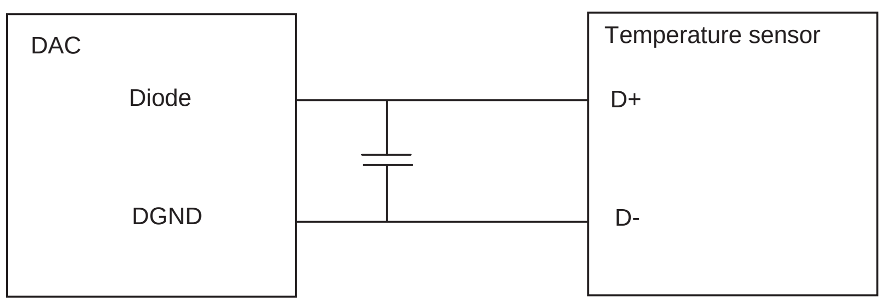
5.9 Gain Adjust GA Function

This function allows to adjust the internal gain of the DAC to cancel the initial gain deviation.
The gain of the DAC can be adjusted by ±11% by tuning the voltage applied on GA by varying GA potential from 0 to $V_{CCA3.}$
GA max is given for GA = 0 and GA min for GA = V_{CCA3}

5.10 Diode Function

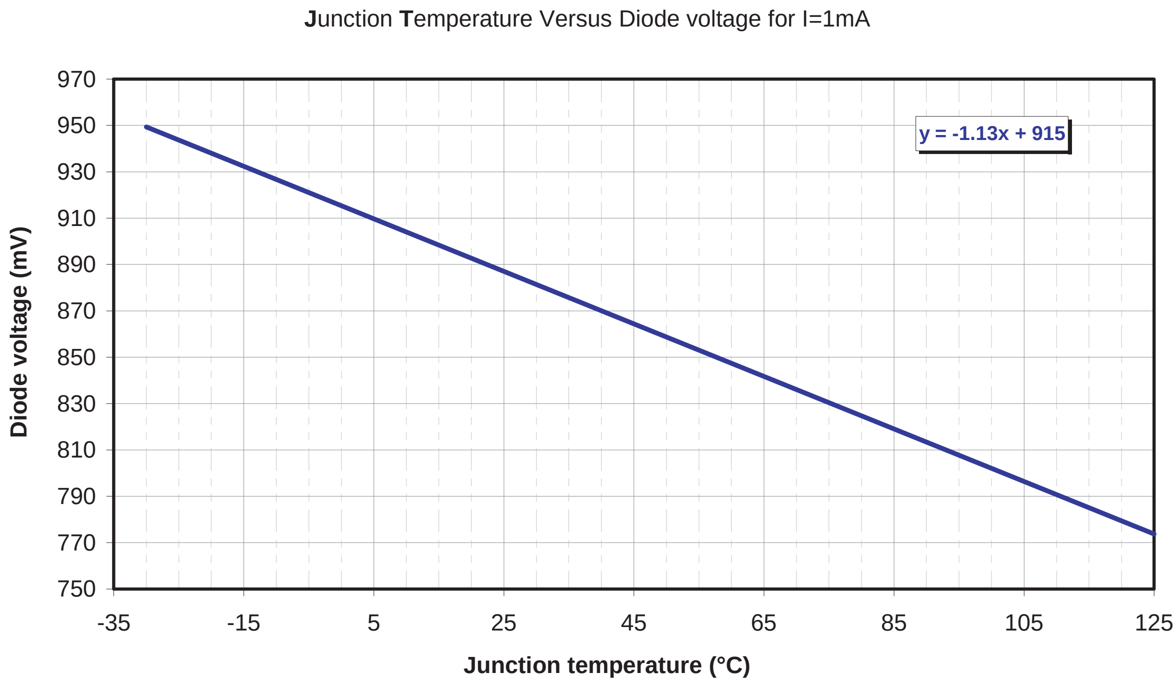
A diode is available to monitor the die junction temperature of the DAC.
For the measurement of die junction temperature, you could use a temperature sensor.

Figure 5-16. Temperature DIODE Implementation



In characterization measurement a current of 1 mA is applied on the DIODE pin. The voltage across the DIODE pin and the DGND pin gives the junction temperature using the intrinsic diode characteristics below Figure 5-17 on page 27.

Figure 5-17. Diode Characteristics for Die Junction Monitoring



6. PIN Description

Figure 6-1. Pinout View fpBGA196 (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DGND	B5	B6	B6N	B9	B9N	B11	C11	C9N	C9	C6N	C6	C5	DGND	A
B	B3	B4	B5N	B7	B8	B10	B11N	C11N	C10	C8	C7	C5N	C4	C3	B
C	B1N	B3N	B4N	B7N	B8N	B10N	DGND	DGND	C10N	C8N	C7N	C4N	C3N	C1N	C
D	B1	B2	B2N	DGND	DGND	VCCD	VCCD	VCCD	VCCD	DGND	DGND	C2N	C2	C1	D
E	A10N	B0	B0N	DGND	DGND	VCCD	VCCD	VCCD	VCCD	DGND	DGND	C0N	C0	D10N	E
F	A10	A11	A11N	VCCD	VCCD	AGND	AGND	AGND	AGND	VCCD	VCCD	D11N	D11	D10	F
G	A8	A8N	A9	A9N	DGND	AGND	AGND	AGND	AGND	DGND	D9N	D9	D8N	D8	G
H	A6	A6N	A7	A7N	DGND	AGND	AGND	AGND	AGND	DGND	D7N	D7	D6N	D6	H
J	A3N	A5	A5N	VCCA3	VCCA3	AGND	AGND	AGND	AGND	VCCA3	VCCA3	D5N	D5	D3N	J
K	A3	A4	A4N	DGND	DGND	AGND	VCCA5	VCCA5	AGND	DGND	DGND	D4N	D4	D3	K
L	A1N	A2	A2N	DGND	Diode	VCCA5	VCCA5	VCCA5	VCCA5	DGND	MUX	D2N	D2	D1N	L
M	A1	A0N	GA	HTVF	STVF	VCCA5	VCCA5	AGND	AGND	MODE0	MODE1	PSS2	D0N	D1	M
N	A0	DSPN	IDC_P	SYNCN	CLKN	AGND	AGND	AGND	AGND	AGND	AGND	OCDS1	OCDS0	D0	N
P	DGND	DSP	IDC_N	SYNC	CLK	AGND	AGND	AGND	OUT	OUTN	AGND	PSS0	PSS1	DGND	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Table 6-1. Pinout Table fpBGA196

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
Power Supplies				
V_{CCA5}	K7, K8, L6, L7, L8, L9, M6, M7	5V analogue power supplies Referenced to AGND	N/A	
V_{CCA3}	J4, J5, J10, J11	3.3V analogue power supply Referenced to AGND	N/A	
V_{CCD}	D6, D7, D8, D9, E6, E7, E8, E9, F4, F5, F11	3.3V digital power supply Referenced to DGND	N/A	
AGND	F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9, K6, K9, M8, M9, N6, N7, N8, N9, N10, N11, P6, P7, P8, P11	Analogue Ground AGND plane should be separated from DGND on the board (the two planes can be connected by 0 ohm resistors)	N/A	

Table 6-1. Pinout Table fpBGA196 (Continued)

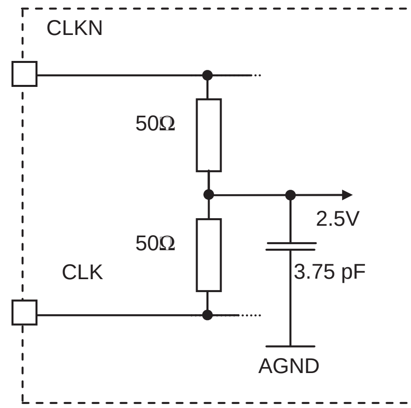
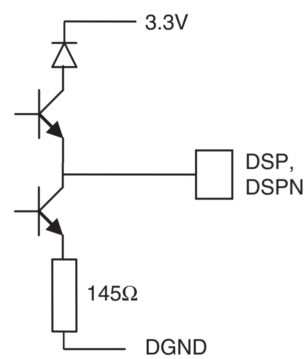
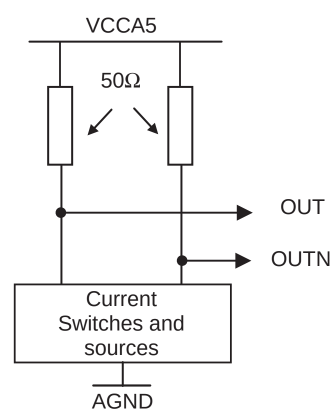
Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
DGND	A1, A14, C7, C8, D4, D5, D10, D11, E4, E5, E10, E11, G5, G10, H5, H10, K4, K5, K10, K11, L4, L10, P1, P14	Digital Ground AGND plane should be separated from DGND on the board (the two planes can be connected by 0 ohm resistors)	N/A	
Clock Signals				
CLK, CLKN	P5, N5	Master sampling clock input (differential) with internal common mode at 2.65V It should be driven in AC coupling. Equivalent internal differential 100Ω input resistor.	I	
DSP, DSPN	P2, N2	Output clock (in-phase and inverted phase	O	
Analog Output Signal				
OUT, OUTN	P9, P10	In phase and Inverted phase analogue output signal (differential termination required)	O	

Table 6-1. Pinout Table fpBGA196 (Continued)

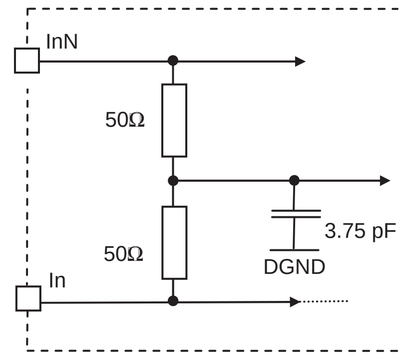
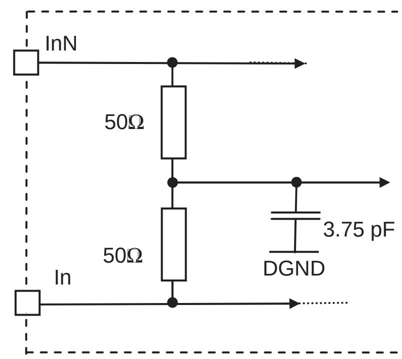
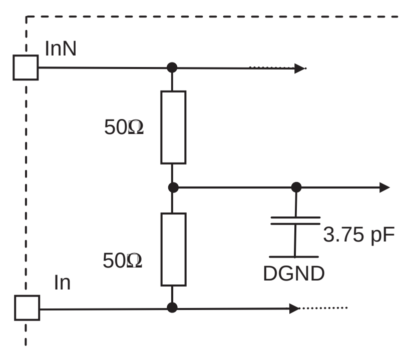
Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
Digital Input Signals				
A0, A0N A1, A1N A2, A2N A3, A3N A4, A4N A5, A5N A6, A6N A7, A7N A8, A8N A9, A9N A10, A10N A11, A11N	N1, M2 M1, L1 L2, L3 K1, J1 K2, K3 J2, J3 H1, H2 H3, H4 G1, G2 G3, G4 F1, E1 F2, F3	In-phase Digital input Port A Data A0, A0N is the LSB Data A11, A11N is the LSB	I	
B0, B0N B1, B1N B2, B2N B3, B3N B4, B4N B5, B5N B6, B6N B7, B7N B8, B8N B9, B9N B10, B10N B11, B11N	E2, E3 D1, C1 D2, D3 B1, C2 B2, C3 A2, B3 A3, A4 B4, C4 B5, C5 A5, A6 B6, C6 A7, B7	Inverted phase Digital input Port B Data B0, B0N is the LSB Data B11, B11N is the LSB	I	
C0, C0N C1, C1N C2, C2N C3, C3N C4, C4N C5, C5N C6, C6N C7, C7N C8, C8N C9, C9N C10, C10N C11, C11N	E13, E12 D14, C14 D13, D12 B14, C13 B13, C12 A13, B12 A12, A11 B11, C11 B10, C10 A10, A9 B9, C9 A8, B8	In-phase Digital input Port B Data 1	I	

Table 6-1. Pinout Table fpBGA196 (Continued)

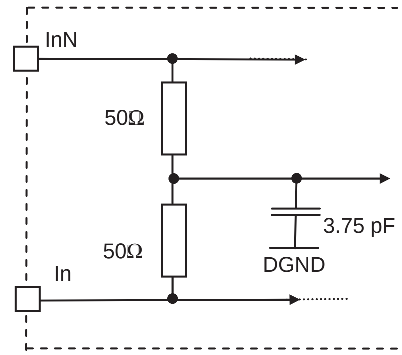
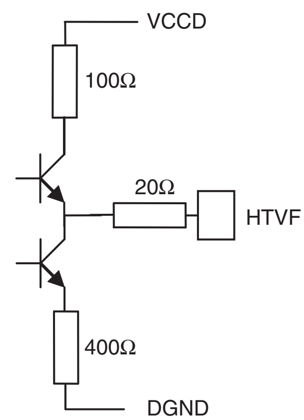
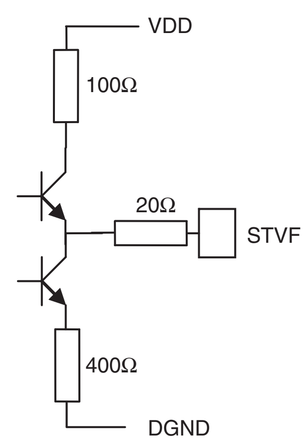
Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
D0, D0N D1, D1N D2, D2N D3, D3N D4, D4N D5, D5N D6, D6N D7, D7N D8, D8N D9, D9N D10, D10N D11, D11N	N14, M13 M14, L14 L13, L12 K14, J14 K13, K12 J13, J12 H14, H13 H12, H11 G14, G13 G12, G11 F14, E14 F13, F12	Inverted phase Digital input Port B Data 1	I	
Control Signals				
HTVF	M4	Setup time violation flag	O	
STVF	M5	Hold time violation flag	O	

Table 6-1. Pinout Table fpBGA196 (Continued)

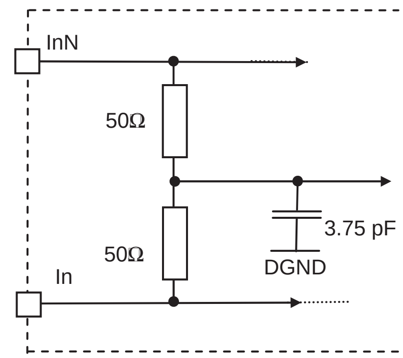
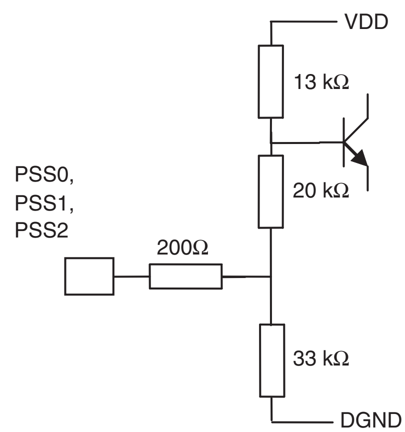
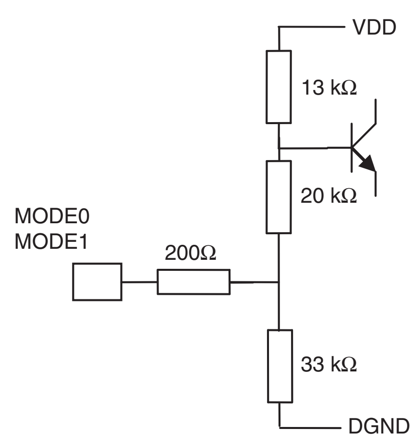
Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
IDC_P, IDC_N	N3, P3	Input data check	I	
PSS0 PSS1 PSS2	P12 P13 M12	Phase Shift Select (PSS2 is the MSB)	I	
MODE0 MODE1	M10 M11	DAC Mode selection bits	I	

Table 6-1. Pinout Table fpBGA196 (Continued)

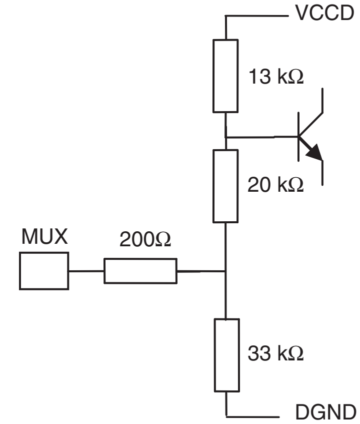
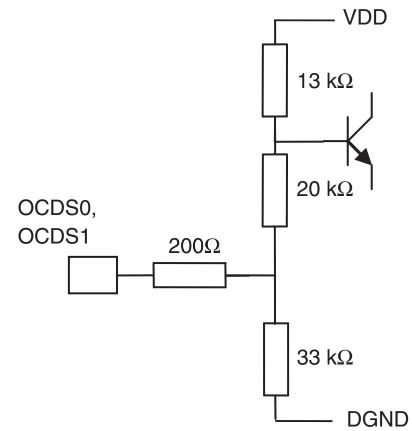
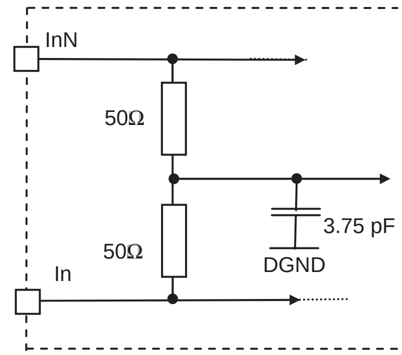
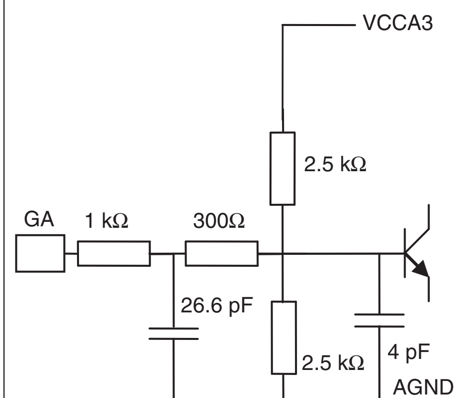
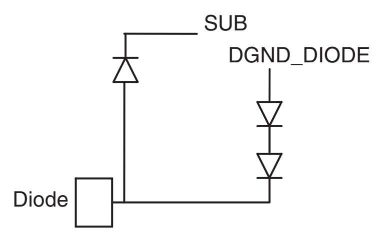
Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
MUX	L11	MUX selection	I	
OCDS0 OCDS1	N13 N12	Output Clock Division Select = these bits allow to select the clock division factor applied on the DSP, DSPN signal.	I	

Table 6-1. Pinout Table fpBGA196 (Continued)

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
SYNC, SYNCN	P4, N4	In phase and Inverted phase reset signal	I	
GA	M3	Gain adjust	I	
Diode	L5	Diode for die junction temperature monitoring	I	

7. Characterization Results

Unless otherwise specified results are given at room temperature (Tj ~ 60°C), nominal power supply, in 4:1 MUX mode, gain at nominal setting.

7.1 Static Performances

7.1.1 DC Gain Characterization

Figure 7-1. DAC DC Gain vs Gain Adjust (Measured in NRZ Mode)

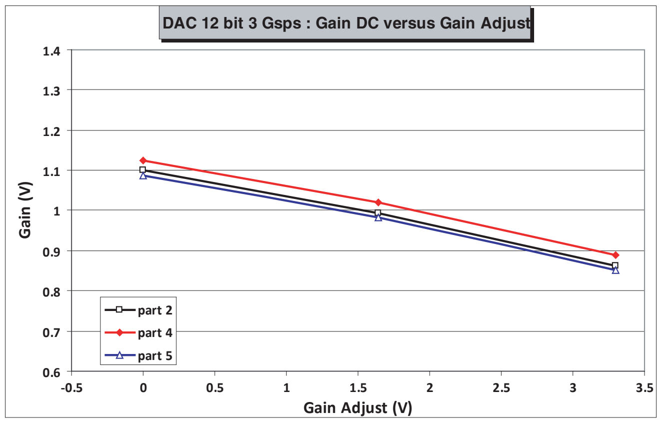


Figure 7-2. DAC DC Gain Drift from Unity Gain vs Temperature (Measured in NRZ Mode)

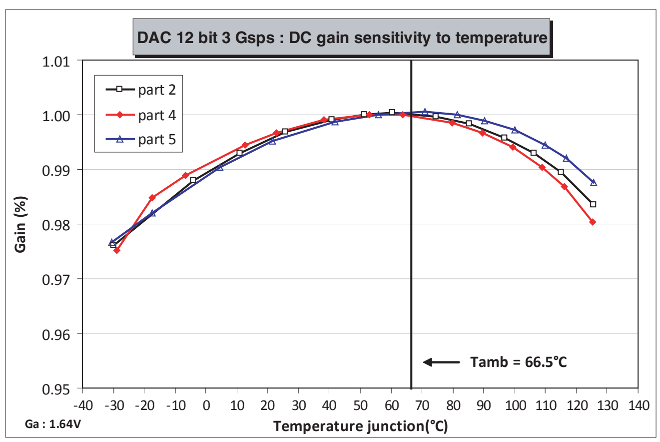
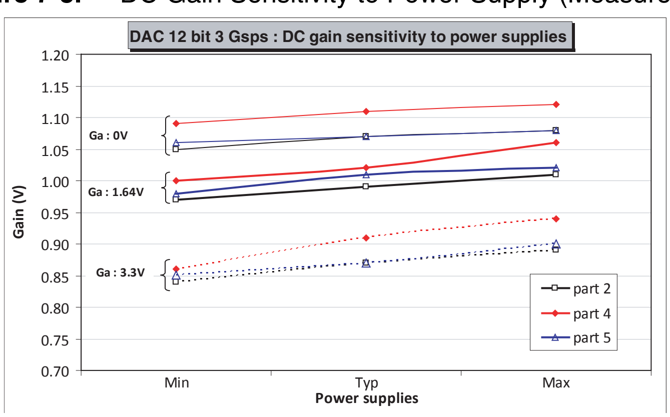


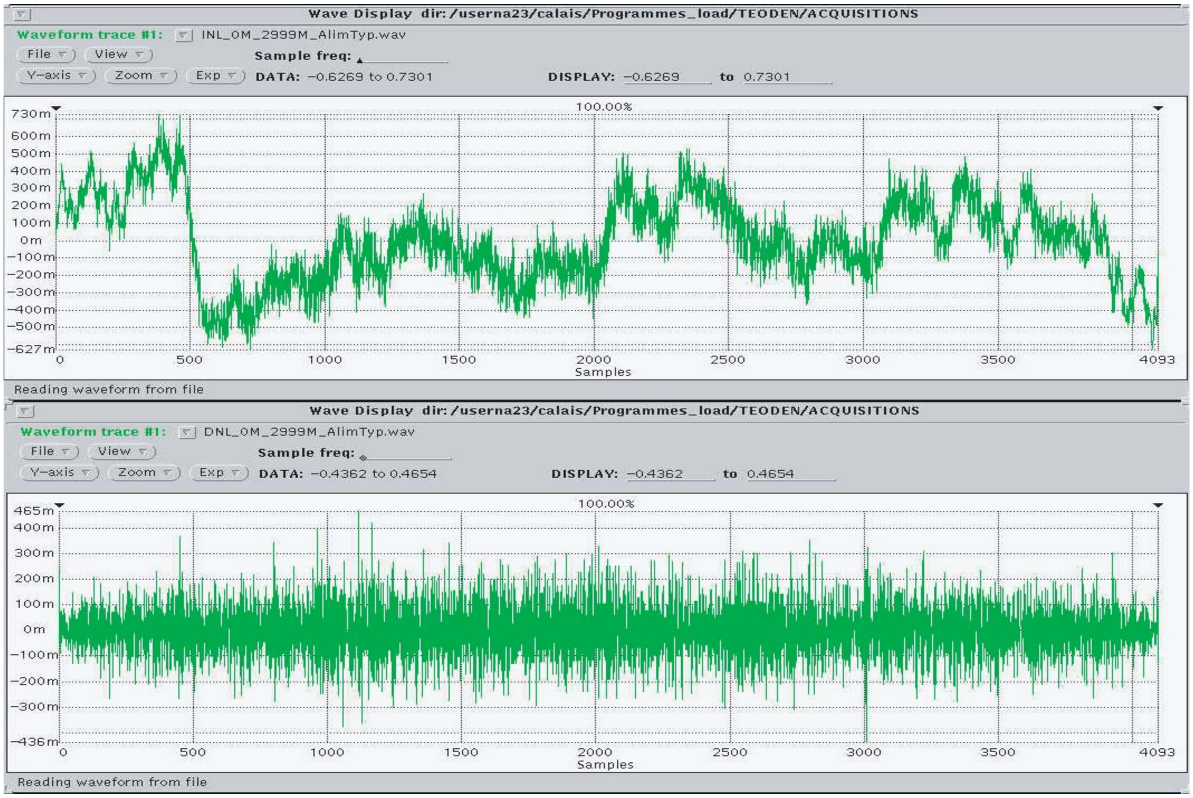
Figure 7-3. DC Gain Sensitivity to Power Supply (Measured in NRZ Output Mode)



Conditions: room temperature, supply levels:
- Min: V_{CCA}: 4.75V // V_{CCA3} = V_{CCD} = 3.15V
- Typ: V_{CCA}: 5V // V_{CCA3} = V_{CCD} = 3.3V
- Max: V_{CCA}: 5.25V // V_{CCA3} = V_{CCD} = 3.45V

7.1.2 Static Linearity

Figure 7-4. INL/DNL Measurement at Fout = 100 kHz and 3 GSps



INL reflects at true 12 bit DAC.

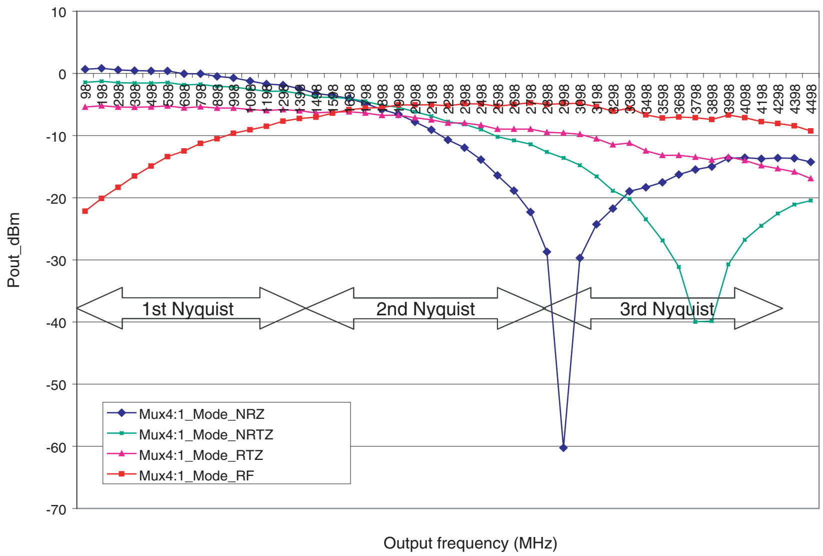
Low DNL values reflect a strictly monotonous 12 bit DAC.

7.2 AC Performances

7.2.1 Available Output Power vs Fout.

The following plots summarize characterization results, for a Fout sweep from 98 MHz to 4498 MHz (step 100 MHz).

Figure 7-5. Available Pout vs Fout from 98 MHz to 4498 MHz in the 4 Output Modes at 3 GSps



NRZ mode offers max power for 1st Nyquist operation.

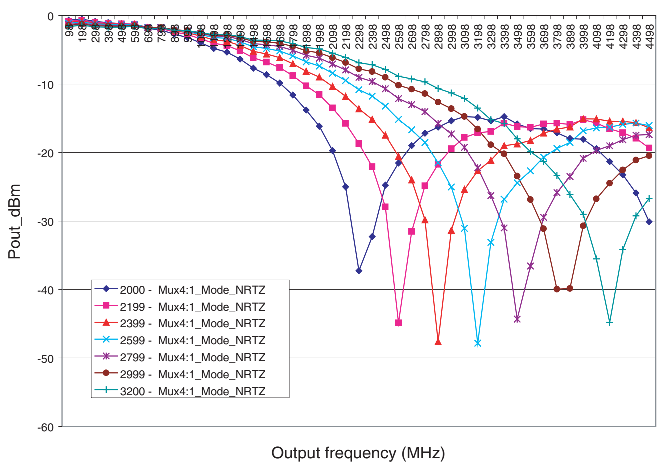
RTZ mode offer slow roll off for 2nd Nyquist operation.

RF mode offers maximum power over 2nd and 3rd Nyquits operation.

NRTZ mode offers optimum power over full 1st and first half of 2nd Nyquist zones.

This is the most relevant in term of performance for operation over 1st and beginning of 2nd Nyquist zone.

Figure 7-6. Available Pout vs Fout from 98 MHz to 4498 MHz and from 2 GSps to 3.2 GSps in NRZ Mode



First notch at F=1/((1/Fclock) - 75ps), second notch at 2xF

Figure 7-7. Available Pout vs Fout from 98 MHz to 4498 MHz and from 2 GSps to 3.2 GSps in NRTZ Mode

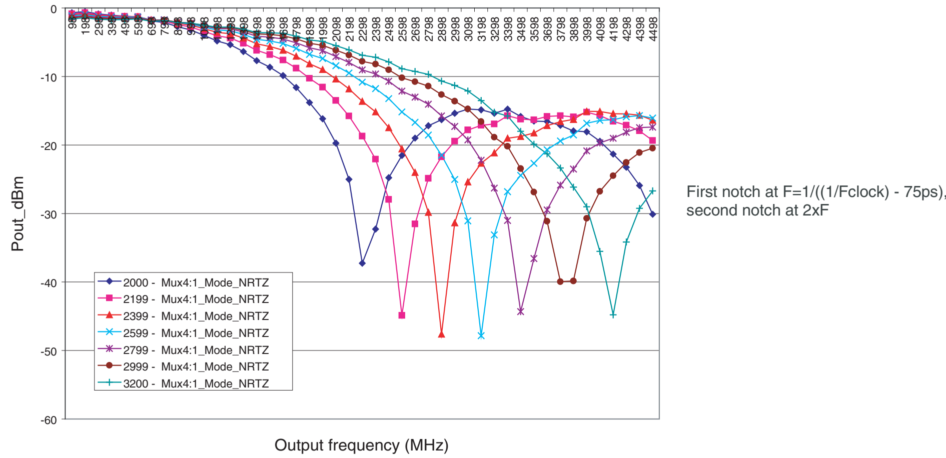


Figure 7-8. Available Pout vs Fout from 98 MHz to 4498 MHz and from 2 GSps to 3.2 GSps in RTZ Mode

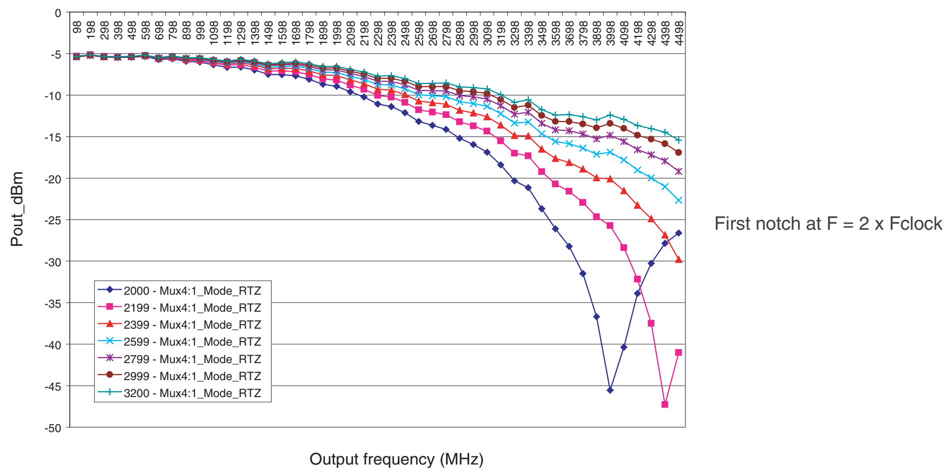
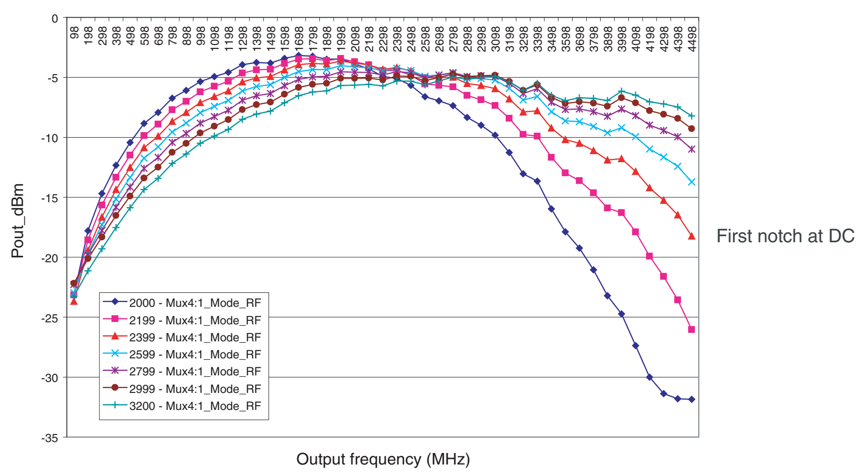


Figure 7-9. Available Pout vs Fout from 98 MHz to 4498 MHz and from 2 GSps to 3.2 GSps in RF Mode

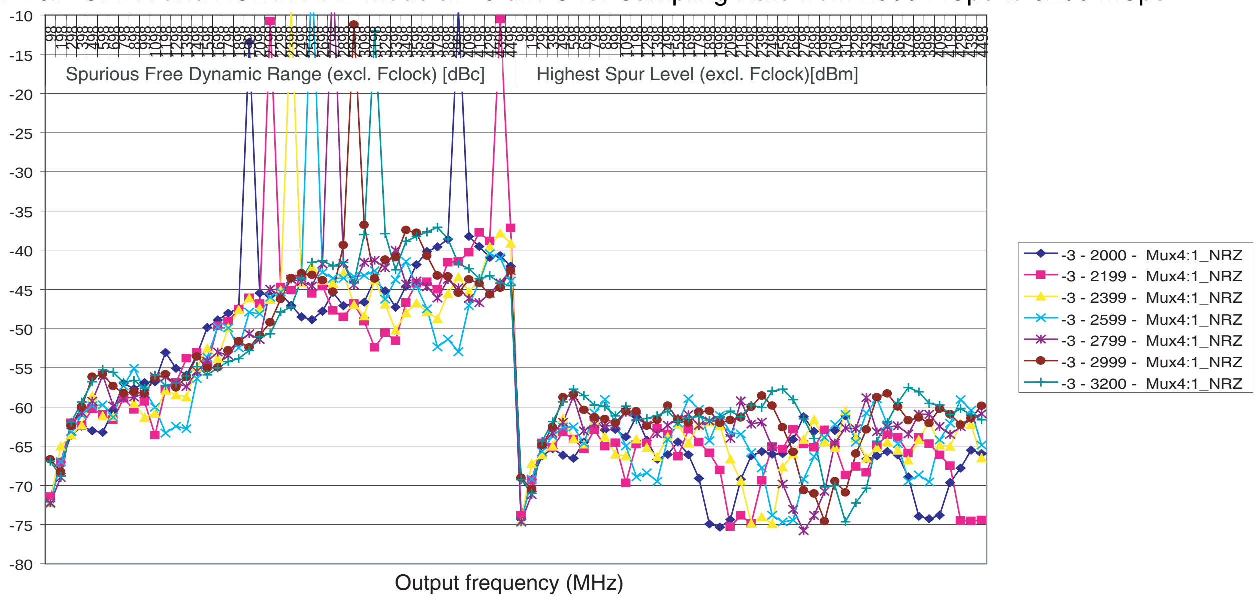


7.2.2 Single Tone Measurements

The following plots summarize characterization results in MUX4:1 mode, for an Fout sweep from 98 MHz to 4498 MHz (step 100 MHz).

The left side of the plot gives SFDR expressed in dBc and the right side gives HSL (Highest Spur Level excluding Fclock spur) expressed in dBm.

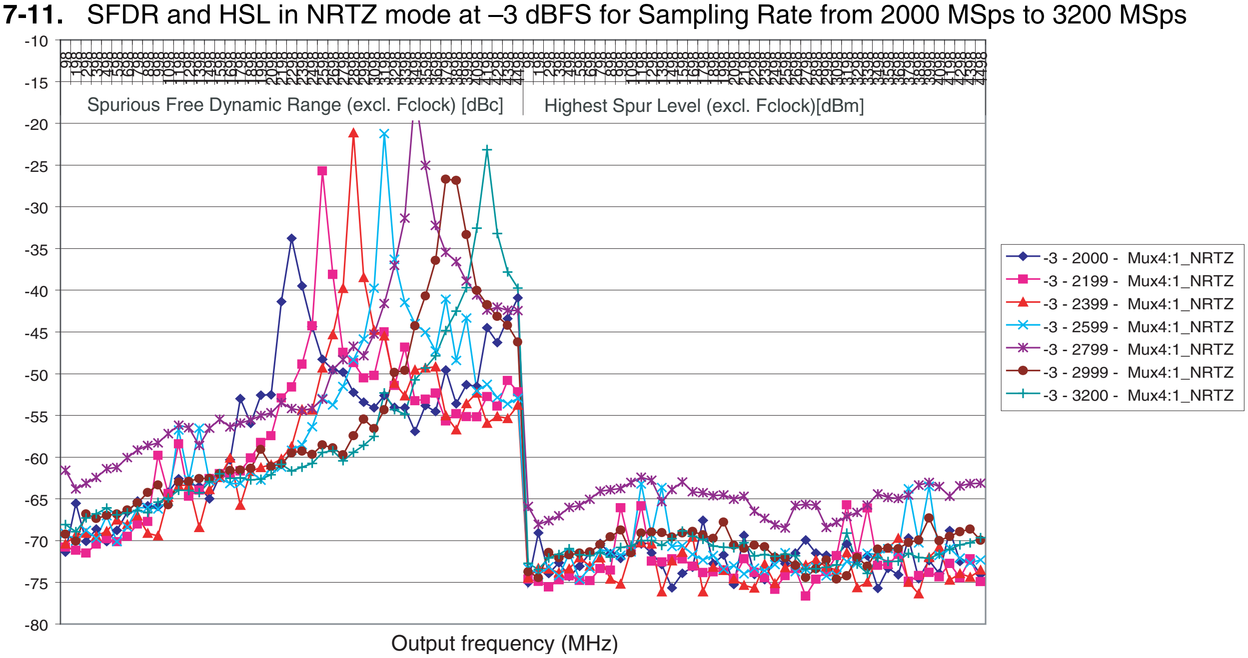
Figure 7-10. SFDR and HSL in NRZ mode at –3 dBFS for Sampling Rate from 2000 MSps to 3200 MSps



NRZ mode is only relevant for Fout below 400 MHz.

The spikes in the SFDR are caused by normalization artefacts due to the Sinc(x) null.

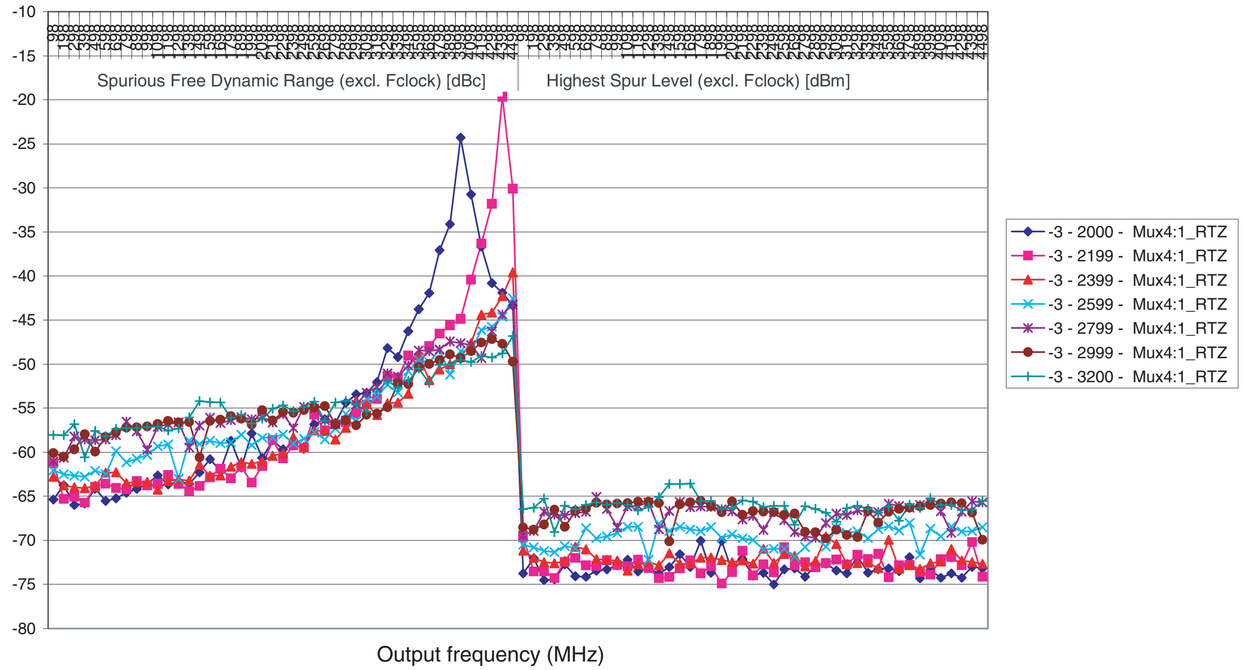
Figure 7-11. SFDR and HSL in NRTZ mode at –3 dBFS for Sampling Rate from 2000 MSps to 3200 MSps



NRTZ mode brings significant improvement regarding NRZ mode. This mode concentrates the benefits of both NRZ mode (high power available) and RTZ mode (extended available dynamic range).

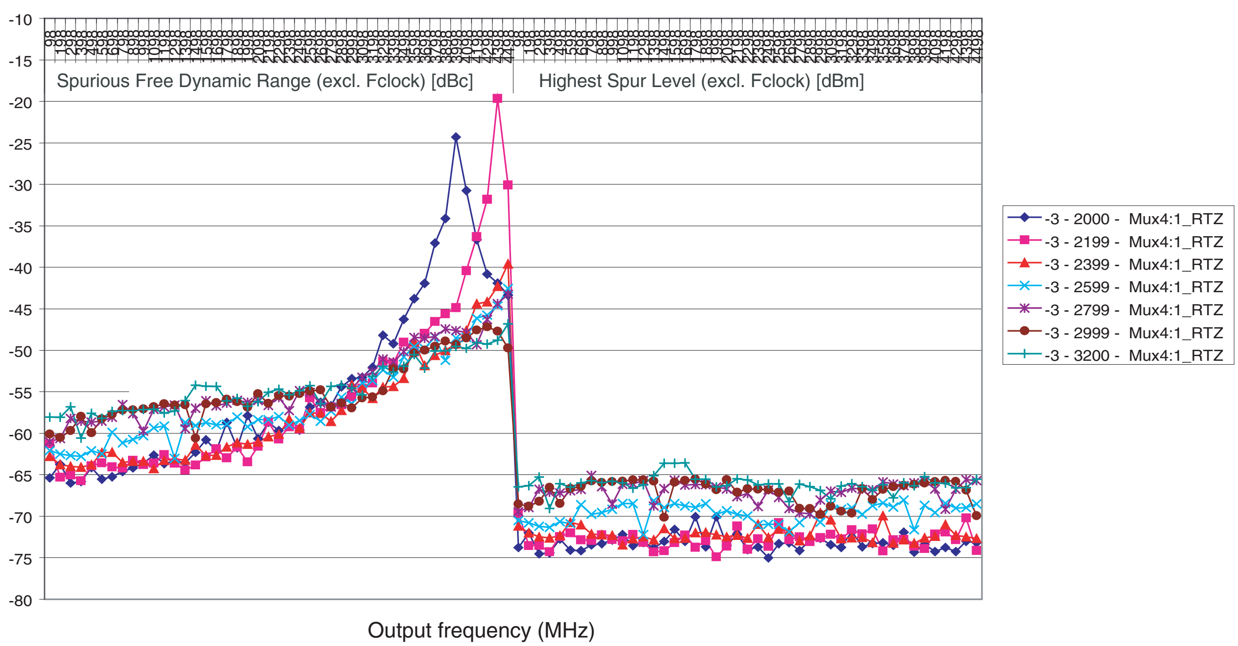
The spikes in the SFDR are caused by normalization artefacts due to the Sinc(x) null.

Figure 7-12. SFDR and HSL in RTZ Mode at –3 dBFS for Sampling Rate from 2000 MSps to 3200 MSps



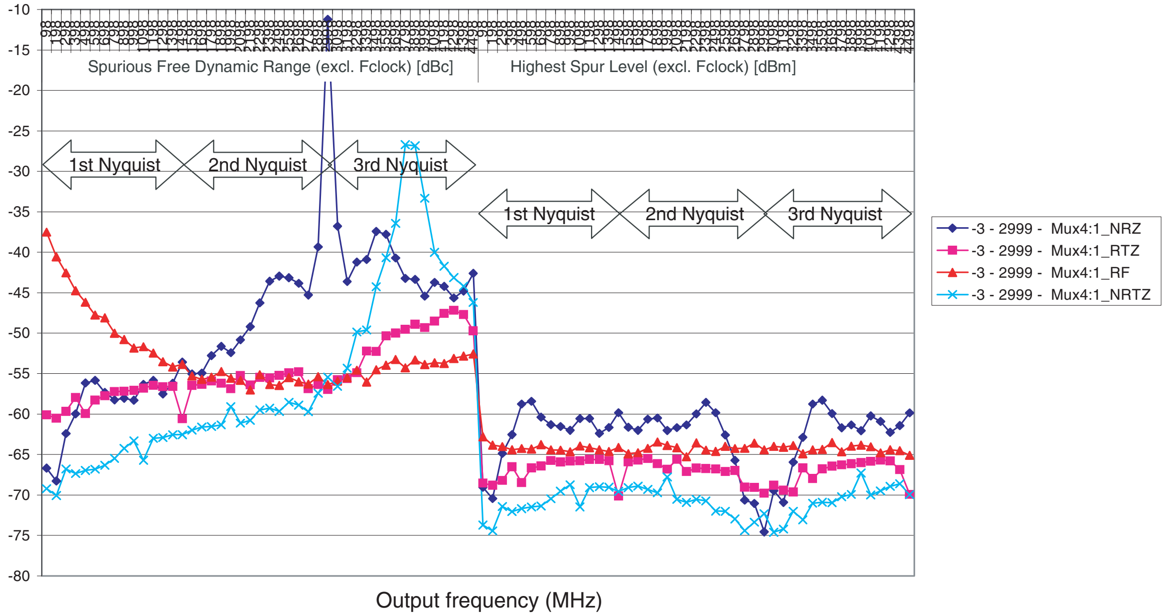
RTZ mode allows for operation over the 3 first Nyquist zones.
In first and beginning of second Nyquist zone NRTZ mode is mode relevant. The spikes in the SFDR are caused by normalization artefacts due to the Sinc(x) null.

Figure 7-13. SFDR and HSL in RF Mode at –3 dBFS for Sampling Rate from 2000 MSps to 3200 MSps



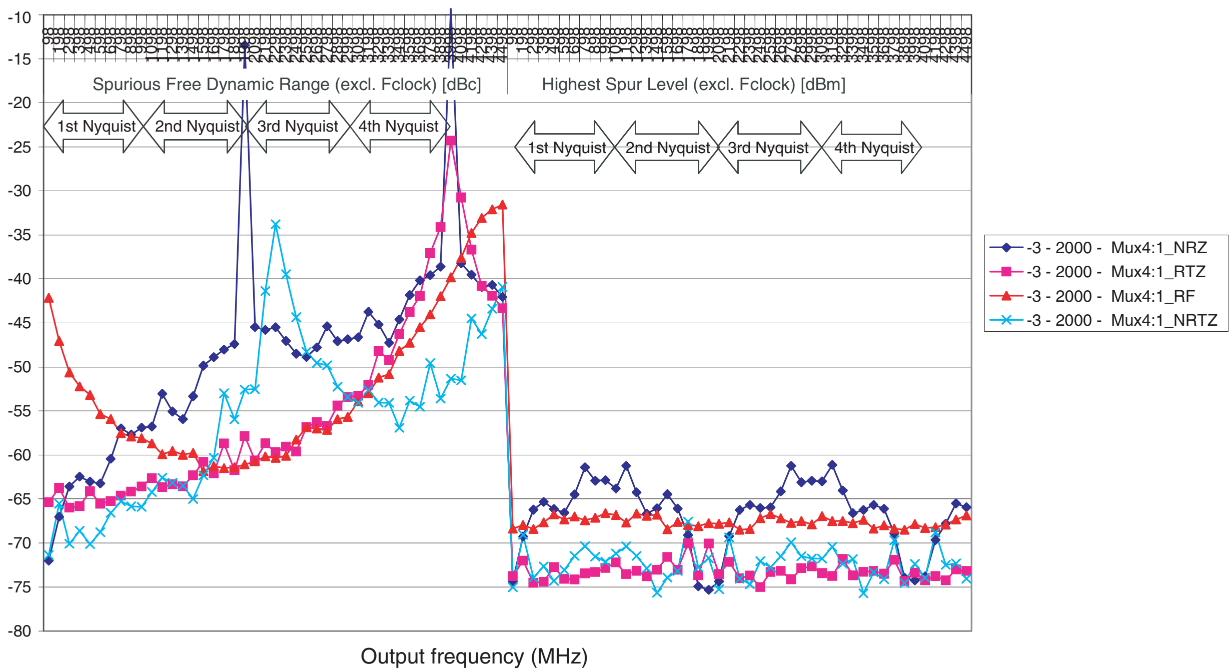
RF mode allows for operation over 3rd Nyquist zones. Performances are not sensitive to output level. Performance roll off occurs beyond 3000 MSps.

Figure 7-14. Comparison of the 4 Output Modes at 2999 MSps and at –3 dBFS: SFDR and HSL



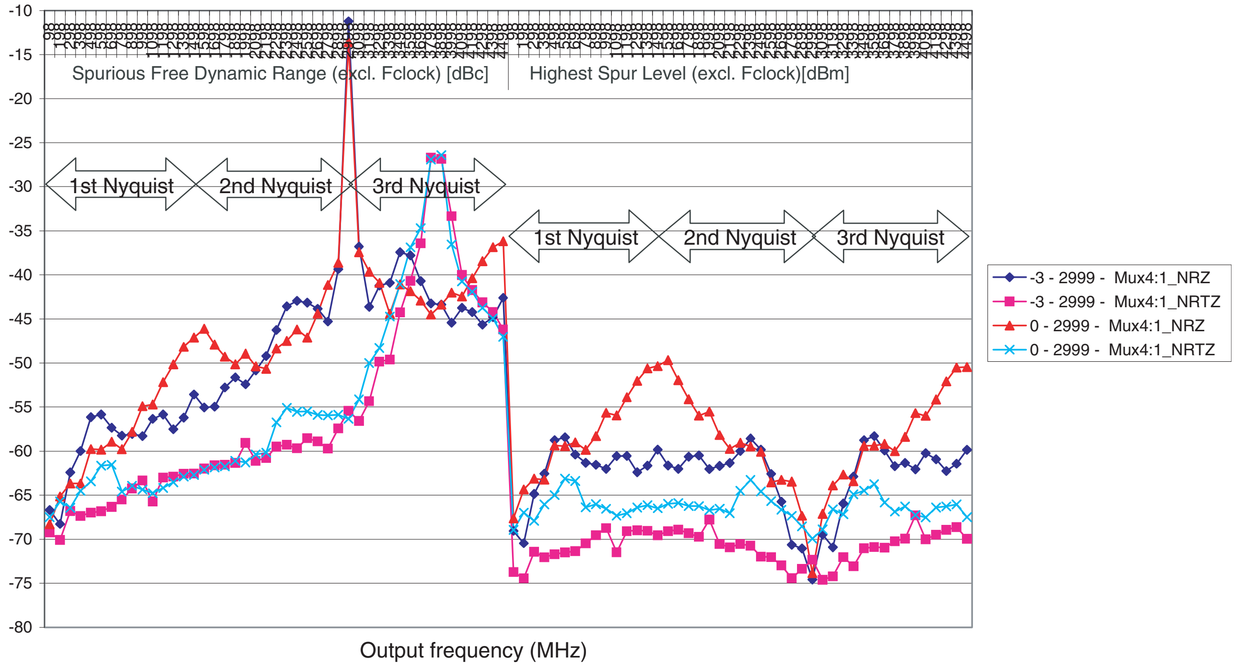
NRZ is interesting only at the very beginning of the first Nyquist zone.
NRTZ is relevant over 1st 2nd and 4th Nyquist zones.
RTZ is relevant over 2nd and 3rd Nyquist zones.
RF mode displays a good behavior over 2nd and 3rd Nyquist Zones.
The spikes in the SFDR are caused by normalization artefacts due to the Sinc(x) null

Figure 7-15. Comparison of the 4 Output Modes at 2000 MSps and –3 dBFS: SFDR and HSL



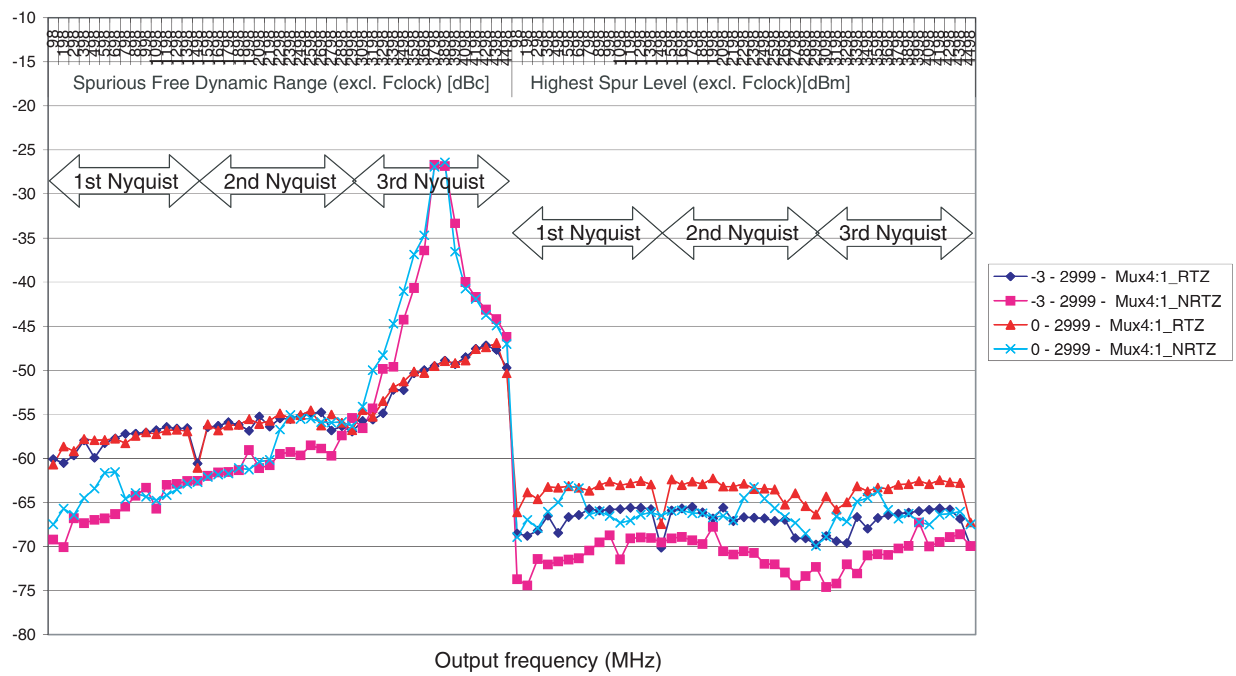
NRTZ is the most relevant over 1st Nyquist zone, 1st half of 2nd Nyquits zone and 4th Nyquist zone.
RF mode is the best choice for 2nd half of 2nd Nyquist Zone and 3rd Nyquist zone.
RTZ gives relevant performances over the three first Nyquist zones.
The spikes in the SFDR are caused by normalization artefacts due to the Sinc(x) null

Figure 7-16. Comparison of NRZ and NRTZ Modes at Full Scale and –3 dBFS at 2999 MSps: SFDR and HSL (Excluding Fclock)



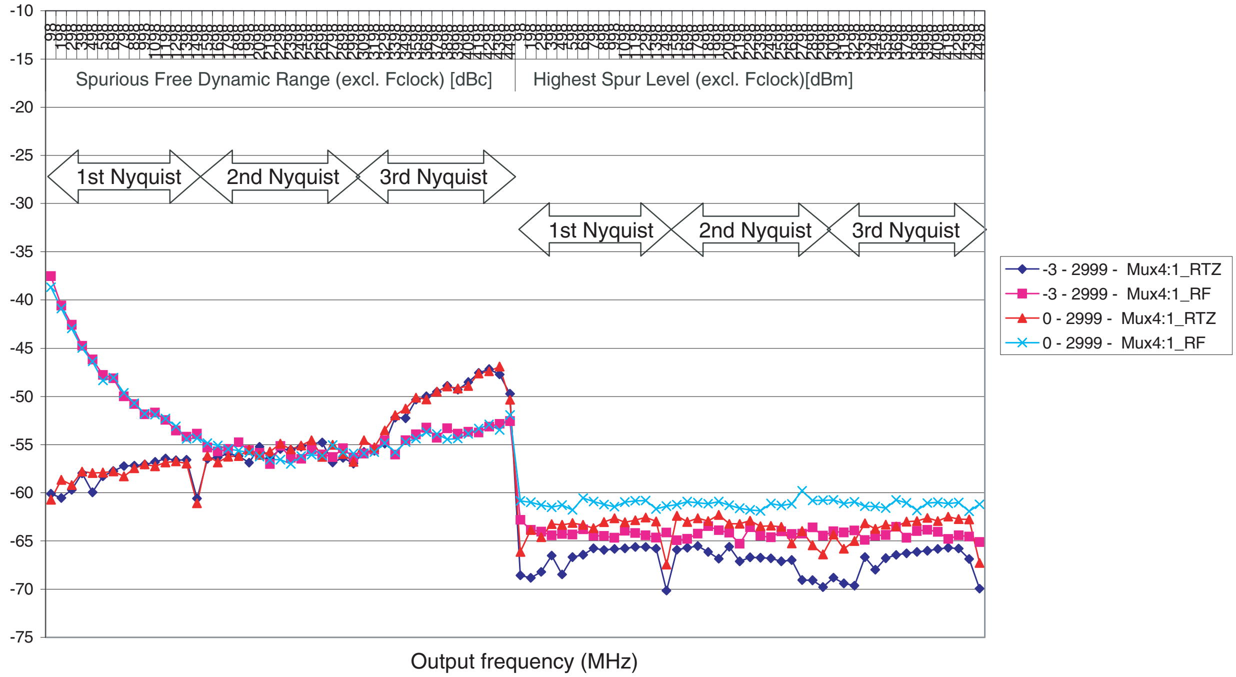
NRTZ gives better performances over 1st and 2nd Nyquist zone, and is much less sensitive to output level.

Figure 7-17. Comparison of NRTZ and RTZ Modes at Full Scale and –3 dBFS at 2999 MSps: SFDR and HSL



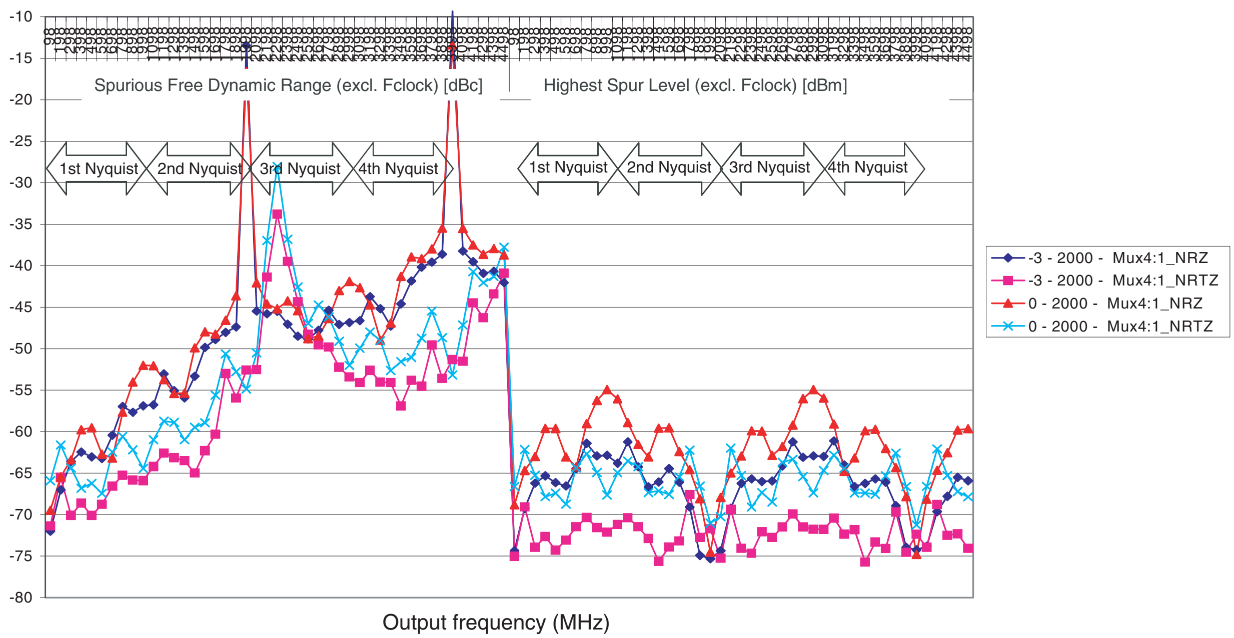
NRTZ is more relevant for 1st Nyquist zone and 1st half of 2nd Nyquist zone. Beyond middle of second Nyquist zone RTZ mode is more relevant.

Figure 7-18. Comparison of RTZ and RF Modes at Full Scale and –3 dBFS at 2999 MSps: SFDR and HSL



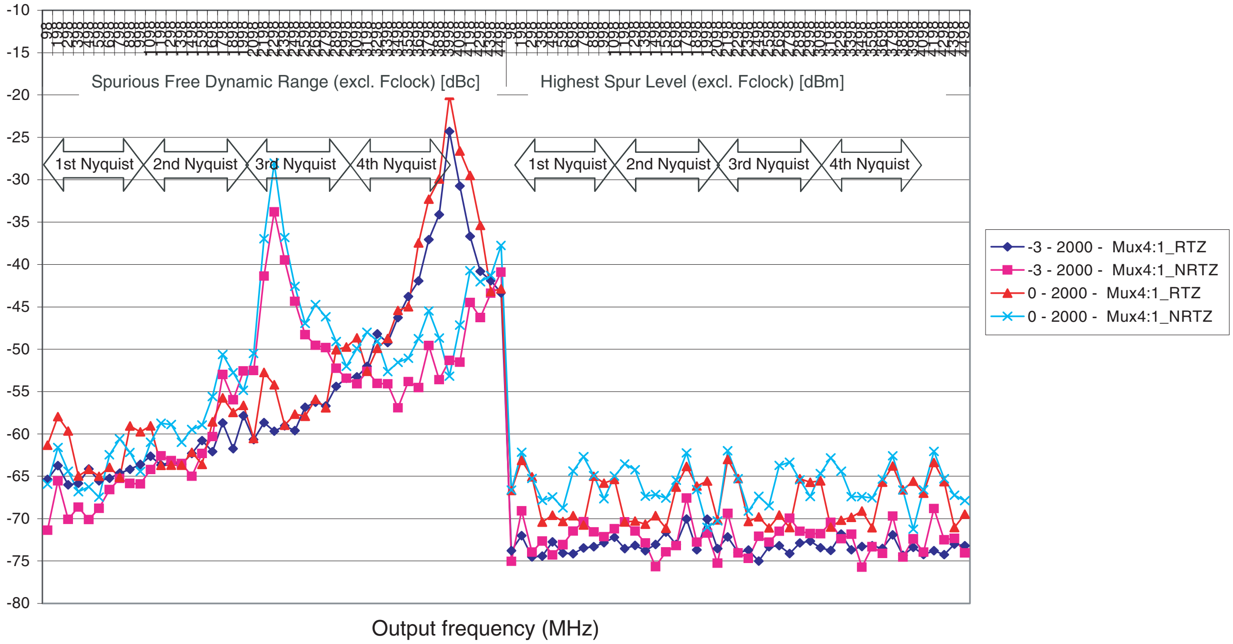
RF mode gives better performance over 3rd Nyquist zone.

Figure 7-19. Comparison of NRZ and NRTZ Modes at Full Scale and –3 dBFS at 2000 MSps: SFDR and HSL (Excluding Fclock)



NRTZ linearity is slightly improved reducing the sampling rate to 2000 MSps, possibility of operation over the 4th Nyquist zone is demonstrated.

Figure 7-20. Comparison of NTRZ and RTZ Modes at Full Scale and –3 dBFS at 2000 MSps: SFDR and HSL (Excluding Fclock)



NRTZ mode is relevant in 1st, 2nd Nyquist zones and is still usable over 4th Nyquist zone with SFDR in excess of 50 dBc.

7.2.3 Single Tone Measurements: Spectrum of a 1482 MHz Pattern Generated at 3 GSps

Measurements hereafter have been performed on an EV12DS130AZPY device, with FSU8 spectrum analyzer, using a 0.5 GHz-7 GHz balun on the analog output, generating a single tone at –3 dBFS.

Figure 7-21. Observation of the 1st and 2nd Nyquist Zones in Output Mode NRZ

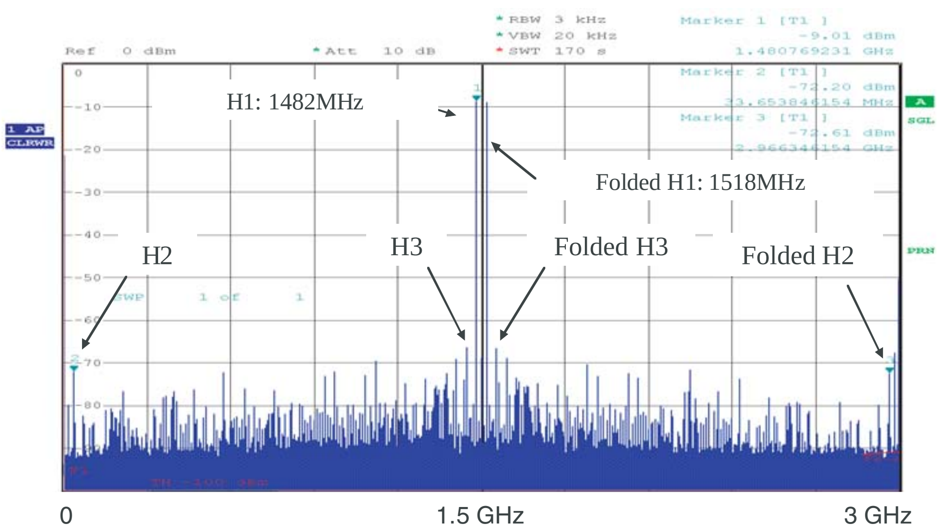


Figure 7-22. Observation of the 1st and 2nd Nyquist Zones in Output Mode NRTZ

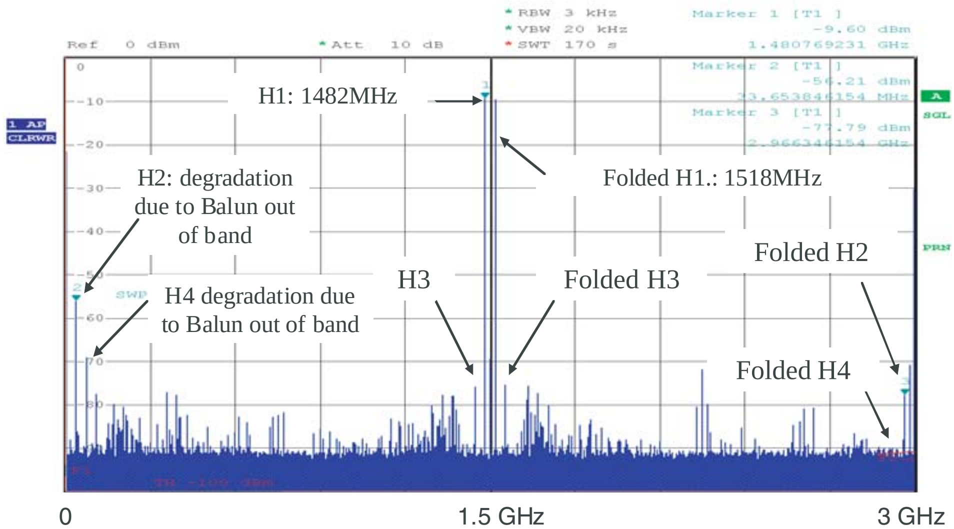
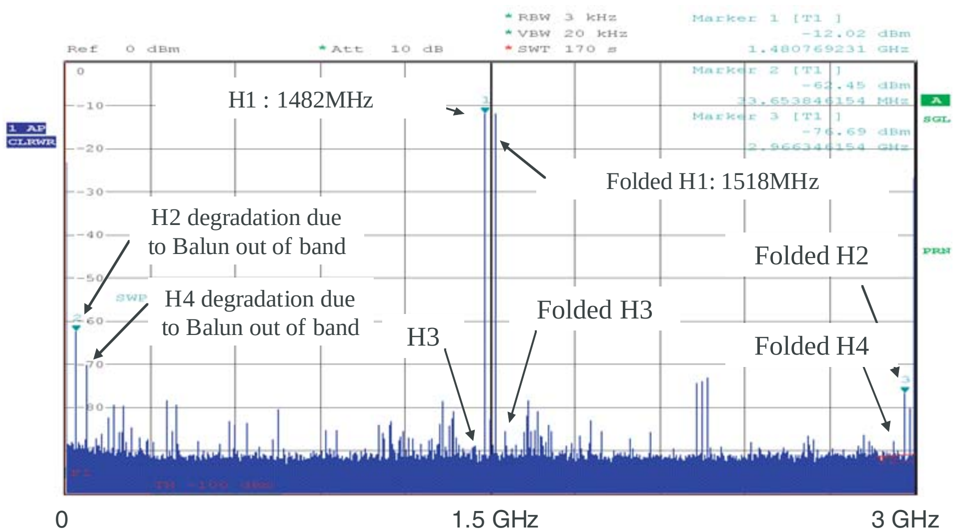


Figure 7-23. Observation of the 1st and 2nd Nyquist Zones in Output Mode RTZ



These three plots show clearly the benefit of NRTZ or RTZ modes over NRZ mode in term of spectral purity for tones generated beyond the 1st quarter of the first Nyquist zone. Further more it illustrates the dramatic degradations induced by an inappropriate Balun choice (part of the band of interest out of the specified domain of the Balun).

Following figures illustrate the possible improvement when using a more appropriate Balun. Measurements are performed in RTZ mode, with FSEB spectrum analyzer, for a –3 dBFS tone generated at the same frequencies for Fclock and Fout, with different Baluns to perform the Differential to single conversion before spectrum analyzer.

Figure 7-24. Spectrum of the 1st Nyquist Zone, Output Mode RTZ, with a 0.5 GHz to 7 GHz Bandwidth Balun

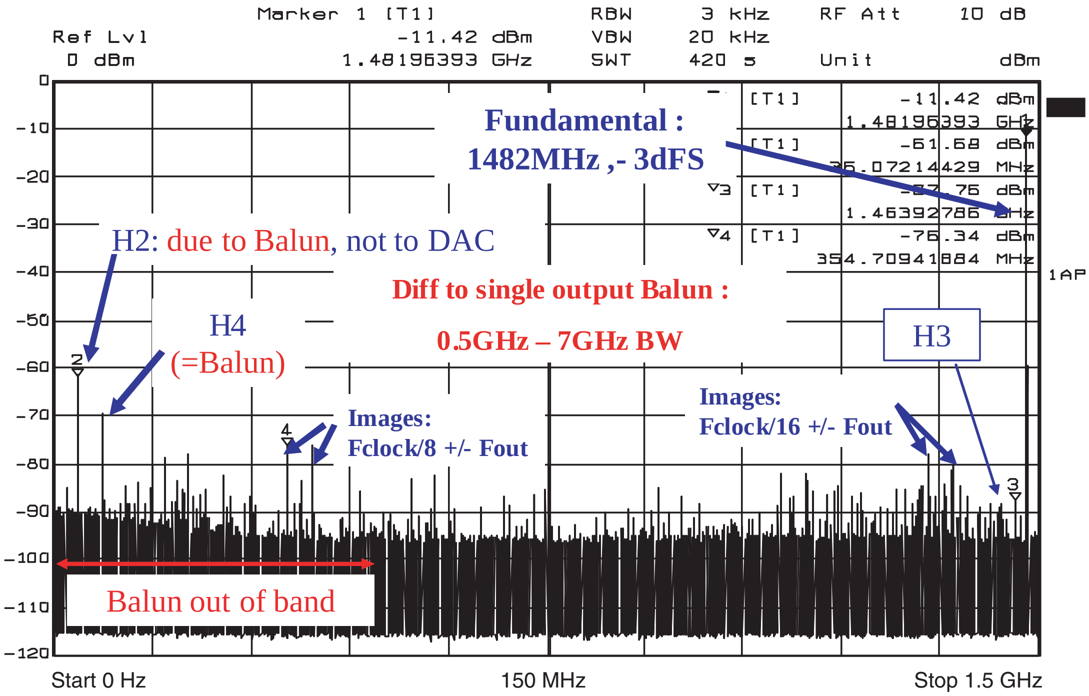


Figure 7-25. Spectrum of the 1st Nyquist Zone, Output Mode RTZ, with a 0.5 MHz to 1.5 GHz Bandwidth Balun

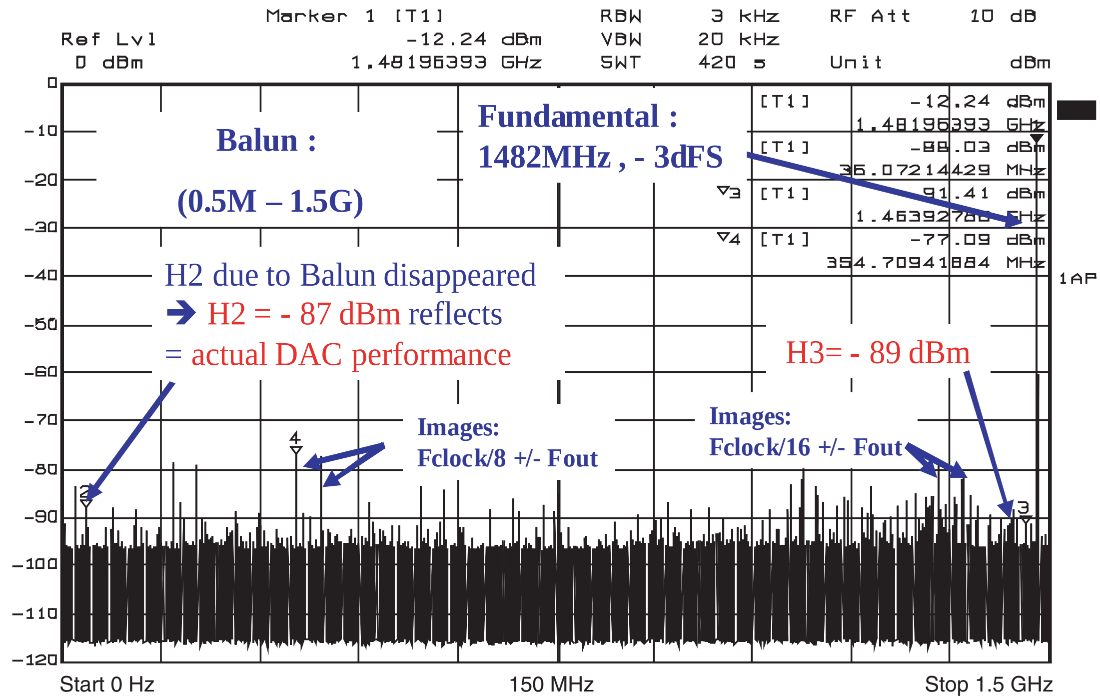
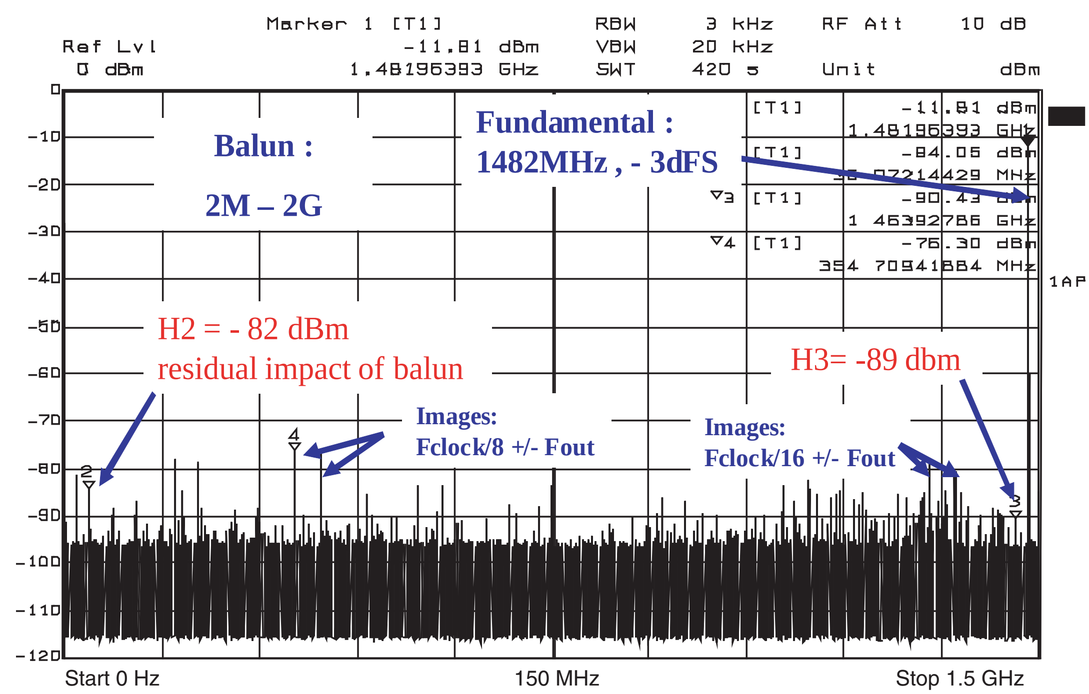


Figure 7-26. Spectrum of the 1st Nyquist Zone, Output Mode RTZ with a 2 MHz to 2GHz Bandwidth Balun



The impact of the output Balun choice on performance in 1st Nyquist Zone is confirmed.

As a consequence the board designer must be aware that optimum performance can be reached only when using a Balun optimal for the band of interest of the application. For operation in the first Nyquist zone it is recommended to select a Balun which is specified from less than 2 MHz to at least 1.5 GHz. For operation in the 2nd or the 3rd Nyquits zone it is recommended to use a Balun specified from 0.5 GHz to 7 GHz.

For practical reason the industrial test is done with a 0.5GHz to 7GHz Balun, whatever the Nyquist zone observed, and therefore all specified values in single tone for the 1st Nyquist zone are pessimistic regarding the performance which can actually be reached using an optimal Balun.

Figures hereafter give spectrum obtained in 1st Nyquist zone in NRZ and NRTZ mode using an optimal Balun, on the same device with the same frequency couples, and indeed they display significant improvement.

Figure 7-27. Spectrum of the 1st Nyquist Zone, Output Mode NRZ, with a 0.5 MHz to 1.5GHz Bandwidth Balun

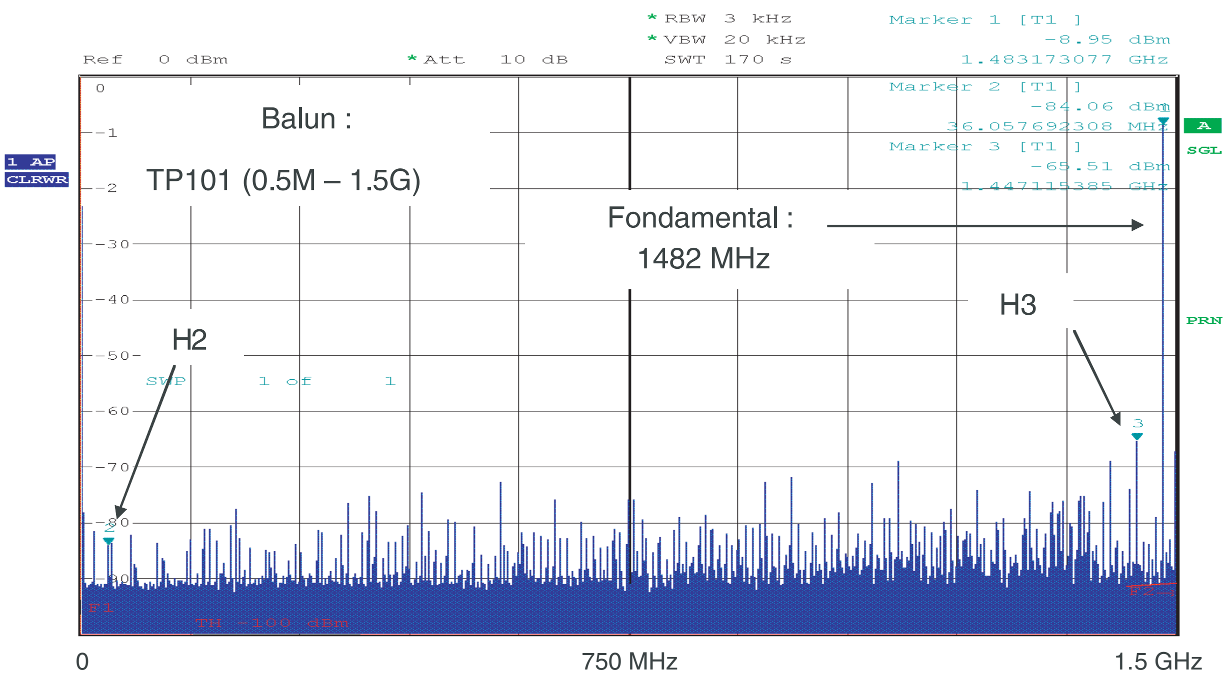
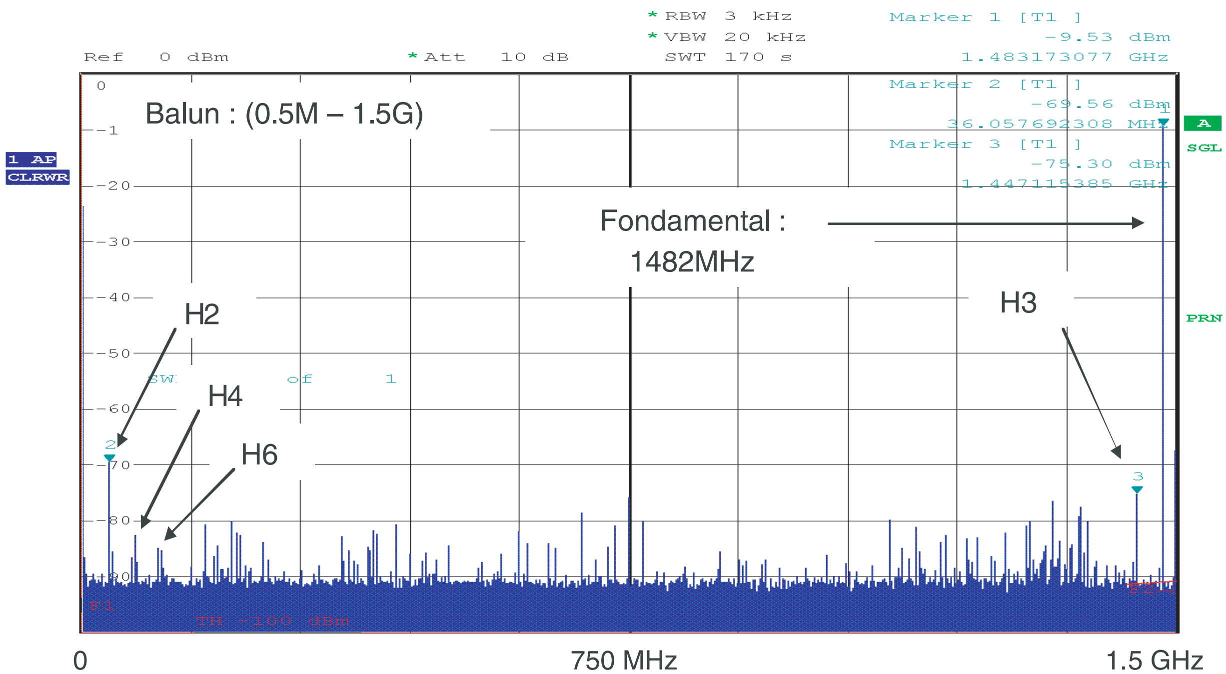


Figure 7-28. Spectrum of the 1st Nyquist Zone, Output Mode NRTZ, with a 0.5 MHz to 1.5 GHz Bandwidth Balun



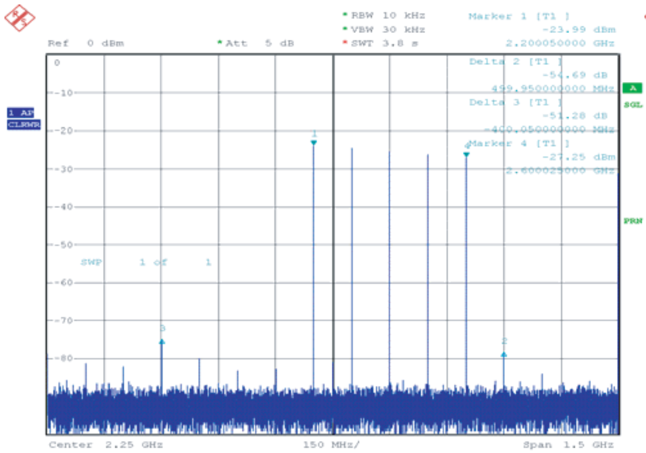
7.2.4 Multi Tone Measurements

A five tones pattern (400 MHz, 500 MHz, 600 MHz, 700 MHz and 800 MHz) is applied to the DAC operating at 3 GSps and results are observed in the 2nd, 3rd, 4th and 5th Nyquist zones.

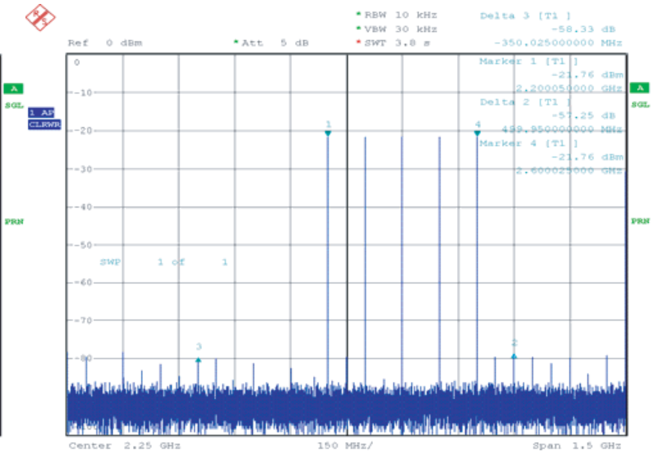
Results are given in the most relevant mode considering the Nyquist zone observed.

Figure 7-29. Observation of the 2nd Nyquist Zone (Tones are pushed from 2.2 GHz to 2.6 GHz): NRTZ, RF and RTZ Modes

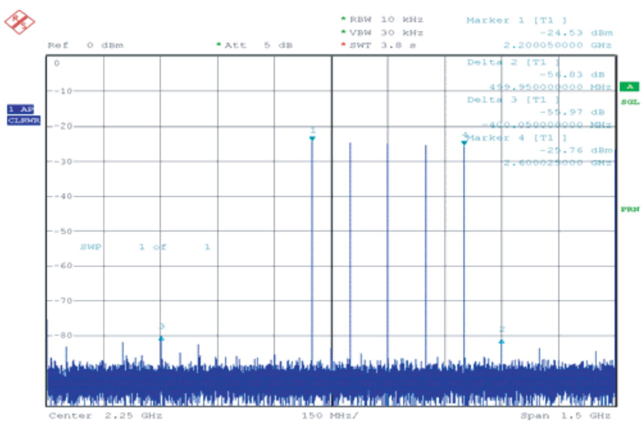
NRTZ mode:



RF mode:



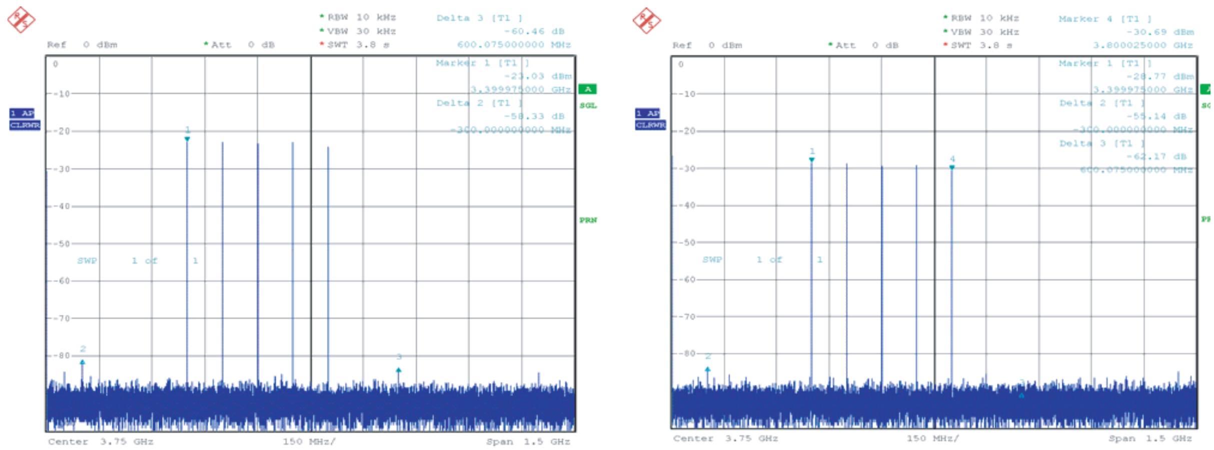
RTZ mode:



	Fout (MHz)	Pout (dBm)	SFDR (freq)	SFDR (dBc)
NRTZ	2200	-23,99	1800	-51,28
RTZ	2200	-24,53	1800	-55,97
RF	2200	-21,76	2700	-57,25

Figure 7-30. Observation of the 3rd Nyquist Zone (Tones are pushed from 3.4GHz to 3.8GHz): RF and RTZ Modes

RF mode: RTZ mode:

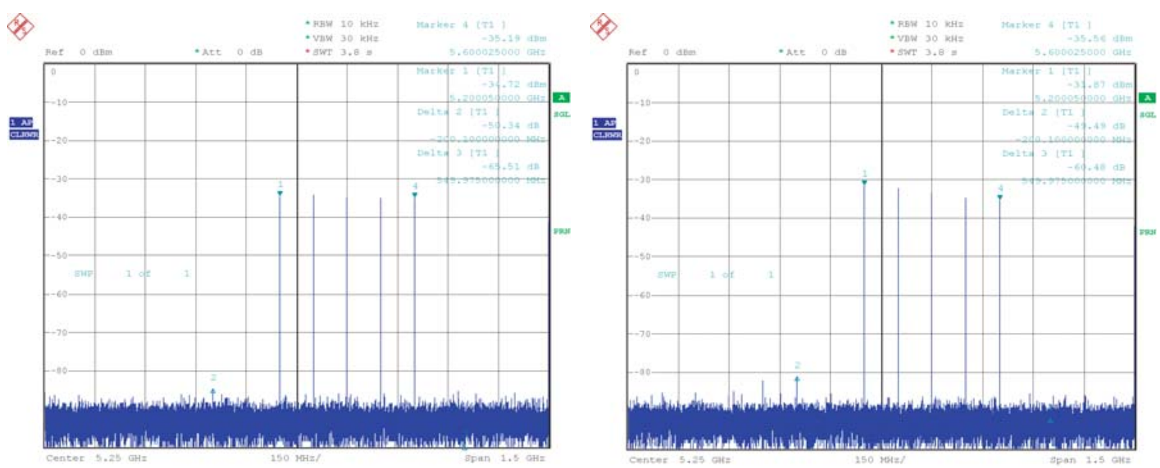


	Fout (MHz)	Pout (dBm)	SFDR (freq)	SFDR (dBc)
NRTZ	3400	–39.43	4000	–44.48
RTZ	3400	–28.77	3100	–55.14
RF	3400	–23.03	3100	–58.33

NRTZ performances are degraded because of the sinc attenuation (first notch in the first half of the 3rd Nyquist zone).

Figure 7-31. Observation of the 4th Nyquist Zone (Tones are pushed from 5.2 GHz to 5.6 GHz): NRTZ and RF Modes

NRTZ mode RF mode

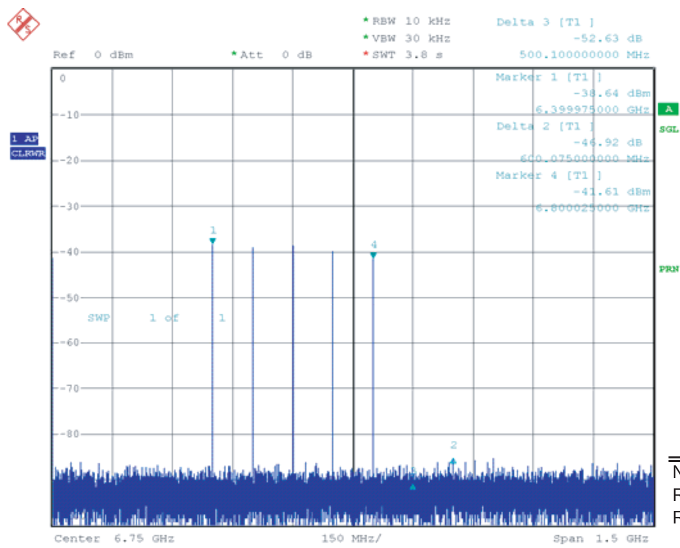


	Fout (MHz)	Pout (dBm)	SFDR (freq)	SFDR (dBc)
NRTZ	5200	–34.72	5000	–50.34
RTZ	5200	–40.37	4700	–45
RF	5200	–31.87	4700	–49.49

RTZ mode is degraded because of the sinc attenuation (first notch at the end of the 4th Nyquist zone). RF mode offers significantly more power than RTZ mode, this is why we still have acceptable performances.

NRTZ operation is possible because the 4th Nyquist zone is fully included in the secondary spectral lobe.

Figure 7-32. Observation of the 5th Nyquist Zone (Tones are pushed from 6.4 GHz to 6.8 GHz): NRTZ Mode



	Fout (MHz)	Pout (dBm)	SFDR (freq)	SFDR (dBc)
N RTZ	6400	-38,64	7000	-46,92
RTZ	6800	-46,69	7000	-39,25
RF	6400	-46,89	7000	-38,01

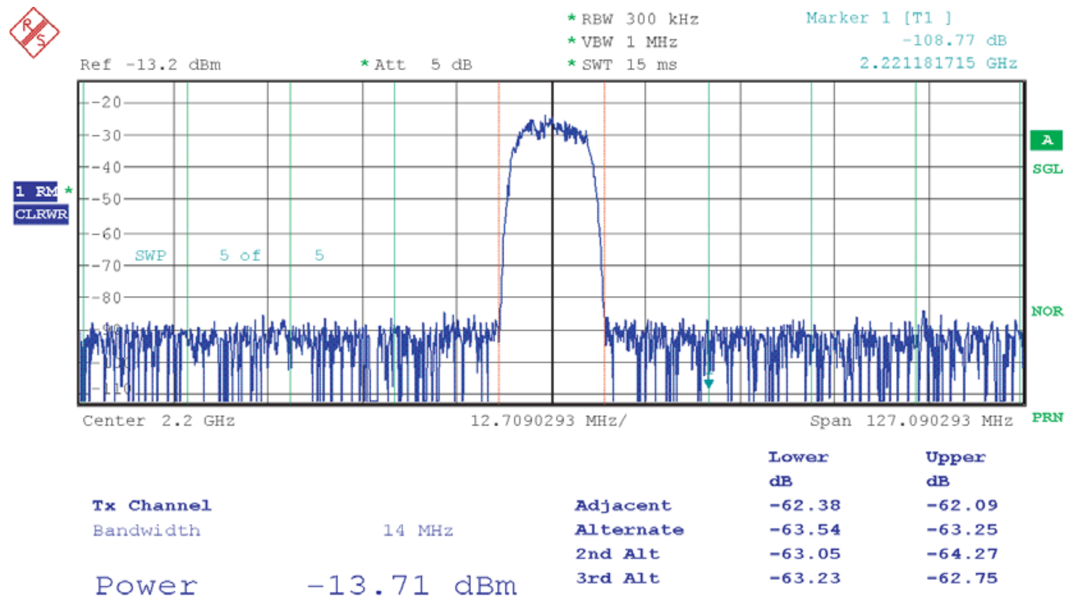
NRTZ mode is still usable in the 5th Nyquist zone (SFDR in excess of 46 dB).

7.2.5 DMWS (Direct Micro Wave Synthesis) Capability Measurements: ACPR

Measurements given here after are performed on the DAC at 3 GSps with a 10 MHz wide QPSK pattern centered on 800 MHz.

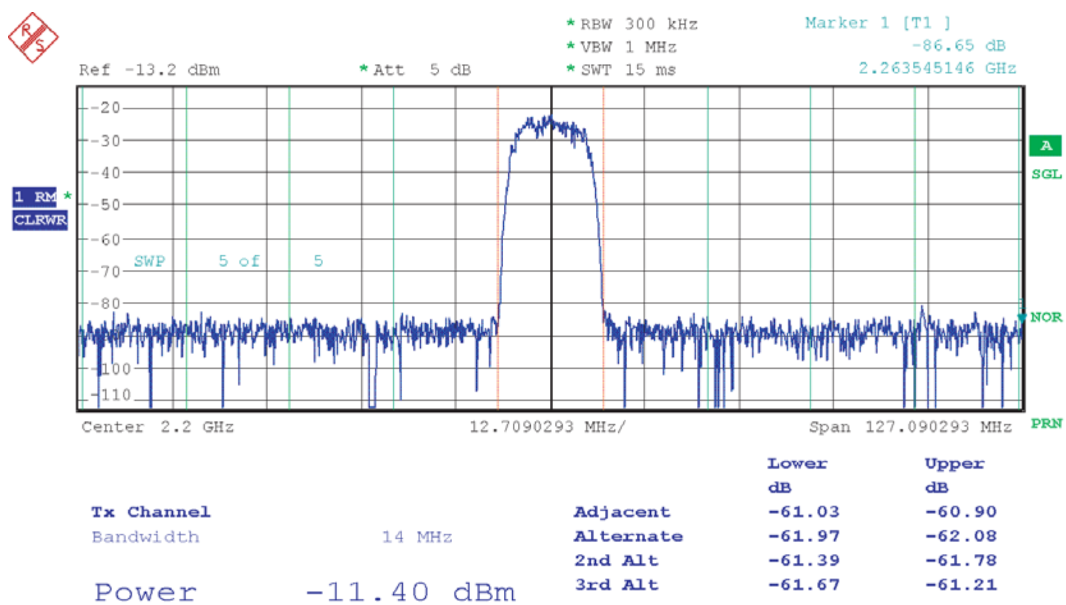
Results are observed in 2nd, 3rd, 4th and 5th Nyquist zones and are given only for the most relevant modes (that is RF and/or NRTZ modes).

Figure 7-33. NRTZ Mode, 2nd Nyquist: Center Frequency is pushed to 3 GHz – 800 MHz = 2.2 GHz



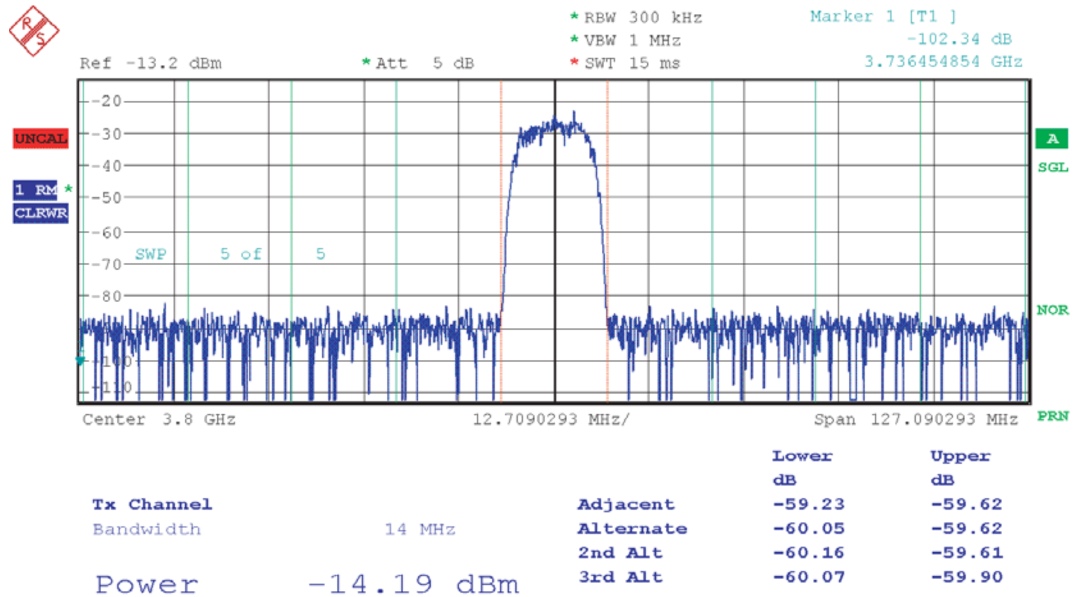
ACPR is in excess of 62 dB. DMWS capability is proven for second Nyquist in NRTZ mode.

Figure 7-34. RF Mode, 2nd Nyquist: Center Frequency is pushed to 3 GHz – 800 MHz = 2.2 GHz



ACPR is in excess of 60 dB. DMWS capability is proven for the second Nyquist zone in RF mode with slightly reduced dynamic range regarding NRTZ mode but with increased output power.

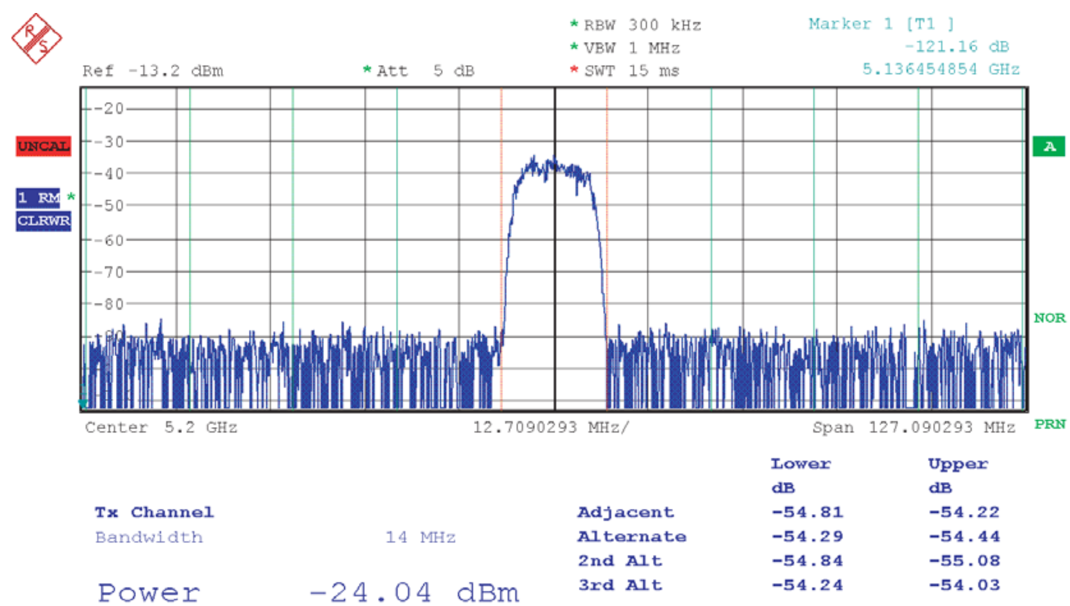
Figure 7-35. RF Mode, 3rd Nyquist Zone: Center Frequency is pushed to 3 GHz+ 800 MHz = 3.8 GHz



ACPR is in excess of 59 dB. DMWS capability is proven for the third Nyquist zone in RF mode.

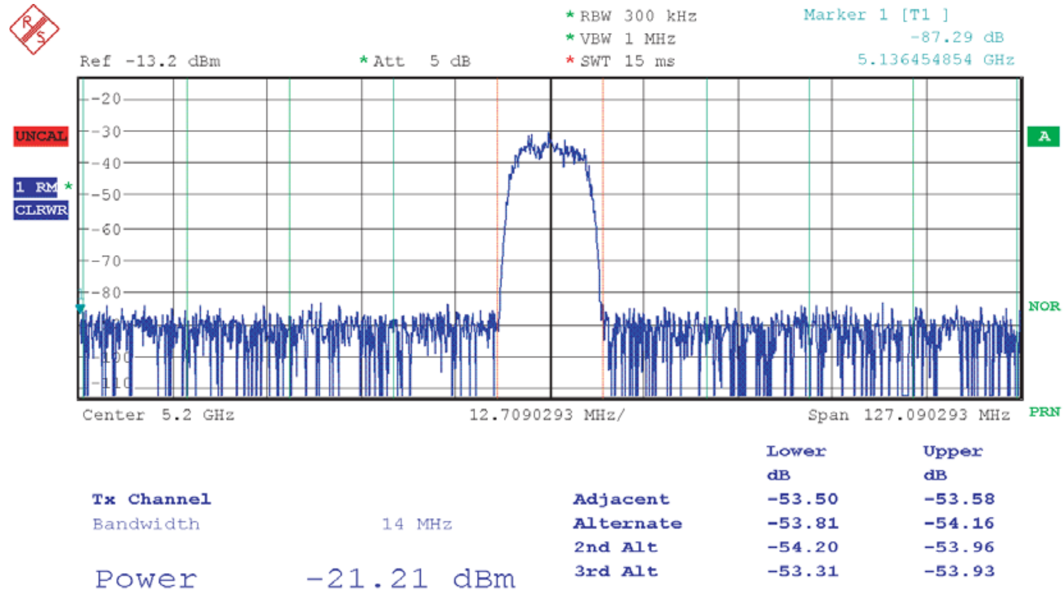
Note: due the notch of available Pout near the middle of the third Nyquist zone, the NRTZ mode is not relevant for DMWS in the third Nyquist zone.

Figure 7-36. NRTZ Mode, 4th Nyquist Zone: Center Frequency is pushed to 6 GHz – 800 MHz = 5.2 GHz



ACPR is in excess of 54 dB. DMWS capability is proven for the fourth Nyquist zone in NRTZ mode.

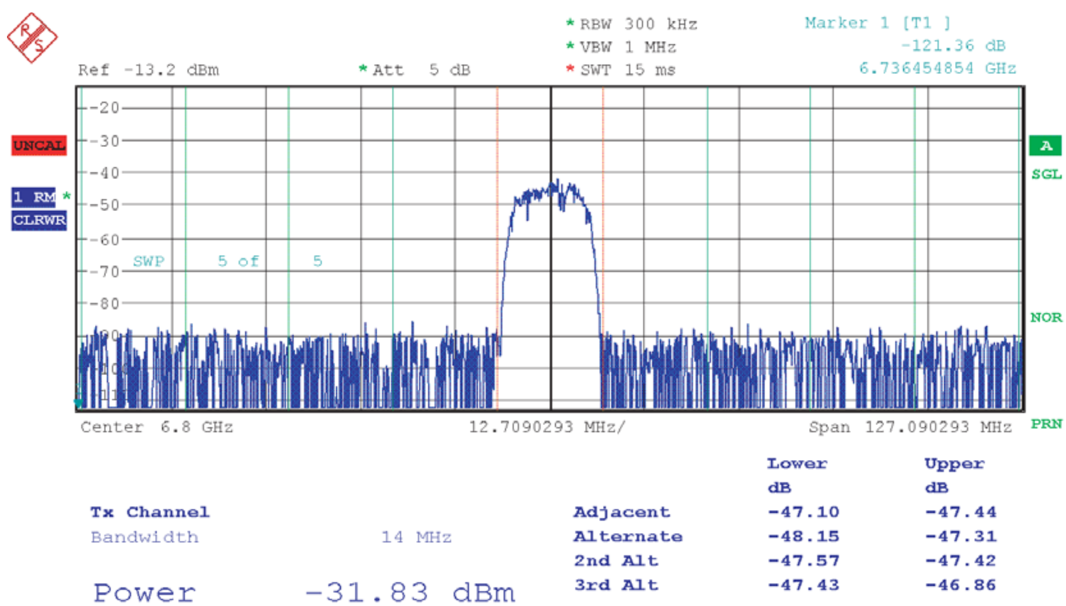
Figure 7-37. RF Mode, 4th Nyquist Zone: Center Frequency is pushed to 6 GHz – 800 MHz = 5.2 GHz



ACPR is in excess of 53 dB. DMWS capability is proven for the fourth Nyquist zone in RF mode.

Note due to a notch of available Pout near the end of the 4th Nyquist zone in RF output mode, for DMWS beyond middle of 4th Nyquist zone it is recommended to use the NRTZ output mode instead of the RF output mode.

Figure 7-38. NRTZ Mode, 5th Nyquist Zone: Center Frequency is pushed to 6 GHz + 800 MHz = 6.8 GHz



ACPR is still in excess of 47 dB. DMWS capability if proven for the fifth Nyquist zone in NRTZ mode with reduced available dynamic range.

7.2.6 DOCSIS v3.0 Capability Measurements

Measurements here after have been carried out on a soldered device EV12DS130AZPY (fPBGA 196), in NRTZ mode.

Figure 7-39. ACPR 1 Channel Centered on 300 MHz, Output Mode NRTZ

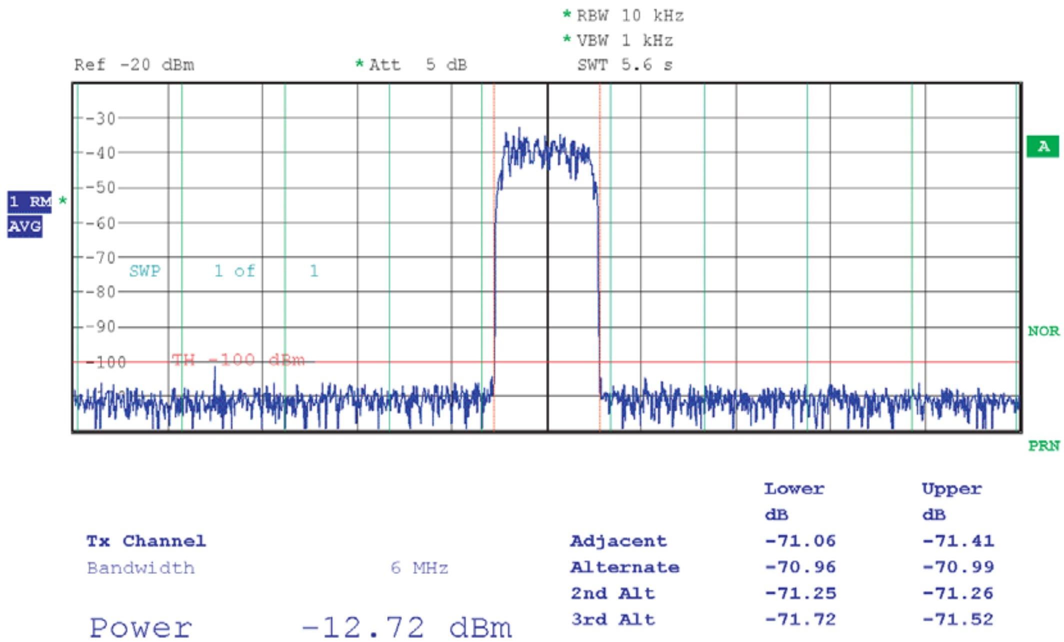
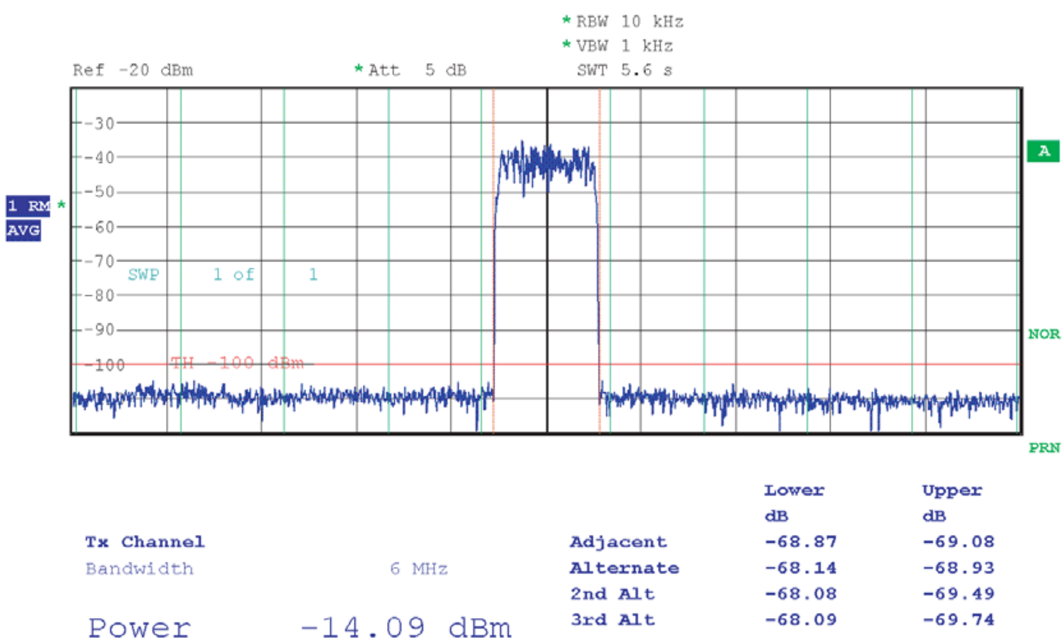


Figure 7-40. ACPR 1 Channel Centered on 900 MHz, Output Mode NRTZ



Measurements here after have been carried out on a soldered device EV12DS130AGS (CI-CGA 255), in NRTZ mode.

Figure 7-41. ACPR 1 channel centered on 300 MHz, Output Mode NRTZ, CI-CGA255

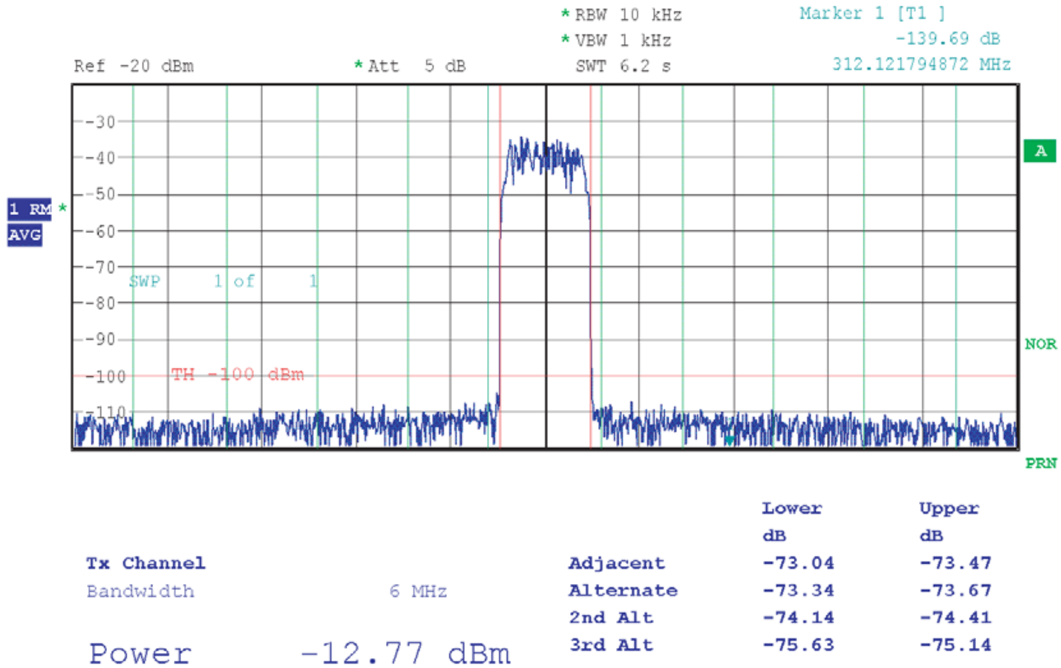


Figure 7-42. ACPR 4 Channels Centered on 300 MHz, Output Mode NRTZ, CI-CGA255

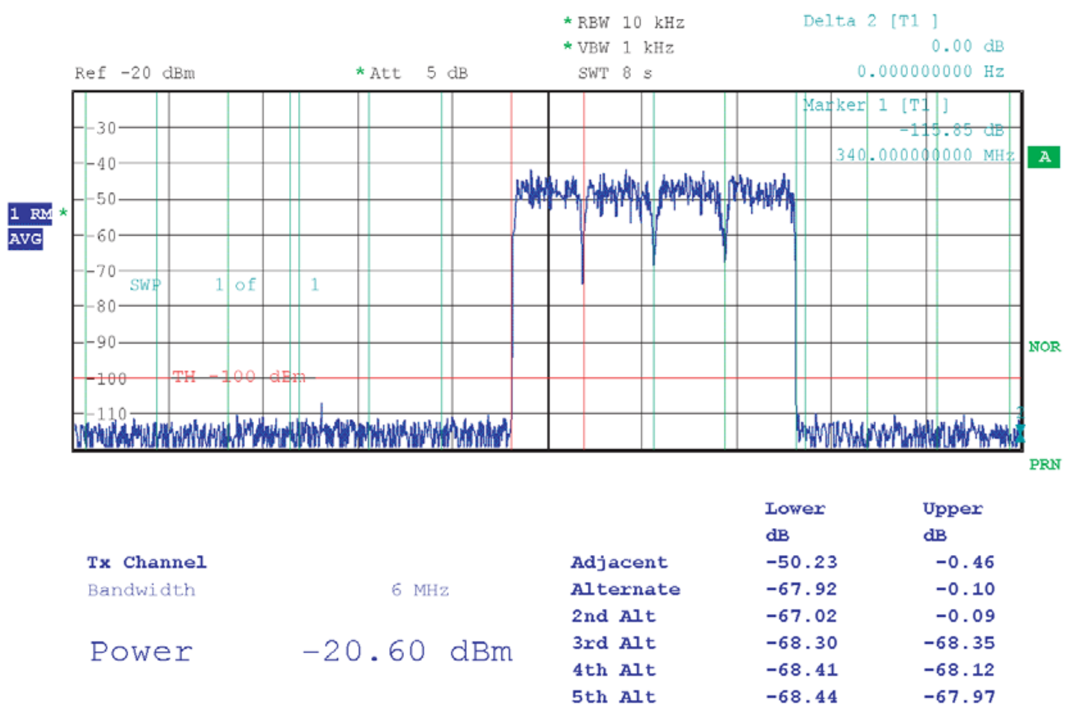


Figure 7-43. ACPR 1 Channel Centered on 900 MHz, Output Mode NRTZ, CI-CGA255

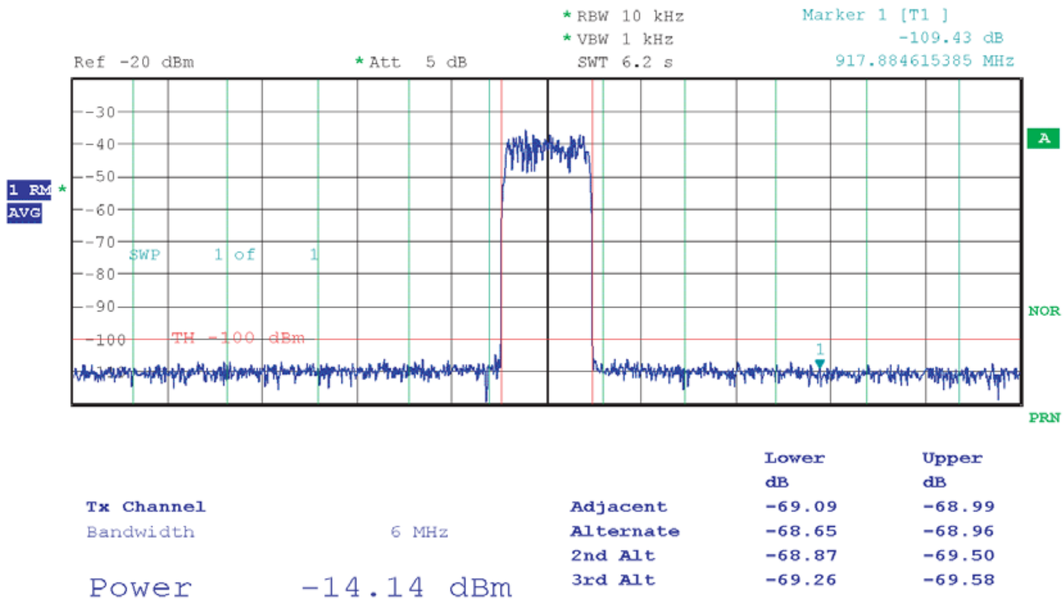
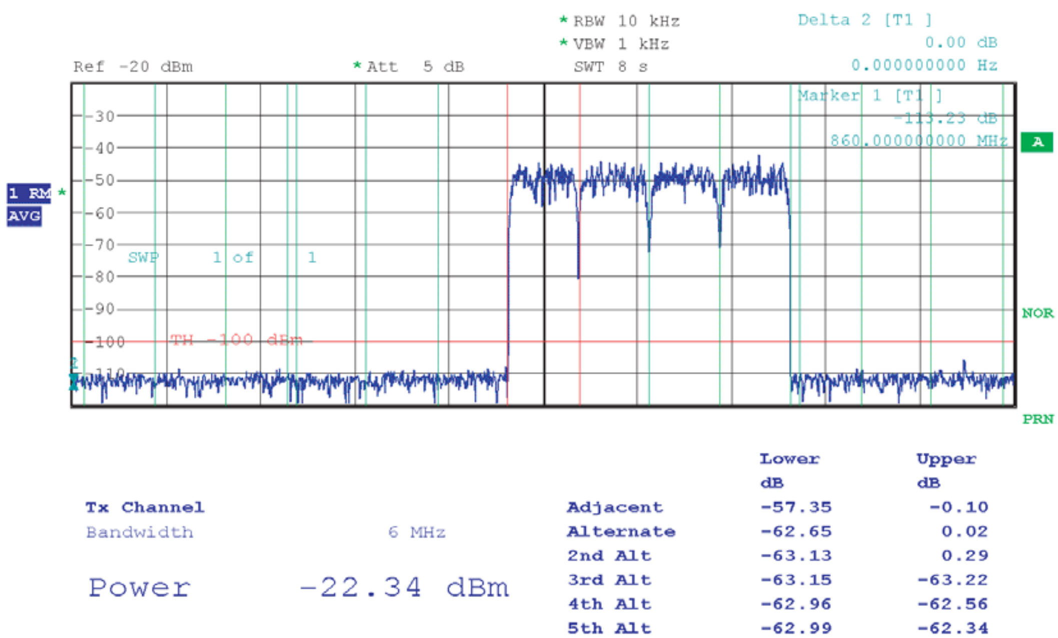


Figure 7-44. ACPR 4 Channels Centered on 900 MHz, Output Mode NRTZ, CI-CGA255



7.2.7 NPR Performance

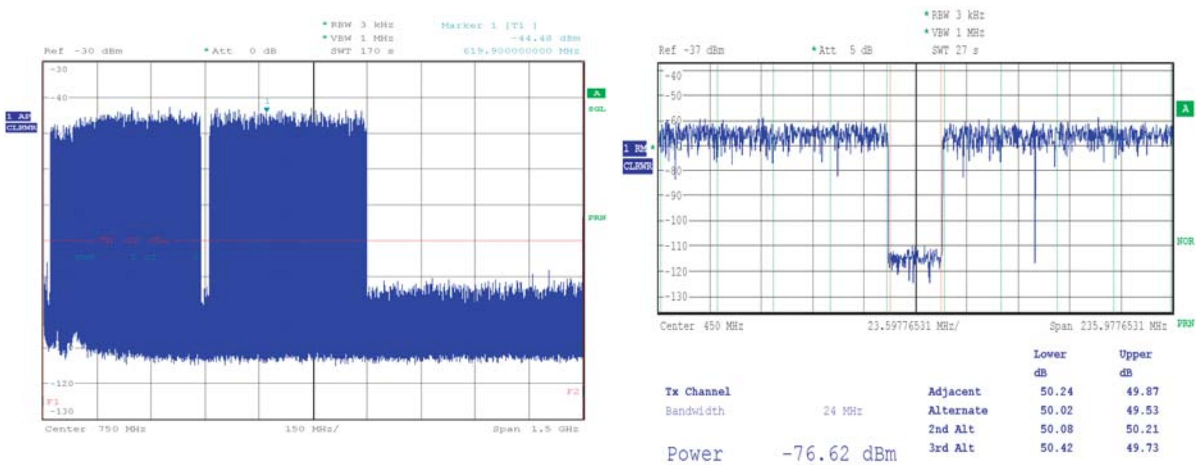
NPR measurements have been carried out at optimum loading factor for a 12 bit DAC, that is –14 dB loading factor (LF), with the DAC operating at 3 GSps.

SNR can be computed from SNR measurement with the formula: $SNR_{[dB]} = NPR_{[dB]} + |LF_{[dB]}| - 3$.

ENOB can be computed with the formula: $ENOB = (SNR_{[dB]} - 1.76) / 6.02$.

Note: Results illustrated hereafter (spectrum and zoom on notch) come for measurement on a EV12DS130AGS device (CI-CGA255 package). Measurements have been carried out using the ACP treatment of the spectrum analyzer Rhode & Schwarz FSU8, in RMS detection mode.

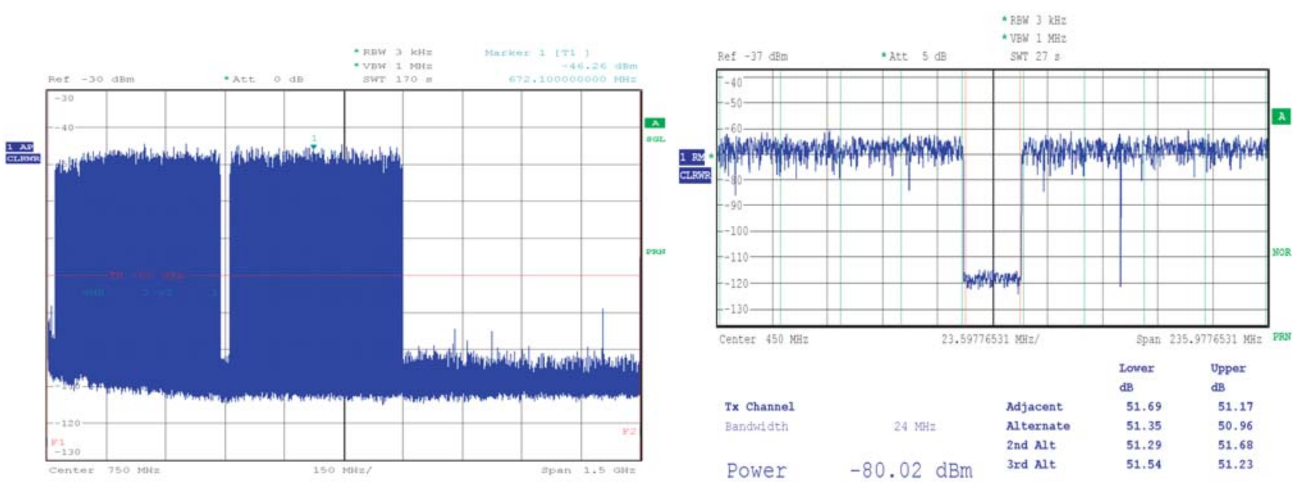
Figure 7-45. NPR in First Nyquist Zone, 20 MHz to 900 MHz Noise Pattern with a 25 MHz Notch Centered on 450 MHz, NRZ mode



Measured average NPR: 50.02 dB, therefore SNR = 61.02 dB and ENOB = 9.84 bit

Effects at low frequency are due to balun and pattern.

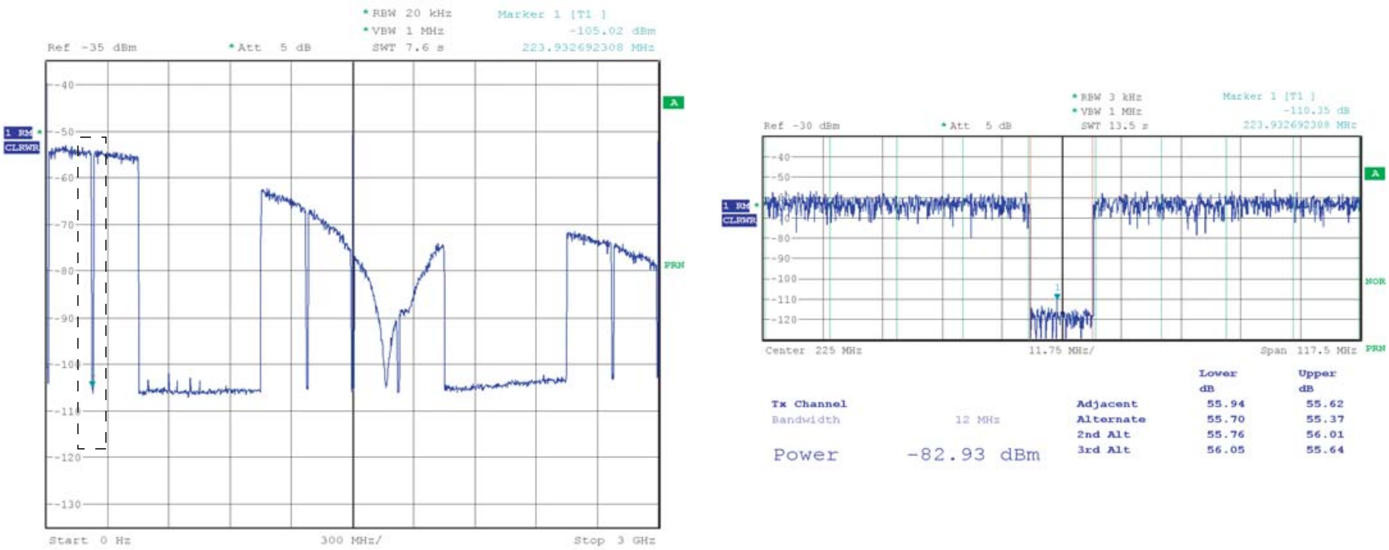
Figure 7-46. NPR in First Nyquist Zone, 20 MHz to 900 MHz Noise Pattern with a 25 MHz Notch Centered on 450 MHz, NRTZ Mode



Measured average NPR: 51.36 dB, therefore SNR = 62.36 dB and ENOB = 10.07 bit.

Effects at low frequency are due to balun and pattern.

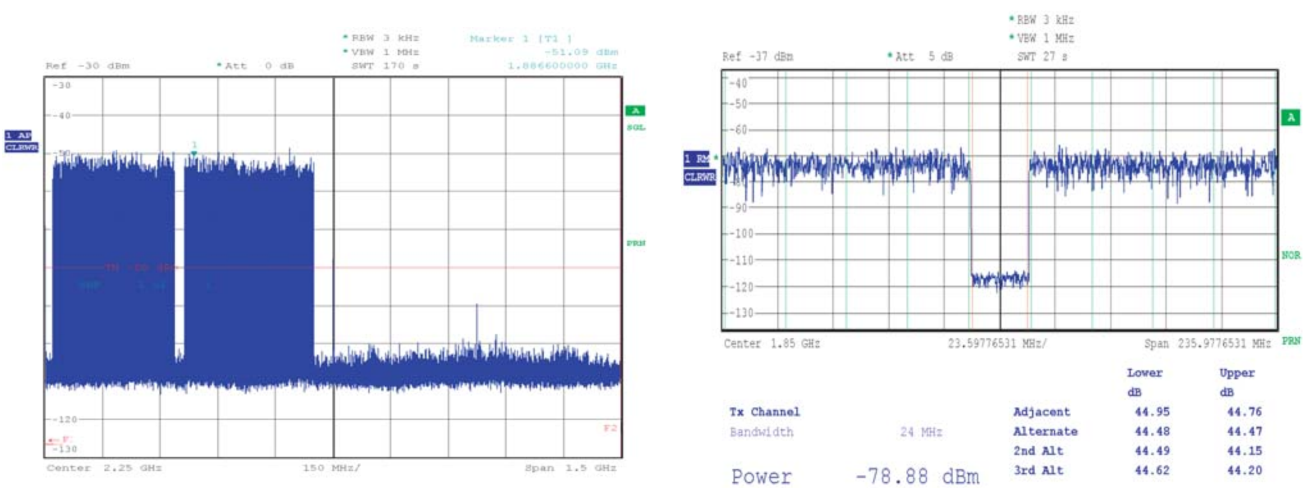
Figure 7-47. NPR in First Nyquist Zone, 10 MHz to 450 MHz Noise Pattern with a 12.5 MHz Notch centered on 225 MHz, NRTZ Mode at Fs = 1.5 GSpS



Measured average NPR: 55.7 dB, therefore SNR = 66.7 dB and ENOB = 10.8 bit.

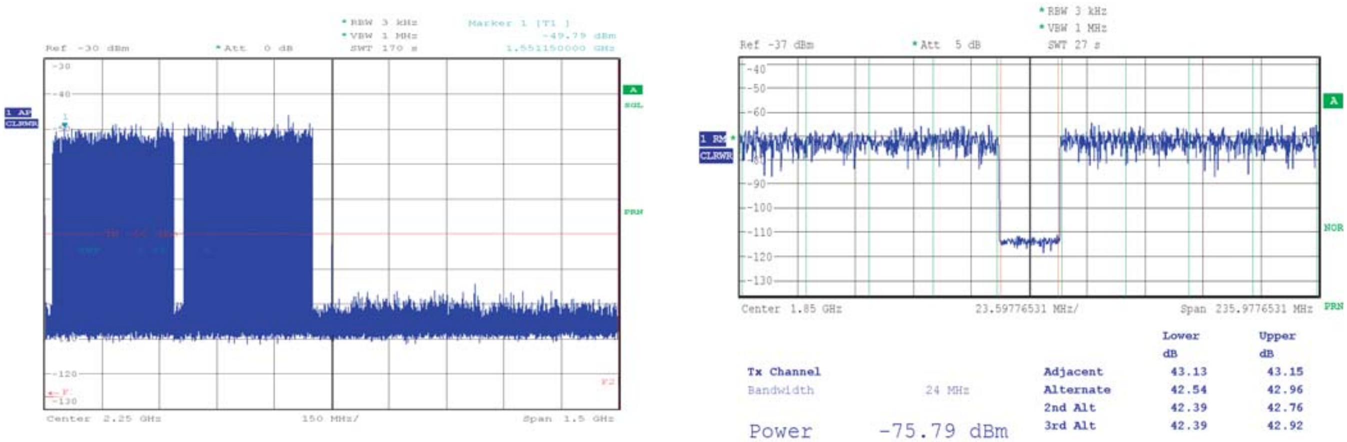
Effects at low frequency are due to balun and pattern.

Figure 7-48. NPR in second Nyquist Zone, 1520 MHz to 2200 MHz Noise Pattern with a 25 MHz Notch centered on 1850 MHz, RTZ mode



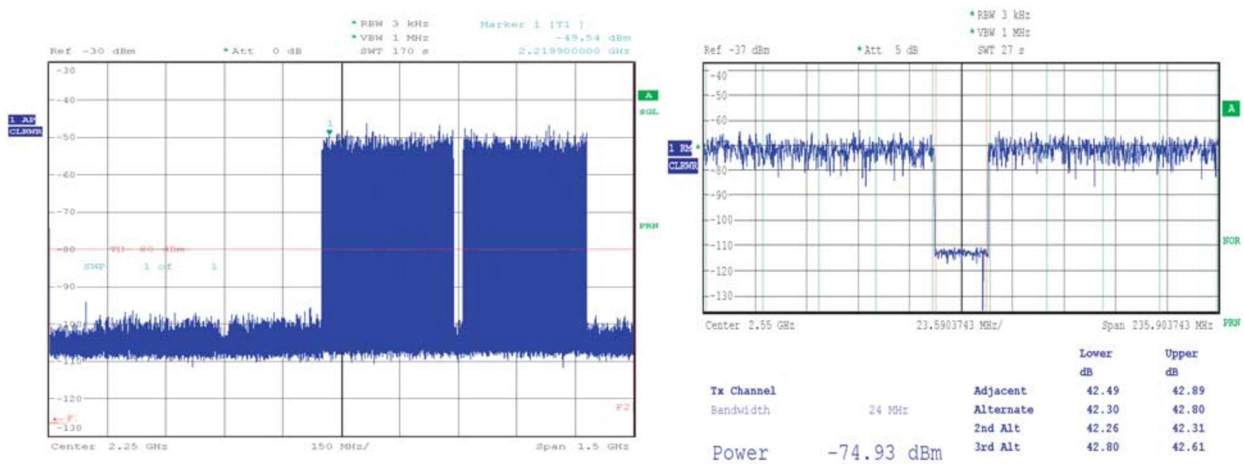
Measured average NPR: 44.6 dB, therefore SNR = 55.6 dB and ENOB = 8.94 bit

Figure 7-49. NPR in second Nyquist Zone, 1520 MHz to 2200 MHz noise pattern with a 25 MHz notch centered on 1850 MHz, RF Mode



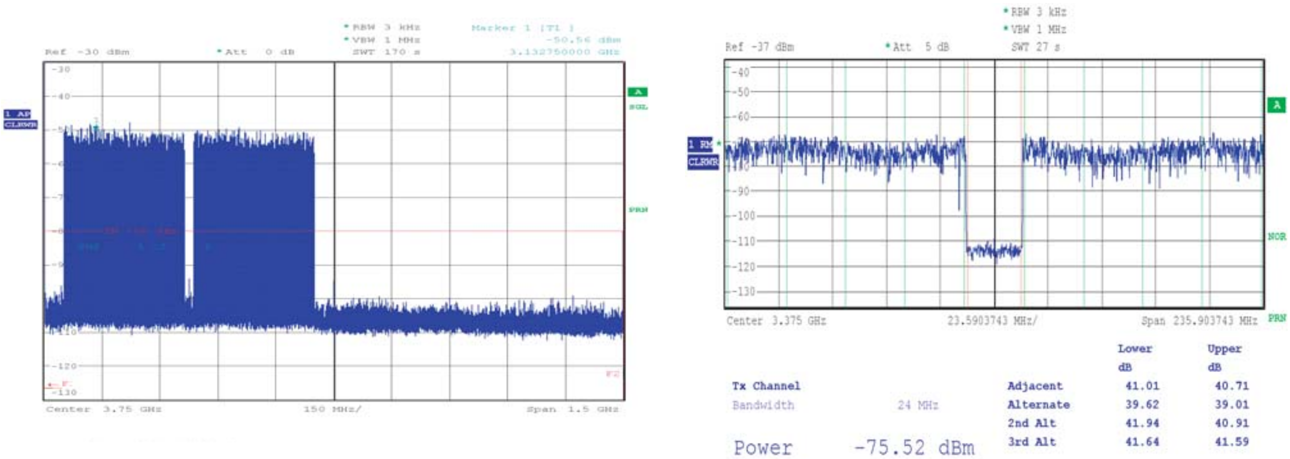
Measured average NPR: 42.78 dB, therefore SNR = 53.78 dB and ENOB = 8.64 bit

Figure 7-50. NPR in second Nyquist Zone, 2200 MHz to 2880 MHz Noise Pattern with a 25 MHz Notch centered on 2550 MHz, RF Mode



Measured average NPR: 42.56 dB, therefore SNR = 53.56 dB and ENOB = 8.6 bit.

Figure 7-51. NPR in Third Nyquist Zone, 3050 MHz to 3700 MHz Noise Pattern with a 25 MHz Notch Centered on 3375 MHz, RF Mode

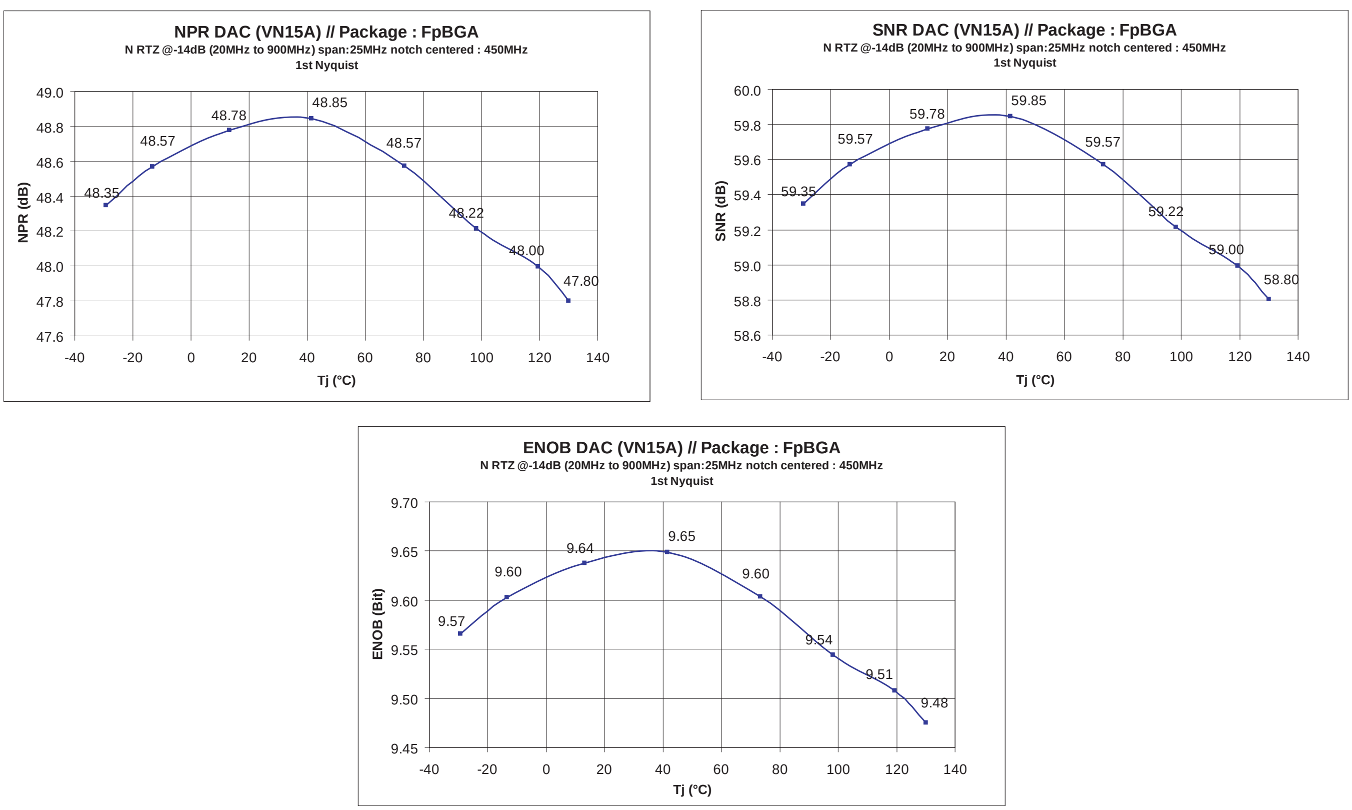


Measured average NPR: 40.08 dB, therefore SNR = 51.08 dB and ENOB = 8.19 bit

The following figures reflect the stability of NPR in first Nyquist in NRTZ mode (and therefore SNR and ENOB) versus temperature.

Measurements have been carried out at nominal power supply on an EV12DS130AZPY, at 3 GSps, with the FSU8 spectrum analyzer in RMS detection mode.

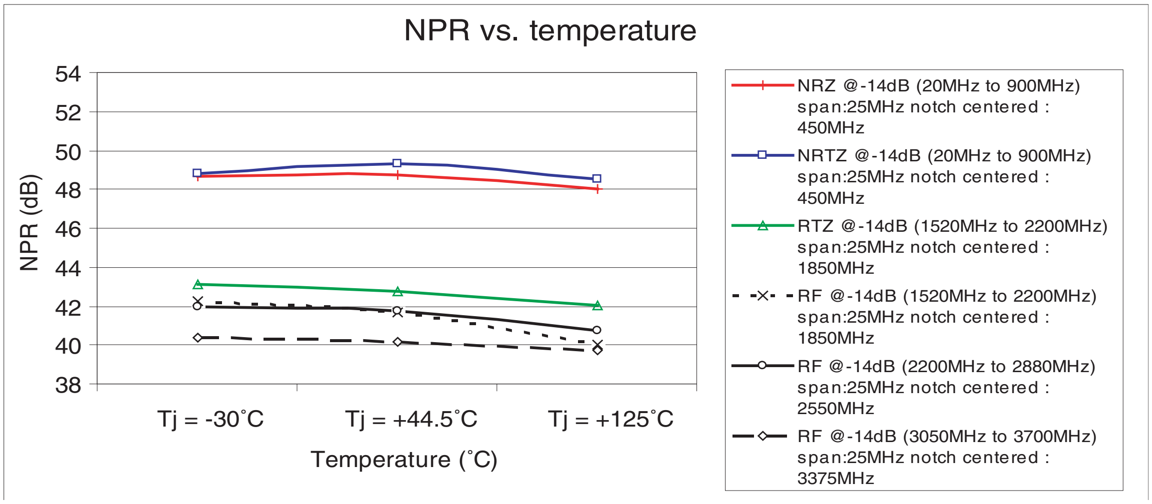
Figure 7-52. Drift of NPR and Associated SNR and ENOB in First Nyquist in NRTZ Mode from Tj = –30°C to Tj = 125°C



Optimum is at Tj = 40°C, degradation over temp is within 1 dB (or 0.15 effective bit).

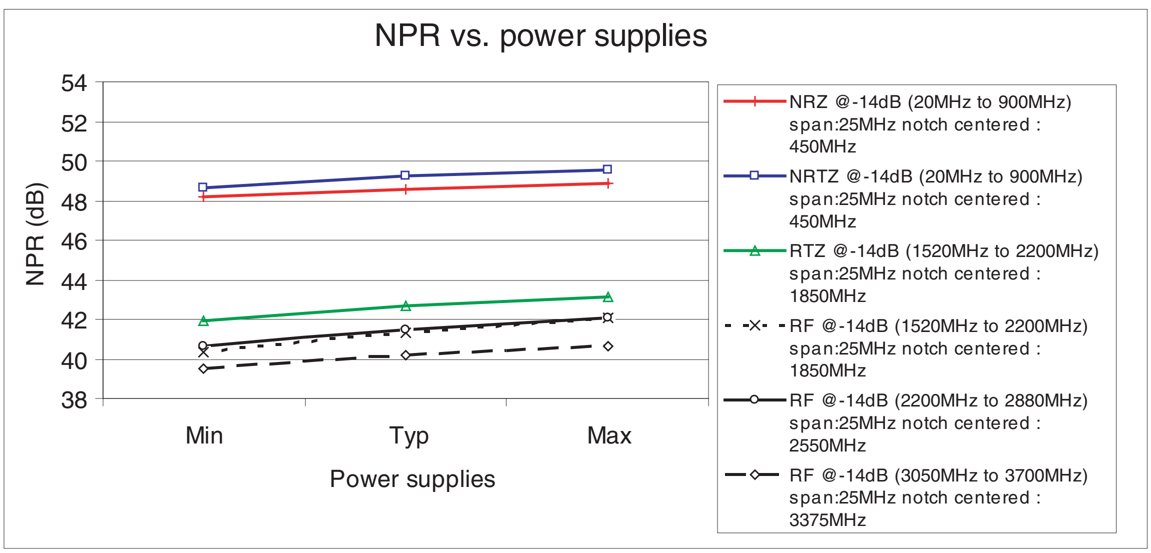
Measurements hereafter have been carried out on an EV12AS130AGS device at 3 GSps, with the FSU8 spectrum analyzer in RMS detection mode.

Figure 7-53. Drift of NPR vs temperature in the 4 Output Modes at Nominal Supply



Conclusion: performances are stable in the four output modes against temperature.

Figure 7-54. NPR vs Power Supply Level in the 4 Output Modes at Room Temperature



Conditions: Typical, excepted: power supplies

Min: V_{CCA}: 4.75V // $V_{CCA3} = V_{CCD} = 3.15V$

Typ: V_{CCA}: 5.0V // $V_{CCA3} = V_{CCD} = 3.3V$

Max: V_{CCA}: 5.25V // $V_{CCA3} = V_{CCD} = 3.45V$.

Conclusion: performances are fairly stable against power supply.

Note: NPR performance at lower clock frequencies is affected by power up sequence. See application note 1087 for further details.

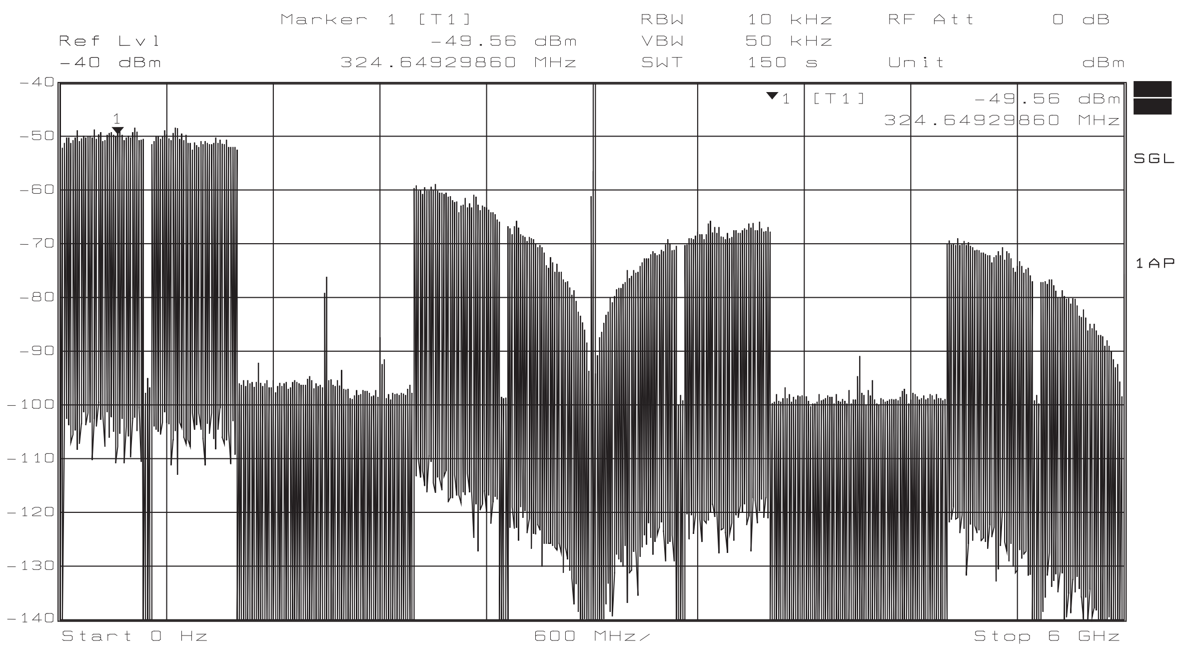
7.2.8 Spectrum over 4 Nyquist Zones in the Four Output Modes

Observation of a 1GHz broadband pattern with a 25 MHz notch centered on 500 MHz spectrum over 4 Nyquist zones at 3 GSps (that is from DC to 6 GHz), measurements performed on an EV12DS130AGS device (CI-CGA 255 package, with an overall 6 GHz bandwidth limitation).

By periodisation of a sampled system each tone F_i of the pattern in the 1st Nyquist zone is duplicated as follows:

- 2nd Nyquist Zone: tone at Fclock - F_i
- 3rd Nyquist Zone: tone at Fclock + F_i
- 4th Nyquist Zone: tone at 2*Fclock - F_i

Figure 7-55. Spectrum over 4 Nyquist Zones at 3 GSps in NRZ Output Mode



First Zero of the sinc() function is at Fclock.

Figure 7-56. Spectrum over 4 Nyquist Zones at 3 GSps in NRTZ Output Mode

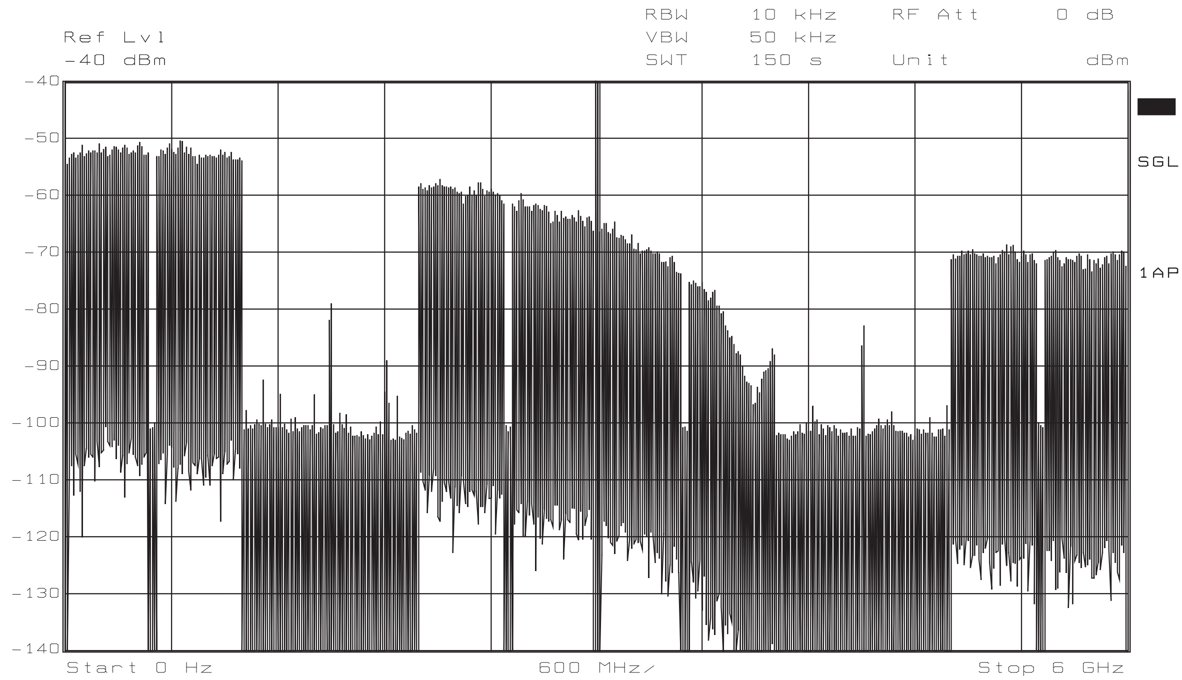
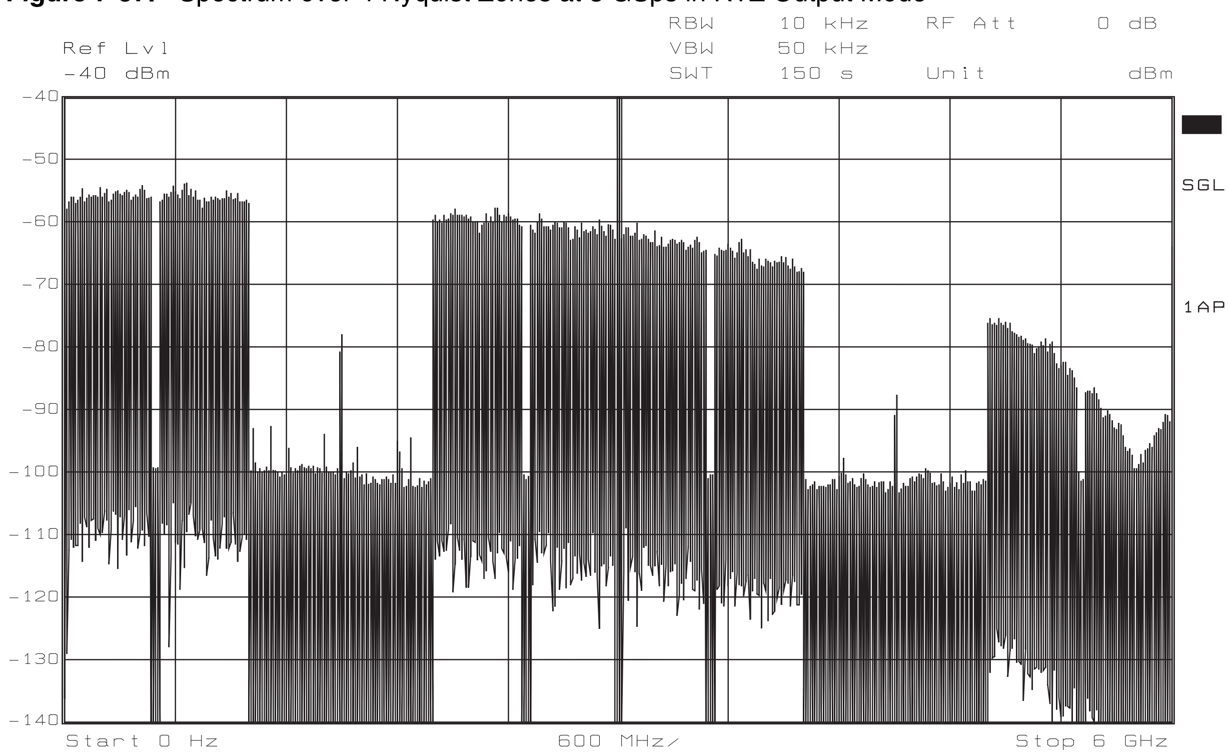
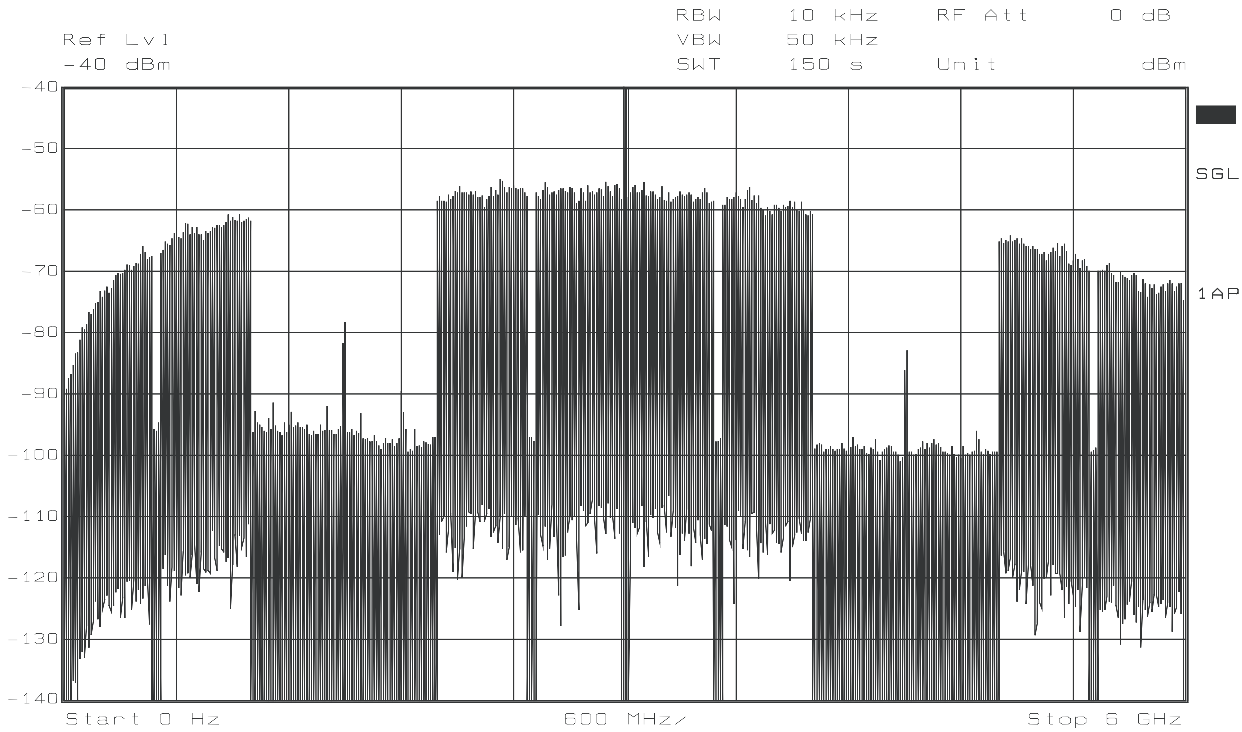


Figure 7-57. Spectrum over 4 Nyquist Zones at 3 GSps in RTZ Output Mode



First Zero of the sinc() function is slightly before 2*Fclock which indicates that the duty cycle of RTZ function is a little bit more than 50%, this is due to the balun which introduced some phase error beyond the 180 degrees between CLK and CLKN thus creating a duty cycle on the clock actually seen by the DAC.

Figure 7-58. Spectrum over 4 Nyquist Zones at 3 GSps in RF Output Mode



Measurements are showing a pretty good fit with theory, see Section 5.2 on page 16.

8. Application Information

For further details, please refer to application note 1087.

8.1 Analog Output (OUT/OUTN)

The analog output should be used in differential way as described in the figures below.

If the application requires a single-ended analog output, then a balun is necessary to generate a single-ended signal from the differential output of the DAC.

Figure 8-1. Analog Output Differential Termination

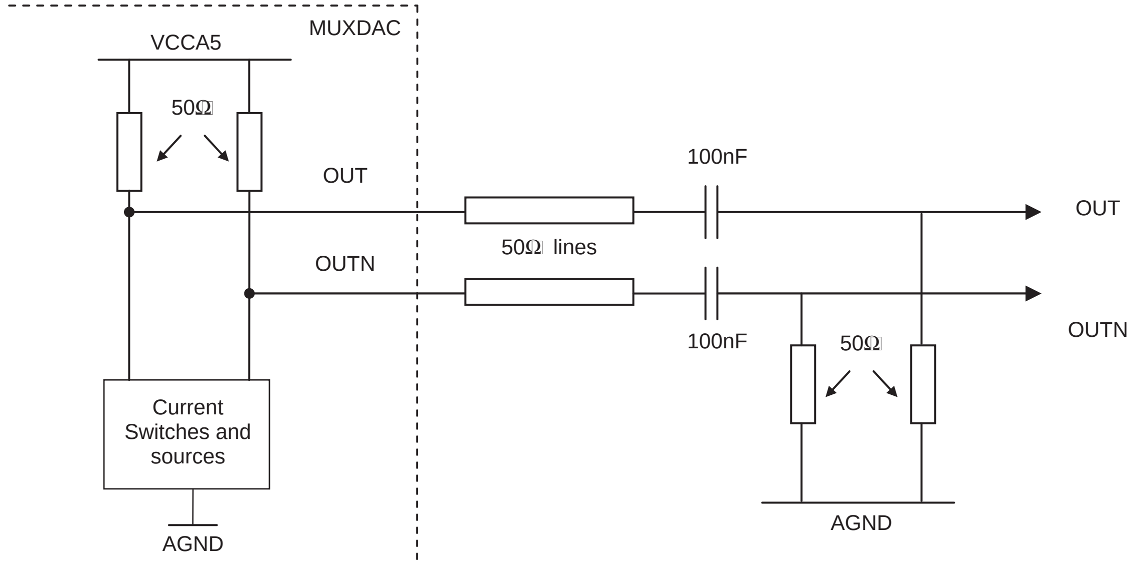
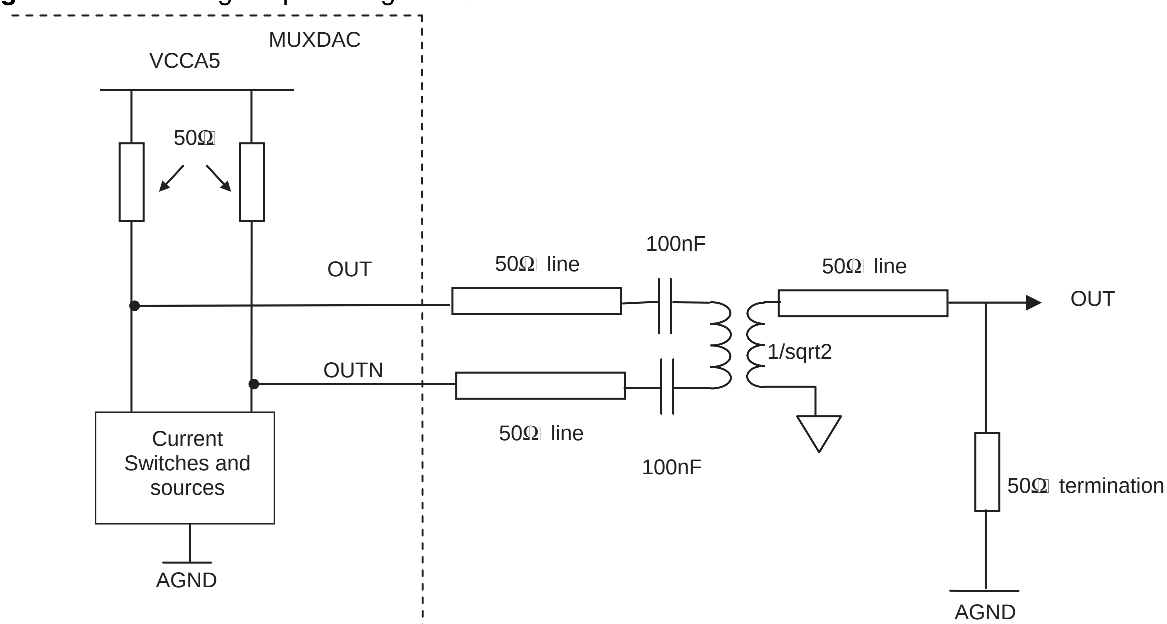


Figure 8-2. Analog Output Using a 1/ √2 Balun

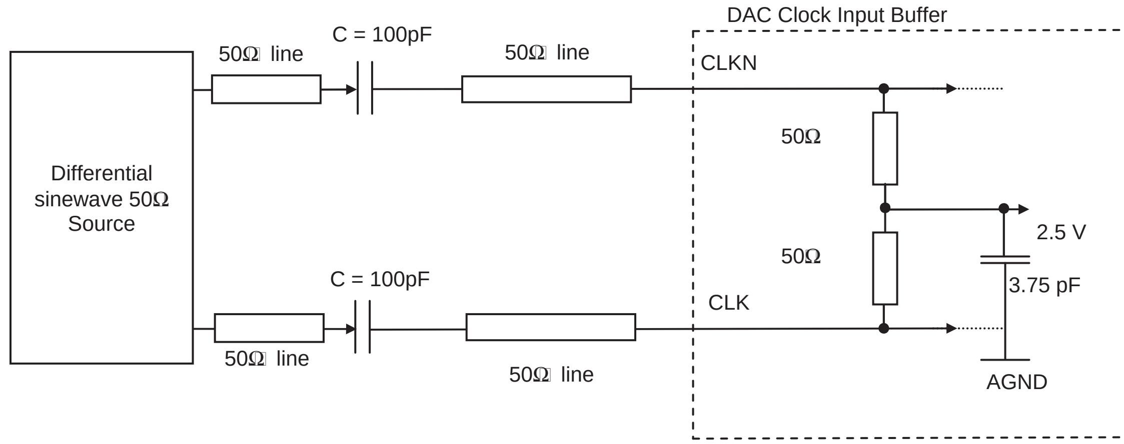


Note: The AC coupling capacitors should be chosen as broadband capacitors with a value depending on the application.

8.2 Clock Input (CLK/CLKN)

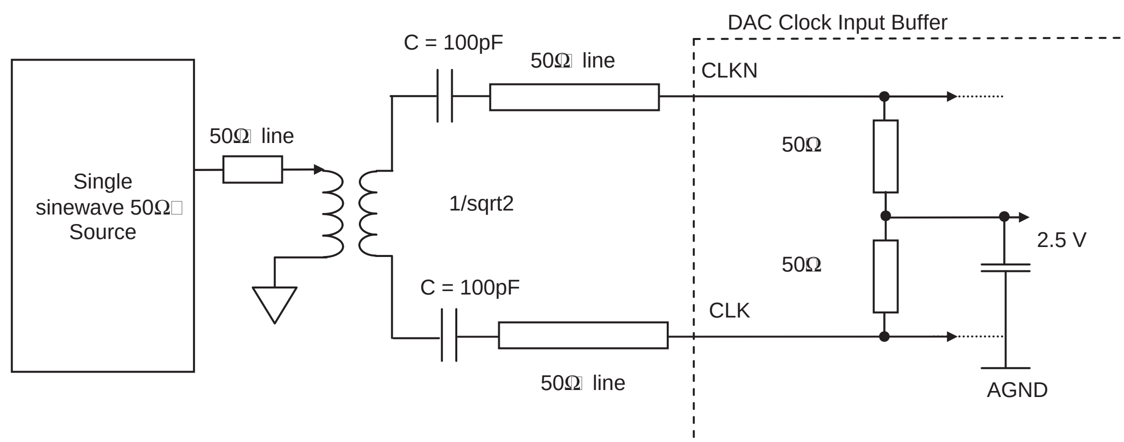
The DAC input clock (sampling clock) should be entered in differential mode as described in Figure 5-9 on page 21.

Figure 8-3. Clock Input Differential Termination



Note: The buffer is internally pre-polarized to 2.5V (buffer between V_{CC5} and AGND).

Figure 8-4. Clock Input Differential with Balun



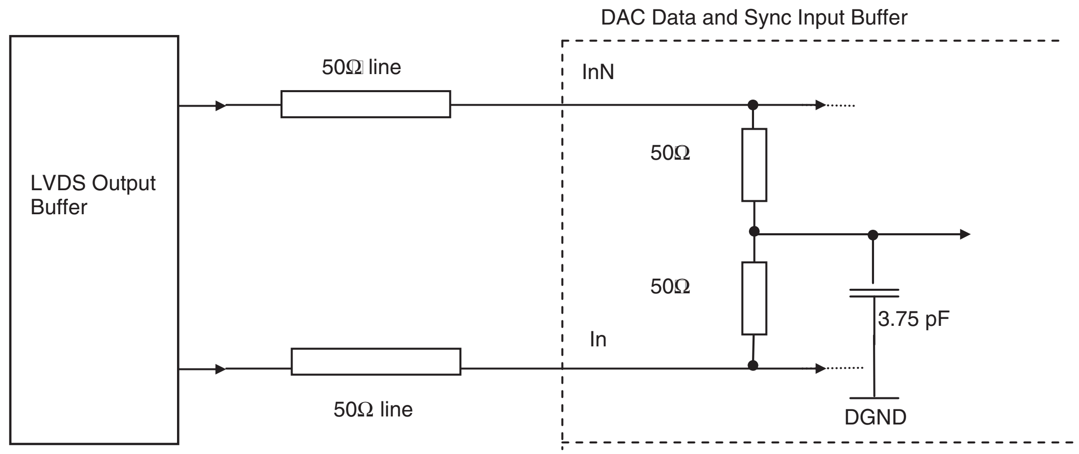
Note: The AC coupling capacitors should be chosen as broadband capacitors with a value depending on the application.

8.3 Digital Data, SYNC and IDC Inputs

LVDS buffers are used for the digital input data, the reset signal (active high) and IDC signal.

They are all internally terminated by 2 × 50Ω to ground via a 3.75 pF capacitor.

Figure 8-5. Digital Data, Reset and IDC Input Differential Termination



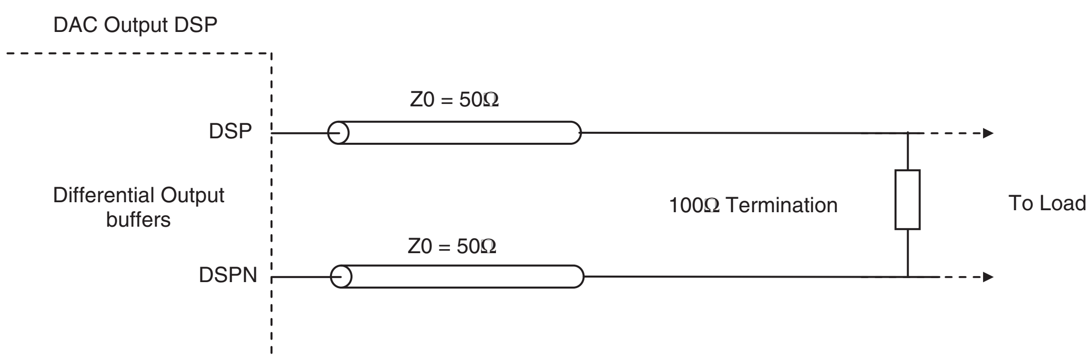
Notes:
1. In the case when only two ports are used (2:1 MUX ratio), then the unused data should be left open (no connect).
2. Data and IDC signals should be routed on board with the same layout rules and the same length than the data.
3. In the case, the SYNC is not used, it is necessary to bias the SYNC to 1.1V and SYNCN to 1.4V

8.4 DSP Clock

The DSP, DSPN output clock signals are LVDS compatible.

They have to be terminated via a differential 100Ω termination as described in Figure 5-11 on page 22.

Figure 8-6. DSP Output Differential Termination



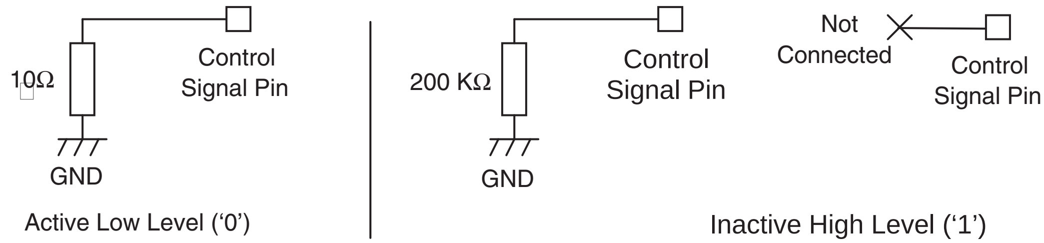
8.5 Control Signal Settings

The MUX, MODE, PSS and OCDS control signals use the same static input buffer.

Logic “1” = 200 KΩ to Ground, or tied to V_{CCD} = 3.3V or left open

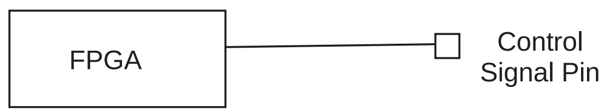
Logic “0” = 10Ω to Ground or Grounded

Figure 8-7. Control Signal Settings



The control signal can be driven by FPGA.

Figure 8-8. Control Signal Settings with FPGA



Logic “1” > V_{IH} or V_{CCD} = 3.3V

Logic “0” < V_{IL} or 0V

8.6 HTVF and STVF Control Signal

The HTVF and STVF control signals is a output 3.3V CMOS buffer.

These signals could be acquired by FPGA.

Figure 8-9. Control Signal Settings with FPGA

In order to modify the V_{OL}/V_{OH} value, pull up and pull down resistances could be used, or a potential divider.

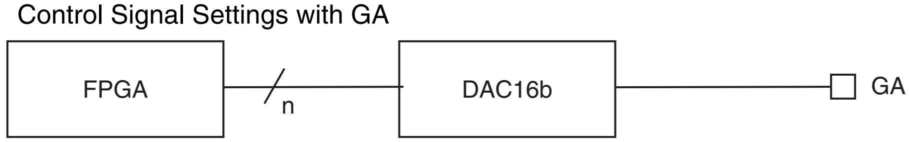
8.7 GA Function Signal

This function allows adjustment of the internal gain of the DAC.

The gain of the DAC can be tuned with applied analog voltage from 0 to V_{CCA3}

This analog input signal could be generated by a DAC control by FPGA or microcontroller.

Figure 8-10. Control Signal Settings with GA



8.8 Power Supplies Decoupling and Bypassing

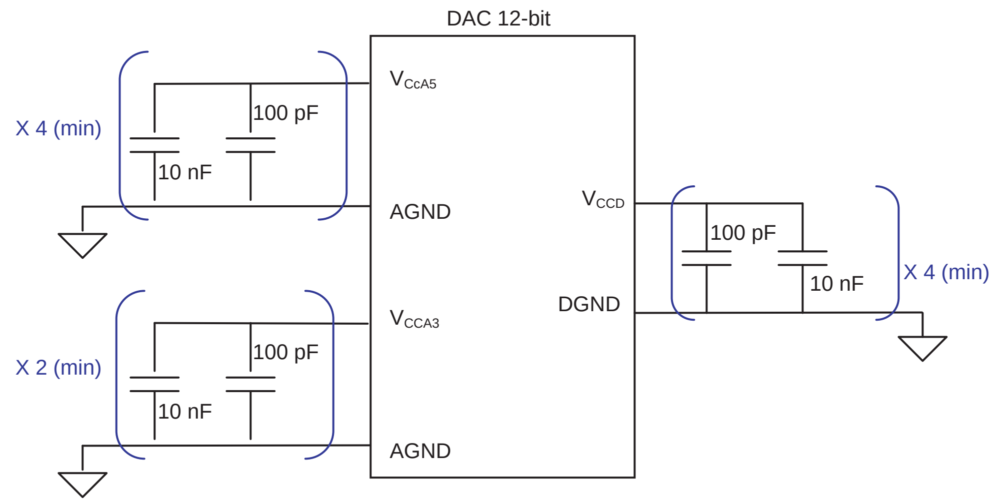
The DAC requires 3 distinct power supplies:

V_{CCA5} = 5.0V (for the analog core)
V_{CCA3} = 3.3V (for the analog part)
V_{CCD} = 3.3V (for the digital part)

It is recommended to decouple all power supplies to ground as close as possible to the device balls with 100 pF in parallel to 10nF capacitors. The minimum number of decoupling pairs of capacitors can be calculated as the minimum number of groups of neighbouring pins.

4 pairs of 100pF in parallel to 10 nF capacitors are required for the decoupling of V_{CCA5}. 4 pairs for the V_{CCA3} is the minimum required and finally, 10 pairs are necessary for V_{CCD}.

Figure 8-11. Power Supplies Decoupling Scheme



Each power supply has to be bypassed as close as possible to its source or access by 100 nF in parallel to 22 µF capacitors (value depending of DC/DC regulators).

Analog and digital ground plane should be merged.

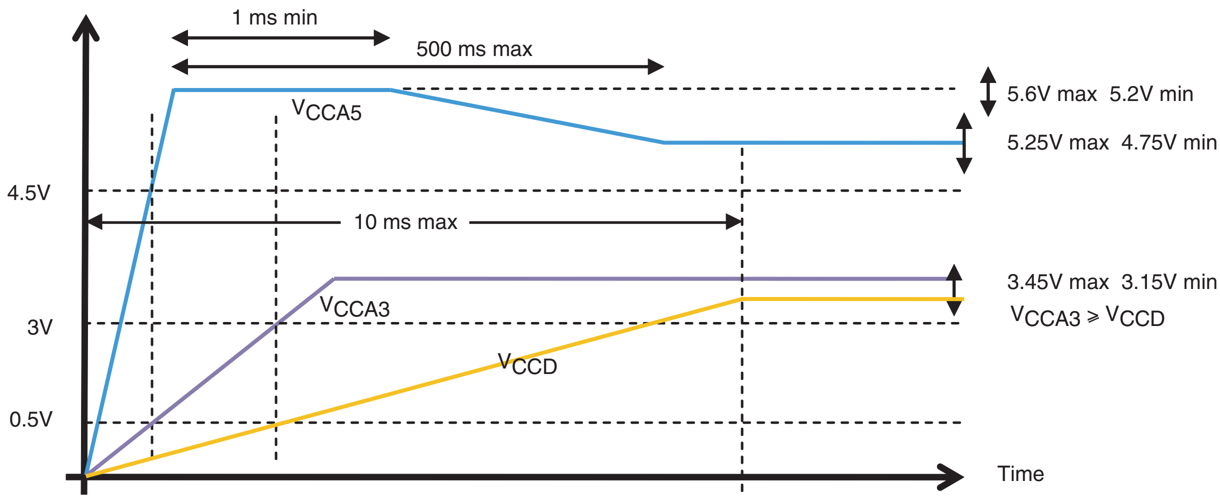
8.9 Power Up Sequencing

Power-up sequence:

It is necessary to raise V_{CCA5} power supply within the range 5.20V up to a recommended maximum of 5.60V during at least 1ms at power up. Then the supply voltage has to settle within 500 ms to a steady nominal supply voltage within a range of 4.75V up to 5.25V.

A power-up sequence on V_{CCA5} that does not comply with the above recommendation will not compromise the functional operation of the device. Only the noise floor will be affected.

Figure 8-12. Power-up Sequence



The rise time for any of the power supplies (V_{CCA5}, V_{CCA3} and V_{CCD}) shall be ≤ 10 ms.

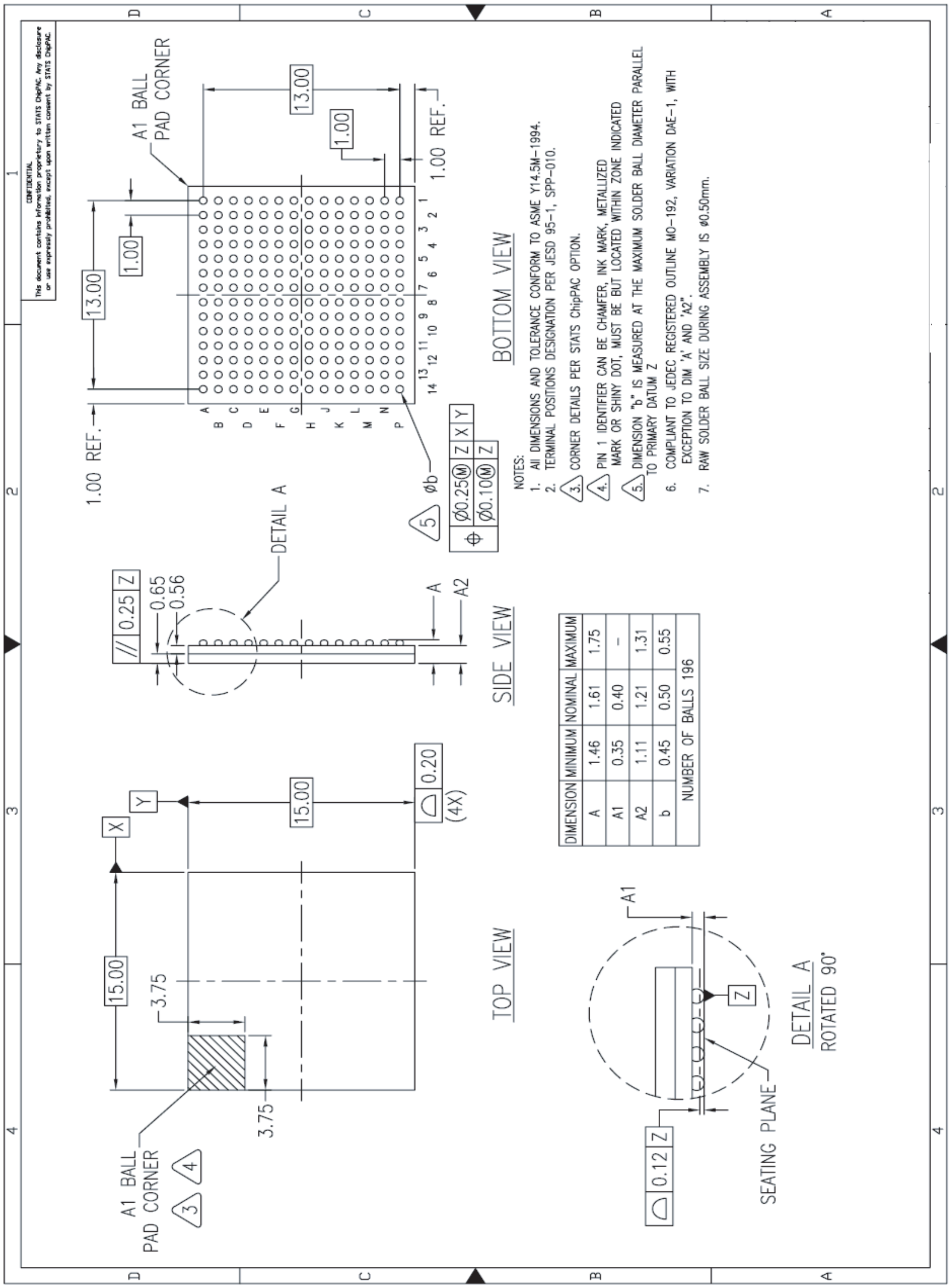
At power-up a SYNC pulse is internally and automatically generated when the following sequence is satisfied: V_{CCD}, V_{CCA3} and V_{CCA5}. To cancel the SYNC pulse at power-up, it is necessary to apply the sequence: V_{CCA5}, V_{CCA3}, V_{CCD}. (V_{CCA3} can not reach 0.5V until V_{CCA5} is greater than 4.5V. V_{CCD} can not reach 0.5V until V_{CCA3} is greater than 3.0V). Any other sequence may not have a deterministic SYNC behaviour. See erratasheet (ref 1125) for specific condition of use relative to the SYNC operation.

Relationship between power supplies:

Within the applicable power supplies range, the following relationship shall always be satisfied $V_{CCA3} \geq V_{CCD}$, taking into account AGND and DGND planes are merged and power supplies accuracy.

9. Package Information

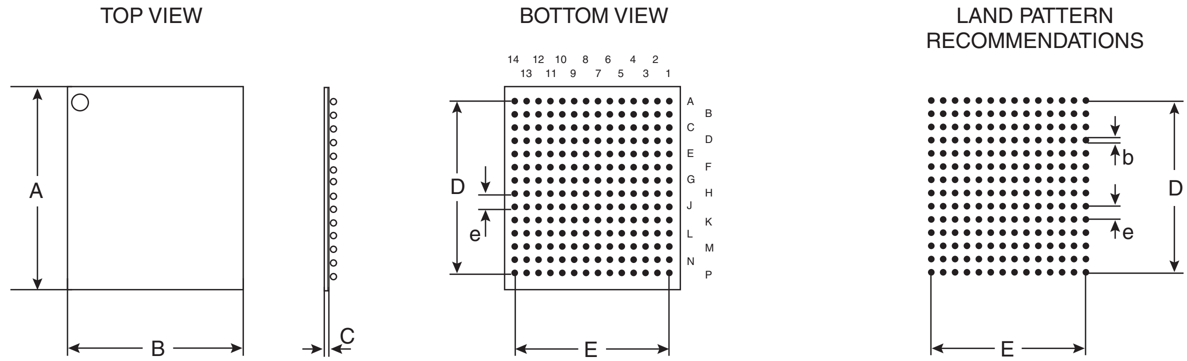
9.1 fpBGA 196 Outline



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	1.46	1.61	1.75
A1	0.35	0.40	–
A2	1.11	1.21	1.31
b	0.45	0.50	0.55
NUMBER OF BALLS 196			

9.2 Land Pattern Recommendation

Figure 9-1. Land Pattern Recommendation



A	B	C	D	E	e	b
15.00	15.00	1.21	13.00	13.00	1.00	0.45

10. Thermal Characteristics fpBGA196

10.1 Thermal Resistance

Assumptions:

Still air
Pure conduction
No radiation
Heating zone = 5% of die surface

Rth Junction – bottom of Balls = 13.3°C/W
Rth Junction – board (JEDEC JESD-51-8) = 17.8°C/W
Rth Junction – top of case = 14.5°C/W

Assumptions:

Heating zone = 5% of die surface
Still air, JEDEC condition
Rth Junction – ambient (JEDEC) = 32°C/W

11. Ordering Information

Table 11-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EVX12DS130AZPY	fpBGA196 RoHS	Ambient	Prototype	
EV12DS130ACZPY	fpBGA196 RoHS	0°C < Tc, Tj < 90°C	Commercial « C » Grade	
EV12DS130AVZPY	fpBGA196 RoHS	–40°C < Tc, Tj < 110°C	Industrial « V » Grade	
EV12DS130AZPY-EB	fpBGA196 RoHS	Ambient	Prototype	Evaluation board
EVX12DS130AZP	fpBGA196	Ambient	Prototype	Contact sales for availability

12. Revision History

This table provides revision history for this document.

Table 12-1. Revision History

Rev. No	Date	Substantive Change(s)
1077E	December 2013	Table 3-3, “Electrical Characteristics,” on page 5: typo error on note 7: $V_{CCA3} \geq V_{CCD}$
1077D	December 2013	Table 3-2, “Recommended Conditions of Use,” on page 4: typo error on note 2: $V_{CCA3} \geq V_{CCD}$
1077C	November 2013	Typo errors corrections OCDS restrictions to OCDS1 & 2 HTVF STVF flag application clarifications Power sequencing modification, relative to SYNC operation
1077B	July 2012	Typo errors corrections Absolute max rating clarifications Addition of pin equivalent schematic description Power up sequencing recommendation
1077A	February 2012	Initial revision

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