EV12DS400AMZP
Military Grade
Low power 12-bit 4.5GSps Digital to Analog Converter with 4/2:1 Multiplexer
Datasheet DS1163

MAIN FEATURES

- 12-bit resolution
- 4.5 GSps guaranteed conversion rate
- –3dB Analog output Bandwidth of 7 GHz
- 4:1 or 2:1 integrated parallel MUX (selectable)
- Selectable output modes:
  Return to Zero (RTZ), Non Return to Zero (NRZ), Narrow Return To Zero (NRTZ) and Radio Frequency (RF)
- Low latency time
- 2.6 Watt Power Dissipation (in 4:1 MUX)
- 3 Wires Serial Interface
- Functions:
  - Selectable MUX ratio 4:1 (up to 4.5 GSps), 2:1 (up to 3.2 GSps)
  - User-friendly functions, digitally controlled through a 3WSI serial interface:

    Gain Adjustment

    Output clock division selection (possibility to change the division ratio of the DSP clock) (OCDS)

    Reshaped Pulse Width (RPW) and Reshaped Pulse Begin (RPB) adjustments for performance optimization

    Clock phase shift select for synchronization with DSP (PSS[2:0])

    Input Under Clocking Mode by 1/2/4 (IUCM)

    Direct access available for bit OCDS and PSS

  - Input data check bit for timing interface with FPGA check (IDC)
  - Timing violation flags (setup or hold) for FPGA communication monitoring (TVF)
  - Diode for die junction temperature monitoring
- LVDS differential data input and DSP clock output.
- Analog output differential swing: 1Vpp (100Ω differential impedance)
- Power on reset
- External reset that can be used for synchronization of multiple DACs
- Power supplies: 3.3 V (Digital), 3.3V & 5V (Analog)
- FpBGA package (15 x 15 mm body size, 1 mm pitch)

PERFORMANCES

Broadband: NPR at –14 dBFS Loading Factor (90% of full Nyquist zone),

1st Nyquist (NRTZ): NPR = 47.5 dB, 9.4 Bit Equivalent at Fs = 4.5 GSps

2nd Nyquist (NRTZ): NPR = 42 dB, 8.5 Bit Equivalent at Fs = 4.5 GSps

3rd Nyquist (RF): NPR = 39 dB, 8 Bit Equivalent at Fs = 4.5 GSps

DOCSIS 3.0 Compatible

Whilst e2v technologies has taken care to ensure the accuracy of the information contained herein it accepts no responsibility for the consequences of any use thereof and also reserves the right to change the specification of goods without notice. e2v technologies accepts no liability beyond the set out in its standard conditions of sale in respect of infringement of third party patents arising from the use of devices in accordance with information contained herein.

e2v technologies (uk) limited, Waterhouse Lane, Chelmsford, Essex CM1 2QU United Kingdom Holding Company: e2v technologies plc

Telephone: +44 (0)1245 493493 Facsimile: +44 (0)1245 492492

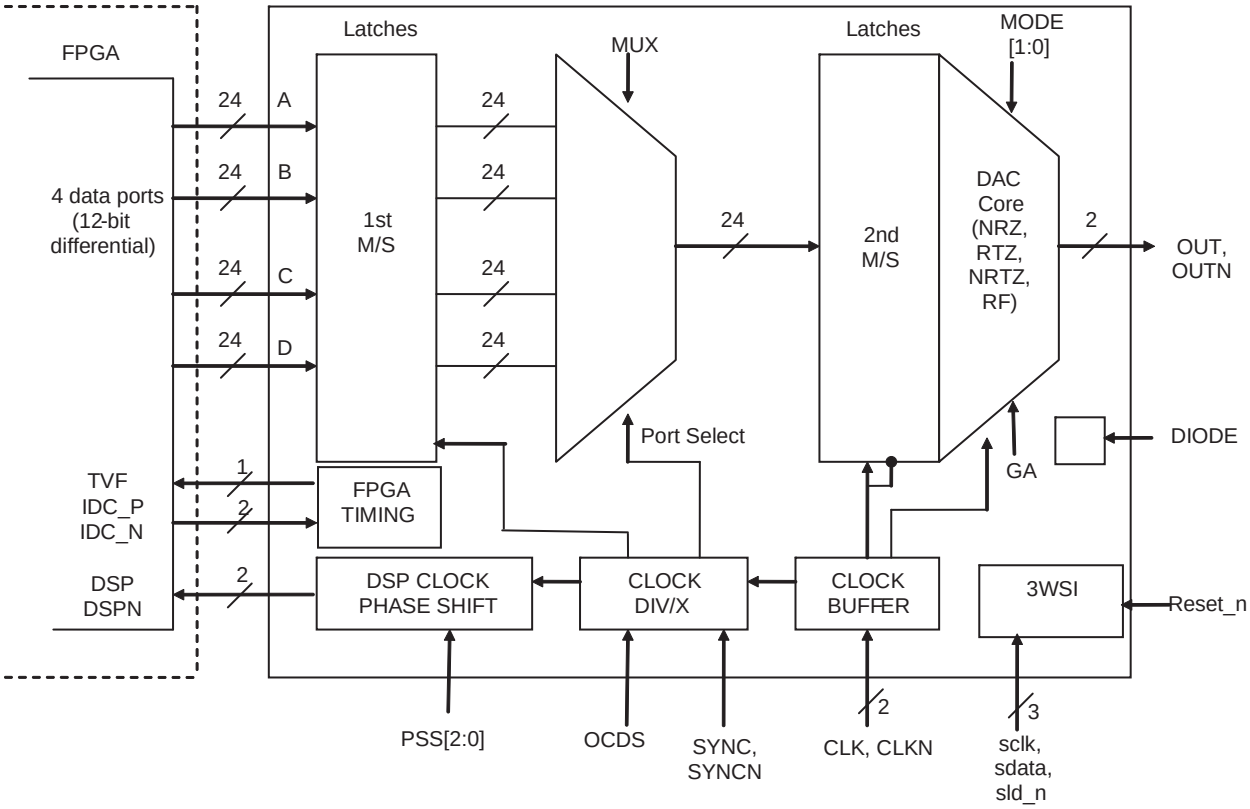
Contact e2v by e-mail: enquiries@e2v.com or visit www.e2v.com for global sales and operations centres.

1163B–BDC–03/16

© e2v technologies (uk) limited 2016

1. BLOCK DIAGRAM

Figure 1-1. Simplified block diagram



2. DESCRIPTION

The EV12DS400A is a 12-bit 4.5 GSps DAC with an integrated 4:1 or 2:1 multiplexer and 7 GHz output bandwidth, allowing easy interface with standard FPGAs thanks to user friendly features such as DSP clock, OCDS, PSS, TVF.

It embeds 4 different output modes (NRZ, RTZ, NRTZ and RF) that allow performance optimizations depending on the Nyquist zone of interest.

© e2v technologies (uk) limited 2016

3. ELECTRICAL CHARACTERISTICS

3.1 Absolute Maximum ratings

Table 3-1. Absolute maximum ratings

Parameter	Symbol	Value		Unit
		min	max	
V_{CCA5} analog supply voltage	V_{CCA5}	–0.6	6.0	V
V_{CCA3} analog supply voltage	V_{CCA3}	–0.6	4.0	V
V_{CCD} digital supply voltage	V_{CCD}	–0.6	4.0	V
Digital input (on each single-ended input), IDC and SYNC signal	$[P_0..P_{11}]$, $[P_{0N}..P_{11N}]$, IDC_P, IDC_N, SYNC, SYNCN	0	V_{CCA3}	V
Digital input maximum differential swing Port P = A, B, C, D			2.0	Vpp
Master clock input (on each single ended input)	CLK, CLKN	1.0	4.0	V
Master clock maximum differential swing			3	Vpp
Control function inputs voltage	PSS[0..2], OCDS, reset_n, sclk, sdata, sld_n	–0.4	V_{CCD} + 0.4	V
Junction temperature	T_J		170	°C

Parameter	Symbol	Value	Unit
Electrostatic discharge human body model	ESD HBM	JESD22-A114-E Class 1C (1000V to < 2000V)	V
Electrostatic discharge machine model	ESD MM	JESD22-A115-C Class M2 (100V to < 200V)	
Latch up		JEDEC 78B Class I & Class II	
Moisture sensitivity level	MSL	3	
Storage temperature range	Tstg	–65 to +150	°C

Notes:
1. Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
2. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performances degradation to complete failure.
3. Maximum ratings enable active inputs with DAC powered off.
4. Maximum ratings enable floating inputs with DAC powered on.
5. DSP clock and TVF output buffers must not be shorted to ground or positive power supply.

© e2v technologies (uk) limited 2016

3.2 Recommended conditions of use

Table 3-2. Recommended conditions of use

Parameter	Symbol	Recommended Value	Unit	Note
V_{CCA5} analog supply voltage	V_{CCA5}	5.0	V	(1)(2)
V_{CCA3} analog supply voltage	V_{CCA3}	3.3	V	(1)(2)
V_{CCD} digital supply voltage	V_{CCD}	3.3	V	(1)(2)
Digital input (on each single ended input), IDC and SYNC signal Port P = A, B, C, D V_{IL} V_{IH} Digital input differential swing	$[P_0..P_{11}]$, $[P_{0N}..P1_{1N}]$, IDC_P, IDC_N, SYNC, SYNCN	 1.075 1.425 350	 V V mVp	
Master Clock input differential mode swing	CLK, CLKN	1.4	Vpp	
Master Clock input power level (differential mode)	P_{CLK}	4	dBm	(3)
Control function inputs V_{IL} V_{IH}	PSS[0..2], OCDS, reset_n, sclk, sdata, sld_n	 0 V_{CCD}	 V V	
RPB & RPW settings for enhanced dynamic performance 4.5 GSps in NRTZ mode	RPB RPW	RPB1 RPW1	– –	(4)
RPB settings for enhanced dynamic performance 4.5 GSps in RTZ mode	RPB	RPB1	– –	(4)
RPB & RPW settings for enhanced dynamic performance 4.5 GSps in RF mode	RPB RPW	RPB3 RPW0	– –	(4)

Notes:
1. See Section 8.8 on page 69 for power on requirement
2. No power-down sequencing is required
3. Clock input power can be decreased when clock frequency is lower as long as it respects the specification.
4. A good compromise for RPB & RPW values is defined for a 4.5GHz clock frequency. This couple of values depends on the clock frequency.

© e2v technologies (uk) limited 2016

3.3 DC Electrical Characteristics

Unless otherwise specified:
Values in the table below are given over temperature range with typical power supplies (V_{CCA5} = 5V, V_{CCA3} = 3.3V, V_{CCD} = 3.3V), with 4:1 MUX ratio, typical swing on input data, typical Pclk, master clock input jitter is below 100 Fs rms integrated over 5GHz bandwidth.

Min and Max values are given over temperature range.
Typ values are given at ambient temperature.

Table 3-3. DC Electrical characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
RESOLUTION			12		bit		
POWER REQUIREMENTS							
Power Supply voltage - Analog - Analog - Digital	 V_{CCA5} V_{CCA3} V_{CCD}	 4.75 3.15 3.15	 5 3.3 3.3	 5.25 3.45 3.45	 V V V	(2)	1, 6
Power Supply current (4:1 MUX) - Analog - Analog - Digital	 I_{CCA5} I_{CCA3} I_{CCD}	 85 165 340	 100 205 425	 120 240 490	 mA mA mA	(8)	1, 6
Power Supply current (2:1 MUX) - Analog - Analog - Digital	 I_{CCA5} I_{CCA3} I_{CCD}	 85 165 300	 100 205 370	 120 240 430	 mA mA mA	(8)	1, 6
Power dissipation (4:1 MUX)	PD4	2.2	2.6	3	W	(8)	1, 6
Power dissipation (2:1 MUX)	PD2	2.0	2.4	2.8	W	(8)	1, 6
DIGITAL DATA INPUTS, SYNC and IDC INPUTS							
Logic compatibility			LVDS				
Digital input voltages: - Differential input voltage - Common mode	 VID VICM	 100 1	 350 1.25	 500 1.6	 mVp V		 1, 6 1, 6
Input capacitance from each single input to ground				2	pF		5
Differential input resistance		80	100	120	Ω		1, 6
CLOCK INPUTS							
Input voltages (Differential operation swing)		0.6	1.4	2.4	Vpp		1, 6
Power level (Differential operation)		–4	4	+8.5	dBm	(3)	1, 6
Common mode		2.4	2.5	2.6	V		1, 6
Input capacitance from each single input to ground (at die level)				2	pF		5
Differential Input resistance:		80	100	120	Ω		1, 6

© e2v technologies (uk) limited 2016

Table 3-3. DC Electrical characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level[1]
DSP CLOCK OUTPUT							
Logic compatibility			LVDS				
Output voltages: - Differential output voltage - Common mode	 VOD VOCM	 100 1.055	 350 1.250	 450 1.375	 mVp V	(10)	 1, 6 1, 6
ANALOG OUTPUT							
Full-scale Differential output voltage (100Ω differentially terminated)		0.89	1	1.08	Vpp		1, 6
Full-scale output power (differential output on 100Ω)			+1		dBm	(4)	1, 6
Single-ended mid-scale output voltage (50Ω terminated)		V_{CCA5}–0.5	V_{CCA5}–0.43	V_{CCA5}–0.36	V	(5)	1, 6
Output capacitance			1.5		pF		5
Nominal Output internal differential resistance		90	100	110	Ω		1, 6
Output VSWR (using e2v's evaluation board) 2.25 GHz 4.5 GHz 6 GHz			 1.2 1.4 1.7				4
–3dB Analog Output bandwidth			7		GHz		4
FUNCTIONS							
Digital functions: sdata, sld_n, sclk, reset_n, OCDS, PSS - Logic 0 - Logic 1	 VIL VIH	 1.6	 0 V_{CCD}	 0.8 	 V V		1, 6
sdata, sld_n, sclk, reset_n - Low Level input current - High Level input current	 IIL IIH	 –120 10	 –55 80	 –10 120	 µA µA		1, 6
OCDS, PSS: - Low Level input current - High Level input current	 IIL IIH	 –150 50	 –100 100	 –50 150	 µA µA		1, 6
Digital output function TVF - Logic 0 - Logic 1	VOL VOH	 1.5		0.6	V V	(8)	1, 6
	IOL IOH			500 500	µA µA		5
DC ACCURACY							
Differential Non-Linearity	DNL+		0.4	0.95	LSB		1, 6
Differential Non-Linearity	DNL-	–0.95	–0.4		LSB		1, 6
Integral Non-Linearity	INL+		0.7	2.5	LSB		1, 6
Integral Non-Linearity	INL-	–2.5	–0.7		LSB		1, 6

© e2v technologies (uk) limited 2016

Table 3-3. DC Electrical characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
DC GAIN							
DAC output voltage (@default value) at ambient temperature		0.89		1.08	Vpp	(6)	1, 6
DAC output voltage adjustment step		–5	0.3	+5	mV		1
DAC output voltage after optimum 3WSI adjustment		0.995	1	1.005	Vpp	(6)	1
DAC output voltage sensitivity to supplies			3.2	5	%	(7)	1
DAC output voltage drift over temperature			55	65	mVpp	(9)	4

Notes:
1. See Section 3.6 on page 17 for explanation of test levels.
2. See Section 8.8 on page 69 for power up sequencing.
3. For use in higher Nyquist zone, it is recommended to use higher power clock within the limit.
4. In NRZ mode only. For the other reshaped modes, the output power will be lower by construction.
5. Single-ended operation is not recommended, this line is given for better understanding of what is output by the DAC.
6. The DAC output voltage can be adjusted close to 1Vpp thanks to the GAIN control register in the 3WSI.
7. DAC output voltage sensitivity to supplies = DAC output voltage at Vmax - DAC output at Vmin. Measurement done with DAC Gain Adjust at its default value (3WSI GA register default value = 0x200)
   Min and Max values are given versus supplies at room temperature
8. Tested with IOL & IOH=500µA
9. DAC output voltage sensitivity to temperature = DAC output voltage at Tmax - DAC output voltage at Tmin.
   Measurement done with DAC Gain Adjust at its default value (3WSI GA register default value = 0x200)
   Min and Max values are given versus temperature with typical supplies
10. It has been noted that at extreme low temperature and/or V_{CCD} min, Common Mode and swing of the DSP clock signal are reduced.
    However it stays above the values generally specified for LVDS input swing and Common Mode and thus should not be an issue at the system level.

3.4 AC Electrical Characteristics

Unless otherwise specified:
Values in the table below are given over temperature range with typical power supplies (V_{CCA5} = 5V, V_{CCA3} = 3.3V, V_{CCD} = 3.3V), with 4:1 MUX ratio, typical swing on input data, typical Pclk, master clock input jitter is below 100 Fs rms integrated over 5GHz bandwidth.

Min and Max values are given over temperature range.
Typ values are given at ambient temperature.

Important note on expected performances:

Figures for performances in NRTZ and RF modes are given for recommended value of RPW (Reshaping Pulse Width). Tuning of RPW by customer is recommended. Increasing RPW improves signal purity (SFDR) at the expense of noise floor (SNR). Decreasing RPW improves noise floor (SNR) at the expense of signal purity (SFDR).

Figures for performance in RTZ, NRTZ and RF modes are given for recommended value of RPB (Reshaping Pulse Begin) which are digitally programmable through the 3 Wires Serial Interface (3WSI).

© e2v technologies (uk) limited 2016

See Section 5.3 on page 25 for more information on RPW and RPB settings. Recommended values for RPB and RPW are given in Table 3-2..

Table 3-4. AC Electrical Characteristics NRZ Mode (First Nyquist Zone)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
Single-tone Spurious Free Dynamic Range							
4:1 MUX							
Fs = 4.5 GSps @ Fout = 45 MHz 0dBFS	|SFDR|		66		dBc	(2)(3)	4
Fs = 4.5 GSps @ Fout = 2205 MHz 0dBFS			51				4
Fs = 3.0 GSps @ Fout = 30 MHz 0dBFS		64	71				1, 6
Fs = 3.0 GSps @ Fout = 1470 MHz 0dBFS		51	58				1, 6
2:1 MUX							
Fs = 3.2 GSps @ Fout = 32 MHz 0dBFS	|SFDR|		70		dBc	(2)(3)	4
Fs = 3.2 GSps @ Fout = 1568 MHz 0dBFS			55				4
Fs = 1.5GSps @ Fout = 15 MHz 0dBFS		65	75				1, 6
Fs = 1.5GSps @ Fout = 735 MHz 0dBFS		57	64				1, 6
Highest spur level							
4:1 MUX							
Fs = 4.5 GSps @ Fout = 45 MHz 0dBFS			–66		dBm		4
Fs = 4.5 GSps @ Fout = 2205 MHz 0dBFS			–56				4
Fs = 3.0 GSps @ Fout = 30 MHz 0dBFS			–70				1, 6
Fs = 3.0 GSps @ Fout = 1470 MHz 0dBFS			–61				1, 6
2:1 MUX							
Fs = 3.2 GSps @ Fout = 32 MHz 0dBFS			–70		dBm		4
Fs = 3.2 GSps @ Fout = 1568 MHz 0dBFS			–60				4
Fs = 1.5 GSps @ Fout = 15 MHz 0dBFS			–74				1, 6
Fs = 1.5 GSps @ Fout = 735 MHz 0dBFS			–66				1, 6
Signal independent Spur (clock-related spur) with 4:1 MUX							
Fc/2 @4.5 GSps			–90		dBm		4
Fc/4 @4.5 GSps			–90		dBm		4
Self-Noise Density at code 0 or 4095 @4.5 GSps			–160		dBm/Hz		4
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 4.5 GSps 2 GHz broadband pattern, 25 MHz notch width	NPR		43		dB	(4)(5)	4
Equivalent ENOB (Computed from NPR figure)	ENOB		8.7		Bit		4
Signal to Noise Ratio (Computed from NPR figure)	SNR		54		dB		4

© e2v technologies (uk) limited 2016

Table 3-4. AC Electrical Characteristics NRZ Mode (First Nyquist Zone) (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 3 GSps 1.33 GHz broadband pattern, 17 MHz notch width	NPR	43	46		dB		1, 6
Equivalent ENOB (Computed from NPR figure)	ENOB	8.7	9.2		Bit		1, 6
Signal to Noise Ratio (Computed from NPR figure)	SNR	54	57		dB		1

Notes:
1. See Section 3.6 on page 17 for explanation of test levels.
2. Refer to Figure 7-25 for SFDR variation versus temperature
3. Refer to Figure 7-24 for SFDR variation versus supplies
4. Refer to Figure 7-43 for NPR variation versus temperature
5. Refer to Figure 7-42 for NPR variation versus supplies

Table 3-5. AC Electrical Characteristics NRTZ Mode (First & Second Nyquist Zone)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
Single-tone Spurious Free Dynamic Range							
4:1 MUX							
Fs = 4.5 GSps @ Fout = 45 MHz 0dBFS			73				4
Fs = 4.5 GSps @ Fout = 2205 MHz 0dBFS			61			(2)(3)	4
Fs = 4.5 GSps @ Fout = 4455 MHz 0dBFS	|SFDR|		56		dBc		4
Fs = 3.0 GSps @ Fout = 30 MHz 0dBFS		62	75				1, 6
Fs = 3.0 GSps @ Fout = 1470 MHz 0dBFS		60	65				1, 6
Fs = 3.0 GSps @ Fout = 2970 MHz 0dBFS		55	60				1, 6
2:1 MUX							
Fs = 3.2 GSps @ Fout = 32 MHz 0dBFS			76				4
Fs = 3.2 GSps @ Fout = 1568 MHz 0dBFS			63			(2)(3)	4
Fs = 3.2 GSps @ Fout = 3168 MHz 0dBFS	|SFDR|		62		dBc		4
Fs =1.5 GSps @ Fout = 15 MHz 0dBFS		65	77				1, 6
Fs =1.5 GSps @ Fout = 735 MHz 0dBFS		60	73				1, 6
Fs =1.5 GSps @ Fout = 1485 MHz 0dBFS		51	57				1, 6

© e2v technologies (uk) limited 2016

Table 3-5. AC Electrical Characteristics NRTZ Mode (First & Second Nyquist Zone) (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
Highest spur level							
4:1 MUX							
Fs = 4.5 GSps @ Fout = 45 MHz 0dBFS			–75				4
Fs = 4.5 GSps @ Fout = 2205 MHz 0dBFS			–66				4
Fs = 4.5 GSps @ Fout = 4455 MHz 0dBFS			–74		dBm		4
Fs = 3.0 GSps @ Fout = 30 MHz 0dBFS			–76				1, 6
Fs = 3.0 GSps @ Fout = 1470 MHz 0dBFS			–69				1, 6
Fs = 3.0 GSps @ Fout = 2970 MHz 0dBFS			–76				1, 6
2:1 MUX							
Fs = 3.2 GSps @ Fout = 32 MHz 0dBFS			–77				4
Fs = 3.2 GSps @ Fout = 1568 MHz 0dBFS			–67				4
Fs = 3.2 GSps @ Fout = 3168 MHz 0dBFS			–80		dBm		4
Fs =1.5 GSps @ Fout = 15 MHz 0dBFS			–76				1, 6
Fs =1.5 GSps @ Fout = 735 MHz 0dBFS			–76				1, 6
Fs =1.5 GSps @ Fout = 1485 MHz 0dBFS			–78				1, 6
Signal independent Spur (clock-related spur) with 4:1 MUX							
Fc @4.5 GSps			–46		dBm		4
Fc/2 @4.5 GSps			< –93		dBm		4
Fc/4 @4.5 GSps			< –93		dBm		4
Self-Noise Density at code 0 or 4095 @4.5 GSps			–151		dBm/Hz		4
Noise Power Ratio (1st Nyquist) –14 dBFS peak to rms loading factor Fs = 4.5 GSps 2 GHz broadband pattern, 25 MHz notch width	NPR		47.5		dB	(4)(5)	4
Equivalent ENOB (Computed from NPR figure)	ENOB		9.4		Bit		4
Signal to Noise Ratio (Computed from NPR figure)	SNR		58.5		dB		4
Noise Power Ratio (1st Nyquist) –14 dBFS peak to rms loading factor Fs = 3 GSps 1.33 GHz broadband pattern, 17 MHz notch width	NPR	47	50		dB		1, 6
Equivalent ENOB (Computed from NPR figure)	ENOB	9.3	9.8		Bit		1, 6
Signal to Noise Ratio (Computed from NPR figure)	SNR	58	61		dB		1, 6
Noise Power Ratio (2nd Nyquist) –14 dBFS peak to rms loading factor Fs = 4.5 GSps 2 GHz broadband pattern, 25 MHz notch width	NPR		42		dB		4

© e2v technologies (uk) limited 2016

Table 3-5. AC Electrical Characteristics NRTZ Mode (First & Second Nyquist Zone) (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
Equivalent ENOB (Computed from NPR figure)	ENOB		8.5		Bit		4
Signal to Noise Ratio (Computed from NPR figure)	SNR		53		dB		4
Noise Power Ratio (2nd Nyquist) –14 dBFS peak to rms loading factor Fs = 3 GSps 1.33 GHz broadband pattern, 17 MHz notch width	NPR	41	43.5		dB		1, 6
Equivalent ENOB (Computed from NPR figure)	ENOB	8.3	8.8		Bit		1, 6
Signal to Noise Ratio (Computed from NPR figure)	SNR	52	54.5		dB		1, 6

Notes: 1. See Section 3.6 on page 17 for explanation of test levels.
2. Refer to Figure 7-25 for SFDR variation versus temperature
3. Refer to Figure 7-24 for SFDR variation versus supplies
4. Refer to Figure 7-43 for NPR variation versus temperature
5. Refer to Figure 7-42 for NPR variation versus supplies

Table 3-6. AC Electrical Characteristics RTZ Mode (Second Nyquist Zone)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
Single-tone Spurious Free Dynamic Range							
4:1 MUX Fs = 4.5 GSps @ Fout = 4455 MHz 0dBFS Fs = 3.0 GSps @ Fout = 2970 MHz 0dBFS	|SFDR|	 59	 52 64		dBc	(2)(3)	 4 1, 6
2:1 MUX Fs = 3.2 GSps @ Fout = 3168 MHz 0dBFS Fs =1.5 GSps @ Fout = 1485 MHz 0dBFS	|SFDR|	 59	 59 66			(2)(3)	 4 1, 6
Highest spur level							
4:1 MUX Fs = 4.5 GSps @ Fout = 4455 MHz 0dBFS Fs = 3.0 GSps @ Fout = 2970 MHz 0dBFS			 –66 –74		dBm		 4 1, 6
2:1 MUX Fs = 3.2 GSps @ Fout = 3168 MHz 0dBFS Fs =1.5 GSps @ Fout = 1485 MHz 0dBFS			 –72 –75		dBm		 4 1, 6
Signal independent Spur (clock-related spur) with 4:1 MUX							
Fc @4.5 GSps			–39		dBm		4
Fc/2 @4.5 GSps			< –90		dBm		4
Fc/4 @4.5 GSps			–86		dBm		4
Self-Noise Density at code 0 or 4095 @4.5 GSps			–141		dBm/Hz		4

© e2v technologies (uk) limited 2016

Table 3-6. AC Electrical Characteristics RTZ Mode (Second Nyquist Zone)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
Noise Power Ratio (2nd Nyquist) –14 dBFS peak to rms loading factor Fs = 4.5 GSps 2 GHz broadband pattern, 25 MHz notch width	NPR		40		dB	(4)(5)	4
Equivalent ENOB (Computed from NPR figure)	ENOB		8.2		Bit		4
Signal to Noise Ratio (Computed from NPR figure)	SNR		51		dB		4
Noise Power Ratio (2nd Nyquist) –14 dBFS peak to rms loading factor Fs = 3 GSps 1.33 GHz broadband pattern, 17 MHz notch width	NPR	43.5	46		dB		1, 6
Equivalent ENOB (Computed from NPR figure)	ENOB	8.8	9.2		Bit		1, 6
Signal to Noise Ratio (Computed from NPR figure)	SNR	54.7	57		dB		1, 6

Notes:
1. See Section 3.6 on page 17 for explanation of test levels.
2. Refer to Figure 7-25 for SFDR variation versus temperature
3. Refer to Figure 7-24 for SFDR variation versus supplies
4. Refer to Figure 7-43 for NPR variation versus temperature
5. Refer to Figure 7-42 for NPR variation versus supplies

Table 3-7. AC Electrical Characteristics RF Mode (Second and Third Nyquist Zones)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
Single-tone Spurious Free Dynamic Range							
4:1 MUX Fs = 4.5 GSps @ Fout = 4455 MHz 0dBFS Fs = 4.5 GSps @ Fout = 6705 MHz 0dBFS	|SFDR|		56 51		dBc	(2)(3)	4 4
Fs = 3.0 GSps @ Fout = 2970 MHz 0dBFS Fs = 3.0 GSps @ Fout = 4470 MHz 0dBFS		56 49	65 58				1, 6 1, 6
2:1 MUX Fs = 3.2 GSps @ Fout = 3168 MHz 0dBFS Fs = 3.2 GSps @ Fout = 4768 MHz 0dBFS	|SFDR|		58 54		dBc	(2)(3)	4 4
Fs = 1.5 GSps @ Fout = 1485 MHz 0dBFS Fs = 1.5 GSps @ Fout = 2235 MHz 0dBFS		64 57	70 65			(6)	1, 6 1, 6
4:1 MUX with IUCM2 Fs = 4.5 GSps @ Fout = 4455MHz 0dBFS	|SFDR|	54	65		dBc	(7)	1, 6

© e2v technologies (uk) limited 2016

Table 3-7. AC Electrical Characteristics RF Mode (Second and Third Nyquist Zones) (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level[1]
Highest spur level							
4:1 MUX Fs = 4.5 GSps @ Fout = 4455 MHz 0dBFS Fs = 4.5 GSps @ Fout = 6705 MHz 0dBFS Fs = 3.0 GSps @ Fout = 2970 MHz 0dBFS Fs = 3.0 GSps @ Fout = 4470 MHz 0dBFS			 –65 –61 –69 –67		dBm		 4 4 1, 6 1, 6
2:1 MUX Fs = 3.2 GSps @ Fout = 1568 MHz 0dBFS Fs = 3.2 GSps @ Fout = 4768 MHz 0dBFS Fs = 1.5 GSps @ Fout = 1485 MHz 0dBFS Fs = 1.5 GSps @ Fout = 2235 MHz 0dBFS			 –65 –66 –73 –75		dBm		 4 4 1, 6 1, 6
4:1 MUX with IUCM2 Fs = 4.5 GSps @ Fout = 4455 MHz 0dBFS			–70		dBm	(7)	1, 6
Signal independent Spur (clock-related spur) with 4:1 MUX							
Fc @4.5 GSps			–42		dBm		4
Fc/2 @4.5 GSps			< –93		dBm		4
Fc/4 @4.5 GSps			< –93		dBm		4
Self-Noise Density at code 0 or 4095 @4.5 GSps			–138		dBm/Hz		4
Noise Power Ratio (2nd Nyquist) –14 dBFS peak to rms loading factor Fs = 4.5 GSps 2 GHz broadband pattern, 25 MHz notch width	NPR		39		dB	(4)(5)	4
Equivalent ENOB (Computed from NPR figure)	ENOB		8.0		Bit		4
Signal to Noise Ratio (Computed from NPR figure)	SNR		50		dB		4
Noise Power Ratio (2nd Nyquist) –14 dBFS peak to rms loading factor Fs = 3 GSps 1.33 GHz broadband pattern, 17 MHz notch width	NPR	42.5	45		dB		1, 6
Equivalent ENOB (Computed from NPR figure)	ENOB	8.6	9.0		Bit		1, 6
Signal to Noise Ratio (Computed from NPR figure)	SNR	53.5	56		dB		1, 6
Noise Power Ratio (3rd Nyquist) –14 dBFS peak to rms loading factor Fs = 4.5 GSps 2 GHz broadband pattern, 25 MHz notch width	NPR		39		dB		4

© e2v technologies (uk) limited 2016

Table 3-7. AC Electrical Characteristics RF Mode (Second and Third Nyquist Zones) (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
Equivalent ENOB (Computed from NPR figure)	ENOB		8.0		Bit		4
Signal to Noise Ratio (Computed from NPR figure)	SNR		50		dB		4
Noise Power Ratio (3rd Nyquist) –14 dBFS peak to rms loading factor Fs = 3 GSps 1.33 GHz broadband pattern, 17 MHz notch width	NPR	39	42		dB		1, 6
Equivalent ENOB (Computed from NPR figure)	ENOB	8	8.5		Bit		1, 6
Signal to Noise Ratio (Computed from NPR figure)	SNR	50	53		dB		1, 6

Notes:
1. See Section 3.6 on page 17 for explanation of test levels.
2. Refer to Figure 7-25 for SFDR variation versus temperature
3. Refer to Figure 7-24 for SFDR variation versus supplies
4. Refer to Figure 7-43 for NPR variation versus temperature
5. Refer to Figure 7-42 for NPR variation versus supplies
6. This measurement at Fs=1.5Gsps is done with RPB1 and RPW1.
7. The corresponding spectrum shows an output frequency at 4455MHz within an 1125MHz wide Nyquist zone.

3.5 Timing Characteristics and Switching Performances

Unless otherwise specified:

Values in the table below are given over temperature range with typical power supplies (V_{CCA5} = 5V, V_{CCA3} = 3.3V, V_{CCD} = 3.3V), with 4:1 MUX ratio, typical swing on input data, typical Pclk, master clock input jitter is below 100 fs rms integrated over 5GHz bandwidth.

Min and Max values are given over temperature range.

Typ values are given at ambient temperature.

Table 3-8. Timing characteristics and Switching Performances

Parameter	Symbol	Value	Unit	Note	Test Level(1)
SWITCHING PERFORMANCE AND CHARACTERISTICS					
Maximum operating clock frequency					
4:1 MUX mode		4.5	GHz		4
2:1 MUX mode		3.2	GHz		4
Minimum operating clock frequency		300	MHz	(2)	5

© e2v technologies (uk) limited 2016

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test Level[1]
TIMING CHARACTERISTICS							
Input Data timing							
Input data setup and hold time	t_{SH}		360		ps	(3)	4
Input data rate (4:1 MUX)				1125	Msps		4
Input data rate (2:1 MUX)				1600	Msps		4
Data clock output timing (DSP, DSPN)							
DSP clock phase tuning steps	PSS		0.5		Tclock		5
Master clock to DSP timing							
Pipeline (4:1 MUX)			3		Tclock	(4)	5
Pipeline (2:1 MUX)			3				5
Delay 4:1 MUX	t_{PD}		540		ps		4
Delay 2:1 MUX			540				4
SYNC timing							
Minimum Sync pulse width			3		Tclock		4
SYNC to DSP, DSPN							
Sync falling edge to DSP rising edge Pipeline in 4:1 MUX			3		Tclock	(5)	5
Sync falling edge to DSP rising edge Pipeline in 2:1 MUX			3		Tclock		5
Sync falling edge to DSP rising edge							
Delay with 2:1 MUX	t_{SDSP}		640		ps		4
Delay with 4:1 MUX			640		ps		4
Sync rising edge to DSP falling edge	t_{SDSPF}		$T_{CLK} + 1/2\ T_{DSP}$		ps		5
SYNC setup and hold time	t_{SSH}		15		ps	(6)	4
SYNC forbidden area lower bound	t_1		100		ps		4
SYNC forbidden area upper bound	t_2		$t_1 - t_{SSH}$		ps		4
Analog output timing							
Analog output rise time (20-80%)	t_{OR}		30		ps		4
Analog output fall time (20-80%)	t_{OF}		30		ps		4
Pipeline (4:1 MUX)			3		Tclock	(4)	5
Pipeline (2:1 MUX)			3				5
Analog output delay	t_{OD}		560		ps	(4)	4

Notes: 1. See Section 3.6 on page 17 for explanation of test levels.

2. Minimum operating clock frequency can be DC. It depends on the clock input AC coupling capacitor used in the final application and limitation due to the environment as circuit itself displays no lower clock frequency limitation.

© e2v technologies (uk) limited 2016

3. Set up and hold time were measured on e2v evaluation board and as such include the impact from the FPGA (jitter and skew) and PCB skew on the board. Refer to Figure 7-44 on Section 7.3. t_{SH} variation over temperature range is around 20 ps.
4. See Figure 3-1 and Figure 3-2 below.
5. See Figure 3-3 below.
6. See Figure 3-4 below.

Figure 3-1. Timing Diagram for 4:1 MUX principle of operation OCDS1, IUCM1

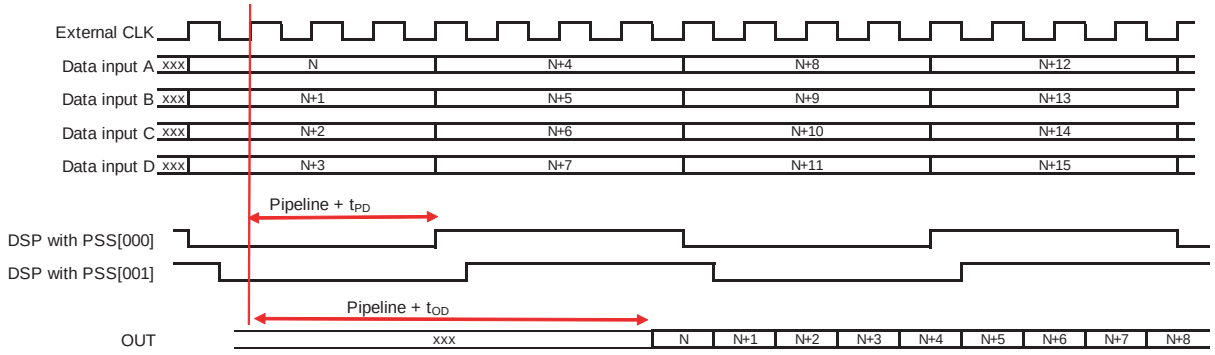


Figure 3-2. Timing Diagram for 2:1 MUX principle of operation OCDS1, IUCM1

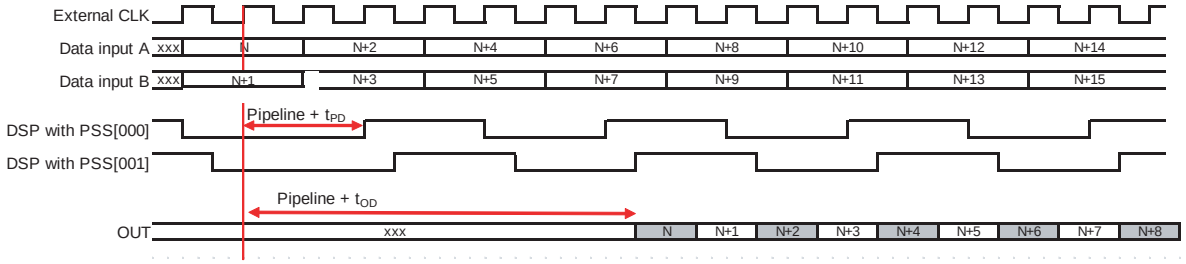
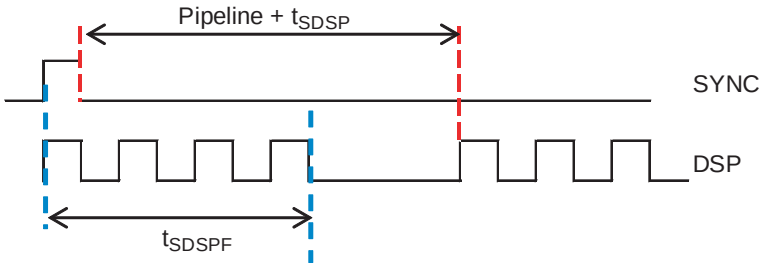
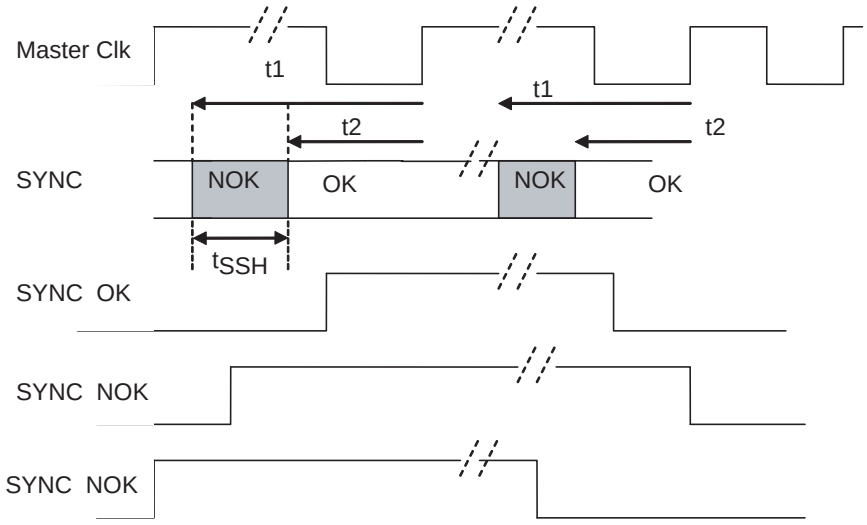


Figure 3-3. Timing relationship between SYNC and DSP



© e2v technologies (uk) limited 2016

Figure 3-4. SYNC Timing Diagram



3.6 Explanation of Test Levels

Table 3-9. Test levels

1	100% production tested at +25°C(1)
2	100% production tested at +25°C(1), and sample tested at specified temperatures.
3	Sample tested only at specified temperatures
4	Parameter is guaranteed by characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter value is only guaranteed by design
6	100% tested over specified temperature range (Military grade)

Only MIN and MAX values are guaranteed.

Note: 1. Unless otherwise specified.

3.7 Digital Input Coding Table

Table 3-10. Coding Table (Theorical values)

Digital output msb……..lsb	**Differential analog output**
000000000000	–500 mV
010000000000	–250 mV
011000000000	–125 mV
011111111111	–0.122 mV
100000000000	0.122 mV
101000000000	+125 mV
110000000000	+250 mV
111111111111	+500 mV

© e2v technologies (uk) limited 2016

4. DEFINITION OF TERMS

Table 4-1. Definition of Terms

Abbreviation	Term	Definition
(SFDR)	Spurious free dynamic range	Ratio expressed in dBC of the signal power, set at Full Scale, to the power of the highest spurious spectral component over the Nyquist zone. The peak spurious component may or may not be a harmonic.
(HSL)	Highest Spur Level	Power of the highest spurious spectral component expressed in dBm.
(ENOB)	Effective Number Of Bits	ENOB is calculated from NPR measurement using the formula: ENOB = $(NPR_{[dB]} + \|LF_{[dB]}\| - 3 - 1.76) / 6.02$ Where LF is the loading factor i.e. the ratio between the Gaussian noise standard deviation versus amplitude full scale of the NPR pattern.
(SNR)	Signal to noise ratio	SNR is calculated from NPR measurement using the formula: $SNR_{[dB]} = NPR_{[dB]} + \|LF_{[dB]}\| - 3$ Where LF is the loading factor i.e. the ratio between the Gaussian noise standard deviation versus amplitude full scale of the NPR pattern.
(NPR)	Noise Power Ratio	The NPR is measured to characterize the DAC performance in response to broad band signals. When applying a notch-filtered broadband white-noise pattern at the input of the DAC under test, the Noise Power Ratio is defined as the ratio between the average noise measured on the shoulder of the notch and inside the notch, using the same integration bandwidth.
(DNL)	Differential non linearity	The Differential Non Linearity for a given code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there is no missing point and that the transfer function is monotonic.
(INL)	Integral non linearity	The Integral Non Linearity for a given code i is the difference between the measured voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
(VSWR)	Voltage Standing Wave Ratio	The VSWR corresponds to the insertion loss linked to the power reflection. For example a VSWR of 1.2 corresponds to a 20dB return loss (i.e. 99% power transmitted and 1% reflected).
(IUCM)	Input Under Clocking Mode	The IUCM principle is to apply a selectable division ratio between the DAC clock section and the MUX clock section.
(PSS)	Phase Shift Select	The Phase Shift Select function is used to tune the phase of the DSP clock.
(OCDS)	Output Clock Division Select	It allows dividing the DSP clock frequency by the OCDS coded value factor.
(NRZ)	Non Return to Zero	Non Return to Zero mode on analog output.
(RF)	Radio Frequency	RF mode on analog output.
(RTZ)	Return To Zero	Return to zero mode on analog output.
(NRTZ)	Narrow Return To Zero	Narrow return to zero mode on analog output.
(RPB)	Reshaped Pulse Begin	Function controlling when the transition of the DAC analog output occurs. (applicable in NRTZ, RTZ and RF mode)
(RPW)	Reshaped Pulse Width	Function controlling the width of the reshaping of the DAC analog output. (applicable in NRTZ and RF mode)

© e2v technologies (uk) limited 2016

5. FUNCTIONAL DESCRIPTION

Figure 5-1. DAC functional diagram

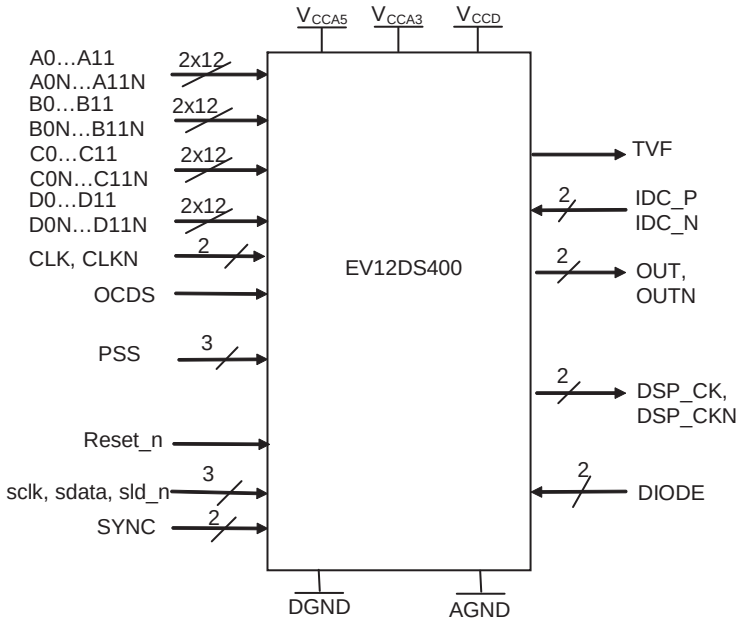


Table 5-1. Functions description

Name	Function	Name	Function
V_{CCD}	3.3V digital power supply	CLK	In-phase master clock
V_{CCA5}	5V analog power supply	CLKN	Inverted phase master clock
V_{CCA3}	3.3V analog power supply	DSP_CK	In-phase output clock
DGND	Digital ground	DSP_CKN	Inverted phase output clock
AGND	Analog ground	PSS[0..2]	Phase shift select
A[11…0]	In-phase digital input port A	Reset_n	Reset of 3WSI registers
A[11..0]N	Inverted phase digital input port A	sld_n	3WSI select
B[11…0]	In-phase digital input port B	sclk, sdata	3WSI clock and data inputs
B[11..0]N	Inverted phase digital input port B	TVF	Setup/hold time violation flag
C[11…0]	In-phase digital input port C	IDC_P, IDC_N	Input data check
C[11..0]N	Inverted phase digital input port C	OCDS	Output Clock Division factor Selection
D[11…0]	In-phase digital input port D	Diode	Diode for temperature monitoring
D[11..0]N	Inverted phase digital input port D	SYNC/ SYNCN	Synchronization signal (active high)
OUT	In-phase analog output	OUTN	Inverted phase analog output

© e2v technologies (uk) limited 2016

Table 5-2. DAC overview functionality and controls

Function	Description	Controllability
MUX	MUX ratio selection (4:1 or 2:1)	3WSI
MODE	Output reshaping mode selection: NRZ, NRTZ, RTZ or RF	3WSI
RPW	Reshaping Pulse Width (applicable in NRTZ and RF mode)	3WSI
RPB	Reshaping Pulse Begin (applicable in NRTZ, RTZ and RF mode)	3WSI
PSS	Phase Shift Select: shift the DSP clock by steps of $T_{CLK}/2$ for FPGA synchronisation	3WSI/external pins
OCDS	Output Clock Division Select: Ratio of division between DSP clock and master clock	3WSI/external pins
IUCM	Internal Under Clocking Mode ratio selection: Allow to work with data rate equal to F_{CLK} divided by 1,2 or 4 with a DAC clocked at F_{CLK}	3WSI
GA	DAC Gain Adjust	3WSI

Note: 1. PSS and OCDS are controlled through the external pin if ECDC bit of 3WSI state register is set to level 1 (default value). See Section 5.13.3 on page 42 for more information.

5.1 Multiplexer

Two multiplexer ratios (N) are allowed:

- N=4: 4:1 MUX, which allows operation up to 4.5 GSps;
- N=2: 2:1 MUX, which allows operation up to 3.2 GSps.

Label	Value	Description	Default setting
MUX	0	4:1 mode (N=4)	0 (4:1MUX mode)
	1	2:1 mode (N=2)	

In 2:1 MUX ratio, the unused data ports (ports C and D) can be left open.

© e2v technologies (uk) limited 2016

5.2 Mode Function

The MODE function allows choosing between NRZ, NRTZ, RTZ and RF modes.

Label	Value	Description	Default setting
MODE[1:0]	00	NRZ mode	01 (NRTZ)
	01	Narrow RTZ (a.k.a. NRTZ) mode	
	10	RTZ Mode (50%)	
	11	RF mode	

Ideal equations describing maximum available output power versus analog output frequency in the four modes are given hereafter, with X being the normalised output frequency (i.e. Fout/F_{CLK}, thus the edges of the Nyquist zones are at X = 0, ½, 1, 3/2, 2, …).

In fact, due to limited bandwidth, an extra term must be added to take into account a first order low pass filter with a 7 GHz cut-off frequency.

In the following formula, Pout (X) is expressed in dBm

NRZ mode:

$$\mathrm{Pout}(X) = 20 \cdot \log_{10} \cdot \left[\frac{k \cdot \mathrm{sinc}(k \cdot \pi \cdot X)}{0.893} \right]$$

where sinc(x) = sin(x)/x, and k = 1

NRTZ mode:

$$\mathrm{Pout}(X) = 20 \cdot \log_{10} \cdot \left[\frac{\left| k \cdot \mathrm{sinc}(k \cdot \pi \cdot X) \right|}{0.893} \right]$$

where k = 1 - RPW/T_{CLK} and RPW is the width of reshaping pulse

RTZ mode:

$$\mathrm{Pout}(X) = 20 \cdot \log_{10} \cdot \left[\frac{\left| k \cdot \mathrm{sinc}(k \cdot \pi \cdot X) \right|}{0.893} \right]$$

where k is the duty cycle of the clock presented at the DAC input. Please note that due to phase mismatch in balun used to convert single ended clock to differential clock the first zero may move around the limit of the 4th and the 5th Nyquist zone. Ideally k=1/2.

RF mode:

$$\mathrm{Pout}(X) = 20 \cdot \log_{10} \cdot \left[\frac{\left| k \cdot \mathrm{sinc}\left(\frac{k \cdot \pi \cdot X}{2} \right) \cdot \sin\left(\frac{k \cdot \pi \cdot X}{2} \right) \right|}{0.893} \right]$$

where k = 1 - RPW/T_{CLK} and RPW is the width of reshaping pulse.

As a consequence:

- NRZ mode offers maximum output power for 1st Nyquist operation;
- RTZ mode have a slow roll off for 2nd Nyquist operation;
- RF mode offers maximum power over 2nd and 3rd Nyquist zones;

© e2v technologies (uk) limited 2016

- NRTZ mode offers optimum power over the 1st and the first half of the 2nd Nyquist zones. It is the most relevant mode in terms of performance for operation over 1st and beginning of 2nd Nyquist zones.

In the two following Figure 5-2 and Figure 5-3, the pink line is the ideal equation's result, and the green line includes a first order 7 GHz cut-off low pass filter to take into account the bandwidth effect due to die and package.

Figure 5-2. Max available output power (Pout) at nominal gain vs output frequency (Fout) in the four output modes at 4.5 GSps, over eight Nyquist zones, computed for different RPW steps

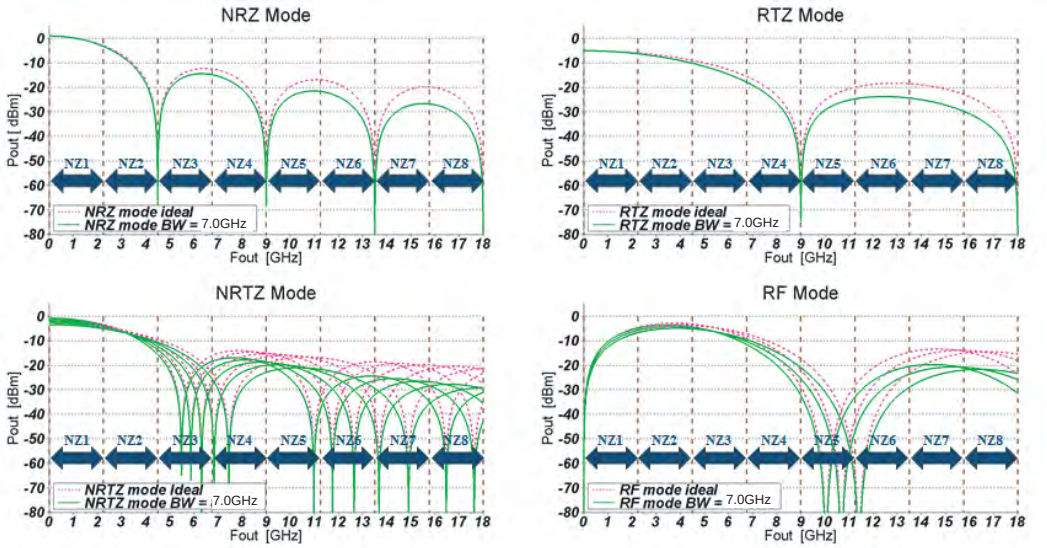
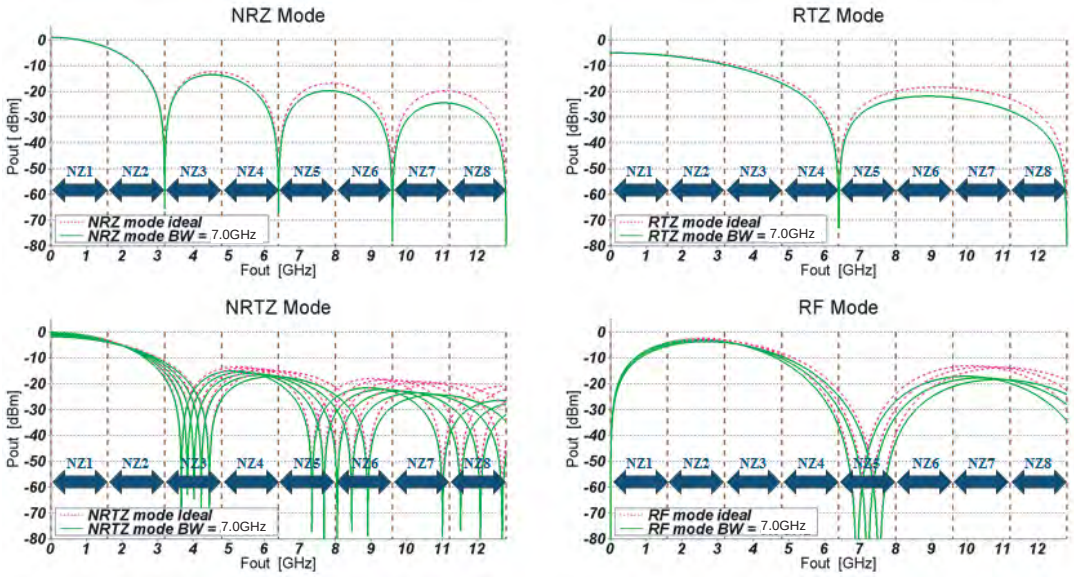


Figure 5-3. Max available output power (Pout) at nominal gain vs output frequency (Fout) in the four output modes at 3.2 GSps, over eight Nyquist zones, computed for different RPW steps



© e2v technologies (uk) limited 2016

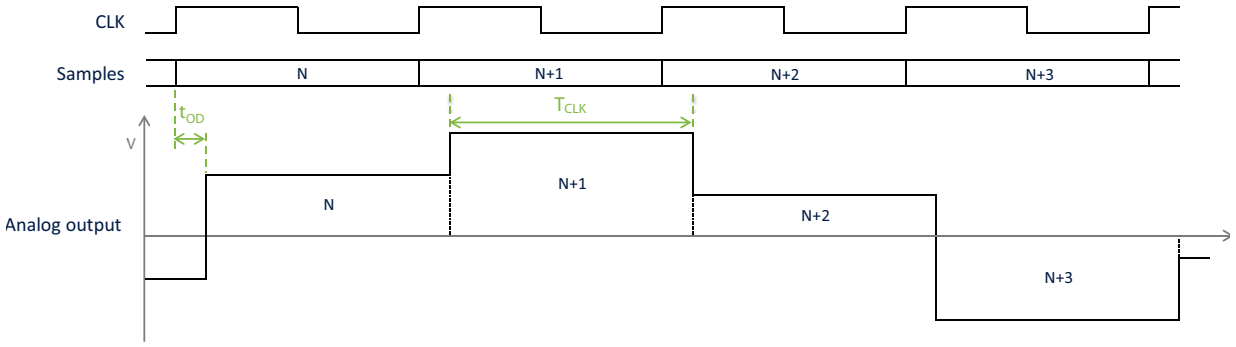
5.2.1 NRZ output mode

This mode does not allow for operation in the 2nd Nyquist zone because of the sin(x)/x notch.

The advantage is that it gives good results at the beginning of the 1st Nyquist zone (less attenuation than in RTZ mode); it also removes the parasitic spur at the clock frequency (in differential).

This legacy mode is provided for noise characterization purpose and is of limited interest beyond the very beginning of the 1st Nyquist frequency band. However it provides the highest output power at the beginning of the 1st Nyquist zone.

Figure 5-4. NRZ timing diagram



5.2.2 Narrow RTZ (NRTZ) output mode

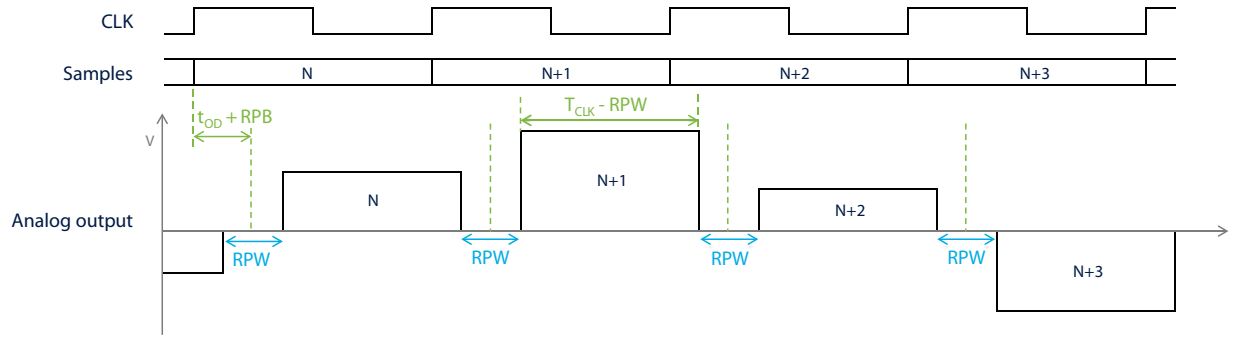
This mode has the following advantages:

- Optimized power in the 1st Nyquist zone and beginning of the 2nd Nyquist zone;
- Extended dynamic and linearity through elimination of noise on transition edges;
- Trade-off between NRZ and RTZ;
- Possible operation in the 4th and 5th Nyquist zones.

And weaknesses:

- Notch in the 3rd Nyquist zone. In fact, notches are at N*(1/(T_{CLK} - RPW)), where T_{CLK} is the external clock period and RPW is the reshaping pulse width;
- By construction clock spur at F_{CLK}.

Figure 5-5. Narrow RTZ timing diagram



The RPB and RPW settings are applicable in this mode; they are programmable through the 3 wire serial interface. For more information on RPB and RPW see Section 5.3 on page 25.

© e2v technologies (uk) limited 2016

5.2.3 RTZ output Mode

The advantage of the RTZ mode is that it enables the operation in the 2nd Nyquist zone but the drawback is that it attenuates more the signal in the first Nyquist zone.

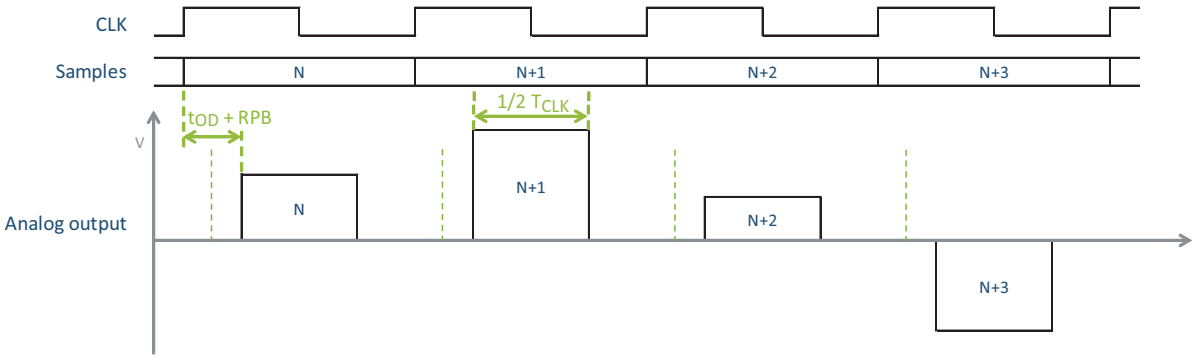
Advantages:

- Extended roll off of sin(x)/x;
- Extended dynamic and linearity through elimination of noise on transition edges;

Weakness:

- By construction strong clock spur at F_{CLK}.

Figure 5-6. RTZ timing diagram



The RPB setting is applicable in this mode; it is programmable through the 3 wires serial interface. For more information on RPB see Section 5.3 on page 25.

5.2.4 RF output mode

RF mode is optimal for operation at high output frequency, since the decay with frequency occurs at higher frequency than for RTZ. Unlike NRZ or RTZ modes, the RF mode presents notches at DC and 2N*(1/(T_{CLK} – RPW), and minimum attenuation for Fout=1/(T_{CLK} – RPW).

Advantages:

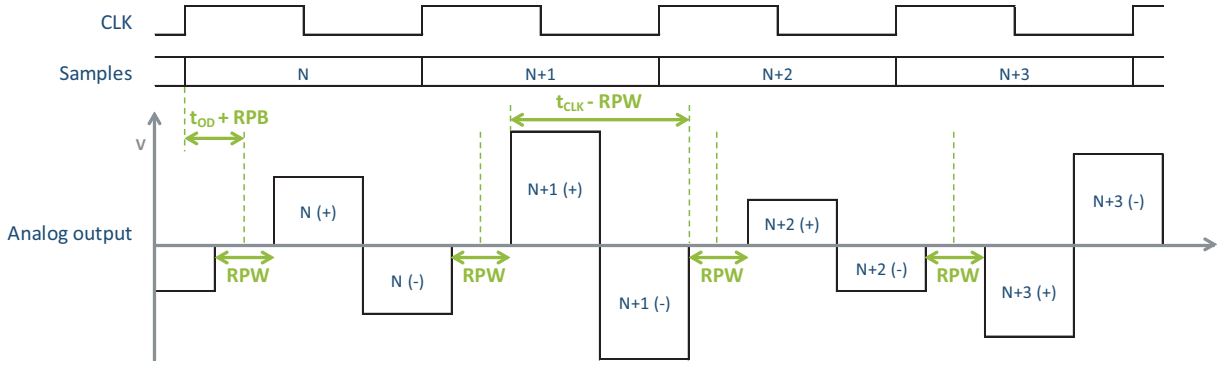
- Optimized for operations over the second half of the 2nd Nyquist zone or over the 3rd Nyquist zone;
- Extended dynamic and linearity through elimination of noise on transition edges;
- Possible operation proven in the first half of the 4th Nyquist zone.

Weakness:

- By construction clock spur at F_{CLK}.
- Next clock spur pushed to 2.F_{CLK}.

© e2v technologies (uk) limited 2016

Figure 5-7. RF timing diagram



RPB and RPW settings are applicable in this mode; they are programmable through the 3 wire serial interface. For more information on RPB and RPW see Section 5.3.

5.3 RPW and RPB Feature

RPB (Reshaping Pulse Begin) and RPW (Reshaping Pulse Width) are new features of the EV12DS400A. They can be used to fine tune the performance of the different modes of the DAC. Their objective is to control the rejection of the signal transitions.

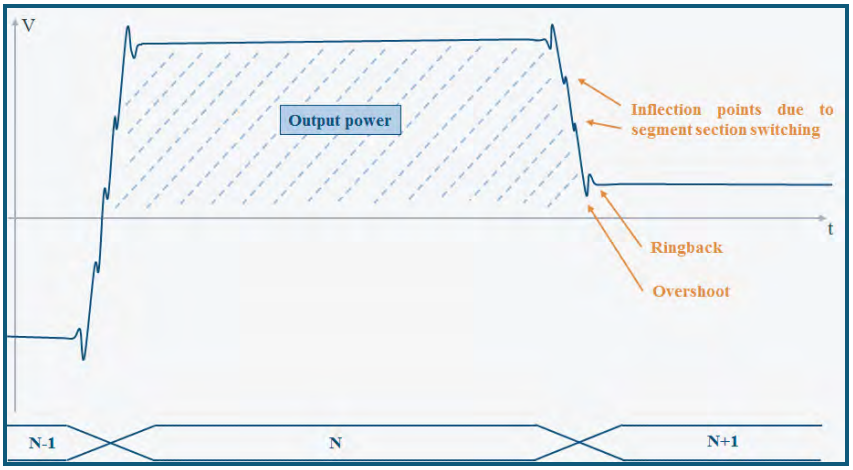
These 2 settings are controlled via the 3WSI interface. See Section 5.13 on page 39 for more information on the 3WSI interface. The different values they can take are specified by mode in the following paragraphs.

Note: In the following figures, the perturbation on the analog output in time domain has been exaggerated to facilitate the comprehension.

NRZ Mode:

See below the output of the DAC in NRZ mode in time domain:

Figure 5-8. DAC output in NRZ and time domain



As can be seen above, in NRZ mode, the transition contains a lot of perturbations that translates into harmonics in the spectrum. However the output power is maximum. RPB or RPW settings are not available in this mode.

© e2v technologies (uk) limited 2016

RTZ Mode:

In RTZ mode, the output is on 50% of the sampling period and off the remaining 50% of the sampling period. Per definition of the RTZ mode, its output power is half the one of the NRZ output power. In this mode, the EV12DS400A features the RPB function which controls when the transition between 50% on and 50% off occurs. Using this feature, the RTZ output linearity performance can be increased. See below the output of the DAC in RTZ mode and time domain, whether RPB is correctly configured or not (the NRZ output mode is traced to show the difference between NRZ and RTZ mode):

Figure 5-9. DAC output in RTZ mode and time domain when RPB is optimum

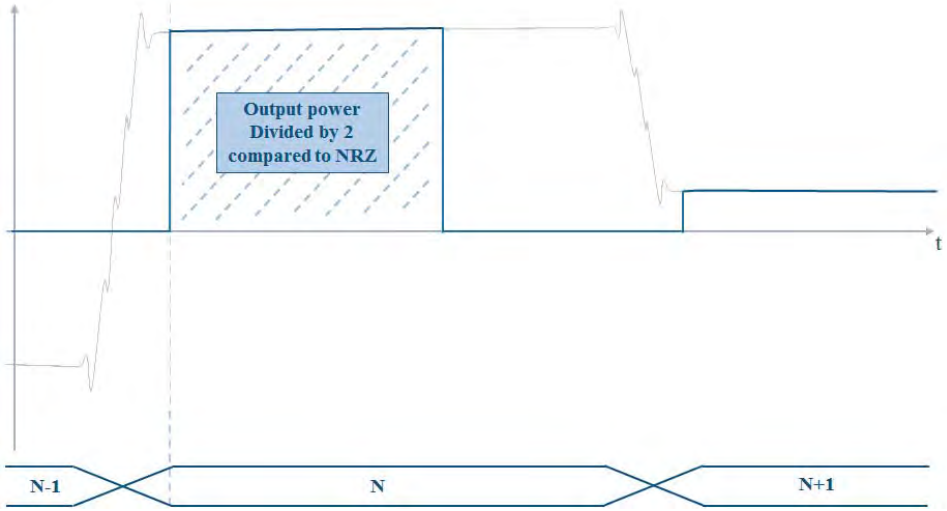
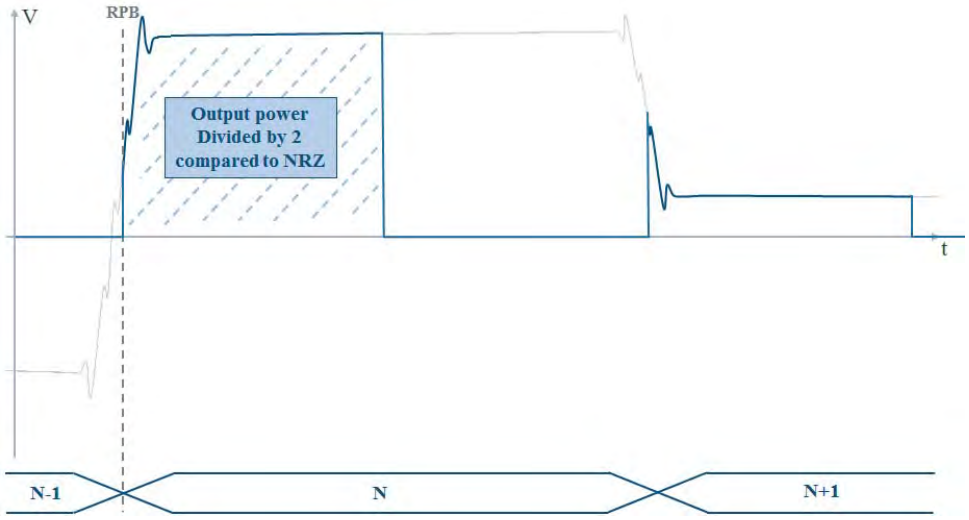


Figure 5-10. DAC output in RTZ mode and time domain when RPB is not optimum



Tuning RPB as depicted in Figure 5-9 will improve the linearity of the output because the transition will be completely rejected. If RPB is not tuned to reject the transitions (see Figure 5-10), the output harmonics will be degraded (mainly H3).

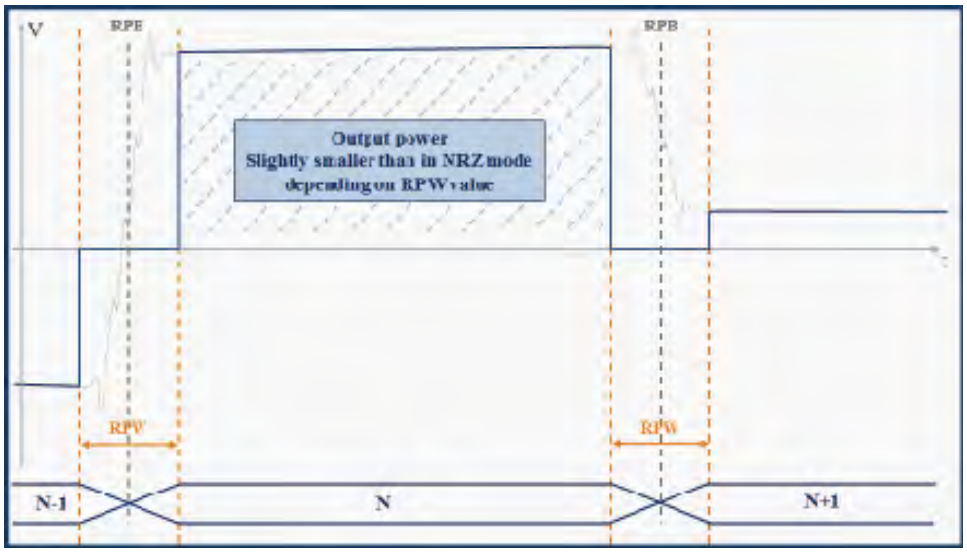
The RPW setting is not available in RTZ mode. See Section 5.13.3 on page 42 for the available values for RPB in RTZ mode.

© e2v technologies (uk) limited 2016

NRTZ Mode:

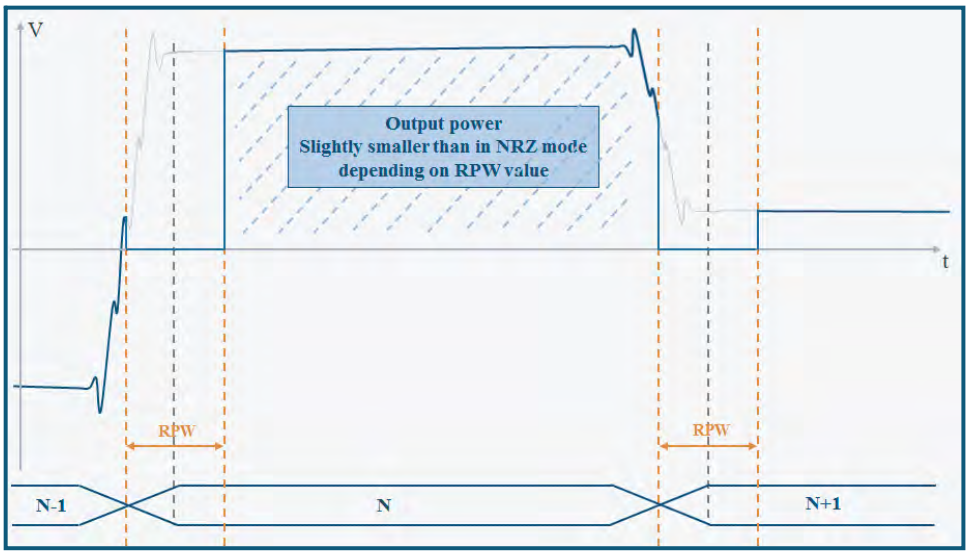
The NRTZ mode is a compromise between the NRZ and the RTZ modes. Its objective is to have the best possible linearity through the removal of the transitions while keeping a high output power. Thus, only the transitions should be cancelled. In this mode both RPB and RPW settings are available. The RPB setting controls the position where the signal is cancelled. The RPW setting controls the wideness of the cancelled signal. See below an example where RPB and RPW are optimum in NRTZ mode (the NRZ output mode is traced to show the difference between NRZ and NRTZ mode):

Figure 5-11. DAC output in NRTZ mode and time domain when RPB/RPW are optimum



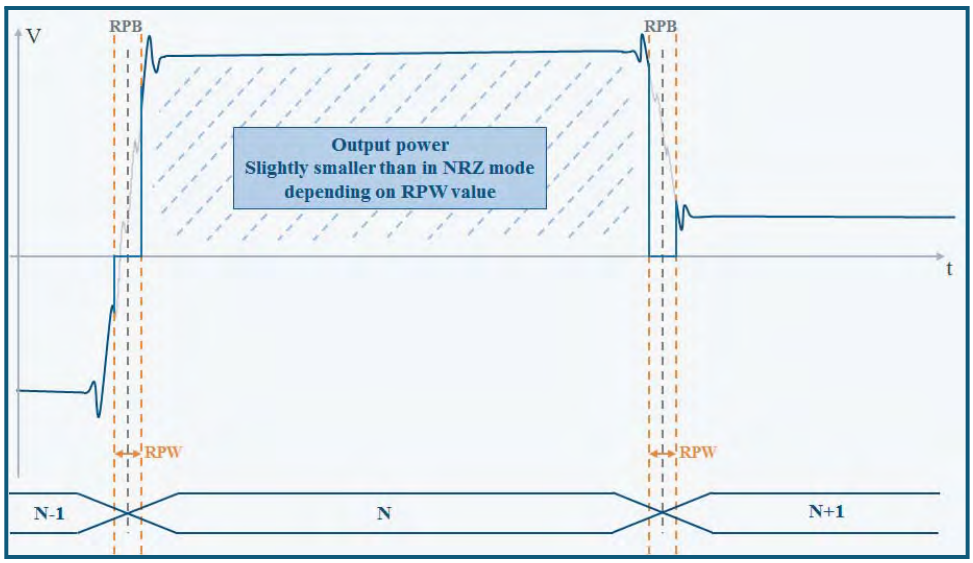
In the case above, the output has a better linearity than in NRZ mode over the complete spectrum while suffering from a slight output power reduction.

Figure 5-12. DAC output in NRTZ mode and time domain when RPB is not optimum



© e2v technologies (uk) limited 2016

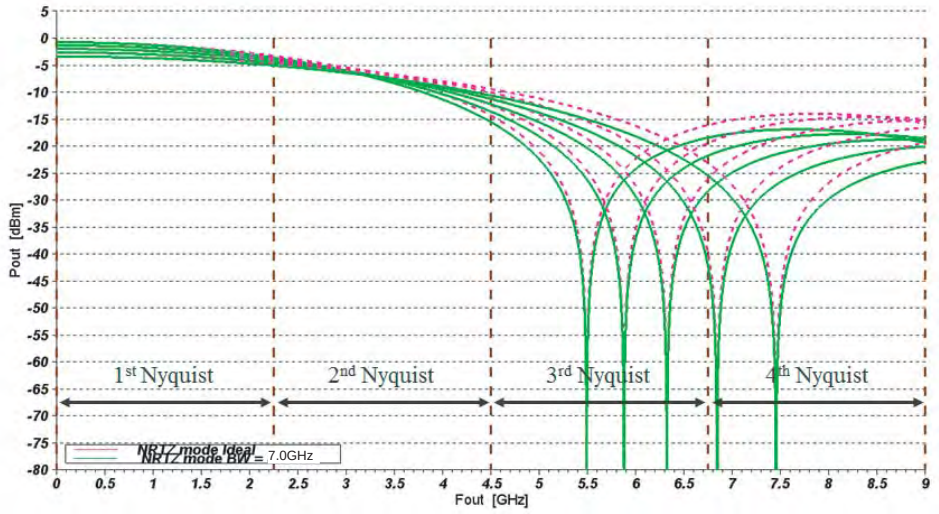
Figure 5-13. DAC output in NRTZ mode and time domain when RPW is not optimum



In case RPB is not optimum (Figure 5-12), the harmonics will be degraded and mainly H3. In case RPW is smaller than the optimum (Figure 5-13), the linearity of the output will be degraded. In case RPW is larger than the optimum, the DAC will have high linearity performance but lower output power.

The RPW setting impacts the frequency response of the mode. See below the Pout vs Fout figure in NRTZ mode with different RPW values:

Figure 5-14. Pout vs Fout @ 4.5 GSps in NRTZ mode over 4 Nyquist zones with different RPW values



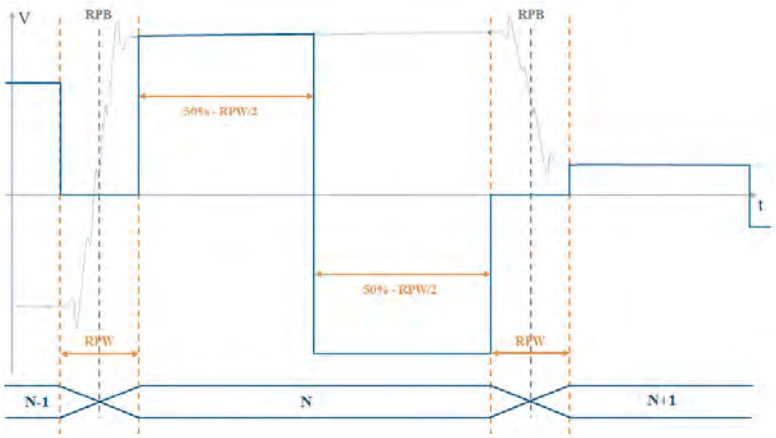
See Section 5.13.3 on page 42 for the available values for RPB and RPW in NRTZ mode.

© e2v technologies (uk) limited 2016

RF Mode:

The RF mode is used in higher Nyquist zones (2nd and 3rd). Its principle is that the output is at its value during half the sampling period and at its opposite value during the remaining half. To improve linearity of this mode both RPB and RPW settings are available. See below an example where RPB and RPW are optimum in RF mode (the NRZ output mode is traced to show the difference between NRZ and RF mode):

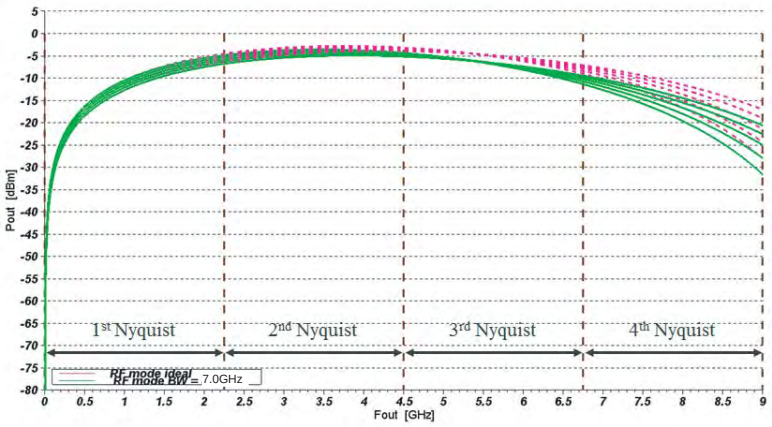
Figure 5-15. DAC output in RF mode and time domain when RPB and RPW are optimum



In case RPB is not optimum, the harmonics will be degraded and mainly H3. In case RPW is smaller than the optimum, the linearity of the output will be degraded. In case RPW is larger than the optimum, the DAC will have high linearity performance but lower output power.

The RPW setting impacts the frequency response of the mode. See below the Pout vs Fout figure in RF mode with different RPW values:

Figure 5-16. Pout vs Fout @ 4.5 GSps in RF mode over 4 Nyquist zones with different RPW values



See Section 5.13.3 on page 42 for the available values for RPB and RPW in RF mode.

© e2v technologies (uk) limited 2016

5.4 Phase Shift Select function (PSS)

It is possible to adjust the timing between the sampling clock and the output DSP clock.

The DSP clock output phase can be tuned over a range of 3.5 input clock cycles (7 steps of half a clock cycle) in addition to the intrinsic propagation delay between the DSP clock (DSP, DSPN) and the sampling clock (CLK, CLKN).

Three bits are provided for the phase shift function: PSS[2:0].

By setting these 3 bits to 0 or 1, one can add a delay on the DSP clock in order to properly synchronize the input data of the DAC and the sampling clock (the DSP clock should be applied to the FPGA and should be used to clock the DAC digital input data).

These 3 bits are either driven directly through the pins PSS[2:0] or through the 3WSI depending on the ECDC bit in the state register of the 3WSI.

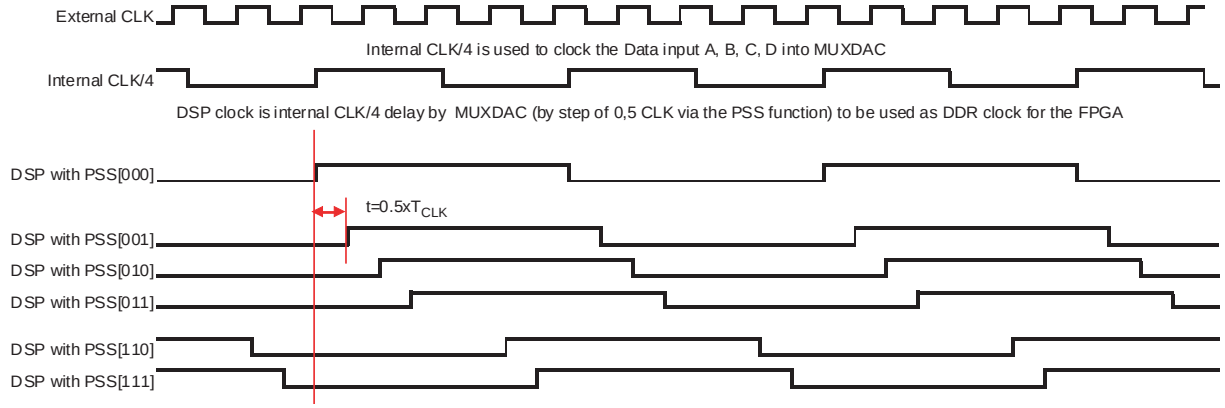
Table 5-3. PSS coding table

Label	Value	Description
PSS[2:0]	000	No additional delay on DSP clock (Default value)
	001	0.5 input clock cycle delay on DSP clock
	010	1 input clock cycle delay on DSP clock
	011	1.5 input clock cycle delay on DSP clock
	100	2 input clock cycles delay on DSP clock
	101	2.5 input clock cycles delay on DSP clock
	110	3 input clock cycles delay on DSP clock
	111	3.5 input clock cycles delay on DSP clock

In order to determine how much delay needs to be added on the DSP clock to ensure the synchronization between the input data and the sampling clock within the DAC, the TVF bit should be monitored.

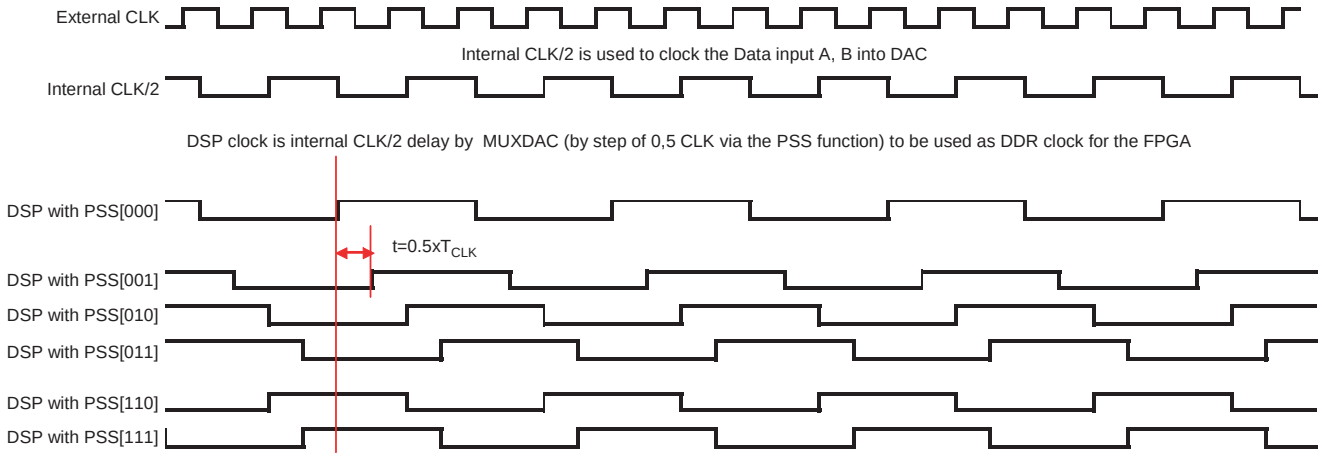
Note: In 4:1 MUX mode the 8 settings are relevant, in 2:1 MUX only the four first settings are relevant; the four last settings will yield the same results.

Figure 5-17. PSS timing diagram for 4:1 MUX, OCDS=0



© e2v technologies (uk) limited 2016

Figure 5-18. PSS timing diagram for 2:1 MUX, OCDS=0



5.5 Output Clock Division Select function (OCDS)

It is possible to change the DSP clock internal division factor from 1 to 2 with respect to the sampling clock/(2*N*M) where N is the MUX ratio (2 or 4), and M is the IUCM ratio (1, 2 or 4). This is possible via the OCDS "Output Clock Division Select" bit through the 3WSI or the external pins if the ECDC bit is high.

OCDS is used to obtain a synchronisation clock for the FPGA slow enough to allow the FPGA to operate with no further internal division of this clock, thus its internal phase is determined by the DSP clock phase. This is useful in a system with multiple DACs and multiple FPGAs to guarantee deterministic phase relationship more easily between the FPGAs after a synchronisation of all the DACs.

Table 5-4. OCDS coding table

Label	Value	Description	Default setting
OCDS	0	OCDS1: DSP clock = Sampling Clock/(2*N*M)	0 (OCDS1)
	1	OCDS2: DSP clock = Sampling Clock/(2*N*M*2)	

Figure 5-19. OCDS timing diagram for 4:1 MUX and IUCM1 mode

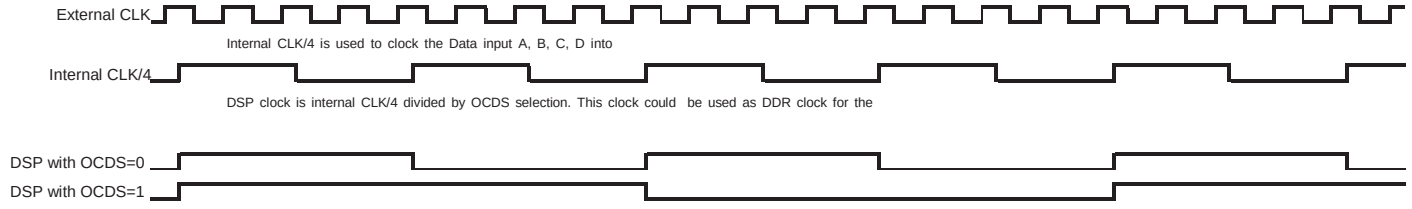
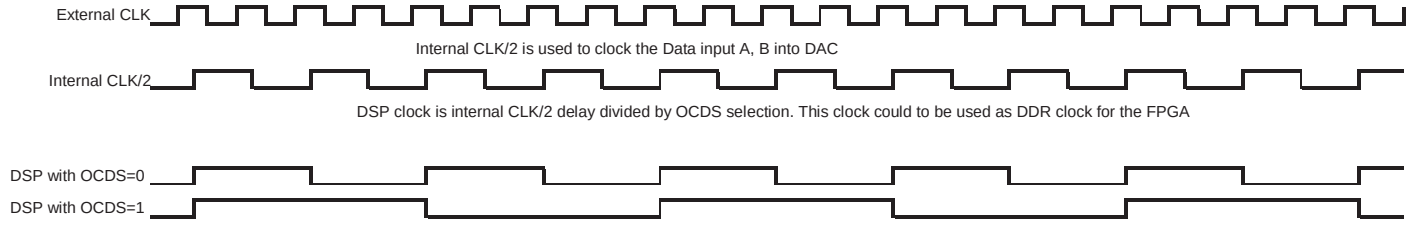


Figure 5-20. OCDS timing diagram for 2:1 MUX and IUCM1 mode



© e2v technologies (uk) limited 2016

5.6 Input Under Clocking Mode (IUCM)

Three Input Under Clocking Modes are available for specific use where the input data are applied to the DAC at half the nominal rate (or a fourth of the nominal rate) with respect to the DAC sampling rate. These modes are available for both 4:1 MUX mode and 2:1 MUX mode.

The principle is to apply a selectable division ratio (1, 2 or 4) between the DAC clock section and the MUX clock section.

Thus there are 3 IUCM modes selectable through the 3WSI (see 3WSI description):

- IUCM1: MUX is driven by the same clock than the DAC section (default mode).
- IUCM2: MUX is driven by a divided by 2 clock coming from the DAC section
- IUCM4: MUX is driven by a divided by 4 clock coming from the DAC section

Detailed explanation is given here-after for IUCM2 mode. IUCM4 mode is operating on the same principle but with a 4 division ratio.

In IUCM1 mode the DAC expects data at half the nominal rate: if the DAC works at Fs sampling rate, then in 4:1 MUX mode, the input data rate should be Fs/4 and the DSP clock should be Fs/(2N*X), with N = MUX ratio (2 or 4) and X = OCDS ratio (1 or 2).

When the IUCM2 mode is selected, the input data rate can be Fs/8 and the DSP clock frequency is Fs/(2N*X*2), with N = MUX ratio (2 or 4) and X = OCDS ratio (1 or 2). This means that in input under clocking mode, the DAC is capable to treat data at half the nominal rate. In this case, the DSP clock is also half its nominal speed. However, the sampling frequency is still Fs.

Label	Logic Value	Description	Default setting
IUCM<1:0>	00 or 01	IUCM1: Input Under Clocking Mode inactive	00 (IUCM1)
	10	IUCM2: clock division ratio between DAC core and MUX: 2	
	11	IUCM4: clock division ratio between DAC core and MUX: 4	

The IUCM2 mode affects spectral response of the different modes.

The first effect is that Nyquist zone edges are no longer at n*Fclock/2 but at n*/Fclock/4 (this is the direct consequence of the division by 2 of the data rate).

The second effect is the modification of the equations ruling the spectral responses in the different modes.

Ideal equations describing maximum available Pout vs Fout in the four output modes when IUCM2 mode is selected are given hereafter, with X= normalised output frequency (i.e. Fout/Fclock, the edges of the Nyquist zones are then at X = 0, ¼, ½, ¾, 1, …)

In fact, due to limited bandwidth, an extra term must be added to take in account a first order low pass filter with an 7 GHz cut-off frequency.

Assuming sinc(x)=sin(x)/x;

NRZ mode: $Pout(X) = 20*\log_{10}(|sinc(\pi*X)*cos(\pi*X)|/0.893)$
NRTZ mode: $Pout(X) = 20*\log_{10}(|k*sinc(k*\pi*X)*cos(\pi*X)|/0.893)$

Where k= 1- RPW/Tclock and RPW is width of reshaping pulse.

© e2v technologies (uk) limited 2016

RTZ mode: $Pout(X) = 20*\log_{10}(|k*sinc(k*\pi*X)*cos(\pi*X)|/0.893)$

Where k is the DAC input clock duty cycle. Please note that due to phase mismatch in the balun used to convert single ended clock into differential clock, the third zero may move around the limit of the 8th and the 9th Nyquist zones. Ideally k=1/2.

RF mode: $Pout(x) = 20*\log_{10}(|k*sinc(k*\pi*X/2)*sin(k*\pi*X/2)*cos(\pi*X)|/0.893)$
where k = 1- RPW/Tclock and RPW is width of reshaping pulse.

Figure 5-21. Max available Pout at nominal gain vs Fout in the four output modes at 4.5 GSps, combined with IUCM2, over eight Nyquist zones, computed for different RPW steps

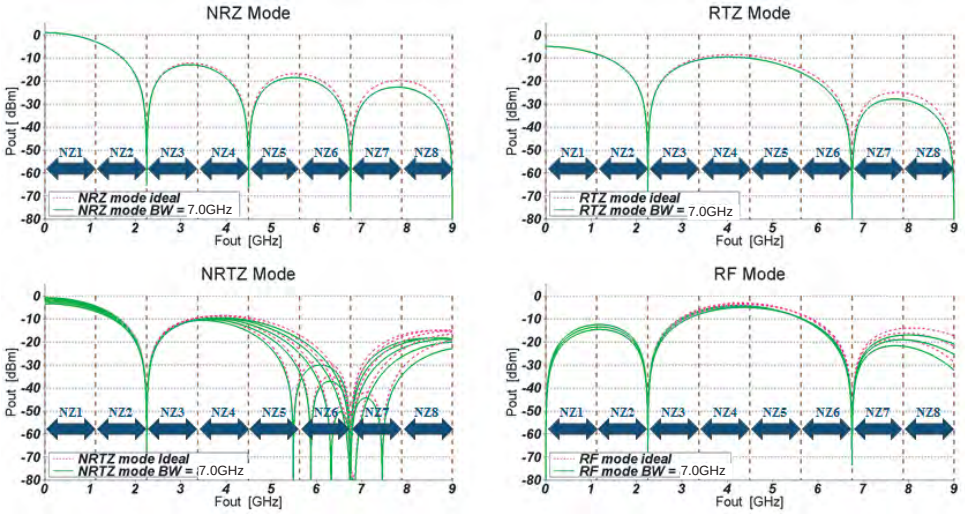
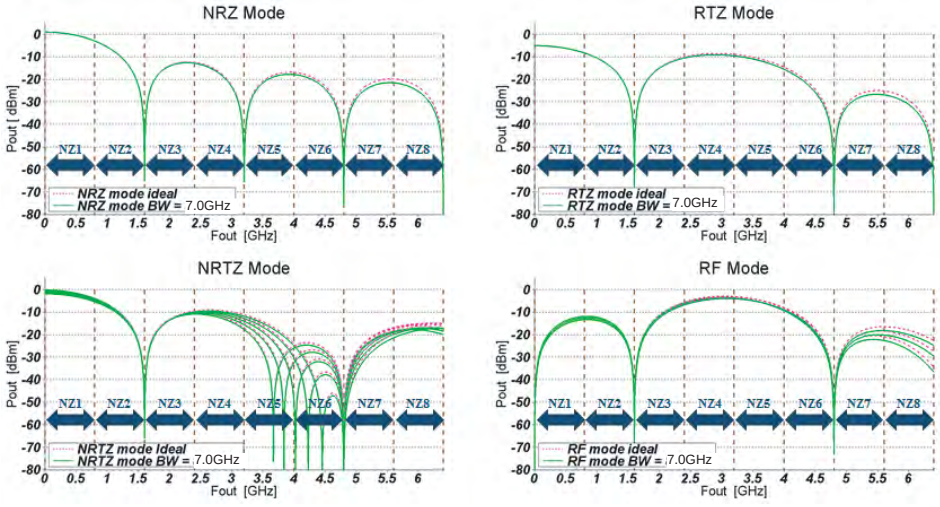


Figure 5-22. Max available Pout at nominal gain vs Fout in the four output modes at 3.2 GSps, combined with IUCM2, over eight Nyquist zones, computed for different RPW steps



© e2v technologies (uk) limited 2016

Figure 5-23. Max available Pout at nominal gain vs Fout in the four output modes at 4.5 GSps, combined with IUCM4, over 16 Nyquist zones, computed for different RPW steps

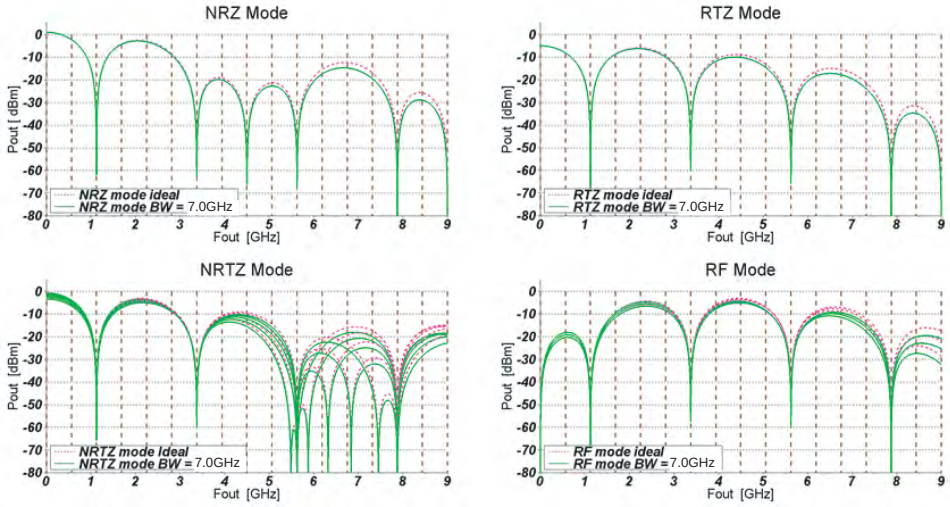
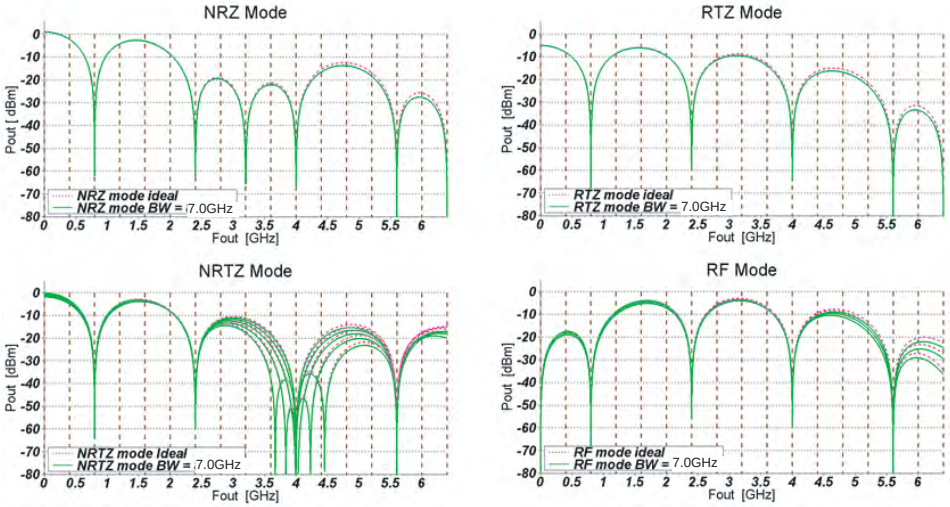


Figure 5-24. Max available Pout at nominal gain vs Fout in the four output modes at 3.2 GSps, combined with IUCM4, over 16 Nyquist zones, computed for different RPW steps



5.7 Synchronization FPGA-DAC: IDC_P, IDC_N and TVF function

- IDC_P, IDC_N: Input Data Check function (LVDS signal).
- TVF: Setup/Hold Time Violation Flag.

The IDC_P, IDC_N signal are LVDS signals. This signal should be toggling at each cycle synchronously with other data bits.

This signal should be generated by the FPGA so that the DAC can check in real-time if the timings between the FPGA and the DAC are correct. The information on the synchronisation is then given by the TVF flag.

IDC should be routed as the data signals (same layout rules and same length). It should be driven to an LVDS low or high level if not used.

© e2v technologies (uk) limited 2016

Figure 5-25. IDC timing vs data input:

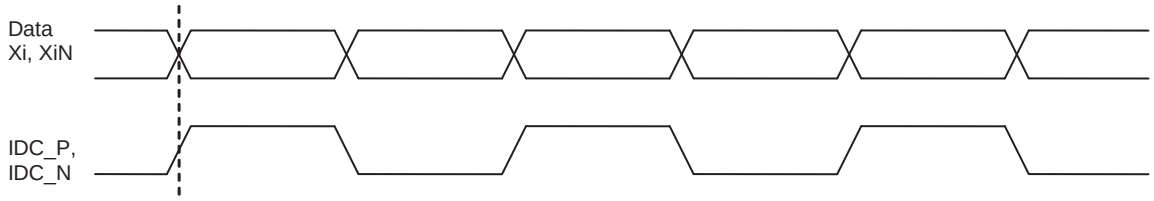
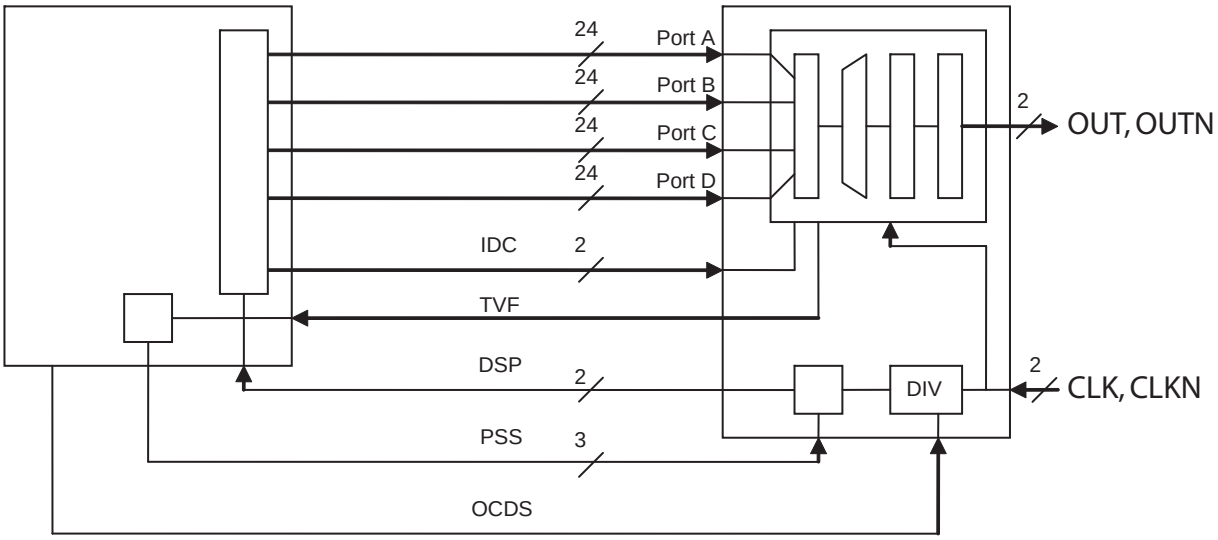


Figure 5-26. FPGA to DAC synoptic



TVF is a 3.3V output signal that indicates if the DAC and the FPGA are synchronised.

Table 5-5. TVF coding table

Label	Value	Description
TVF	0	SYNCHRO OK
	1	Data setup or hold time violation detected

Principle of Operation:

The IDC signal is sampled in parallel by 2 clocks. One is delayed positively by half a clock period, the other one is delayed negatively by half a clock period. The result of the sampling of the IDC input by both these clocks is then compared.

If both sampled outputs are equivalent, then TVF is at "0" to indicate that DAC and FPGA are synchronised. If not, TVF is set to "1" which means that the edge of the internal sampling clock is inside this window.

In that case it is recommended to either:

- Shift the DSP clock timing (possible by using the PSS function inside the DAC).
- Shift the phase of the FPGA PLL (if this functionality is available in the FPGA) to change the timing of the digital data compared to the DAC clock.

© e2v technologies (uk) limited 2016

5.8 DSP output clock

The DSP output clock DSP, DSPN is an LVDS signal which is used to synchronize the FPGA generating the digital patterns with the DAC sampling clock.

The DSP clock frequency is a fraction of the sampling clock frequency. The division factor depends on OCDS and IUCM settings. The DSP clock frequency is equal to (sampling frequency / [2N*X*M]) where N is the MUX ratio (2 or 4) and X is the output clock division factor (1 or 2), determined by the OCDS bit and M is the IUCM division ratio (1, 2 or 4) determined by the IUCM bits.

For example, in a 4:1 MUX ratio application with a sampling clock at 4 GHz and OCDS set to "0" (i.e. Factor of 1) and in IUCM1, then the input data rate is 1000 MSps and the DSP clock frequency is 500 MHz.

This DSP clock is used in the FPGA to control the digital data sequencing. Its phase can be adjusted thanks to the PSS[2:0] bits in order to ensure a proper synchronization between the data coming to the DAC and the sampling clock.
The TVF bit should be used to check whether the timing between the FPGA and the DAC is correct. TVF bit will indicate whether the DAC and FPGA are aligned or not. PSS bits should then be used to shift the DSP clock and thus the input data of the DAC, so that a correct timing is achieved between the FPGA and the DAC.

5.9 OCDS, IUCM and MUX combinations summary

The table here after gives the DSP clock division ratio with respect to the DAC input clock.

DSPclk=F_{CLK}/(2*N*M*X)
DataRate=F_{CLK}/(N*M)

Where N: MUX Ratio (2 or 4), M: IUCM Ratio (1, 2 or 4), X: OCDS Ratio (1 or 2)

Table 5-6. OCDS, MUX, IUCM and PSS combinations summary

MUX Ratio		IUCM Ratio		OCDS Ratio		PSS Range / Steps	Input Data Rate
4:1	0	IUCM1	00	OCDS1: DSP Clock = F_{CLK}/8	0	0 to 7/(2*F_{CLK}) 1/(2*F_{CLK}) steps	F_{CLK}/4
				OCDS2: DSP Clock = F_{CLK}/16	1		
		IUCM2	10	OCDS1: DSP Clock = F_{CLK}/16	0	0 to 7/(2*F_{CLK}) 1/(2*F_{CLK}) steps	F_{CLK}/8
				OCDS2: DSP Clock = F_{CLK}/32	1		
		IUCM4	11	OCDS1: DSP Clock = F_{CLK}/32	0	0 to 7/(2*F_{CLK}) 1/(2*F_{CLK}) steps	F_{CLK}/16
				OCDS2: DSP Clock = F_{CLK}/64	1		
2:1	1	IUCM1	00	OCDS1: DSP Clock = F_{CLK}/4	0	0 to 7/(2*F_{CLK}) 1/(2*F_{CLK}) steps	F_{CLK}/2
				OCDS2: DSP Clock = F_{CLK}/8	1		
		IUCM2	10	OCDS1: DSP Clock = F_{CLK}/8	0	0 to 7/(2*F_{CLK}) 1/(2*F_{CLK}) steps	F_{CLK}/4
				OCDS2: DSP Clock = F_{CLK}/16	1		
		IUCM4	11	OCDS1: DSP Clock = F_{CLK}/16	0	0 to 7/(2*F_{CLK}) 1/(2*F_{CLK}) steps	F_{CLK}/8
				OCDS2: DSP Clock = F_{CLK}/32	1		

Notes: 1. Behaviour according to MUX, OCDS, IUCM and PSS combination is independent of output mode.
2. In 2:1 MUX, only 4 steps of PSS are useful, the 4 other gives the same result.

© e2v technologies (uk) limited 2016

5.10 Synchronisation function

The timer of the DAC must be reset after the following changes of configuration:

- At power-on;
- Whenever one of the following parameter is modified: OCDS, MUX or IUCM;
- Whenever the master clock is modified (amplitude, frequency...).

There are two SYNC functions integrated in this DAC which reset its timer:

- A power up reset, which is triggered by the power supplies if the dedicated power up sequence is applied V_{CCD} -> V_{CCA3} ->V_{CCA5} (the clock must be supplied to the DAC prior to this power up sequence being generated);
- An external SYNC, which is triggered by a pulse applied to the differential SYNC/SYNCN inputs.

At power-on, there are 2 possibilities:

- The power-up sequence of the DAC is V_{CCD}, V_{CCA3} then V_{CCA5}. In that case an internal power on reset is generated by the DAC. There is no need to send a SYNC pulse as long as OCDS, MUX or IUCM and the master clock are not modified (see Section 8.8 on page 69 for more information).
- If the power-up sequence is different from the one above, a SYNC pulse must be sent to the DAC.

The external SYNC is LVDS compatible. It is active high. After the application of the SYNC signal, the DSP clock from the DAC will stop and after a constant and known time (t_{DSP}); the DSP clock will start up again.

The external SYNC can also be used to synchronize multiple DACs.

The pulse duration should be at least of 3 master clock cycles in OCDS1 and IUCM1.

Depending on the settings of OCDS, IUCM, PSS and also on the MUX ratio the width of the SYNC pulse must be greater than a certain number of external clock pulses. It is also necessary that the sync pulse width shall be a whole number of clock cycles.

5.11 Gain Adjust function

This function allows the adjustment of the internal gain of the DAC so that it can be tuned to the unity gain.

The gain of the DAC can be adjusted by setting the GAIN register through the 3WSI. The gain can be adjusted by 1024 steps. GA min is given for GAIN = 0x000 and GA max for GAIN = 0x3FF. Default value is GA typ given for GAIN = 0x200.

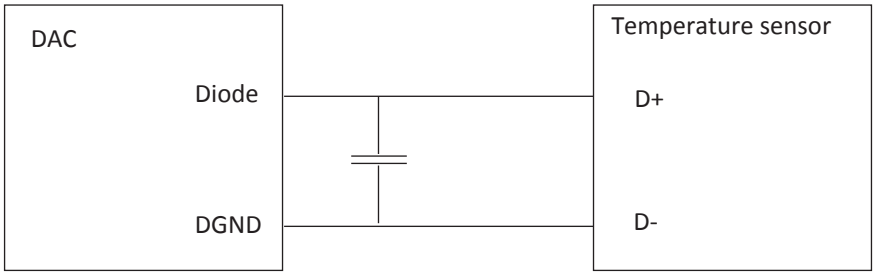
Note: The gain voltage step is indicated in Section 3.3 on page 5 Table 3-3.

© e2v technologies (uk) limited 2016

5.12 Diode function

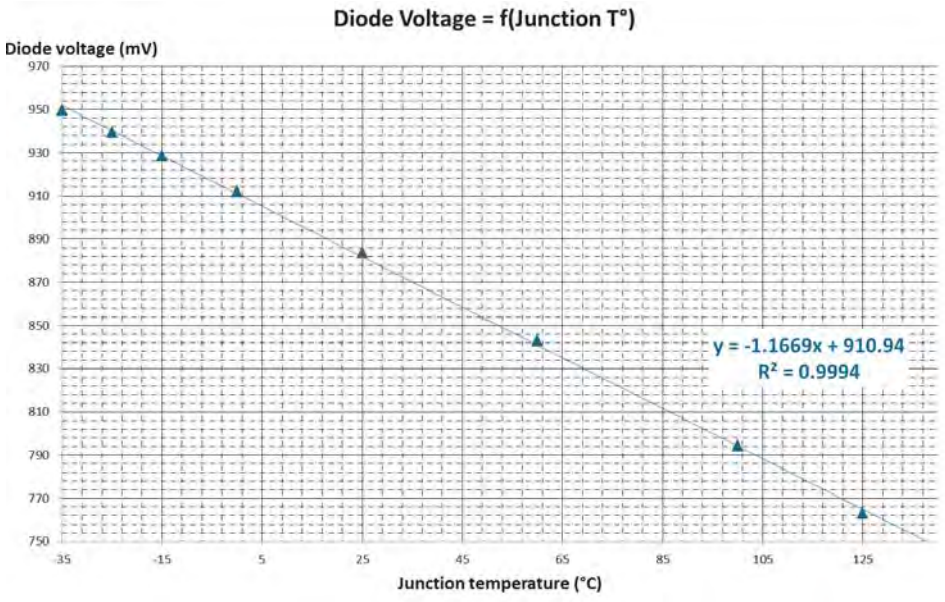
A diode for die junction temperature monitoring, is available in this DAC. For the measurement of die junction temperature, a temperature sensor can be used.

Figure 5-27. Temperature diode implementation



In characterization measurement a current of 1 mA is applied on the DIODE pin. The voltage across the DIODE pin and the DGND pin gives the junction temperature using the intrinsic diode characteristics below

Figure 5-28. Diode Characteristics for Die Junction Temperature Monitoring



© e2v technologies (uk) limited 2016

5.13 DAC 3WSI Description (DAC Controls)

5.13.1 3WSI timing description

The 3WSI is a synchronous write only serial interface made of 4 signals:

"reset_n": asynchronous 3WSI reset, active low
"sclk": serial clock input
"sld_n": serial load enable input
"sdata": serial data input.

The 3WSI gives a "write-only" access to up to 16 different internal registers of up to 12 bits each. The input format is fixed with 4 bits of register address followed by 12 bits of data. Address and data are sent MSB first.

The write procedure is fully synchronous with the clock rising edge of "sclk" and described in the following chronogram.

"sld_n" and "sdata" are sampled on each rising clock edge of "sclk" (clock cycle).
"sld_n" must be set at "1" when no write procedure is done.

A write starts on the first clock cycle when "sld_n" is at "0". "sld_n" must stay at "0" during the complete write procedure.

In the first 4 clock cycles with "sld_n" at "0", 4 bits of register address from MSB (a[3]) to LSB (a[0]) are entered.

In the next 12 clock cycles with "sld_n" at "0", 12 bits of data from MSB (d[11]) to LSB (d[0]) are entered.

This gives 16 clock cycles with "sld_n" at "0" for a normal write procedure.

A minimum of one clock cycle with "sld_n" returned at "1" is requested to end the write procedure, before the interface is ready for a new write procedure. Any clock cycle with "sld_n" at "1" before the write procedure is completed interrupts this procedure and no data transfer to internal registers is done. It is possible to have only one clock cycle with "sld_n" at "1" between two following write procedures. Additional clock cycles with "sld_n" at "0" after the parallel data have been transferred to the register do not affect the write procedure and are ignored.

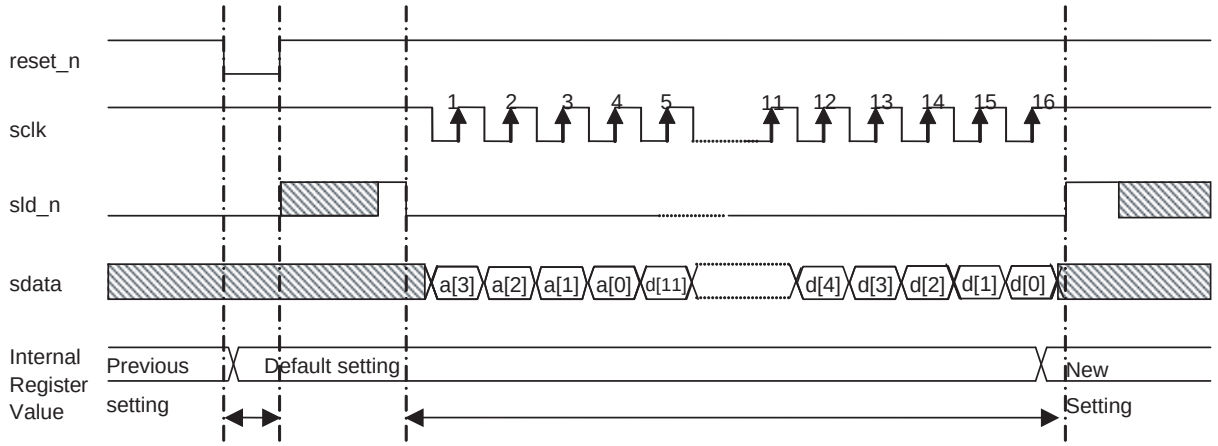
12 bits of data must always be sent, even if the internal addressed register has less than 12 bits. Unused bits (usually MSB's) are ignored. Bit signification and bit position for the internal registers are detailed in the section "Registers".

The "reset_n" pin combined with the "sld_n" pin can be used as a reset to program the chip to the "reset setting".

"reset_n" high: no effect
"reset_n" low and "sld_n" low: programming of registers to default values

© e2v technologies (uk) limited 2016

Figure 5-29. 3WSI Timing Diagram



Timings related to 3WSI are given in the table below

Table 5-7. 3WSI Timings

Name	Parameter	Min	Typ	Max	Unit	Note
Tsclk	Period of sclk	1			µs	
Twsclk	High or low time of sclk	0.5			µs	
Tssld_n	Setup time of sld_n before rising edge of sclk	4			µs	
Thsld_n	Hold time of sld_n after rising edge of sclk	2			µs	
Tssdata	Setup time of sdata before rising edge of sclk	4			ns	
Thsdata	Hold time of sdata after rising edge of sclk	2			ns	
Twlreset	Minimum low pulse width of reset_n	5			ns	
Tdreset	Minimum delay between an edge of reset_n and the rising edge of sclk	5			µs	

© e2v technologies (uk) limited 2016

5.13.2 3WSI: Address and Data Description

This 3WSI is activated with the control bit sld_n going low (please refer to "write timing" in next section).

The length of the word is 16 bits: 12 for the data and 4 for the address.

The maximum serial logic clock frequency is 1 MHz.

Table 5-8. Registers Mapping

Address	Label	Description	Default Setting
0000	State Register	MUX ratio Selection Output MODE selection IUCM ratio selection External Control for DSP Clock Reshaping Pulse Width (RPW) adjust Reshaping Pulse Begin (RPB) adjust	0x922
0001	GA Register	Gain Adjust register	0x200
0010		Not available	
0011		Not available	
0100		Not available	
0101	DSP Register	PSS, OCDS controls	0x080
0110		Not available	
0111		Not available	
1000 to 1111		Not available	

© e2v technologies (uk) limited 2016

5.13.3 State Register (address 0000)

Table 5-9. State register Mapping (Address 0000)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RPW<2:0>			RPB<2:0>			ECDC	IUCM<1:0>		MODE<1:0>		MUX

Default value: 0x922

Table 5-10. State register Coding (Address 0000)

Label		Coding	Description	Default Value	Notes
MUX	D0	0	4:1 MUX mode	0	(1)
		1	2:1 MUX mode		
MODE<1:0>	D1, D2	00	NRZ mode	01	(1)
		01	Narrow RTZ (a.k.a. NRTZ) mode		
		10	RTZ Mode		
		11	RF mode		
IUCM<1:0>	D3,D4	00	IUCM1 (MUX at DAC core speed)	00	(1)
		01	IUCM1 (MUX at DAC core speed)		
		10	IUCM2 (MUX at DAC core speed/2)		
		11	IUCM4 (MUX at DAC core speed/4)		
ECDC	D5	0	OCDS and PSS ruled by DSP register at address 0101	1	(1)(2)
		1	OCDS and PSS externally controlled		
RPB<2:0>	D6, D7, D8	000	RPB2 = 38 ps	100	(3)
		001	RPB2 = 38 ps		
		010	RPB0 = 12 ps		
		011	RPB1 = 25 ps		
		100	RPB2 = 38 ps		
		101	RPB3 = 51 ps		
		110	RPB4 = 64ps		
		111	RPB2 = 38 ps		
RPW<2:0>	D9, D10, D11	000	RPW2 66 ps in NRTZ mode / 68 ps in RF mode	100	(4)
		001	RPW2 66 ps in NRTZ mode / 68 ps in RF mode		
		010	RPW0 43 ps in NRTZ mode / 52 ps in RF mode		
		011	RPW1 49 ps in NRTZ mode / 60 ps in RF mode		

© e2v technologies (uk) limited 2016

Table 5-10. State register Coding (Address 0000) (Continued)

Label		Coding	Description	Default Value	Notes
		100	RPW2 66 ps in NRTZ mode / 68 ps in RF mode		
		101	RPW3 78 ps in NRTZ mode / 86 ps in RF mode		
		110	RPW4 100 ps in NRTZ mode / 110 ps in RF mode		
		111	RPW2 66 ps in NRTZ mode / 68 ps in RF mode		

Notes:
1. Default mode is 4:1 MUX, NRTZ output mode, IUCM1, and PSS & OCDS externally controlled. Default mode is programmed by power up reset or low level pulse on *reset_n* pin while *sld_n* pin is low.
2. ECDC: when ECDC is High the timing of the DSP clock is controlled externally through pins PSS<2:0> and OCDS; when ECDC is low, this functionality is controlled through the 3WSI by the DSP register at address 0101.
3. RPB setting is applicable in NRTZ, RTZ and RF modes. RPB values are design values.
4. RPW setting is applicable in NRTZ and RF modes. RPW values are typical values measured on 1 part.

5.13.4 GA Register (address 0001)

Table 5-11. GA register Mapping (Address 0001)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		GA<9:0>									

Default value: 0x200

5.13.5 DSP Register (address 0101)

Table 5-12. DSP register Mapping (Address 0101)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				<reserved>			PSS<2:0>				OCDS

Default value: 0x080 (OCDS = 0, PSS = 000)

© e2v technologies (uk) limited 2016

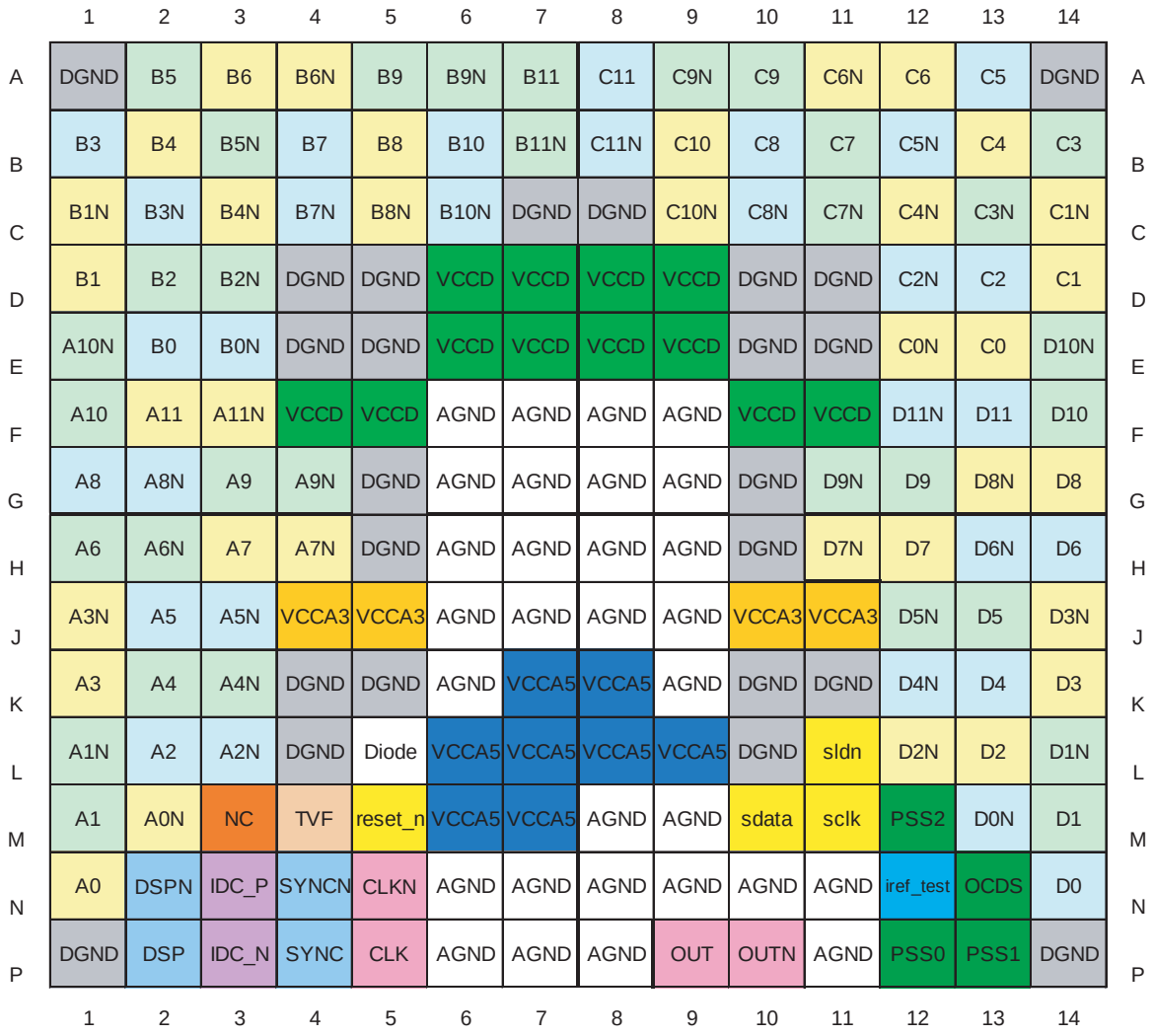
Table 5-13. Registers 0000 to 0101 Summary

Address	Description	Default register value	Default parameter value	Register value for max value	Parameter max value	Register value for min value	Parameter min value	Step
0000	RPB Adjust	0x922	RPB2	0x9A2	RPB4	0x8A2	RPB0	1bit
0000	RPW Adjust	0x922	RPW2	0xD22	RPW4	0x522	RPW0	1bit
0000	ECDC	0x922	ECDC1	0x922	ECDC1	0x902	ECDC0	N/A
0000	IUCM	0x922	IUCM1	0x93A	IUCM4	0x922	IUCM1	N/A
0000	MODE	0x922	NRTZ	0x926	RF	0x920	NRZ	N/A
0000	MUX	0x922	4:1 MUX	0x923	2:1 MUX	0x922	4:1 MUX	N/A
0001	Gain Adjust	0x200	1	0x3FF	1.15	0x000	0.85	300ppm
0101	PSS	0x080	PSS0	0x09C	PSS7	0x080	PSS0	N/A
0101	OCDS	0x080	OCDS1	0x081	OCDS2	0x080	OCDS1	N/A

© e2v technologies (uk) limited 2016

6. PIN DESCRIPTION

Figure 6-1. Pinout view fpBGA196 (Top view)



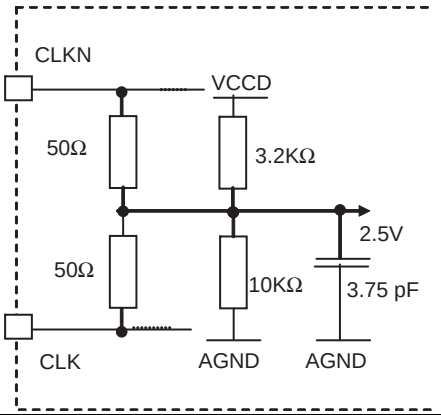
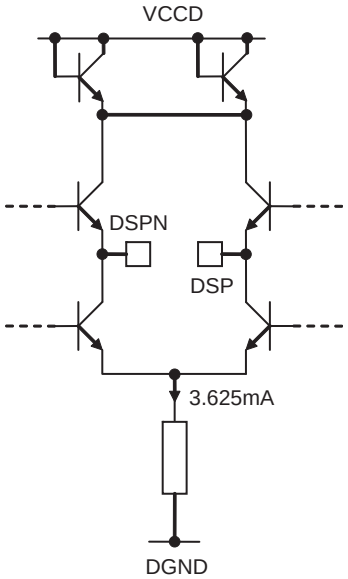
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DGND	B5	B6	B6N	B9	B9N	B11	C11	C9N	C9	C6N	C6	C5	DGND	A
B	B3	B4	B5N	B7	B8	B10	B11N	C11N	C10	C8	C7	C5N	C4	C3	B
C	B1N	B3N	B4N	B7N	B8N	B10N	DGND	DGND	C10N	C8N	C7N	C4N	C3N	C1N	C
D	B1	B2	B2N	DGND	DGND	VCCD	VCCD	VCCD	VCCD	DGND	DGND	C2N	C2	C1	D
E	A10N	B0	B0N	DGND	DGND	VCCD	VCCD	VCCD	VCCD	DGND	DGND	C0N	C0	D10N	E
F	A10	A11	A11N	VCCD	VCCD	AGND	AGND	AGND	AGND	VCCD	VCCD	D11N	D11	D10	F
G	A8	A8N	A9	A9N	DGND	AGND	AGND	AGND	AGND	DGND	D9N	D9	D8N	D8	G
H	A6	A6N	A7	A7N	DGND	AGND	AGND	AGND	AGND	DGND	D7N	D7	D6N	D6	H
J	A3N	A5	A5N	VCCA3	VCCA3	AGND	AGND	AGND	AGND	VCCA3	VCCA3	D5N	D5	D3N	J
K	A3	A4	A4N	DGND	DGND	AGND	VCCA5	VCCA5	AGND	DGND	DGND	D4N	D4	D3	K
L	A1N	A2	A2N	DGND	Diode	VCCA5	VCCA5	VCCA5	VCCA5	DGND	sldn	D2N	D2	D1N	L
M	A1	A0N	NC	TVF	reset_n	VCCA5	VCCA5	AGND	AGND	sdata	sclk	PSS2	D0N	D1	M
N	A0	DSPN	IDC_P	SYNCN	CLKN	AGND	AGND	AGND	AGND	AGND	AGND	iref_test	OCDS	D0	N
P	DGND	DSP	IDC_N	SYNC	CLK	AGND	AGND	AGND	OUT	OUTN	AGND	PSS0	PSS1	DGND	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Table 6-1. Pinout Table fpBGA196

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
Power supplies				
V_{CCA5}	K7, K8, L6, L7, L8, L9, M6, M7	5.0V analog power supplies Referenced to AGND	N/A	
V_{CCA3}	J4, J5, J10, J11	3.3V analog power supply Referenced to AGND	N/A	
V_{CCD}	D6, D7, D8, D9, E6, E7, E8, E9, F4, F5, F10, F11	3.3V digital power supply Referenced to DGND	N/A	

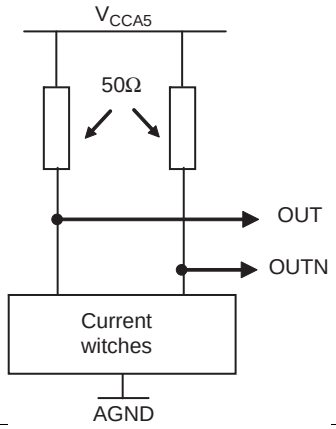
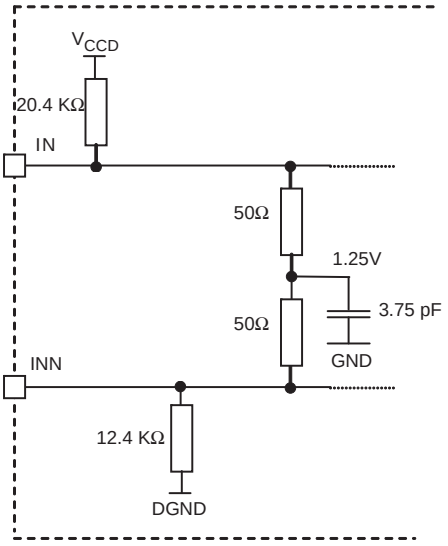
© e2v technologies (uk) limited 2016

Table 6-1. Pinout Table fpBGA196 (Continued)

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
AGND	F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9, K6, K9, M8, M9, N6, N7, N8, N9, N10, N11, P6, P7, P8, P11	Analog Ground	N/A	
DGND	A1, A14, C7, C8, D4, D5, D10, D11, E4, E5, E10, E11, G5, G10, H5, H10, K4, K5, K10, K11, L4, L10, P1, P14	Digital Ground	N/A	
Clock signals				
CLK CLKN	P5 N5	Master sampling clock input (differential) with internal common mode at 2.5V It should be driven in AC coupling. Equivalent internal differential 100Ω input resistor.	I	
DSP DSPN	P2 N2	Output clock (in-phase and inverted phase) If not used, should be 100Ω terminated	O	

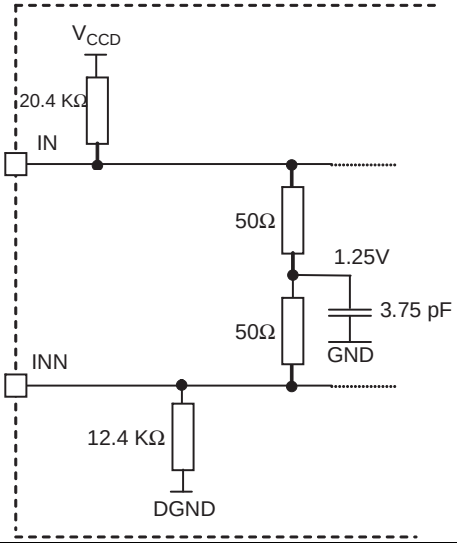
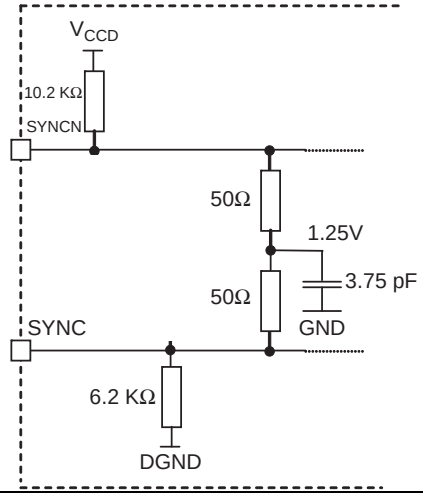
© e2v technologies (uk) limited 2016

Table 6-1. Pinout Table fpBGA196 (Continued)

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
Analog output signal				
OUT OUTN	P9 P10	In phase and inverted phase analog output signal (differential termination required)	O	
Digital Input signals				
A0, A0N A1, A1N A2, A2N A3, A3N A4, A4N A5, A5N A6, A6N A7, A7N A8, A8N A9, A9N A10, A10N A11, A11N	N1, M2 M1, L1 L2, L3 K1, J1 K2, K3 J2, J3 H1, H2 H3, H4 G1, G2 G3, G4 F1, E1 F2, F3	Differential Digital input Port A Data A0, A0N is the LSB Data A11, A11N is the MSB	I	
B0, B0N B1, B1N B2, B2N B3, B3N B4, B4N B5, B5N B6, B6N B7, B7N B8, B8N B9, B9N B10, B10N B11, B11N	E2, E3 D1, C1 D2, D3 B1, C2 B2, C3 A2, B3 A3, A4 B4, C4 B5, C5 A5, A6 B6, C6 A7, B7	Differential Digital input Port B Data B0, B0N is the LSB Data B11, B11N is the MSB	I	

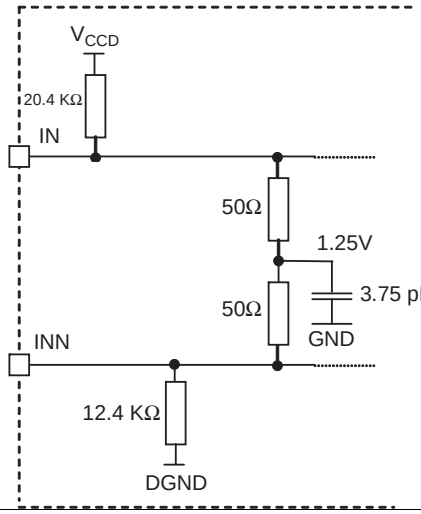
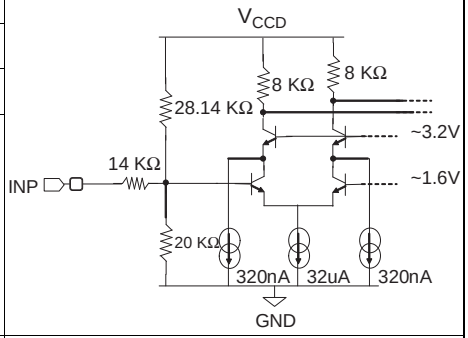
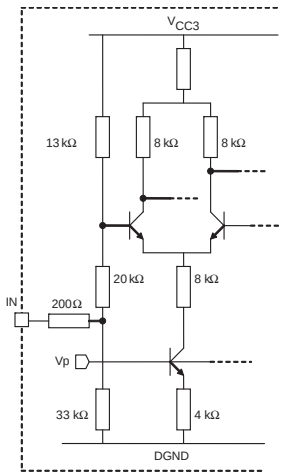
© e2v technologies (uk) limited 2016

Table 6-1. Pinout Table fpBGA196 (Continued)

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
C0, C0N C1, C1N C2, C2N C3, C3N C4, C4N C5, C5N C6, C6N C7, C7N C8, C8N C9, C9N C10, C10N C11, C11N	E13, E12 D14, C14 D13, D12 B14, C13 B13, C12 A13, B12 A12, A11 B11, C11 B10, C10 A10, A9 B9, C9 A8, B8	Differential Digital input Port C Data C0, C0N is the LSB Data C11, C11N is the MSB	I	
D0, D0N D1, D1N D2, D2N D3, D3N D4, D4N D5, D5N D6, D6N D7, D7N D8, D8N D9, D9N D10, D10N D11, D11N	N14, M13 M14, L14 L13, L12 K14, J14 K13, K12 J13, J12 H14, H13 H12, H11 G14, G13 G12, G11 F14, E14 F13, F12	Differential Digital input Port D Data D0, D0N is the LSB Data D11, D11N is the MSB	I	
Control signals				
SYNC, SYNCN	P4 N4	In phase and Inverted phase reset signal	I	

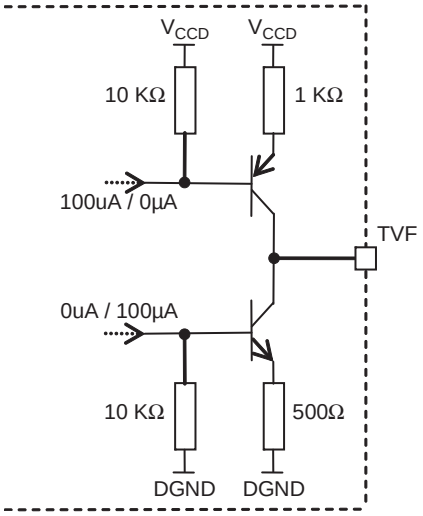
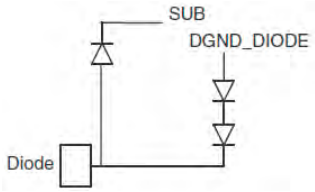
© e2v technologies (uk) limited 2016

Table 6-1. Pinout Table fpBGA196 (Continued)

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
IDC_P, IDC_N	N3 P3	Input data check	I	
sdata	M10	3WSI serial data input.	I	
sclk	M11	3WSI clock.		
reset_n	M5	Reset for the 3WSI registers		
sld_n	L11	3WSI serial load enable input.		
OCDS	N13	Output Clock Division Select	I	Driven by resistor: 10Ω or 10 KΩ Driven by voltage: <0.5 V or > 2 V
PSS0 PSS1 PSS2	P12 P13 M12	Phase Shift Select (PSS2 is the MSB)		

© e2v technologies (uk) limited 2016

Table 6-1. Pinout Table fpBGA196 (Continued)

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
TVF	M4	Setup/Hold time violation flag	O	
Diode	L5	Diode for die junction temperature monitoring	I	
Iref test	N12	Bandgap output for test purpose. To leave unconnected	O	
NC	M3	Not connected		

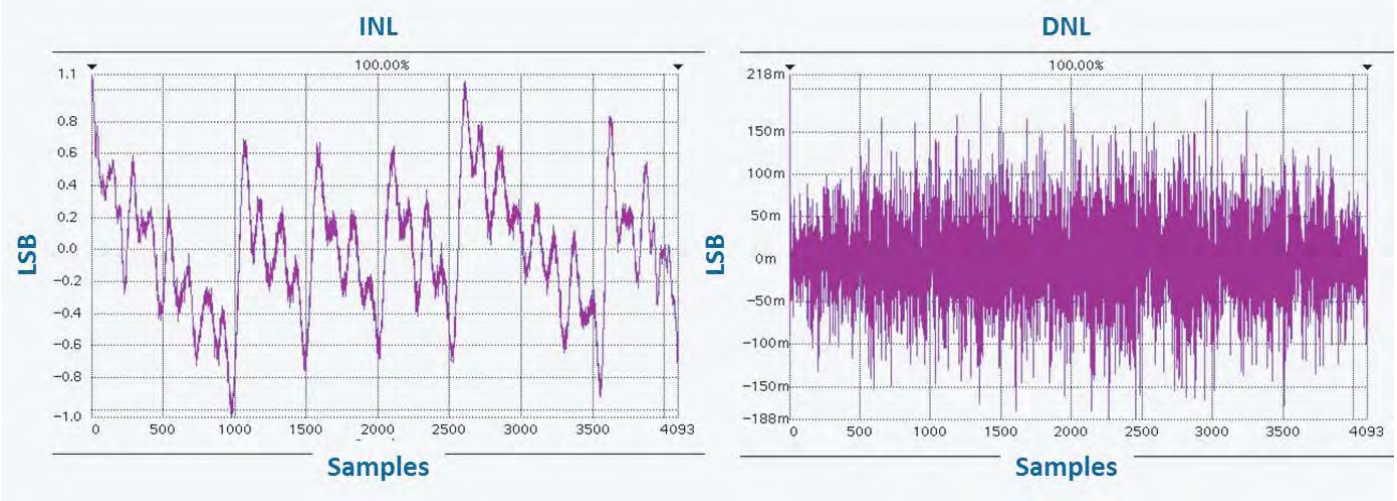
© e2v technologies (uk) limited 2016

7. CHARACTERIZATION RESULTS

7.1 Static performances

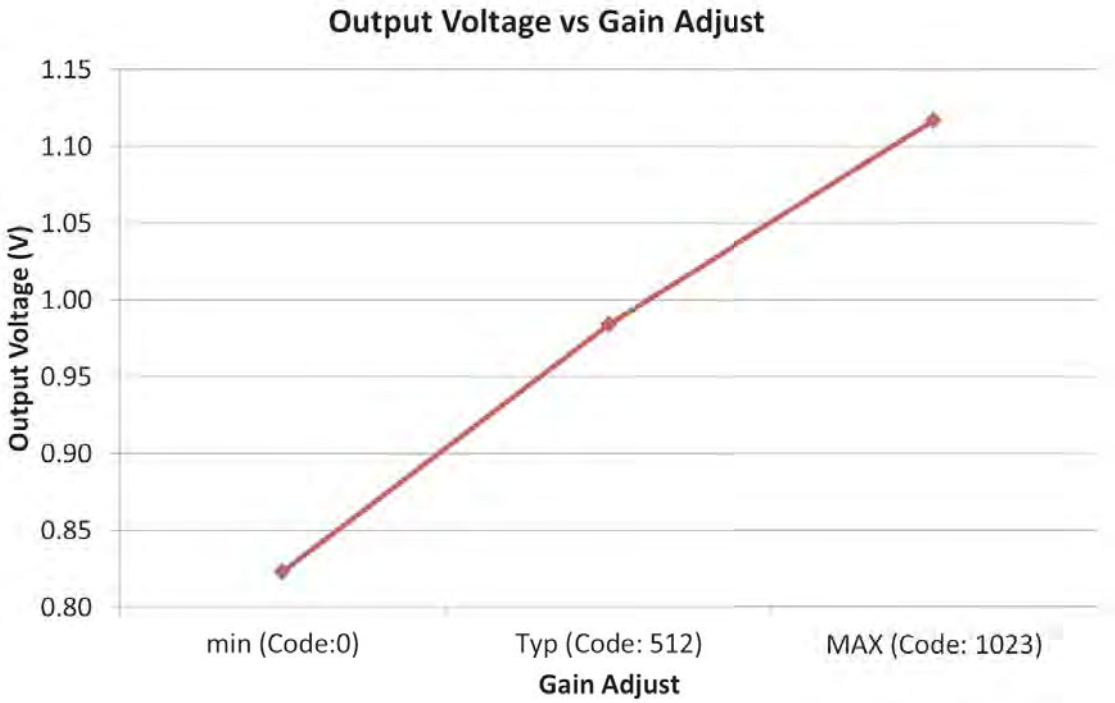
7.1.1 INL/DNL

Figure 7-1. INL & DNL measurements at Fout = 100kHz, Fclock = 3GHz



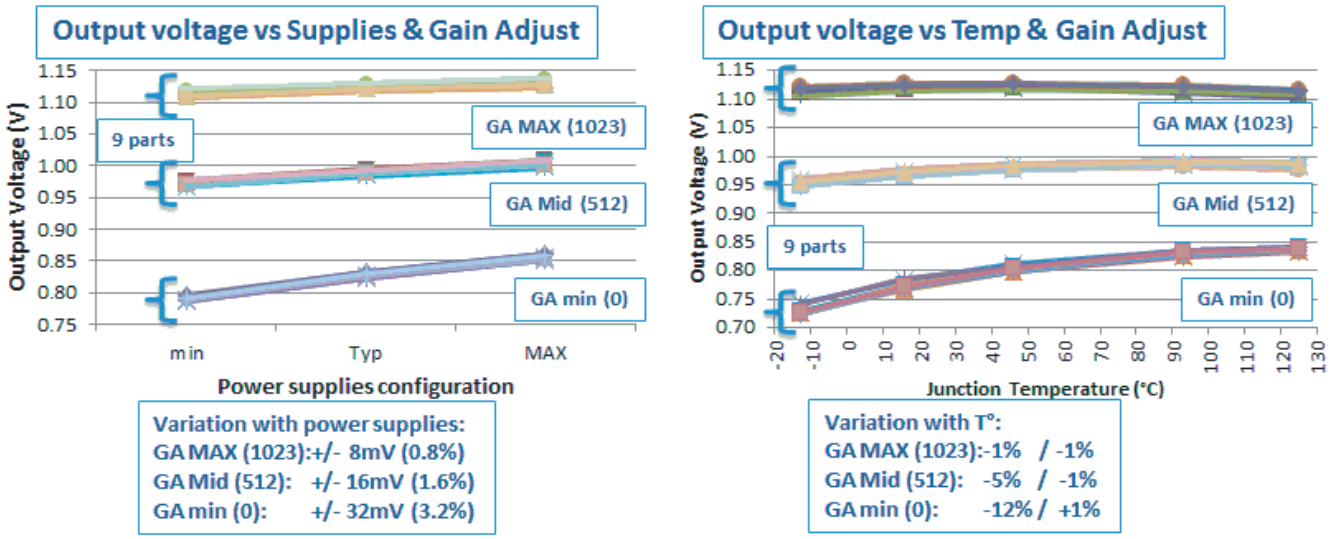
7.1.2 DC Gain

Figure 7-2. Output Voltage variations versus Gain Adjust



© e2v technologies (uk) limited 2016

Figure 7-3. Output voltage variation vs Power supplies & temperature vs Gain Adjust



7.2 AC performances

7.2.1 Available Output Power vs Fout.

NRZ mode offers max power for 1st Nyquist operation.
NRTZ mode offers optimum power over full 1st and first half of 2nd Nyquist zones.
RTZ mode offers slow roll off for 2nd Nyquist operation.
RF mode offers maximum power over 2nd and 3rd Nyquist operation.

© e2v technologies (uk) limited 2016

Figure 7-4. Pout vs Fout from 45MHz to 6705MHz in the 4 output modes at 4.5GSps in MUX4:1

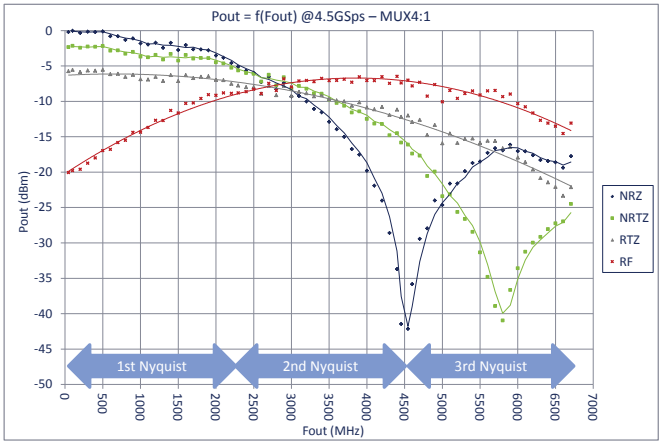


Figure 7-5. Pout vs Fout from 32MHz to 4768MHz in the 4 output modes at 3.2GSps in MUX2:1

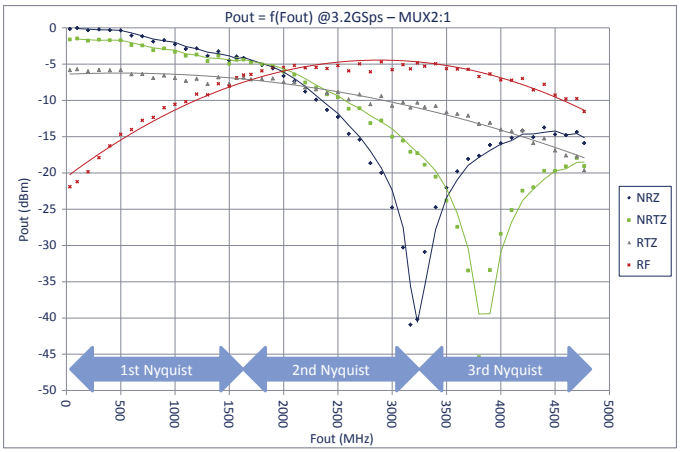


Figure 7-6. Pout vs Fout from 45MHz to 6705MHz and from 3.7GSps to 4.5GSps in NRZ mode in MUX4:1

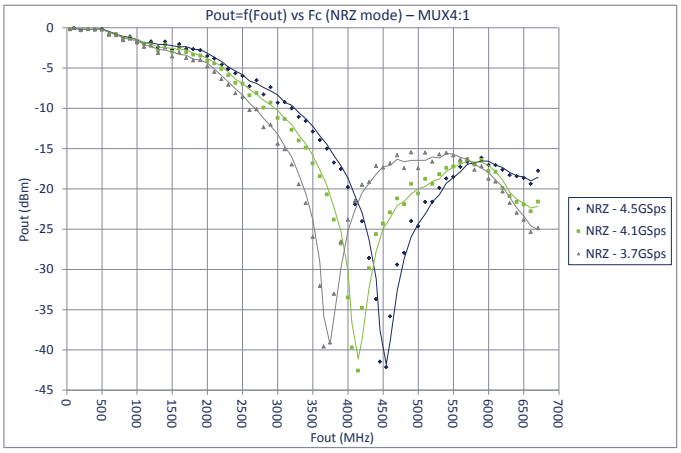


Figure 7-7. Pout vs Fout from 45MHz to 6705MHz and from 3.7GSps to 4.5GSps in NRTZ mode in MUX4:1

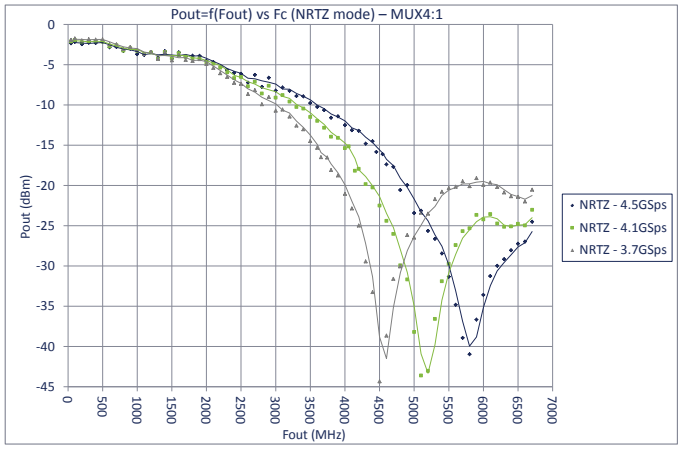


Figure 7-8. Pout vs Fout from 45MHz to 6705MHz and from 3.7GSps to 4.5GSps in RTZ mode in MUX4:1

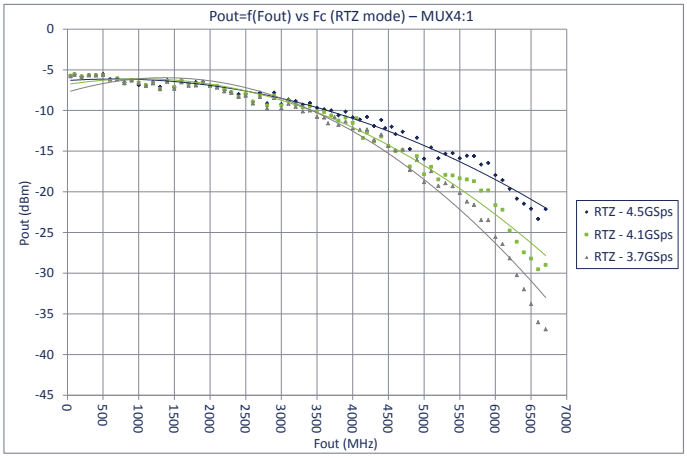
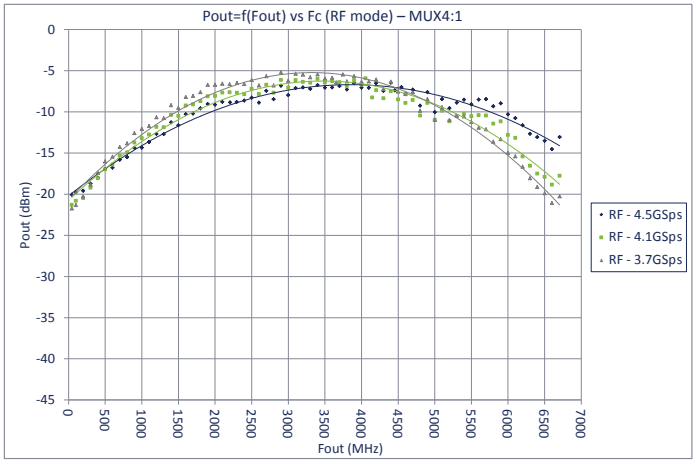


Figure 7-9. Pout vs Fout from 45MHz to 6705MHz and from 3.7GSps to 4.5GSps in RF mode in MUX4:1



© e2v technologies (uk) limited 2016

7.2.2 Single Tone Measurements

The following plots summarize characterization results in MUX4:1 mode, for an Fout sweep from 45 MHz to 6705 MHz (step 100 MHz).

The following plots summarize characterization results in MUX2:1 mode, for an Fout sweep from 32 MHz to 4768 MHz (step 100 MHz).

Figure 7-10. SFDR in the 4 output modes at 4.5GSps in MUX4:1

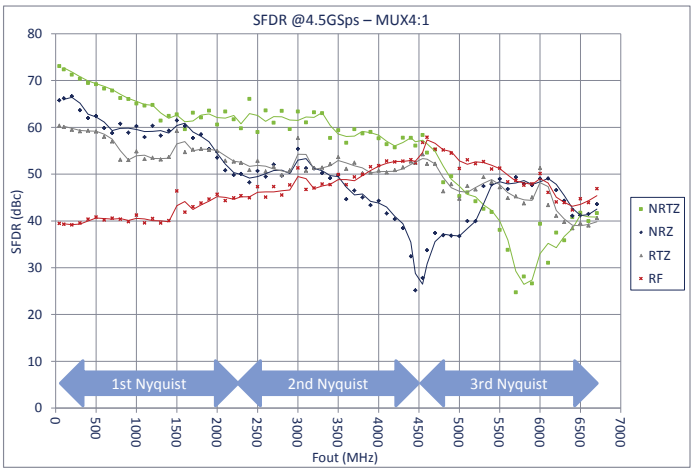
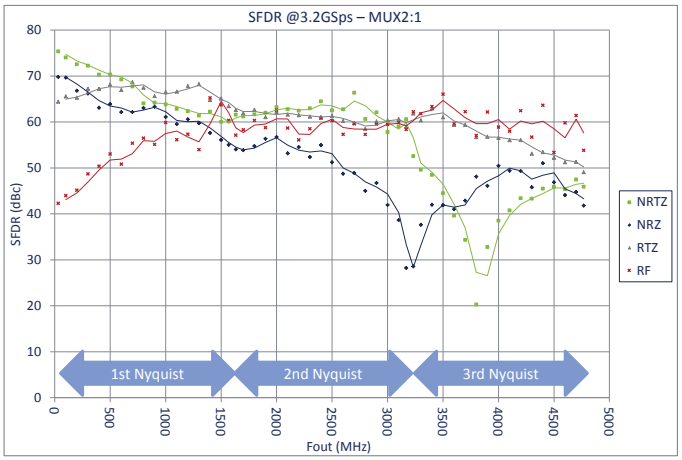


Figure 7-11. SFDR in the 4 output modes at 3.2GSps in MUX2:1



7.2.3 Single tone measurements: typical spectra

The following figures show typical SFDR spectra obtained for the four DAC modes on an EV12DS400A device.

Conditions: typical power supplies, ambient temperature, MUX4:1 with Fs = 4.5 Gsps or MUX2:1 with Fs= 3.2 Gsps.

7.2.3.1 MUX 4:1

Figure 7-12. Typical SFDR spectrum in NRZ mode. Fout = 45MHz (1st Nyquist), MUX4:1, Fs = 4.5Gsps. SFDR = 67dBc

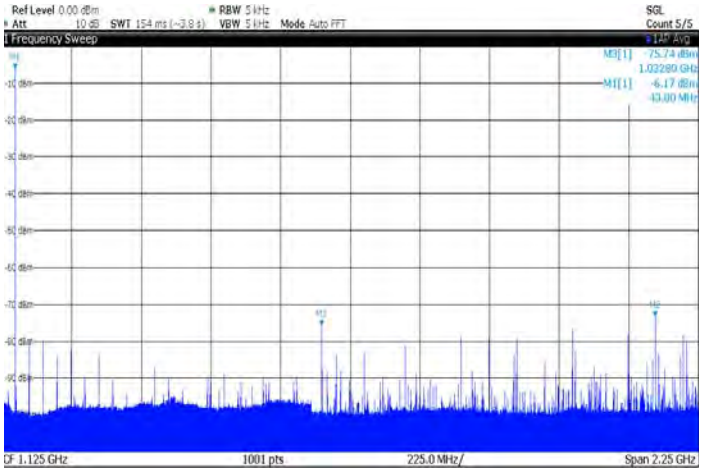
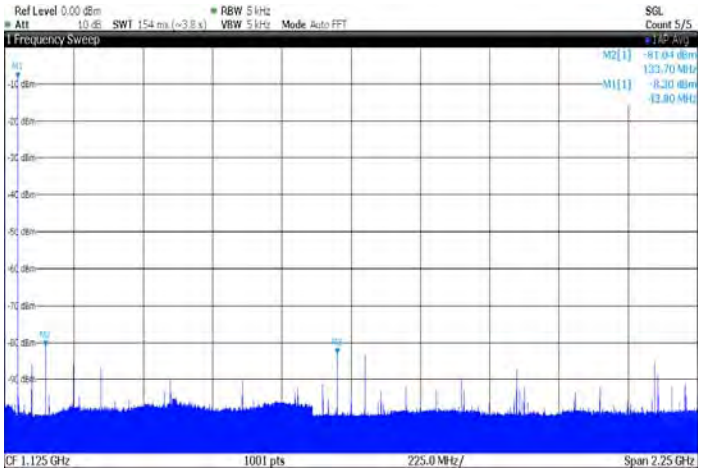


Figure 7-13. Typical SFDR spectrum in NRTZ mode. Fout = 45MHz (1st Nyquist), MUX4:1, Fs = 4.5Gsps. SFDR = 73 dBc



© e2v technologies (uk) limited 2016

Figure 7-14. Typical SFDR spectrum in NRTZ mode. Fout = 2205MHz (1st Nyquist), MUX4:1, Fs = 4.5Gsps. SFDR = 60 dBc

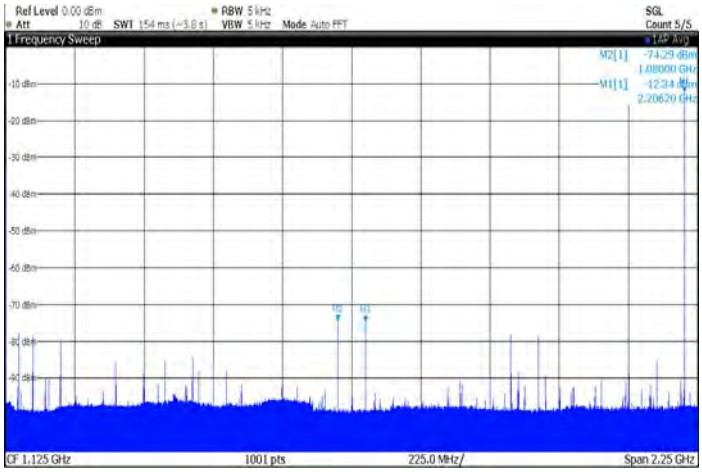


Figure 7-15. Typical SFDR spectrum in RTZ mode. Fout = 4455MHz (2nd Nyquist), MUX4:1, Fs = 4.5Gsps. SFDR = 53 dBc

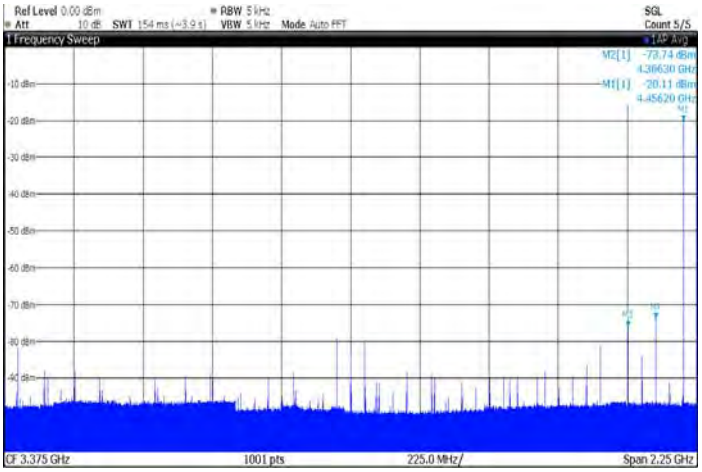


Figure 7-16. Typical SFDR spectrum in RF mode. Fout = 4455MHz (2nd Nyquist), MUX4:1, Fs = 4.5Gsps. SFDR = 58 dBc

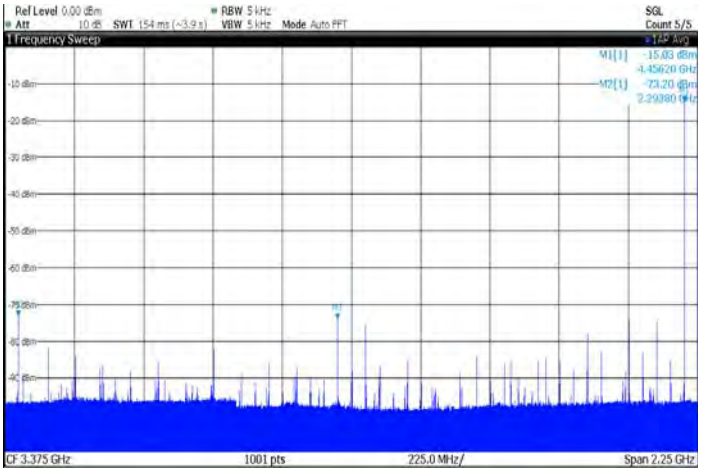
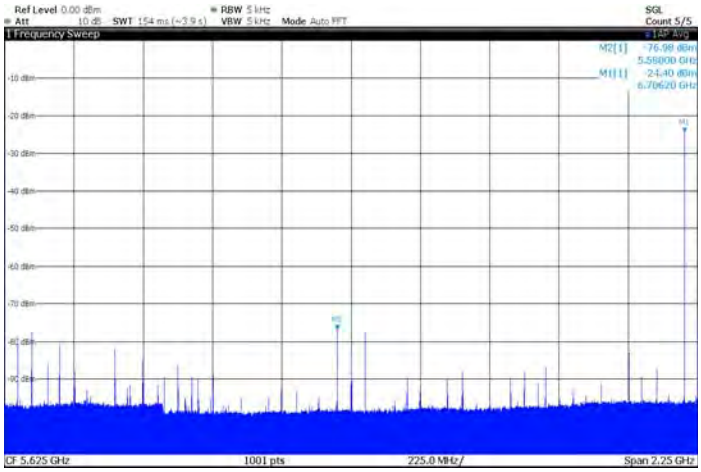


Figure 7-17. Typical SFDR spectrum in RF mode. Fout = 6705MHz (3rd Nyquist), MUX4:1, Fs = 4.5Gsps. SFDR = 52 dBc



© e2v technologies (uk) limited 2016

7.2.3.2 MUX 2:1

Figure 7-18. Typical SFDR spectrum in NRZ mode. Fout = 32MHz (1st Nyquist), MUX2:1, Fs = 3.2Gsps. SFDR = 70 dBc

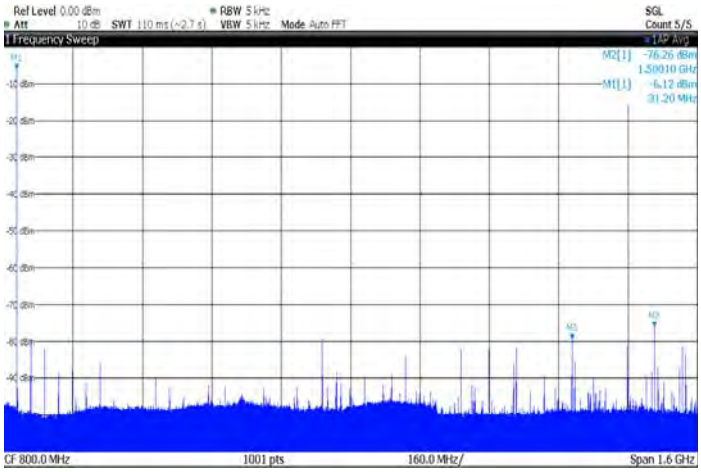


Figure 7-19. Typical SFDR spectrum in NRTZ mode. Fout = 32MHz (1st Nyquist), MUX2:1, Fs = 3.2Gsps. SFDR = 76 dBc

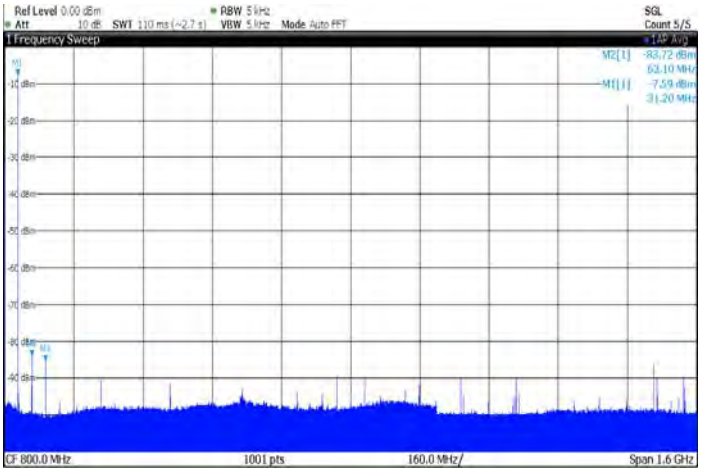
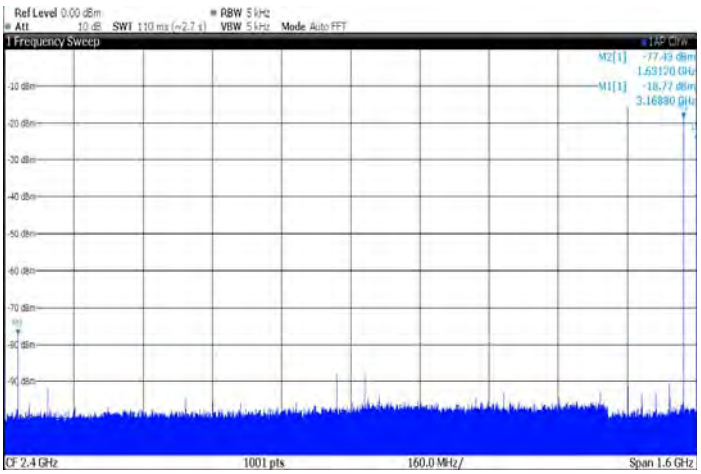


Figure 7-20. Typical SFDR spectrum in NRTZ mode. Fout = 1568MHz (1st Nyquist), MUX2:1, Fs = 3.2Gsps. SFDR = 65 dBc

Figure 7-21. Typical SFDR spectrum in RTZ mode. Fout = 3168MHz (2nd Nyquist), MUX2:1, Fs = 3.2Gsps. SFDR = 59 dBc



© e2v technologies (uk) limited 2016

Figure 7-22. Typical SFDR spectrum in RF mode.
Fout = 3168MHz (2nd Nyquist), MUX2:1,
Fs = 3.2Gsps. SFDR = 58 dBc

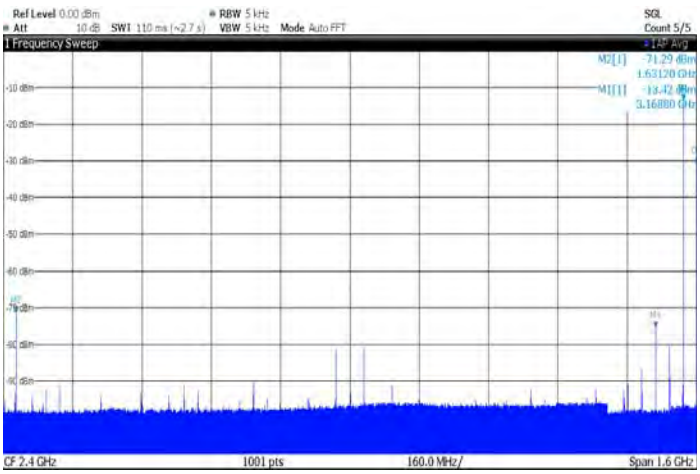
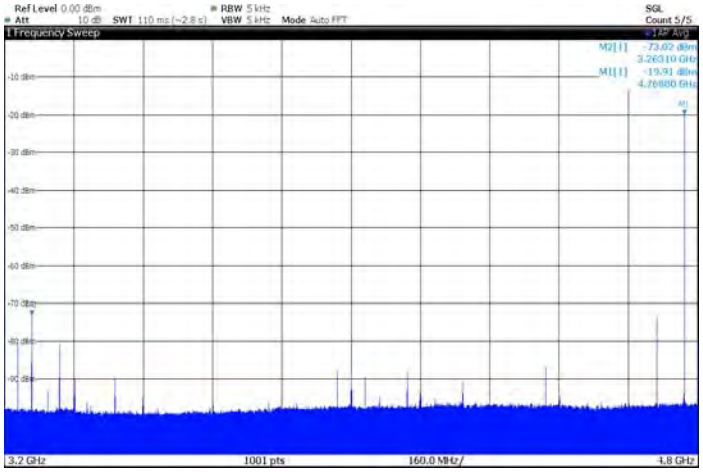


Figure 7-23. Typical SFDR spectrum in RF mode.
Fout = 4768MHz (3rd Nyquist), MUX2:1,
Fs = 3.2Gsps. SFDR = 53 dBc



7.2.3.3 SFDR vs Power supplies & Temperature

Figure 7-24. SFDR vs Power supplies
MUX 2:1 @ 3.2 GSps
MUX 4:1 @ 4.5 GSps

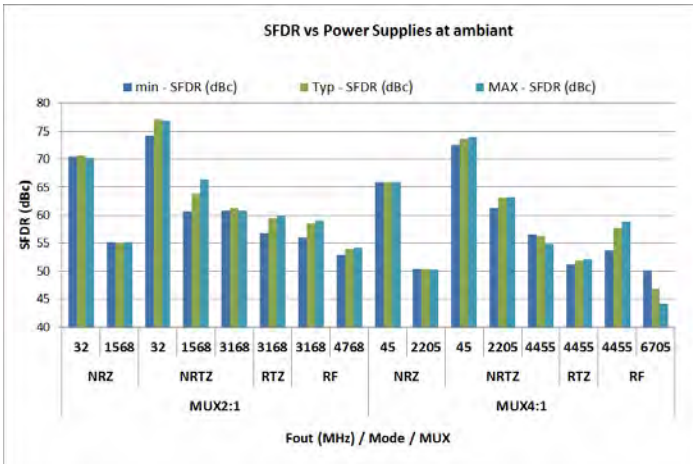
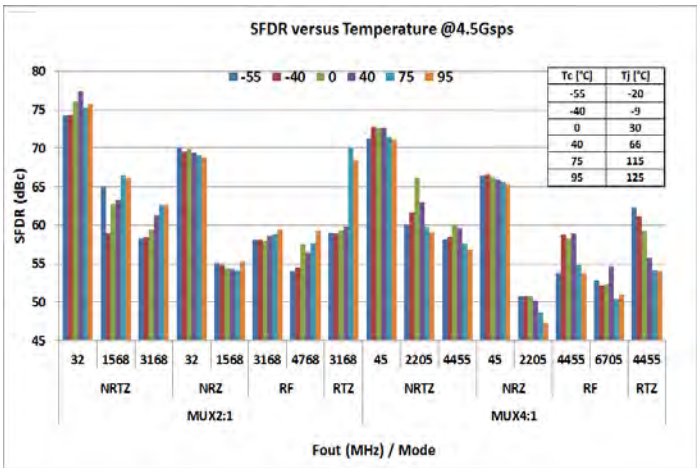


Figure 7-25. SFDR vs temperature
MUX 2:1 @ 3.2 GSps
MUX 4:1 @ 4.5 GSps



© e2v technologies (uk) limited 2016

7.2.4 Multi Tone Measurements

7.2.4.1 Dual Tones

Figure 7-26. Observation of the 1st Nyquist Zone: NRTZ Mode. Fout1: 2000MHz, –8dBFS, Fout2: 2010MHz, –8dBFS

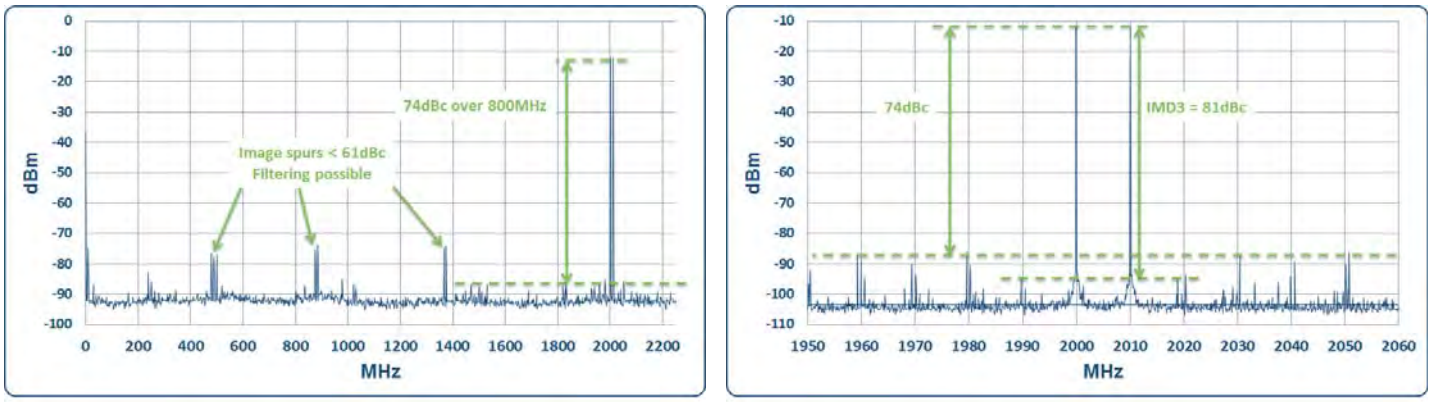


Figure 7-27. Observation of the 2nd Nyquist Zone: RF Mode

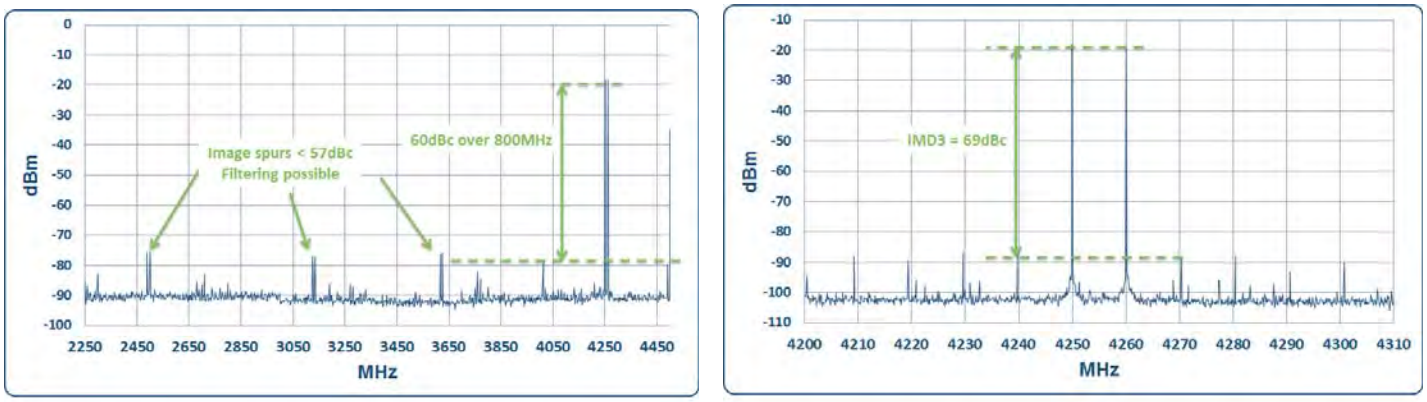
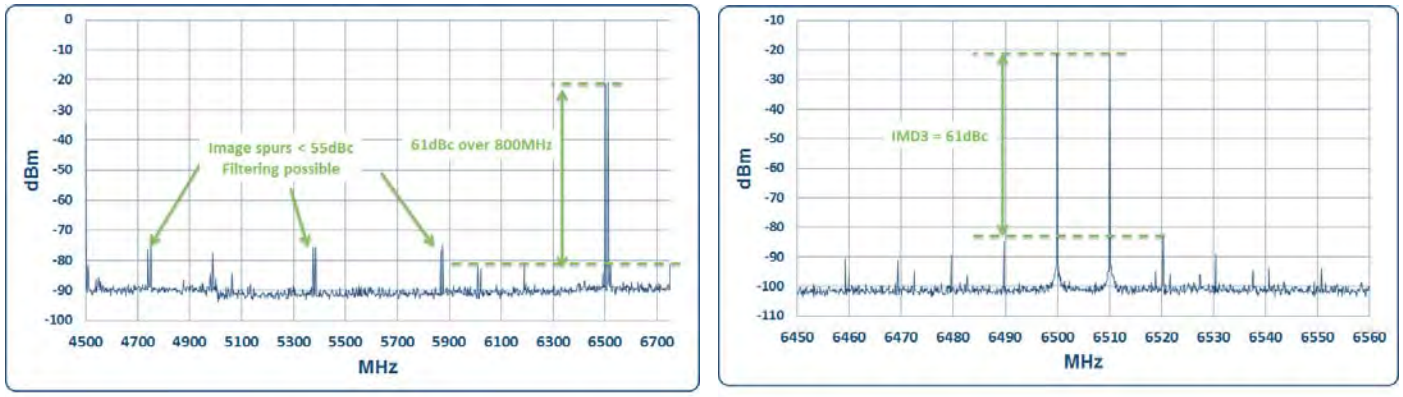


Figure 7-28. Observation of the 3rd Nyquist Zone: RF Mode

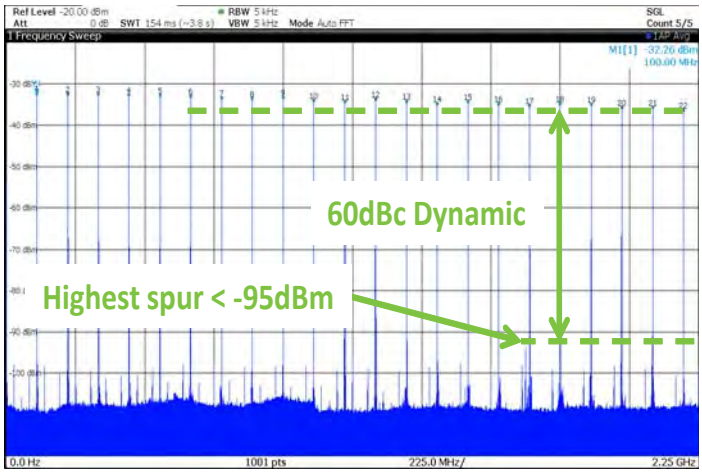


© e2v technologies (uk) limited 2016

7.2.4.2 *Multi tones*

A twenty two tones pattern (100 MHz to 2200MHz with a step of 100MHz) is applied to the DAC operating at 4.5 Gsps and results are observed in the 1st, 2nd and 3rd Nyquist zones.

Figure 7-29. Observation of the 1st and 2nd Nyquist Zones: NRTZ Mode



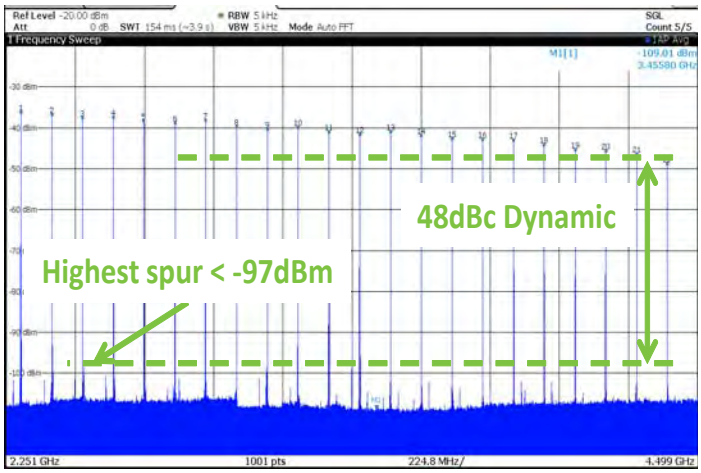
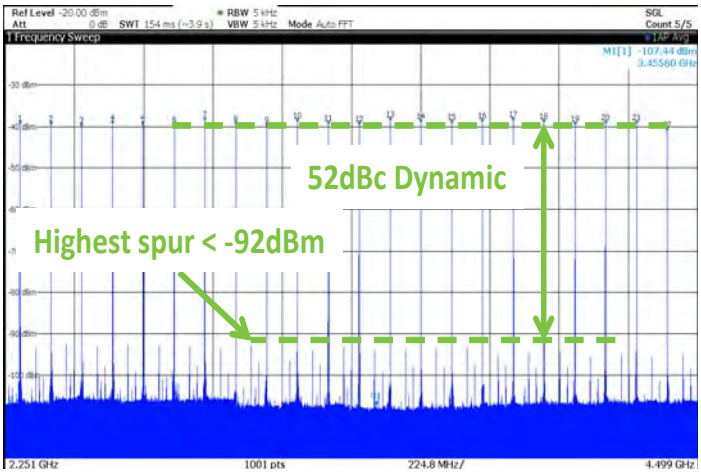
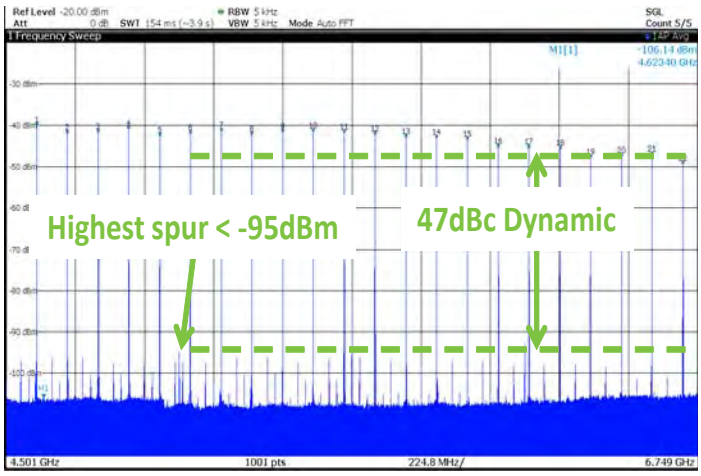


Figure 7-30. Observation of the 2nd and 3rd Nyquist Zones: RF Mode





© e2v technologies (uk) limited 2016

7.2.5 ACPR measurements

Measured in NRTZ mode. Fc=4.5GHz. Channel width = 6 MHz

Figure 7-31. 1 channel ACPR. Center frequency: 954MHz

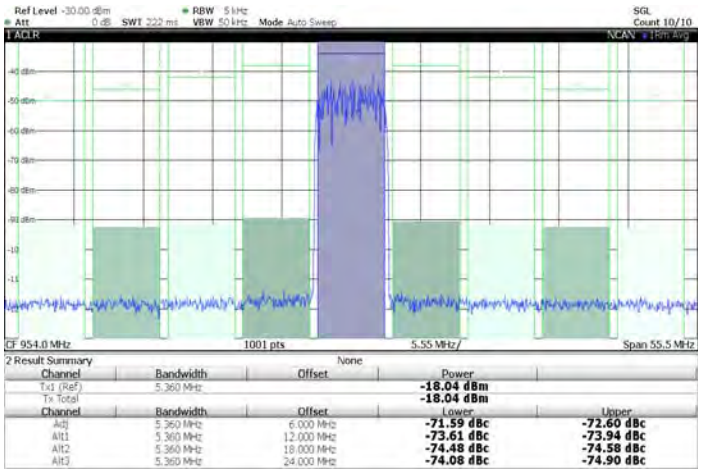


Figure 7-32. 1 channel ACPR versus channel center frequency (100MHz to 2000MHz)

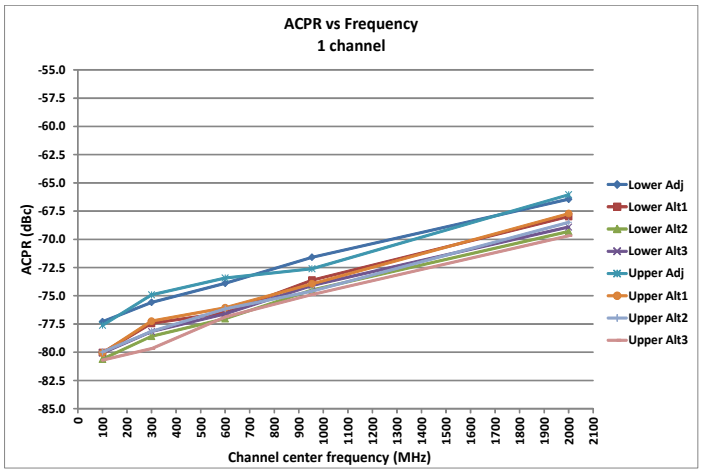


Figure 7-33. 4 channels ACPR. 1st channel center frequency: 954MHz

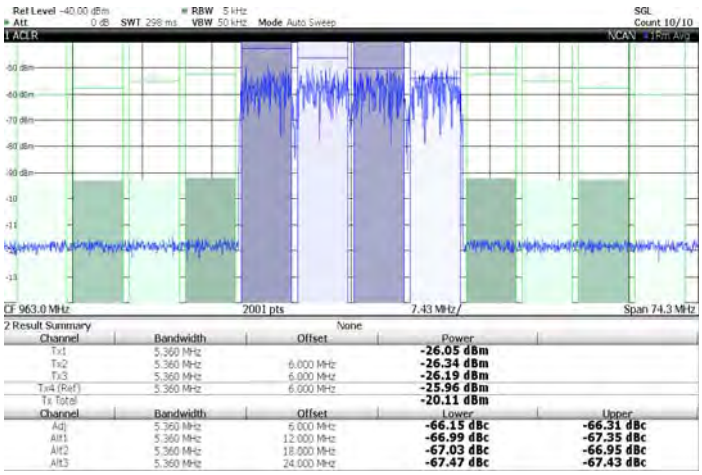
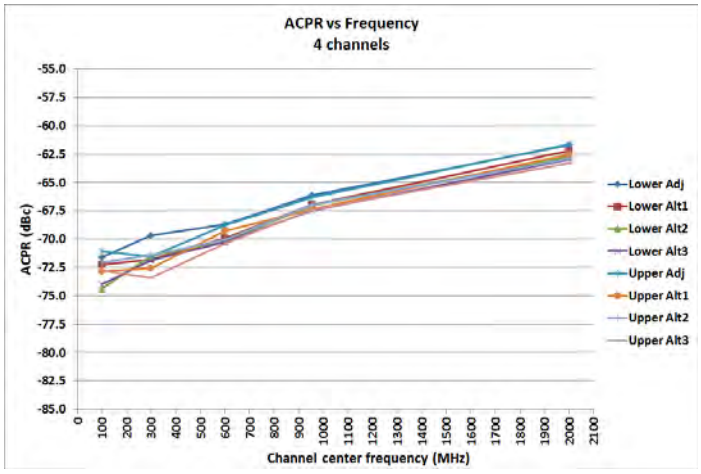


Figure 7-34. 4 channels ACPR versus 1st channel center frequency (100MHz to 2000MHz)



© e2v technologies (uk) limited 2016

Figure 7-35. 8 channels ACPR. 1st channel center frequency: 954MHz

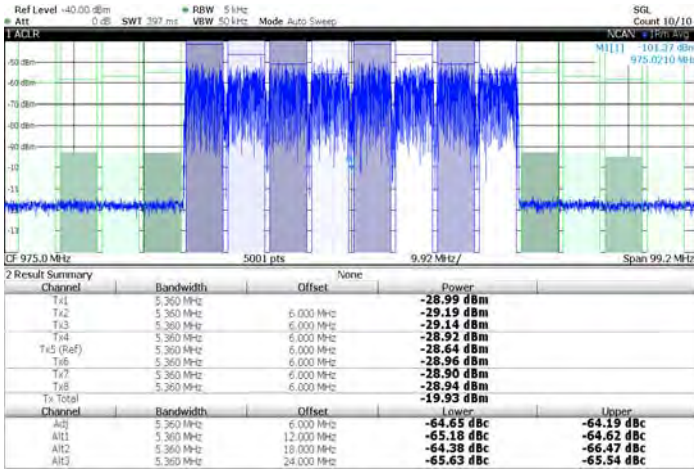
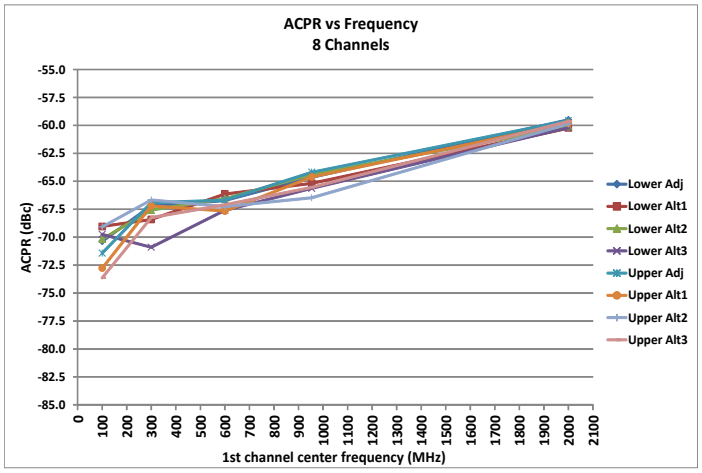


Figure 7-36. 8 channels ACPR versus 1st channel center frequency (100MHz to 2000MHz)



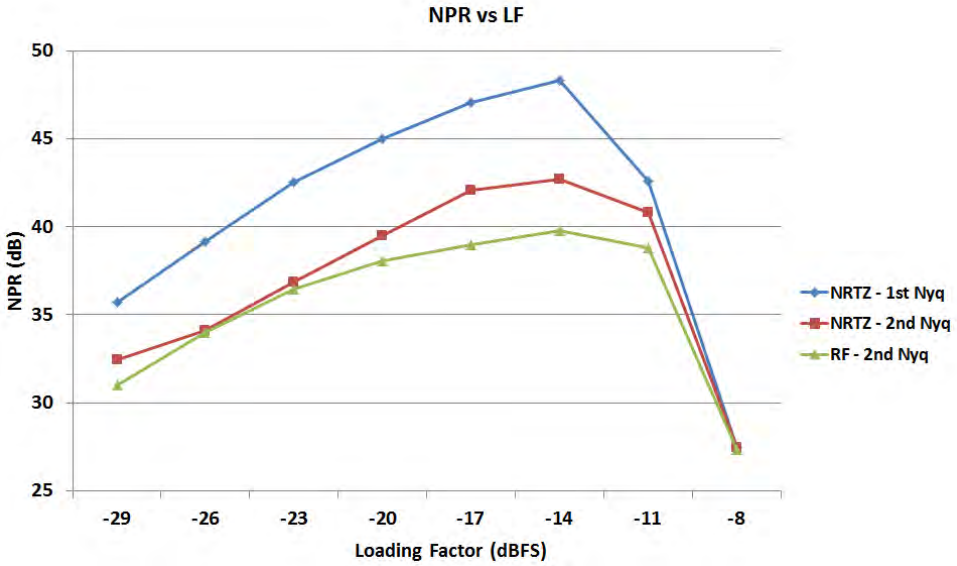
7.2.6 NPR performance

7.2.6.1 NPR vs Loading Factor (LF)

NPR pattern covers a 2GHz bandwidth (125MHz to 2125MHz) with a 25MHz notch width centered at 1100MHz.

Figure 7-37 shows NPR evolution versus loading factor. Optimum NPR value is achieved for LF = –14dBFS.

Figure 7-37. NPR versus loading factor @4.5Gsps



© e2v technologies (uk) limited 2016

7.2.6.2 NPR vs Mode

NPR measurements have been carried out at optimum loading factor (LF) for a 12 bit DAC, that is –14 dBFS, with the DAC operating at 4.5 Gsps.
SNR can be computed from NPR measurement with the formula: SNR[dB] = NPR[dB] + ILF[dB]I - 3.
ENOB can be computed with the formula: ENOB = (SNR[dB] - 1.76) / 6.02.

Figure 7-38. NPR in 1st Nyquist Zone, 125 MHz to 2125 MHz Noise Pattern with a 25 MHz Notch Centered on 1100 MHz, NRTZ mode

Measured average NPR: 47.5 dB, therefore SNR = 58.5 dB and ENOB = 9.4bit

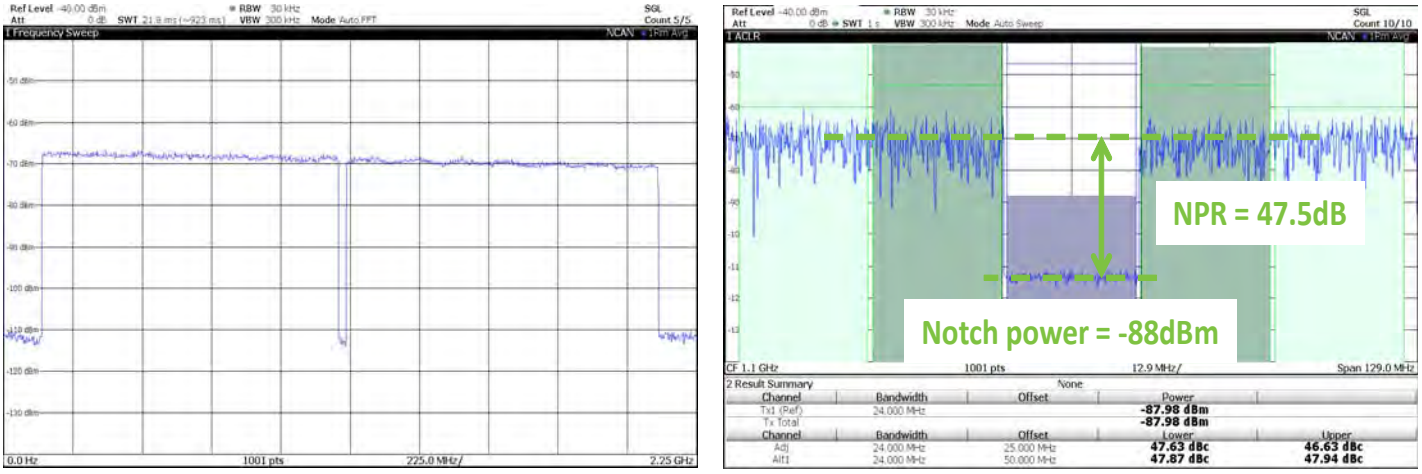
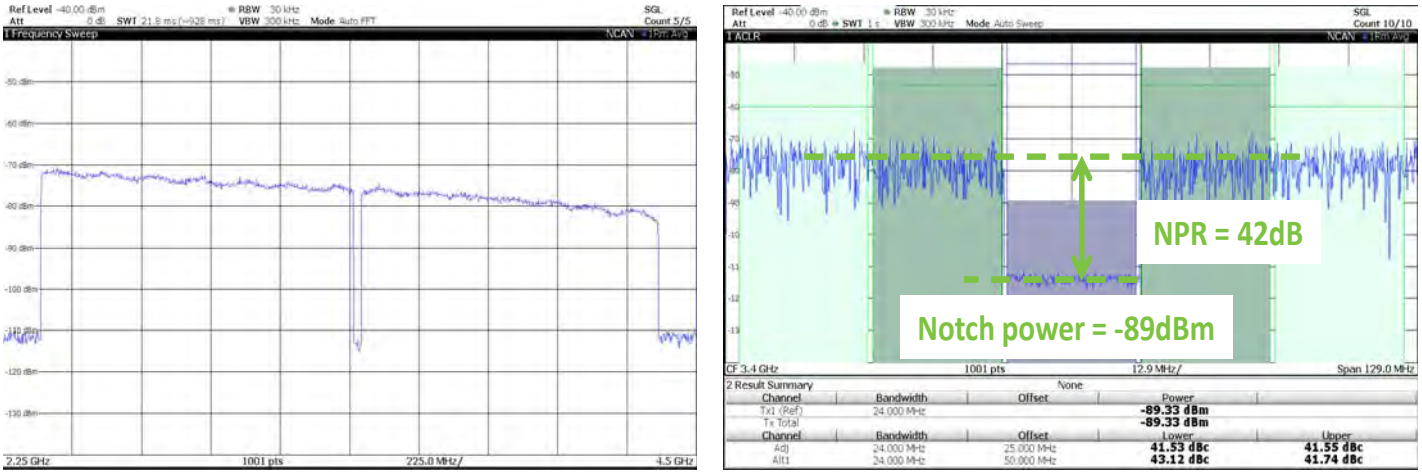


Figure 7-39. NPR in 2nd Nyquist Zone, 2400 MHz to 4400 MHz Noise Pattern with a 25 MHz Notch Centered on 3400 MHz, NRTZ mode.

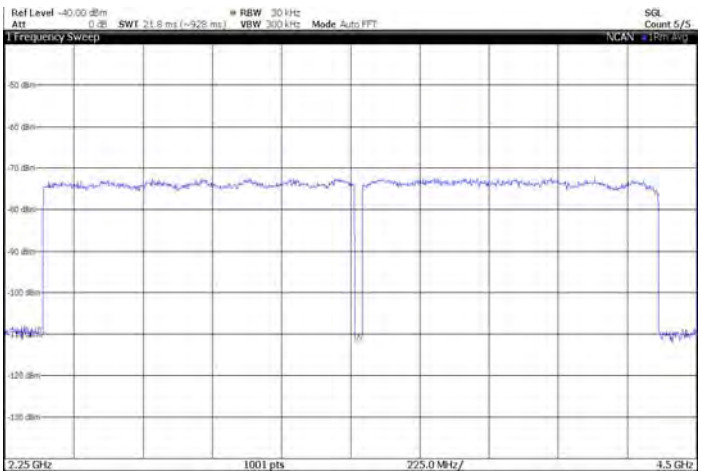
Measured average NPR: 42.0 dB, therefore SNR = 50.0 dB and ENOB = 8.5bit



© e2v technologies (uk) limited 2016

Figure 7-40. NPR in 2nd Nyquist Zone, 2400 MHz to 4400 MHz Noise Pattern with a 25 MHz Notch Centered on 3400 MHz, RF mode.

Measured average NPR: 39.0 dB, therefore SNR = 50.0 dB and ENOB = 8.0bit



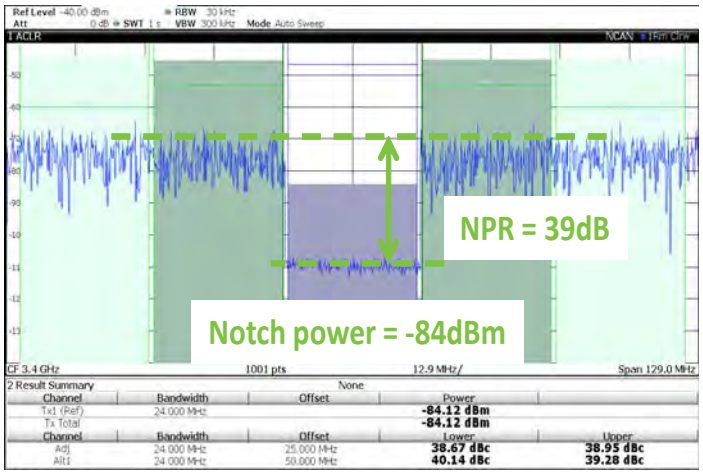
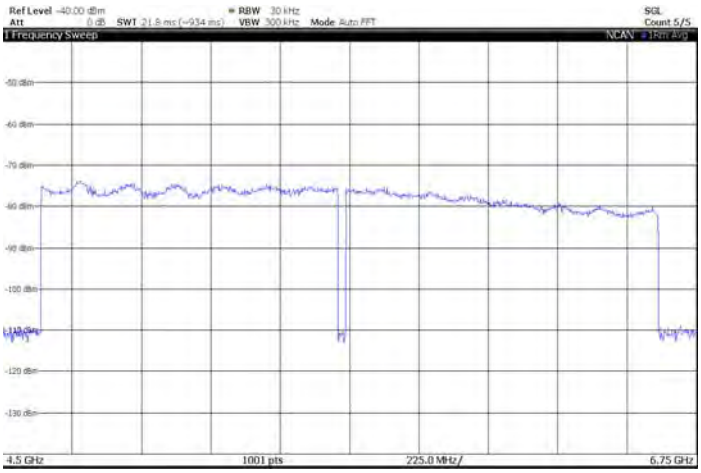
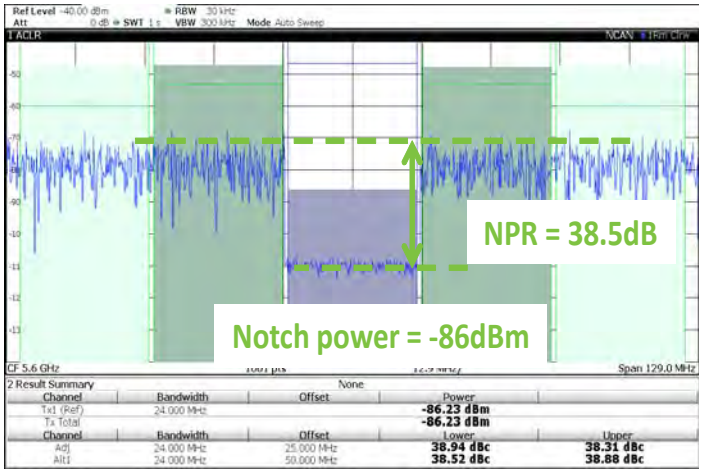


Figure 7-41. NPR in 3rd Nyquist Zone, 4600 MHz to 6600 MHz Noise Pattern with a 25 MHz Notch Centered on 5600 MHz, RF mode.

Measured average NPR: 38.5 dB, therefore SNR = 49.5 dB and ENOB = 7.9bit





© e2v technologies (uk) limited 2016

7.2.6.3 NPR vs Power supplies & Temperature

Figure 7-42. NPR vs power supply for the 4 output modes at room temperature.
min: V_{CCA5}: 4.75V // V_{CCA3} = V_{CCD} = 3.15V;
Typ: V_{CCA5}: 5.00V // V_{CCA3} = V_{CCD} = 3.30V;
MAX: V_{CCA5}: 5.25V // V_{CCA3} = V_{CCD} = 3.45V

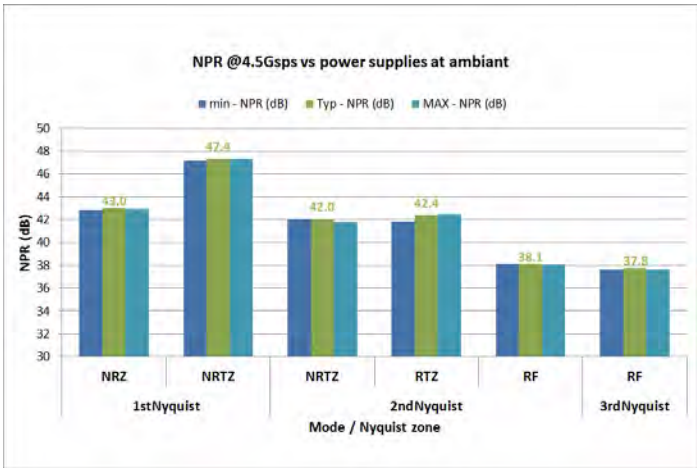
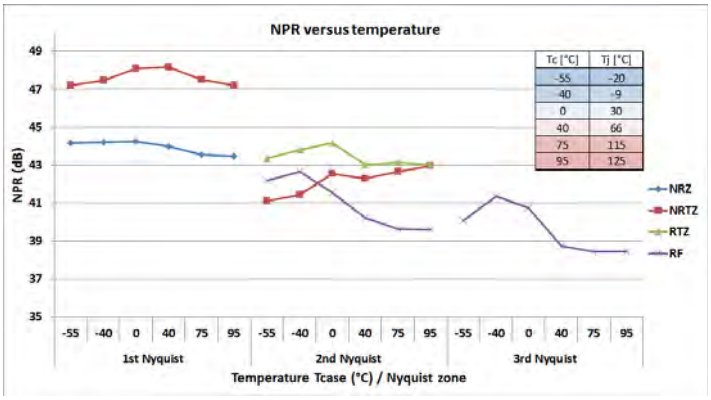


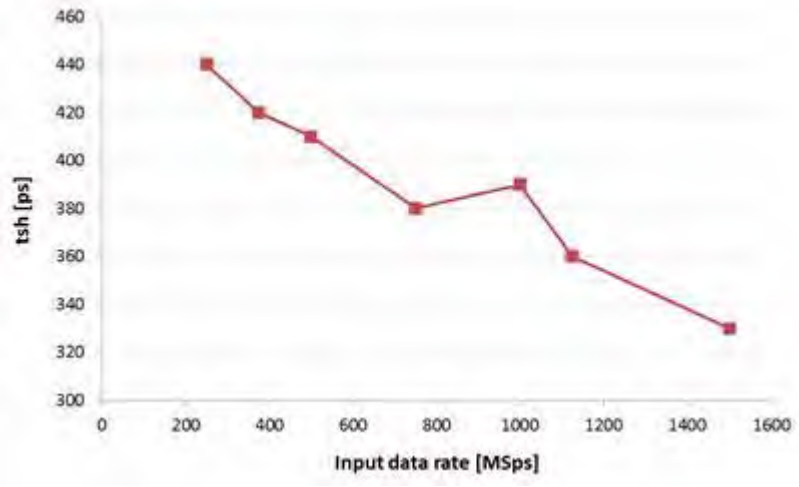
Figure 7-43. NPR versus temperature at 4.5Gsps in 4:1MUX, for the four output modes from Tc = –55°C to Tc = 95°C (Tj = –20°C to 125°C)



7.3 Input Data Set-up and Hold time vs Input Data Rate

The figure below shows t_{SH} variation versus input data rate.

Figure 7-44. t_{SH} vs input data rate



© e2v technologies (uk) limited 2016

8. APPLICATION INFORMATION

8.1 Analog output (OUT/OUTN)

The analog output should be used as a differential signal, as described in the figures below.

If the application requires a single-ended analog output, then a balun is necessary to generate a single ended signal from the differential output of the DAC.

Figure 8-1. Analog output differential termination

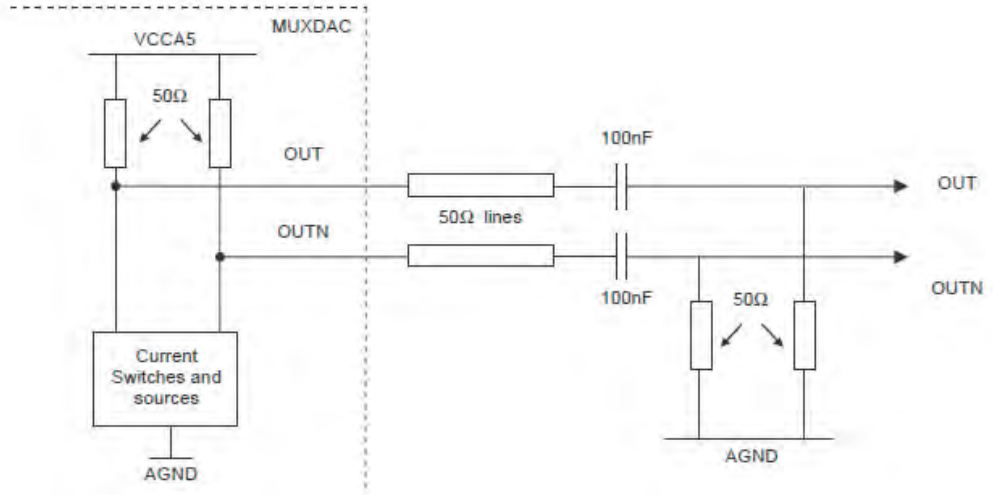
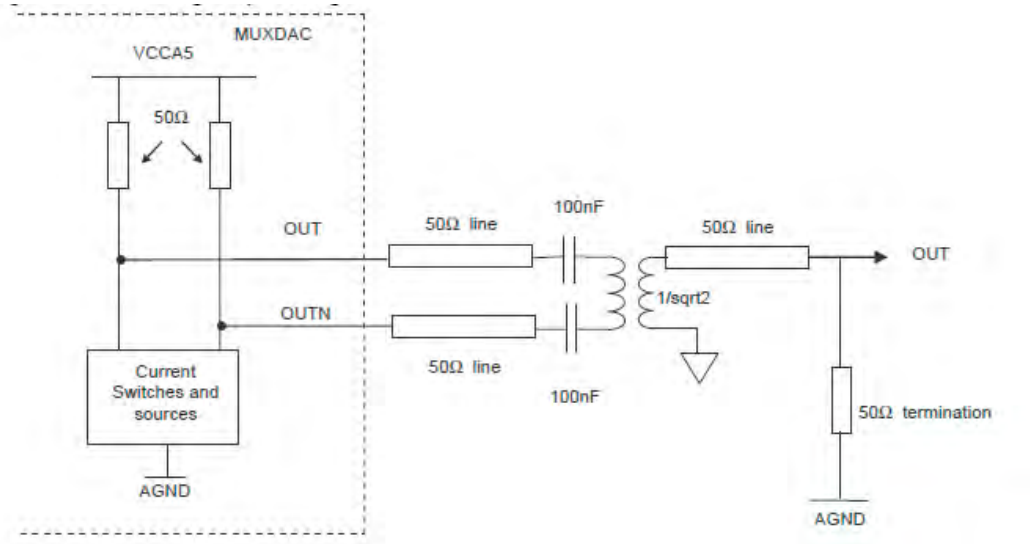


Figure 8-2. Analog output using a 1/sqrt(2) Balun



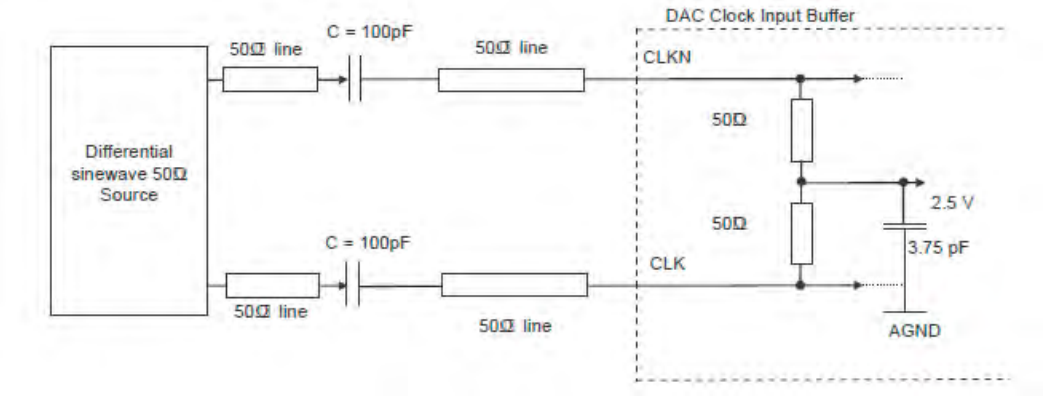
Note: The AC coupling capacitors should be chosen as broadband capacitors with a value depending on the application.

© e2v technologies (uk) limited 2016

8.2 Clock Input (CLK/CLKN)

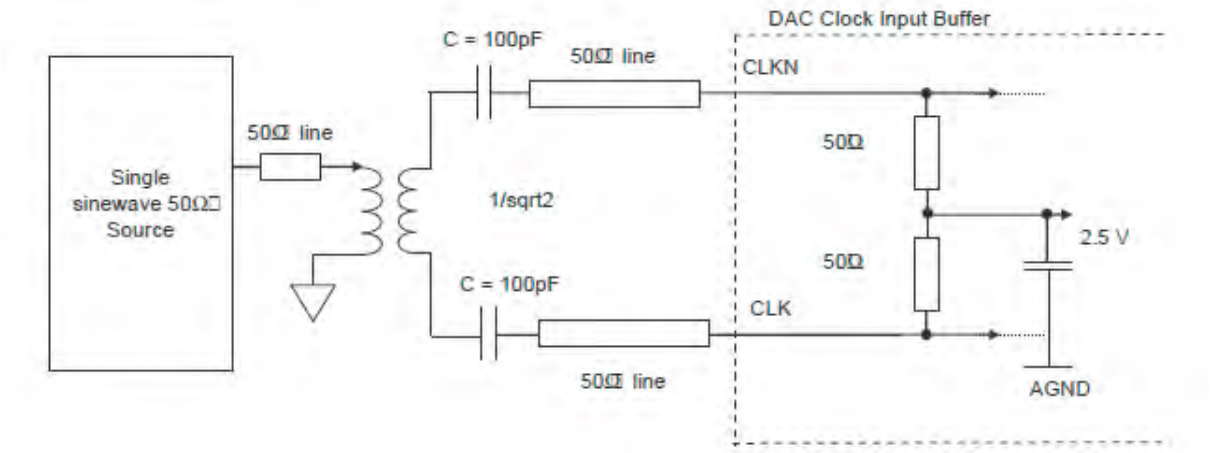
The DAC input clock (sampling clock) should be provided as a differential signal as described in the following figures:

Figure 8-3. Clock input differential termination



Note: The buffer is internally pre-polarized to 2.5V (buffer between V_{CCA5} and AGND).

Figure 8-4. Clock input differential with balun



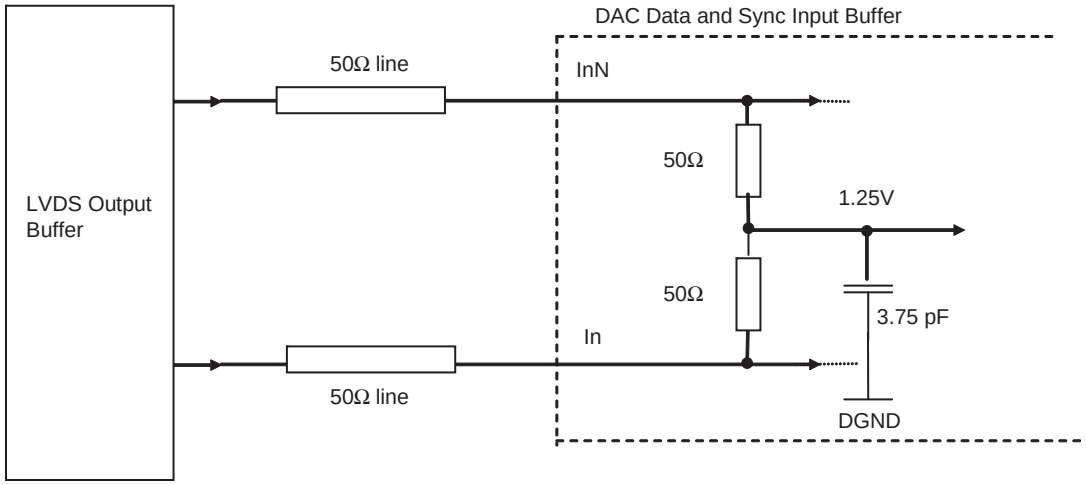
The AC coupling capacitors should be chosen as broadband capacitors with a value depending on the application).

© e2v technologies (uk) limited 2016

8.3 Digital Data, SYNC and IDC inputs

LVDS buffers are used for the digital input data, the SYNC signal (active high) and the IDC signal. They are all internally terminated by 2 × 50Ω to ground via a 3.75 pF capacitor.

Figure 8-5. Digital data, SYNC and IDC input differential termination



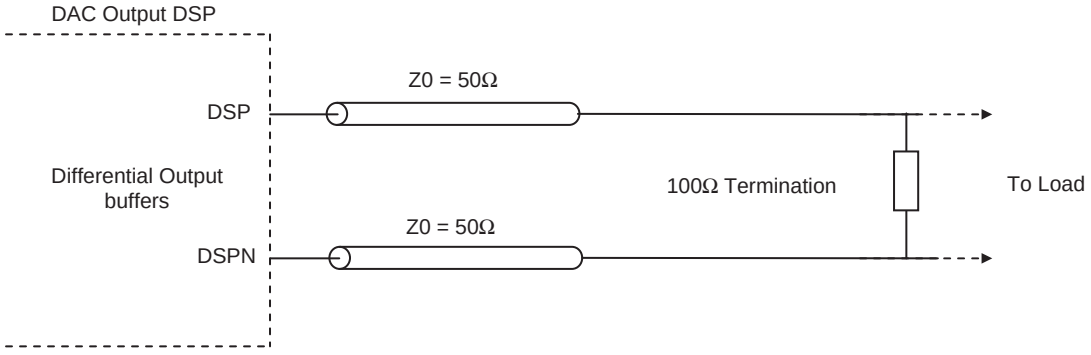
Notes:
1. In the case when only two ports are used (2:1 MUX ratio), then the unused data can be left floating (unconnected).
2. Data and IDC signals should be routed on board with the same layout rules and the same length than the data
3. In case the SYNC is not used, it is recommended to bias the SYNC to 1.1V and SYNCN to 1.4V.

8.4 DSP Clock

The DSP, DSPN output clock signals are LVDS compatible.

If DSP is not used, they have to be terminated via a differential 100Ω termination as described in the following figure:

Figure 8-6. DSP output differential termination



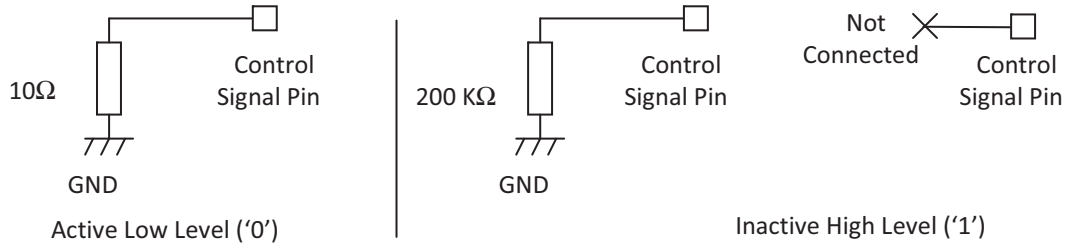
© e2v technologies (uk) limited 2016

8.5 Control signal settings

The PSS and OCDS control signals use the same static input buffer.

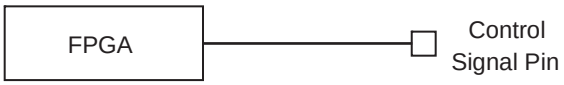
Logic '1' = 200 KΩ to Ground, or tied to V_{CCD} = 3.3V or left open
Logic '0' = 10Ω to Ground or Grounded

Figure 8-7. Control signal output differential termination



The control signals can be driven by an FPGA.

Figure 8-8. Control signal settings with FPGA



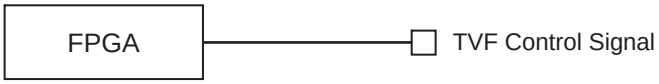
Logic "1" > VIH or V_{CCD} = 3.3V
Logic "0" < VIL or 0V

8.6 TVF Control signal

The TVF control signal is a 3.3V CMOS output signal.

This signal could be acquired by FPGA.

Figure 8-9. Control signal settings with FPGA



In order to modify the VOL/VOH value, pull up and pull down resistor or a potential divider could be used.

8.7 Power Supply Decoupling and Bypassing

The DAC requires 3 distinct power supplies:

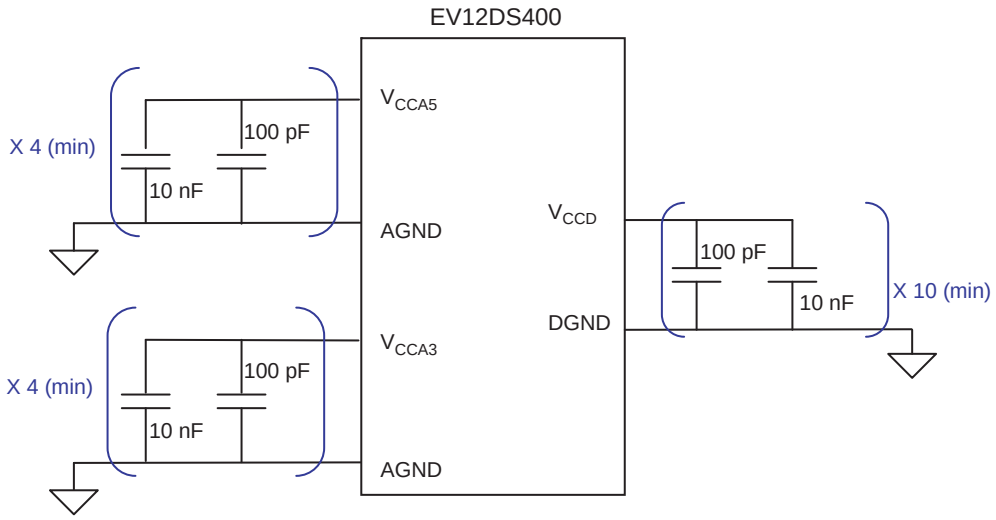
V_{CCA5} = 5.0V (for the analog core)
V_{CCA3} = 3.3V (for the analog part)
V_{CCD} = 3.3V (for the digital part)

It is recommended to decouple all power supplies to ground as close as possible to the device balls with 100 pF in parallel to 10nF capacitors. The minimum number of decoupling pairs of capacitors can be calculated as the minimum number of groups of neighbouring pins.

© e2v technologies (uk) limited 2016

4 pairs of 100pF in parallel to 10 nF capacitors are required for the decoupling of V_{CCA5}. 4 pairs for the V_{CCA3} and 10 pairs are necessary for V_{CCD}.

Figure 8-10. Power Supplies Decoupling Scheme



Each power supply has to be bypassed as close as possible to its source and accessed by 100 nF in parallel to 22 µF capacitors (the optimum value depends on the regulators).

8.8 Power on/off requirement and power on reset function

The DAC timing circuitry must be reset either by a power on reset (see below) or through the use of the SYNC input to set it to the right state. Refer to Section 5.10.

At power-up a reset pulse is internally and automatically generated when the following sequence is satisfied: V_{CCD}, V_{CCA3} then V_{CCA5}.

This pulse has two effects:

- Resetting of the 3WSI interface registers to their default values.
- Synchronizing the timing circuitry.

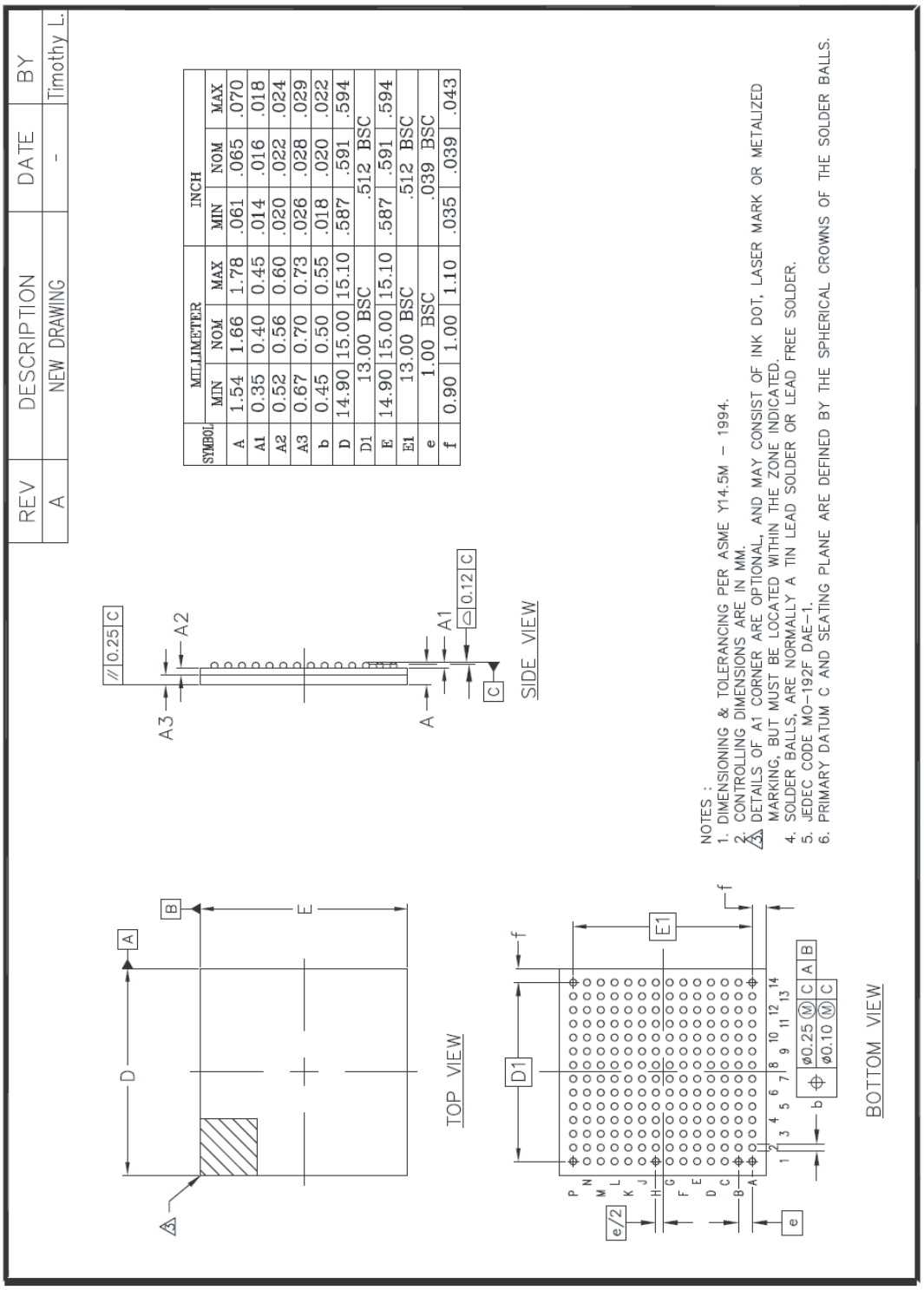
To cancel the SYNC pulse at power-up, it is necessary to apply the sequence: V_{CCA5} then V_{CCA3} and V_{CCD}. Any other sequence may not have a deterministic SYNC behaviour but can be used.

There is no specific requirement to power down the device.

© e2v technologies (uk) limited 2016

9. PACKAGE DESCRIPTION

9.1 fpBGA 196 Outline



© e2v technologies (uk) limited 2016

9.2 Thermal Characteristics

Assumptions:

- Still air
- Pure conduction
- No radiation
- Heating zone = 8.9% of die surface

Rth Junction - bottom of Balls = 13°C/W

Rth Junction - board (JEDEC JESD-51-8) = 17.3°C/W

Rth Junction - top of case = 14°C/W

Assumptions:

- Heating zone = 8.9% of die surface
- Still air, JEDEC condition

Rth Junction - ambient (JEDEC) = 32.0 °C/W

The hot spot point is 6°C above the temperature given by the diode

10. ORDERING INFORMATION

Table 10-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EVX12DS400AZPY	FpBGA196 RoHS	Ambient	General Sample Prototype	
EV12DS400ACZPY	FpBGA196 RoHS	0°C < Tc, Tj < 90°C	Commercial "C" Grade	Refer to datasheet 1130
EV12DS400AVZPY	FpBGA196 RoHS	–40°C < Tc, Tj < 110°C	Industrial "V" Grade	Refer to datasheet 1130
EV12DS400AMZPY	FpBGA196 RoHS	–55°C < Tc, Tj < 125°C	Military "M" Grade	
EV12DS400ACZP	FpBGA196	0°C < Tc, Tj < 90°C	Commercial "C" Grade	Refer to datasheet 1130
EV12DS400AVZP	FpBGA196	–40°C < Tc, Tj < 110°C	Industrial "V"Grade	Refer to datasheet 1130
EV12DS400AMZP	FpBGA196	–55°C < Tc, Tj < 125°C	Military "M" Grade	
EV12DS400AZPY-EB	FpBGA196 RoHS	Ambient	Prototype	Evaluation Board

© e2v technologies (uk) limited 2016

11. REVISION HISTORY

This table provides revision history for this document.

Table 11-1. Revision History

Rev. No	Date	Substantive Change(s)
1163B	March 2016	Add min and max limits on Section 3.3 and Section 3.4 Table 3-8: add note 3 about set up and hold time Figure 5-17 and Figure 5-18 : correct typo about DSP with PSS [111] Table 6-1: remove note about AGND and DGND planes Table 6-1: add note about DSP clock that needs to be 100Ω terminated. Update of Figure 7-24 about SFDR vs supplies. Add Figure 7-3 about t_{SH} vs input data rate. Section 8.4: DSP needs to be 100Ω terminated even if not used. Section 8.7: Remove note about AGND and DGND ground planes
1163A	December 2015	Initial Revision

© e2v technologies (uk) limited 2016

Table of Contents

© e2v technologies (uk) limited 2016

© e2v technologies (uk) limited 2016