eZ801905050MOD

eZ80190 Module

Product Specification

PS019101-1003

PRELIMINARY

ZiLOG Worldwide Headquarters • 532 Race Street • San Jose, CA 95126
Telephone: 408.558.8500 • Fax: 408.558.8300 • www.ZiLOG.com

This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

ZiLOG Worldwide Headquarters
532 Race Street
San Jose, CA 95126
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

Document Disclaimer

Table of Contents

List of Figures iv
List of Tables v
The eZ80190 Module 1
Module Features 1
eZ80190 Processor Features 1
Block Diagram 3
Pin Description 4
I/O Connector (JP2) 4
Peripheral Bus Connector (JP1) 7
Onboard Component Description 12
Logic-Level I/Os 12
Onboard Battery Backup 12
Ethernet Media Access Controller 12
Ethernet LEDs 12
Ethernet Connector 13
GPIO Pins for Enabling LAN Activity, Sleep, Interrupt 13
EMAC Ports 14
EMAC Access 14
Memory 14
Wait States 14
Static RAM 14
Flash Memory 15
Real-Time Clock 15
Reset Generator 16
Serial Interface Ports 16
Physical Dimensions 17
ESD/EMI Protection 19
Absolute Maximum Ratings 20
Power Supply 20
Document Number Description 22
Change Log 22
Schematic Diagrams 23
Customer Feedback Form 31

List of Figures

Figure 1. eZ80190 Functional Block Diagram 3
Figure 2. eZ80190 Module Peripheral Bus Connector Pin Configuration—JP1 4
Figure 3. eZ80190 Module I/O Connector Pin Configuration—JP2 8
Figure 4. Physical Dimensions of the eZ80190 Module 17
Figure 5. eZ80190 Module—Top Layer 18
Figure 6. eZ80190 Module—Bottom Layer 19
Figure 7. Power Supply Examples 21
Figure 8. eZ80190 Module Schematic Diagram, #1 of 9—CPU 23
Figure 9. eZ80190 Module Schematic Diagram, #2 of 9—36-Pin SRAM Device 24
Figure 10. eZ80190 Module Schematic Diagram, #3 of 9—NOR Flash Device 25
Figure 11. eZ80190 Module Schematic Diagram, #4 of 9—Ethernet Module . 26
Figure 12. eZ80190 Module Schematic Diagram, #5 of 9—Ethernet Module Logic 27
Figure 13. eZ80190 Module Schematic Diagram, #6 of 9—Ethernet Module Peripherals 28
Figure 14. eZ80190 Module Schematic Diagram, #7 of 9—Headers 29
Figure 15. eZ80190 Module Schematic Diagram, #8 of 9—Power Supply . . . 30

List of Tables

Table 1. eZ80190 Module Peripheral Bus Connector Pin Identification 5
Table 2. eZ80190 Module I/O Connector Pin Identification 8
Table 3. Ethernet Connector Pin Assignments 13
Table 4. Chip Frequency to Wait State Cycle Time Calculation 14
Table 5. Real-Time Clock Registers 16
Table 6. Absolute Maximum Ratings 20

The eZ80190 Module

The eZ80190 Module is a compact, high-performance Ethernet module specially designed for the rapid development and deployment of embedded systems requiring control and Internet/Intranet connectivity. It features the low-cost eZ80190 microprocessor powered by ZiLOG's latest power-efficient, high-speed eZ80® CPU.

The eZ80190 microprocessor is a high-speed single-cycle instruction-fetch microprocessor, which can operate with a clock speed of 50MHz. It can operate in Z80-compatible addressing mode (64KB) or full 24-bit addressing mode (16MB).

The rich peripheral set of the eZ80190 makes it suitable for a variety of applications, including industrial control, communication, security, automation, point-of-sale terminals, and embedded networking applications.

Module Features

- eZ80190 microprocessor operating at 50MHz
- Ethernet Media Access Controller+ PHY with RJ45 connector
- 512KB zero-wait-state onboard SRAM
- 1MB onboard NOR Flash ROM (90–100ns)
- Real-Time Clock with 32.768kHz Crystal with battery backup
- I/O connector provides 32 general-purpose 5V-tolerant I/O pinouts
- Onboard peripheral bus connector provides I/O bus for external peripheral connections (IRQ, CS, 24 address, 8 data)
- Small footprint 78.7mm x 63.5mm; height is 24mm
- Module operates from external 3.3V power supply
- Standard operating temperature range: 0ºC to +70ºC

eZ80190 Processor Features

- Single-cycle instruction fetch, high-performance, pipelined eZ80® CPU core
- Low power features including SLEEP mode and HALT mode
- Two UARTs with independent baud rate generators
- Two SPI interfaces with independent clock rate generators

- Two I^2C interfaces with independent clock rate generators
- Fast multiply accumulate unit (MACC)
- DMA Controller for fast memory-to-memory transfers
- Glueless external memory and I/O interface featuring 4 chip selects with individual wait state generators
- Fixed-priority vectored interrupts (both internal and external) and interrupt controller
- Six 16-bit Counter/Timers with prescalers and direct input/output drive
- Watch-Dog Timer
- 32 bits of general-purpose I/O
- 2-wire ZDI debug interface
- 100-pin LQFP package
- 3.3V±0.3V supply voltage with 5V tolerant inputs
- Standard operating temperature range: 0ºC to +70ºC

Note: All signals with an overline are active Low. For example, $\overline{B/W}$, for which WORD is active Low, and B/W, for which BYTE is active Low.

Block Diagram

Figure 1 illustrates a block diagram of the eZ80190 microprocessor.

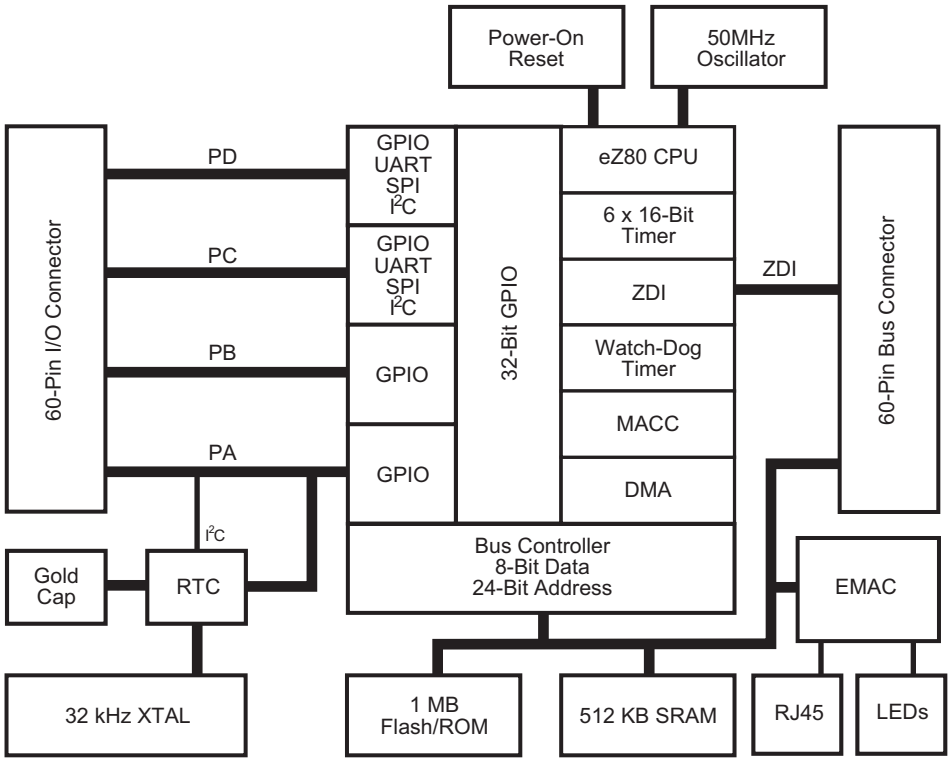


Figure 1. eZ80190 Functional Block Diagram

Pin Description

I/O Connector (JP2)

Figure 2 illustrates the pin layout of the 60-pin Peripheral Bus Connector (JP1) of the eZ80190 Module. The eZ80® Development Platform, however, features a 50-pin connector. The eZ80190 Module is designed to interface pin 60 of its JP1 connector to pin 50 of the eZ80® Development Platform's JP1 connector so that pins 1–10 of the eZ80190 Module overlap the edge of the eZ80® Development Platform. Table 1 identifies the pins and their functions.

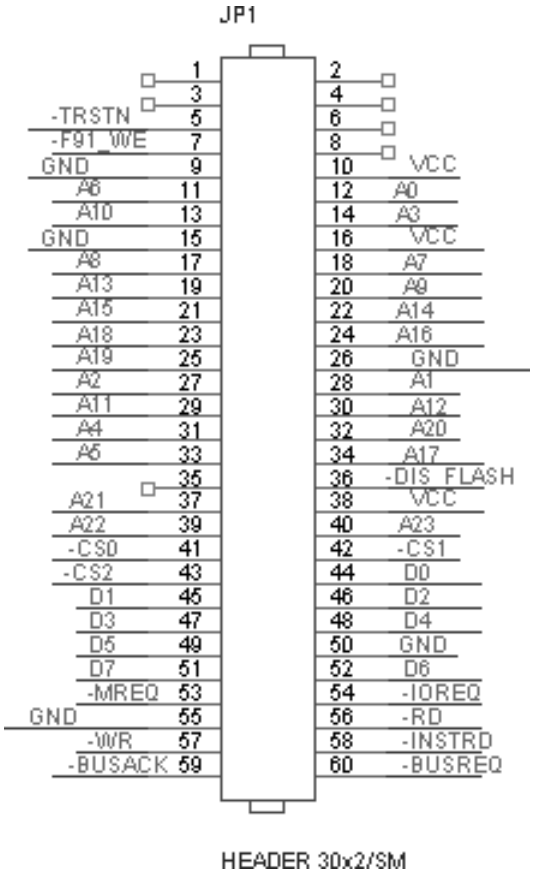


Figure 2. eZ80190 Module
Peripheral Bus Connector Pin Configuration—JP1

Table 1. eZ80190 Module Peripheral Bus Connector Pin Identification*

Pin #	Symbol	Pull Up/Down*	Signal Direction	Comments
1	Reserved			
2	Reserved			
3	Reserved			
4	Reserved			
5	$\overline{\text{TRSTN}}$		Input	Reset for On-Chip Instrumentation (OCI); not used with the eZ80190 Module.
6	Reserved			
7	$\overline{\text{F91\_WE}}$	PU 10KΩ	Input	A Low enables a Write to on-chip Flash memory. If this pin is unconnected, on-chip Flash memory is write-protected; not used with the eZ80190 Module.
8	Reserved			
9	GND			V_{SS}/Ground (0V).
10	V_{CC}			3.3V supply input pin.
11	A6		Bidirectional	
12	A0		Bidirectional	
13	A10		Bidirectional	
14	A3		Bidirectional	
15	GND			V_{SS}/Ground (0V).
16	V_{CC}			3.3V supply input pin.
17	A8		Bidirectional	
18	A7		Bidirectional	
19	A13		Bidirectional	
20	A9		Bidirectional	
21	A15		Bidirectional	
22	A14		Bidirectional	

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80190 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 1. eZ80190 Module Peripheral Bus Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down*	Signal Direction	Comments
23	A18		Bidirectional	
24	A16		Bidirectional	
25	A19		Bidirectional	
26	GND			V_{SS}/Ground (0V).
27	A2		Bidirectional	
28	A1		Bidirectional	
29	A11		Bidirectional	
30	A12		Bidirectional	
31	A4		Bidirectional	
32	A20		Bidirectional	
33	A5		Bidirectional	
34	A17		Bidirectional	
35	Reserved			
36	$\overline{\text{DIS\_Flash}}$	PU 10KΩ	Input	A Low disables onboard Flash memory. Flash is enabled if DIS_Flash is not connected; CMOS Input 3.3V (5V tolerant).
37	A21		Bidirectional	
38	V_{CC}			3.3V supply input pin.
39	A22		Bidirectional	
40	A23		Bidirectional	
41	$\overline{\text{CS0}}$		Output	
42	$\overline{\text{CS1}}$		Output	
43	$\overline{\text{CS2}}$		Output	
44	D0	PU 4k7Ω	Bidirectional	
45	D1	PU 4k7Ω	Bidirectional	

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80190 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 1. eZ80190 Module Peripheral Bus Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down*	Signal Direction	Comments
46	D2	PU 4k7Ω	Bidirectional	
47	D3	PU 4k7Ω	Bidirectional	
48	D4	PU 4k7Ω	Bidirectional	
49	D5	PU 4k7Ω	Bidirectional	
50	GND			V_{SS}/Ground (0V).
51	D7	PU 4k7Ω	Bidirectional	
52	D6		Bidirectional	
53	$\overline{\text{MREQ}}$		Bidirectional	
54	$\overline{\text{IORQ}}$		Bidirectional	
55	GND			V_{SS}/Ground (0V).
56	$\overline{\text{RD}}$		Bidirectional	
57	$\overline{\text{WR}}$		Bidirectional	
58	$\overline{\text{INSTRD}}$		Output	
59	$\overline{\text{BUSACK}}$		Output	
60	$\overline{\text{BUSREQ}}$	PU 2k2Ω	Input	

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80190 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Peripheral Bus Connector (JP1)

Figure 3 illustrates the pin layout of the 60-pin I/O Connector (JP2) of the eZ80190 Module. The eZ80® Development Platform, however, features a 50-pin connector. The eZ80190 Module is designed to interface pin 60 of its JP2 connector to pin 50 of the eZ80® Development Platform's JP2 connector so that pins 1–10 of the eZ80190 Module overlap the edge of the eZ80® Development Platform. Table 2 identifies the pins and their functions.

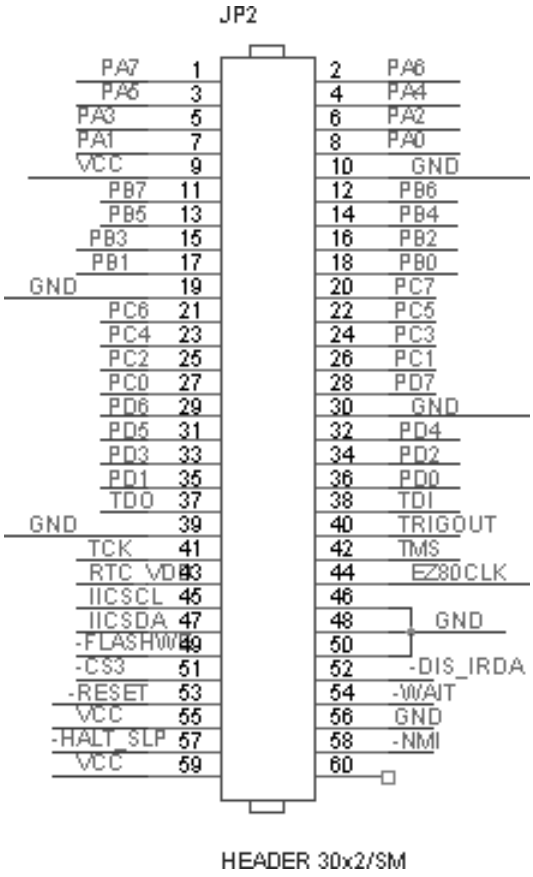


Figure 3. eZ80190 Module
I/O Connector Pin Configuration—JP2

Table 2. eZ80190 Module I/O Connector Pin Identification*

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
1	PA7		Bidirectional	
2	PA6		Bidirectional	
3	PA5		Bidirectional	

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80190 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 2. eZ80190 Module I/O Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
4	PA4		Bidirectional	
5	PA3		Bidirectional	
6	PA2		Bidirectional	
7	PA1		Bidirectional	
8	PA0		Bidirectional	
9	V_{CC}			3.3V supply input pin.
10	GND			V_{SS}/Ground (0V).
11	PB7		Bidirectional	
12	PB6		Bidirectional	
13	PB5		Bidirectional	
14	PB4		Bidirectional	
15	PB3		Bidirectional	
16	PB2		Bidirectional	
17	PB1		Bidirectional	
18	PB0		Bidirectional	
19	GND			V_{SS}/Ground (0V).
20	PC7		Bidirectional	
21	PC6		Bidirectional	
22	PC5		Bidirectional	
23	PC4		Bidirectional	
24	PC3		Bidirectional	
25	PC2		Bidirectional	
26	PC1		Bidirectional	
27	PC0		Bidirectional	

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80190 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 2. eZ80190 Module I/O Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
28	PD7		Bidirectional	
29	PD6		Bidirectional	
30	GND			V_{SS}/Ground (0V).
31	PD5		Bidirectional	
32	PD4	PD 4k7	Bidirectional	
33	PD3		Bidirectional	
34	PD2		Bidirectional	
35	PD1		Bidirectional	
36	PD0		Bidirectional	
37	TDO		Output	ZDI Data Output pin; not used with the eZ80190 Module.
38	TDI		Input	ZDI Data Input pin.
39	GND			V_{SS}/Ground (0V).
40	TRIGOUT		Output	Active High trigger event indicator; not used with the eZ80190 Module.
41	TCK	PU 10KΩ	Input	ZDI Clock. High on reset enables ZDI mode; Low on reset enables OCI debug.
42	TMS	PU 10KΩ	Input	JTAG Test Mode Select Input; not used with the eZ80190 Module.
43	RTC_V_{DD}			RTC supply from GoldCap (or external battery).
44	EZ80CLK		Output	Synchronous CPU clock output.
45	I^2CSCL	PU 4k7	Bidirectional	I^2C Bus Clock.
46	GND			V_{SS}/Ground (0V).
47	I^2CSDA	PU 4k7	Bidirectional	I^2C Data Clock.
48	GND		Power	V_{SS}/Ground (0V).

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80190 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 2. eZ80190 Module I/O Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
49	$\overline{\text{FlashWE}}$	PU 10KΩ	Input	A Low enables a Write to external Flash memory boot block area. If this pin is unconnected, the Flash memory boot block area is write-protected.
50	GND			V_{SS}/Ground (0V).
51	$\overline{\text{CS3}}$		Output	Connected to the CS8900 EMAC.
52	$\overline{\text{DIS\_IRDA}}$	PU 10KΩ	Input	A Low disables the onboard IRDA transceiver to use PC0/PC1 UART pins externally; not used with the eZ80190 Module.
53	$\overline{\text{RESET}}$	PU 2k2	Bidirectional	Reset Output from module or push-button reset.
54	$\overline{\text{WAIT}}$	PU 2k2	Input	Driving the $\overline{\text{WAIT}}$ pin Low forces the CPU to provide additional clock cycles for an external peripheral or external memory to complete its Read or Write operation; not used with the eZ80190 Module.
55	V_{CC}			3.3V supply input pin.
56	GND			V_{SS}/Ground (0V).
57	$\overline{\text{HALT\_SLP}}$		Output, Active Low	A Low on this pin indicates that the CPU enters either HALT or SLEEP mode because of execution of either a HALT or SLP instruction.
58	$\overline{\text{NMI}}$	PU 10KΩ	Schmitt Trigger Input, Active Low	The $\overline{\text{NMI}}$ input is a higher priority input than the maskable interrupts. It is always recognized at the end of an instruction, regardless of the state of the interrupt enable control bits. This input includes a Schmitt trigger to allow RC rise times. This external NMI signal is combined with an internal NMI signal generated from the WDT block before being connected to the $\overline{\text{NMI}}$ input of the CPU.
59	V_{CC}			3.3V supply input pin.
60	Reserved		NC	Reserved—No Connection.

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80190 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Onboard Component Description

Logic-Level I/Os

The I/O connector features 32 general-purpose 3.3V CMOS I/O pins that can be used as outputs or inputs interfacing to external logic. All I/Os are 5V tolerant. Some of the General-Purpose I/O pins support dual mode functions (SPI, I^2C, UARTs, and bit I/O with edge- or level-triggered interrupt functions on each pin). For more information on eZ80190 dual modes, please refer to the eZ80190 Product Specification (PS0066).

Onboard Battery Backup

An onboard 0.1F capacitor (GoldCap) is used to bridge power outages of 2–4 hours if the power supply to the module is disconnected. The capacitor is charged to 3.1V during normal operation and is discharged through the on-chip Real Time Clock. The V_{RTC} pin is available on the I/O connector of the module to connect external components to a power supply or to a larger GoldCap.

Caution: Do not connect a Lithium Battery to the GoldCap capacitor, because onboard charging circuitry for the capacitor can destroy the lithium battery.

Ethernet Media Access Controller

The eZ80190 contains a CS8900A EMAC which is attached to the data/address bus of the processor. This chip is connected to the processor's CS3 Chip Select, A0–A3, D0–D7, RD, WR, and PD4 pins for interrupt purposes. Connection of pins PD6 and PD7 for LANACT (wake-up from sleep) and SLEEP is optional and resistor-selectable onboard.

Ethernet LEDs

There are two green LEDs, a Link LED and a LAN LED, that are located adjacent to each other on the eZ80190 Module. A steady LAN LED (top) indicates received link pulses from the Ethernet. A flashing Link LED (bottom) indicates Traffic (RX or TX) on the LAN.

An RJ45 loopback connector can be used to verify the correct operation of the Receiver and the Transmitter. The green LED should be on if RX+ is connected with TX+ and RX– is connected with TX–.

Ethernet Connector

The eZ80190 is equipped with an RJ45 connector that features integrated magnetics (transformer, common mode chokes). The remaining pins on the onboard RJ45 connector are not connected.

Node assignments for the RJ45 Ethernet connector are shown in Table 3.

Table 3. Ethernet Connector Pin Assignments

Pin	Function
1	TX+
2	TX–
3	RX+
6	RX–

Node assignment, in contrast to hub assignment, means that a straight-through cable (equivalent pin numbers on both sides of the cable are connected to each other) is used to attach the board to an Ethernet hub or switch. To connect the eZ80190 Module directly to another node (e.g., a personal computer), a crossover cable must be used.

The EMAC can be additionally protected by placing a U9 ESD protection array on the module. This array can be either of the LCDA15C-6 (Semtech) or ESDA25B1 (ST Microelectronics) devices.

GPIO Pins for Enabling LAN Activity, Sleep, Interrupt

GPIO input bit PD4 serves as an active High interrupt input for the EMAC's INTRQ0 output.

GPIO output bit PD7 can be used to place the EMAC into SLEEP mode. In SLEEP mode, the CS8900 draws less current, because only the receiver is operating. A zero-Ohm resistor at position R14 on the eZ80190 is required for this function. In this case, the PD6 pin is not available for GPIO on the I/O connector.

If LAN activity is detected, the LANACT signal is pulled Low. The LANACT is connected to GPIO input PD6 and can be used in interrupt edge-detection mode to wake up and reinitialize the Ethernet chip. A zero-Ohm resistor at position R15 on

the module is required for this function. In this case, the PD6 pin is not available for GPIO on the I/O connector.

EMAC Ports

The I/O base address is user-selectable. The EMAC is connected as an 8-bit device.

EMAC Access

For 50MHz operation, set CS3_CTL (I/O address 0xB3) to 0xF8 (7 wait states for I/O). CS3 is used for selecting the Ethernet MAC. By pulling JP1 pin 25 (DIS_Eth) Low, access to the Ethernet MAC can be disabled on a per-cycle basis.

Memory

The eZ80190 offers SRAM and Flash memories and the wait states that support memory operations, as described in this section.

Wait States

To ensure that valid data is read from or written to slower memories, a number of wait states must be inserted into the memory or I/O access operations by the processor. The number of wait states that are required should be added by programming the chip select control registers. To calculate the minimum number of wait states required, refer to Table 4.

Table 4. Chip Frequency to Wait State Cycle Time Calculation

MHz	Cycle Time
20	50.0ns
24	41.7ns
40	25.0ns
50	20.0ns

Static RAM

The eZ80190 features 512KB of fast SRAM. Access speed is typically 12ns or faster, allowing zero-wait-state operation at 50MHz. With the CPU at 50MHz,

onboard SRAM can be accessed with zero wait states. The CS1_CTL register can be set to 08h (no wait states).

Flash Memory

The Flash Boot Loader, application code, and user configuration data are held permanently in NOR Flash memory. A typical application requires eight times more ROM for code than RAM. As an example, for 128KB onboard SRAM, 1MB of ROM is required. The eZ80190 allows NOR Flash memories between 4megabits (512KB) and 32 megabits (4MB) to be used. The chips are housed in wide TSOP40 cases. Typical Flash ROM access time is 100ns.

For 50MHz CPU operation, set the Chip Select Control register CS0_CTL (I/O address 0xAA) to 0xA8. This setting selects 5 wait states. CS0 is used for selecting Flash memory. By pulling JP1 pin 26 (DIS_Flash) Low, access to Flash memory can be disabled on a per-cycle basis.

Real-Time Clock

An onboard real-time-clock operates continually, even if the system power supply is down. An onboard capacitor (GoldCap) or external accumulator/battery serves as a standby power supply. The Real-Time-Clock M41T11 contains Binary Coded Decimal (BCD) counting registers for Seconds, Minutes, Hours, Day, Month, and Year; a Century bit and 56 bytes of backed-up RAM are also included. The fully charged 0.1F GoldCap bridges power outages with a maximum of 4 hours. The GoldCap, in contrast to a battery or an accumulator, offers the dual advantage of no service (replacement) requirements and no effects upon memory.

The I^2C addresses of the RTC are 0xD0 for WRITE and 0xD1 for READ. The I^2C sequence for writing to the RTC is:

Start → 0xD0 → RegNo → VALUE1 → … → VALUEn → Stop

and the sequence for reading from the RTC is:

Start → 0xD1 → RegNo → VALUE1 → … → VALUEn → Stop

where VALUE1…VALUEn… are sent by the RTC. The processor (I^2C Master) requests another value by sending an ACK. The first register to be read is set by a preceding WRITE sequence, without sending data values. Clock updates do not occur while any of the seven clock registers are being read. See Figure 5.

Table 5. Real-Time Clock Registers

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
0	ST	10 Seconds				Seconds			Seconds	00–59
1	X	10 Minutes				Minutes			Minutes	00–59
2	CEB*	CB	10 Hours			Hours			Hours	0–1/00–23
3	X	X	X	X	X	Day			Day	01–07
4	X	X	10 Date			Date			Date	01-31
5	X	X	X	10 M.		Month			Month	01–12
6	10 Years					Years			Year	00–99
7	OUT	FT	S			Calibration			Control	

Notes: *When CEB is set to 1, CB toggles from 0 to 1 or from 1 to 0 every 100 years, depending upon the initial vale set. When CEB is set to 0, CB does not toggle.

Keys: S = Sign bit, FT = Frequency Test bit, ST = Stop bit, OUT = Output level, X = Don't care, CEB = Century Enable bit, CB = Century Bit.

For further details, please refer to the M41T11 data sheet from SGS-Thomson at www.st.com.

Reset Generator

The onboard Reset Generator Chip performs reliable Power-On Reset. The chip generates a reset pulse with a duration of 200 ms if the power supply drops below 2.93 V. This reset pulse ensures that the board always starts in a defined condition. The RESET pin on the I/O connector reflects the status of the RESET line. It is a bidirectional pin for resetting external peripheral components or for resetting the eZ80190 with a low-impedance output (e.g. a 100-Ohm pushbutton).

Serial Interface Ports

The processor contains two 16550-style UARTs with programmable baud rate generators. When the eZ80190 Module is plugged in to the eZ80® Development Platform, UART0 is connected to a console connector and UART1 is connected to a modem connector. There are no RS232-level shifters on the eZ80190.

Note: Do not connect an RS-232 interface without level shifters.

Physical Dimensions

The footprint of the eZ80190 Module PCB is 63.5mmx78.7mm. With an RJ-45 Ethernet connector, the overall height is 25mm. See Figure 4.

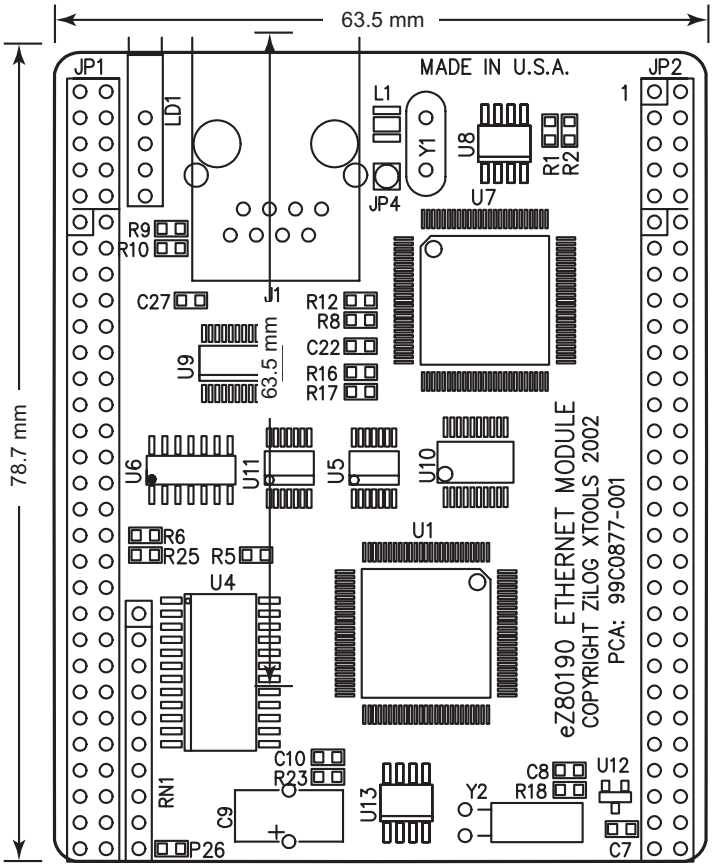


Figure 4. Physical Dimensions of the eZ80190 Module

Figure 5 illustrates the top layer silkscreen of the eZ80190 Module.

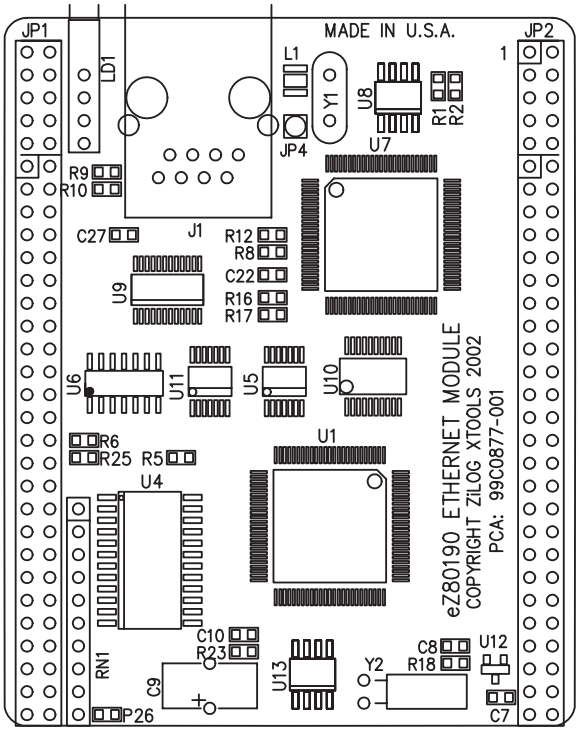


Figure 5. eZ80190 Module—Top Layer

Figure 6 illustrates the bottom layer silkscreen of the eZ80190 Module.

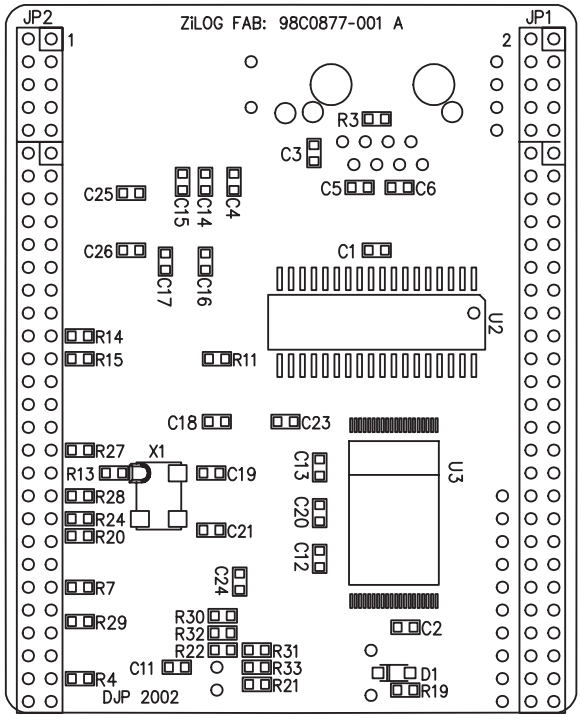


Figure 6. eZ80190 Module—Bottom Layer

ESD/EMI Protection

Caution: The eZ80190 is a component that is intended to be part of a system design for end-user devices. Therefore, the user must exercise caution to use ESD protection on the I/O pins.

The EMAC can be additionally protected by placing an ESD protection array on the eZ80190 at position U9. Either use ESDA25B1 from ST Microelectronics or LCDA15C-6 from Semtech. A mounting hole on the board can be used for grounding the shield of the Ethernet RJ45 jack to prevent surge or ESD currents from flowing through the digital circuitry.

The RJ45 Ethernet Connector on the eZ80190 contains a transformer and common mode chokes for EMI suppression.

Caution: CMOS I/Os are ESD-sensitive and must be handled with care. Handling of the module should be performed in ESD-safe environments (for example with a wrist-wrap attached). When

developing applications, the user must provide for proper ESD protection on external, user-accessible I/Os (e.g. suppressor arrays for the I/Os).

The components are mounted on a multilayer PCB to provide a stable ground plane for onboard components. The module features several GND pins next to pins with higher switching frequency for short ground returns. If unused, the clock output can be separated from the module header by removing a series resistor on the module. Removing the series resistor further reduces electromagnetic emissions.

Absolute Maximum Ratings

Stresses greater than those listed in Table 6 can cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, unused inputs should be tied to one of the supply voltages (V_{DD} or V_{SS}).

Table 6. Absolute Maximum Ratings

Parameter	Min	Max	Units
Standard operating temperature	0	+70	ºC
Storage temperature	–45	+85	ºC
Operating Humidity (RH @ 50ºC)	25%	90%	
Operating Voltage (±5%)	—	3.3	V

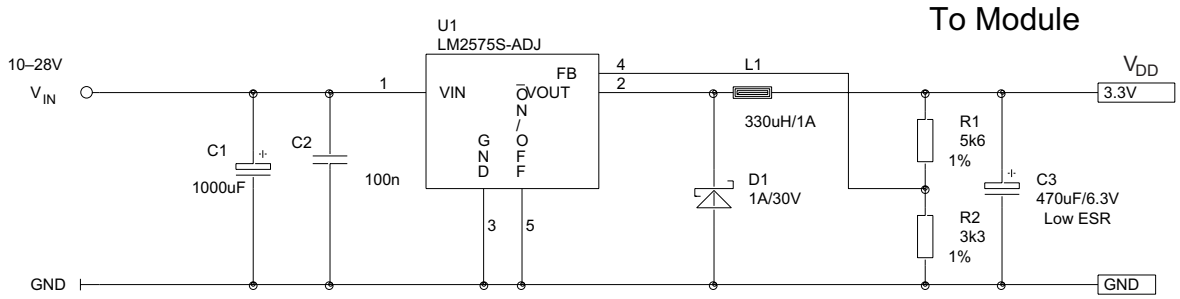
Power Supply

The eZ80™ Webserver-i E-NET Module requires a regulated external 3.3VDC/ 0.5A power supply. You may use a Low Dropout Regulator (LDO) to get 3.3V from 5V or use the following switcher circuit to generate 3.3V from unregulated 10-28V power supply.

Power connections follow these conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Switcher 10–28V → 3.3V



LDO 5V → 3.3V

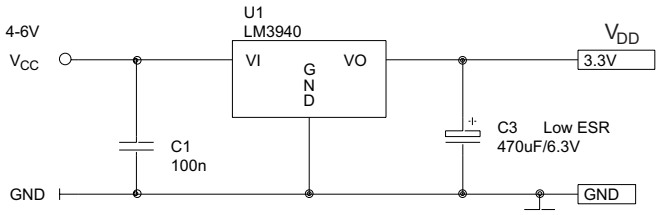


Figure 7. Power Supply Examples

Document Number Description

The Document Control Number that appears in the footer of each page of this document contains unique identifying attributes, as indicated in the following table:

PS	Product Specification
0191	Unique Document Number
01	Revision Number
1003	Month and Year Published

Change Log

Rev	Date	Purpose	By
01	October 2003	Original issue	M. Staubermann

Schematic Diagrams

Figures 8 through 15 present the schematics of the eZ80190 Module.

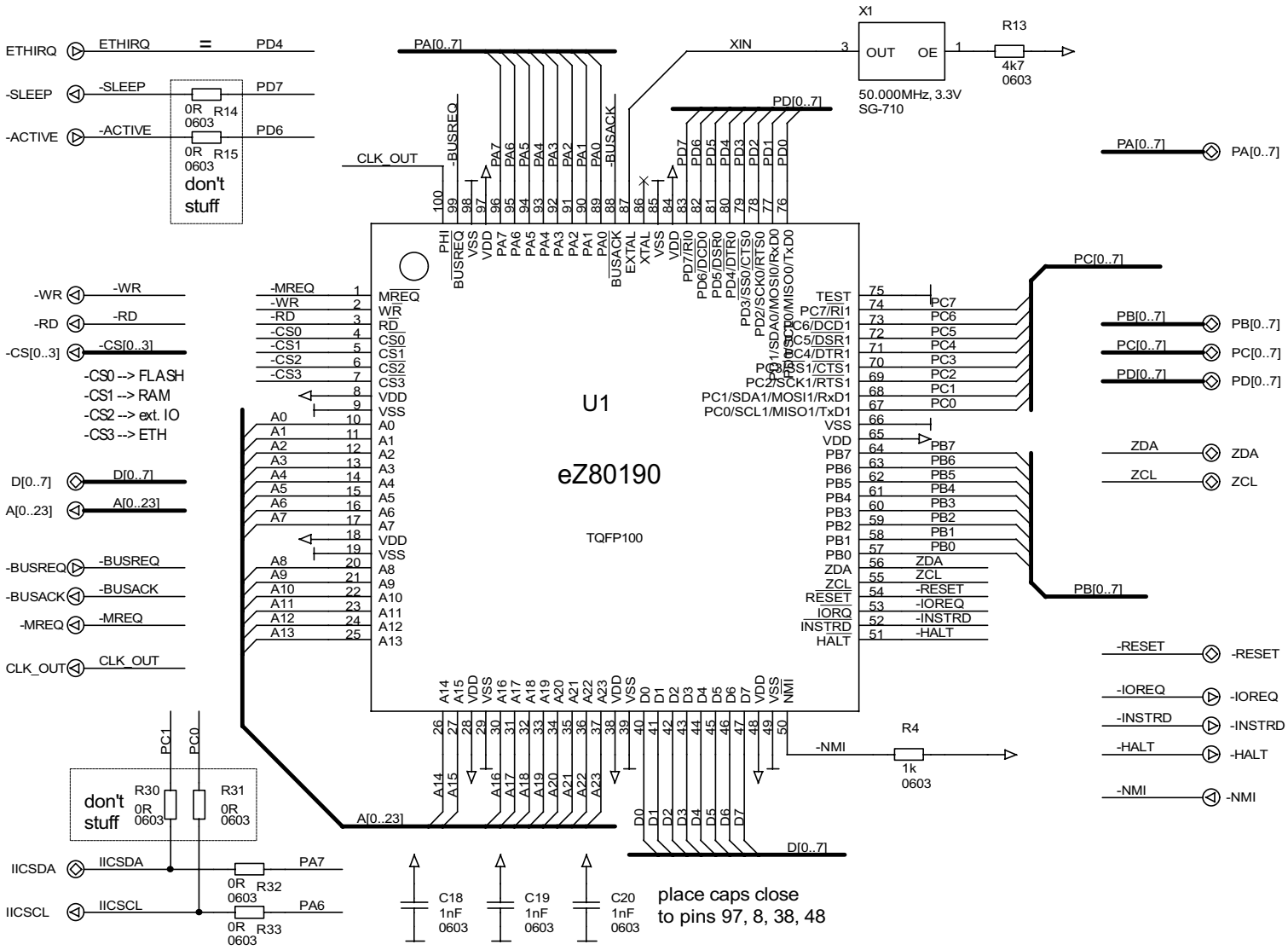


Figure 8. eZ80190 Module Schematic Diagram, #1 of 9—CPU

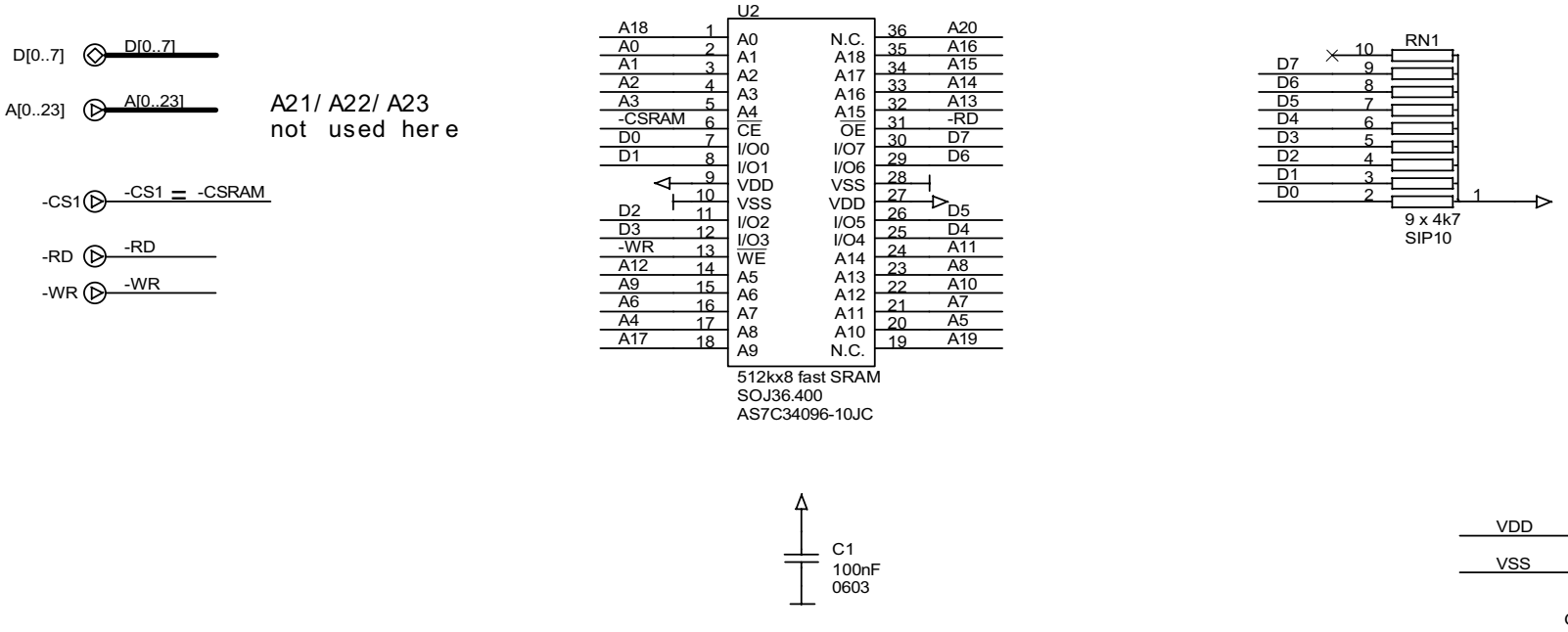


Figure 9. eZ80190 Module Schematic Diagram, #2 of 9—36-Pin SRAM Device

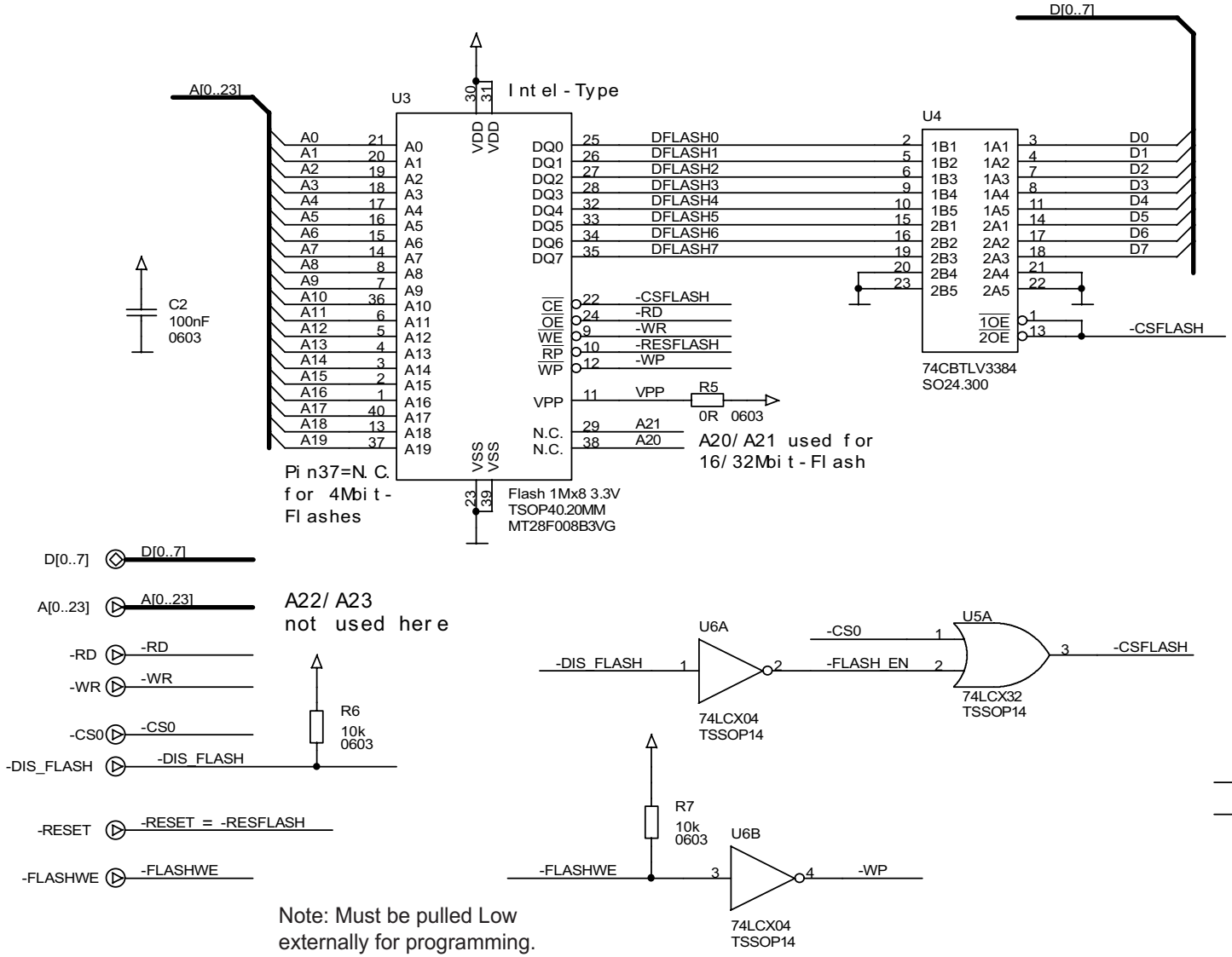


Figure 10. eZ80190 Module Schematic Diagram, #3 of 9—NOR Flash Device

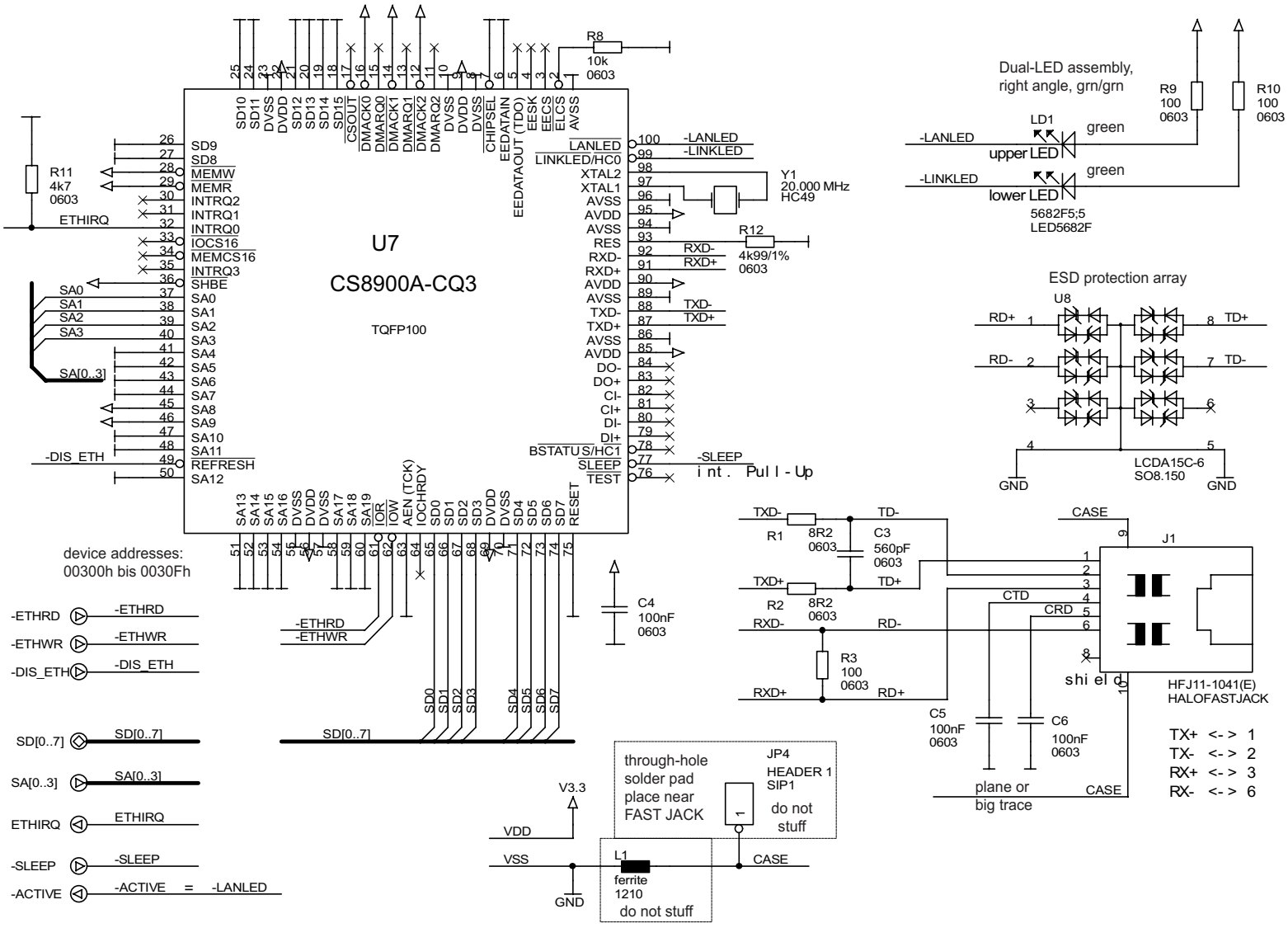


Figure 11. eZ80190 Module Schematic Diagram, #4 of 9—Ethernet Module

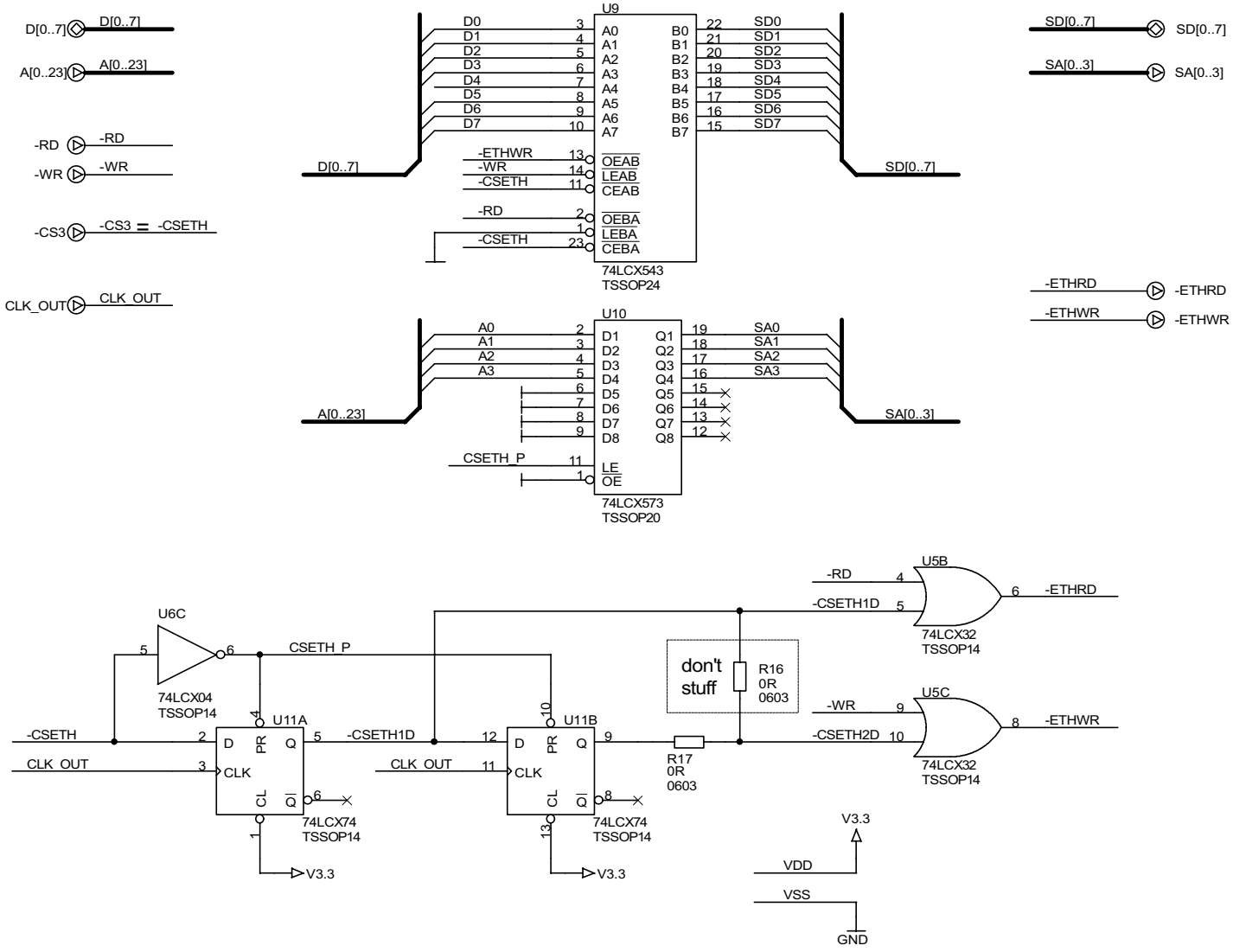


Figure 12. eZ80190 Module Schematic Diagram, #5 of 9—Ethernet Module Logic

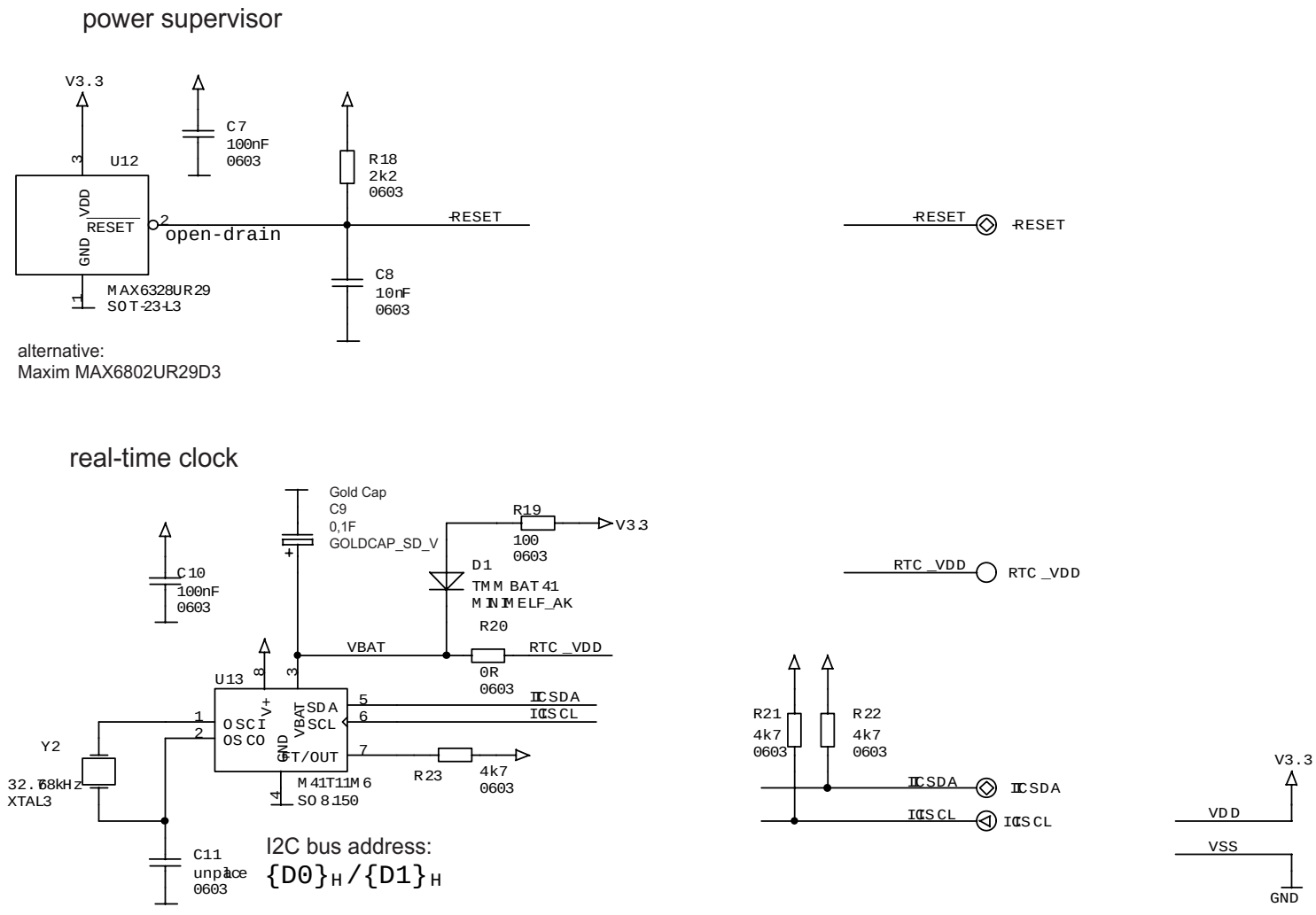


Figure 13. eZ80190 Module Schematic Diagram, #6 of 9—Ethernet Module Peripherals

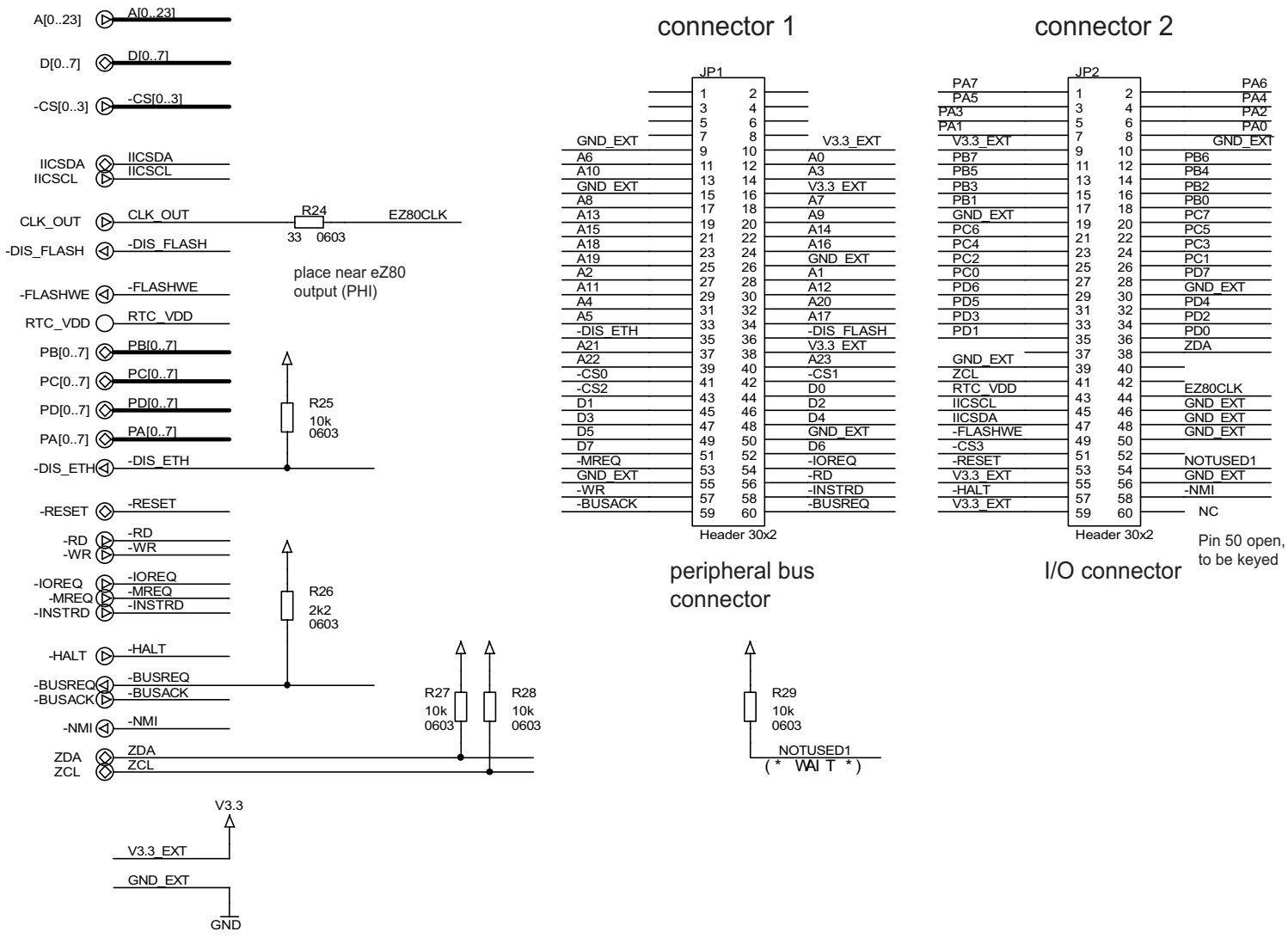
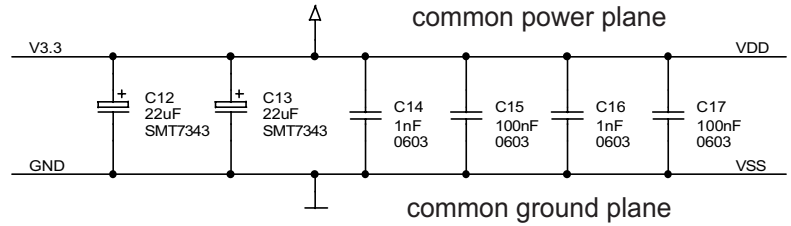


Figure 14. eZ80190 Module Schematic Diagram, #7 of 9—Headers

no power supply on board

Input: VDD (= V3.3) = 3.3V ±5%
Power: Pmax = tbd
Ptyp = tbd
Current: Imax = tbd
Ityp = tbd



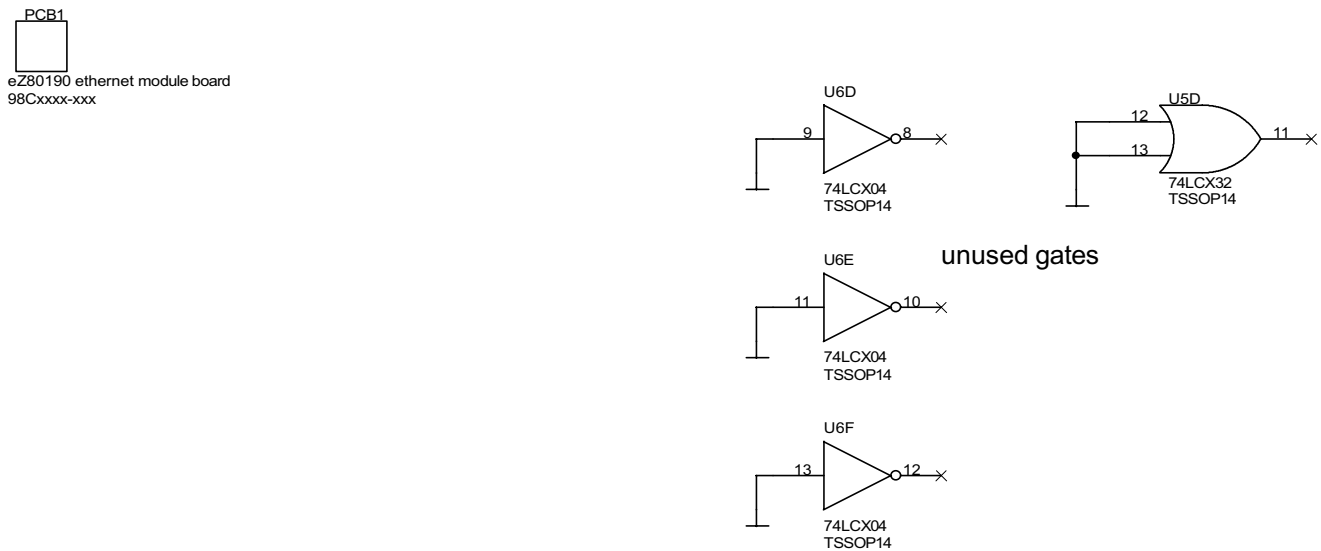


Figure 15. eZ80190 Module Schematic Diagram, #8 of 9—Power Supply

Customer Feedback Form

The eZ80190 Module Product Specification

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see *Return Information*, below). We also welcome your suggestions!

Customer Information

Name	Country
Company	Phone
Address	Fax
City/State/Zip	Email

Product Information

Serial # or Board Fab #/Rev. #
Software Version
Document Number
Host Computer Description/Type

Return Information

ZiLOG
System Test/Customer Support
532 Race Street
San Jose, CA 95126
Phone: (408) 558-8500
Fax: (408) 558-8536
ZiLOG Customer Support

Problem Description or Suggestion

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.