National Semiconductor

August 1990

F100371
Low Power Triple 4-Input Multiplexer with Enable

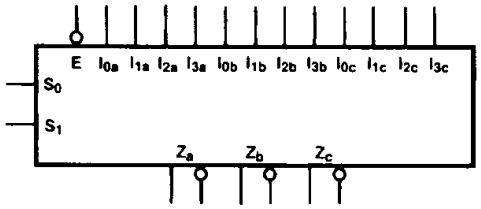
General Description

The F100371 contains three 4-input multiplexers which share a common decoder (inputs S_0 and S_1). Output buffer gates provide true and complement outputs. A HIGH on the Enable input ($\overline{E}$) forces all true outputs LOW (see Truth Table). All inputs have 50 kΩ pull-down resistors.

Features

- 35% power reduction of the F100171
- 2000V ESD protection
- Pin/function compatible with F100171
- Voltage compensated operating range = −4.2V to −5.7V

Logic Symbol



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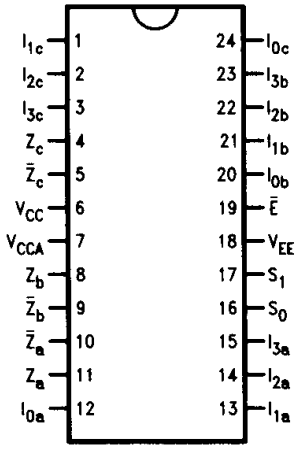
Pin Names	Description
I_{0x}–I_{3x}	Date Inputs
S_0, S_1	Select Inputs
$\overline{E}$	Enable Input (Active LOW)
Z_a–Z_c	Data Outputs
$\overline{Z}_a$–$\overline{Z}_c$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP



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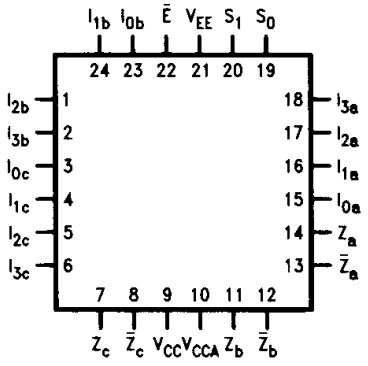
24-Pin Quad Cerpak



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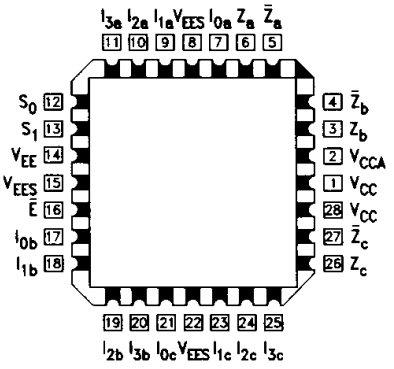
28-Pin PCC



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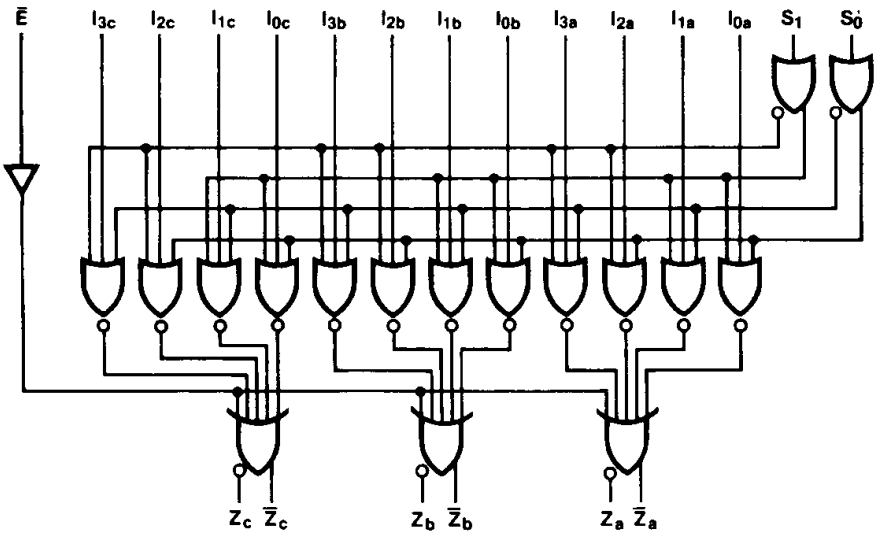
Logic Diagram



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Truth Table

Inputs			Outputs
$\overline{E}$	S_0	S_1	Z_n
L	L	L	I_{0x}
L	H	L	I_{1x}
L	L	H	I_{2x}
L	H	H	I_{3x}
H	X	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	
Commercial	−5.7V to −4.2V
Military	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current I_{0X}–I_{3X} S_0, S_1, $\overline{E}$			340 300	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−75		−39	mA	Inputs Open	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{0x}–I_{3x} to Output	0.45	1.50	0.45	1.50	0.45	1.60	ns	*Figures 1* and *2* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	0.90	2.40	0.90	2.40	1.00	2.60	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	0.65	2.30	0.65	2.30	0.75	2.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	*Figures 1* and *2*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{0x}–I_{3x} to Output	0.45	1.30	0.45	1.30	0.45	1.40	ns	*Figures 1* and *2* (Note 2)
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	0.90	2.20	0.90	2.20	1.00	2.40	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	0.65	2.10	0.65	2.10	0.75	2.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	*Figures 1* and *2*
$t_{s, G-G}$	Skew, Gate to Gate		TBD		TBD		TBD	ps	PCC Only (Note 1)

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version - Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current I_{0X}–I_{3X} S_0, S_1, $\overline{E}$		340 300	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
	I_{0X}–I_{3X} S_0, S_1, $\overline{E}$		490 450	μA	−55°C			
I_{EE}	Power Supply Current	−80	−30	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissapation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version - Preliminary (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay I_{0x}–I_{3x} to Output	0.30	1.90	0.40	1.70	0.30	2.00	ns	*Figures 1* and *2*	1, 2, 3, 5
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	0.40	2.70	0.60	2.40	0.50	2.90	ns		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	0.50	2.70	0.60	2.40	0.50	2.90	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.60	0.30	1.50	0.20	1.60	ns		4

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay I_{0x}–I_{3x} to Output	0.30	1.90	0.40	1.70	0.30	2.00	ns	*Figures 1* and *2*	1, 2, 3, 5
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	0.40	2.70	0.60	2.40	0.50	2.90	ns		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	0.50	2.70	0.60	2.40	0.50	2.90	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.60	0.30	1.50	0.20	1.60	ns		4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each mfg. lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

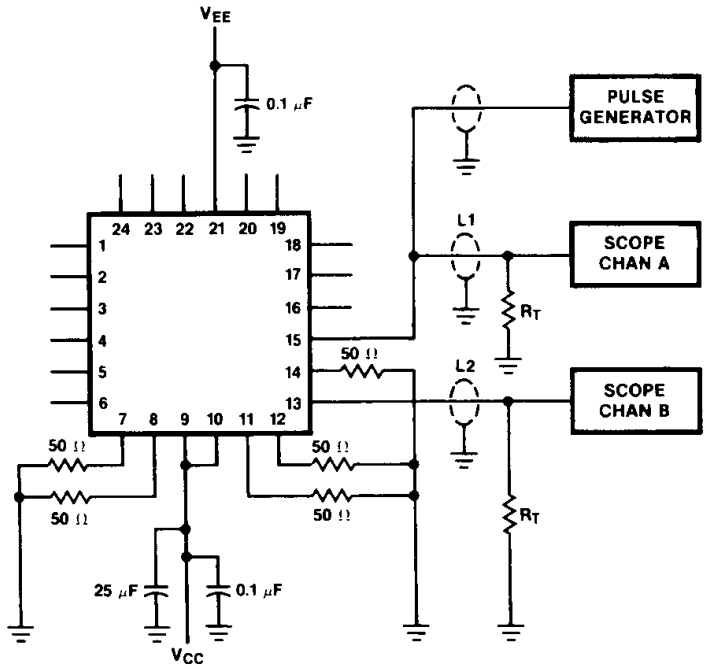

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FIGURE 1. AC Test Circuit

Switching Waveforms

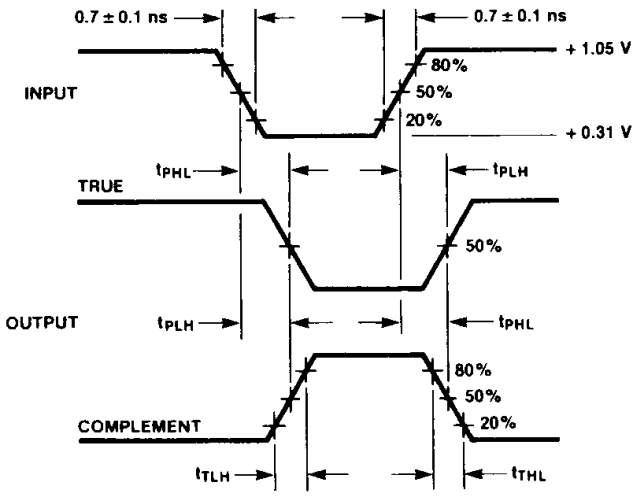

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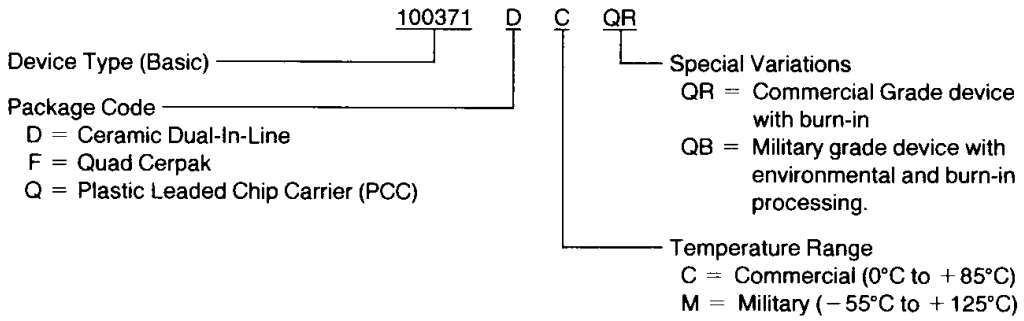
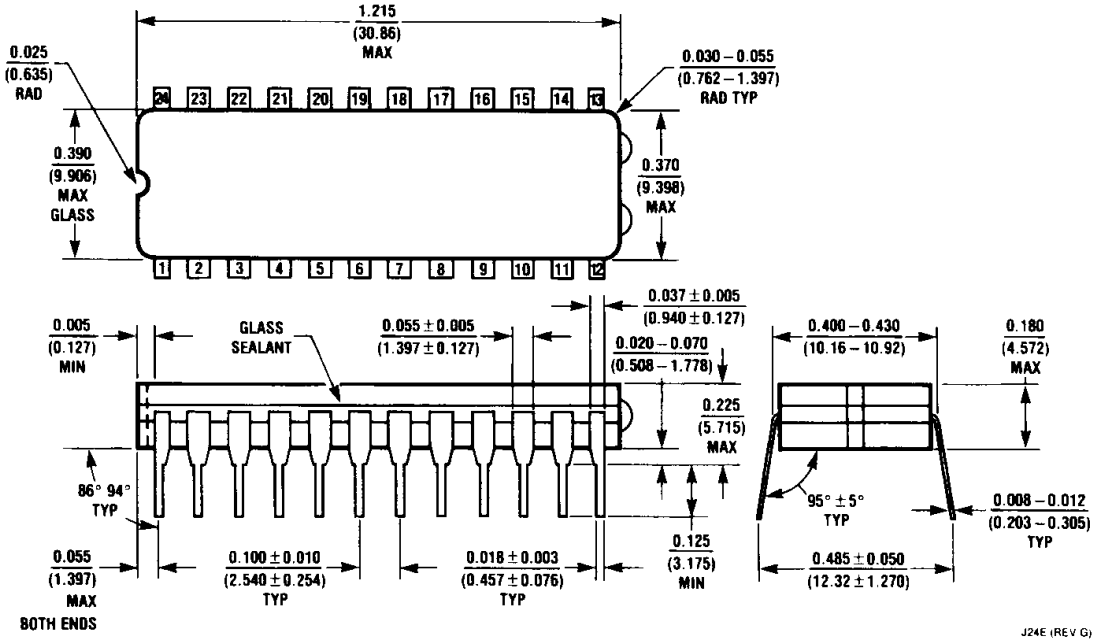
FIGURE 2. Propagation Delay and Transition Times

Ordering Information

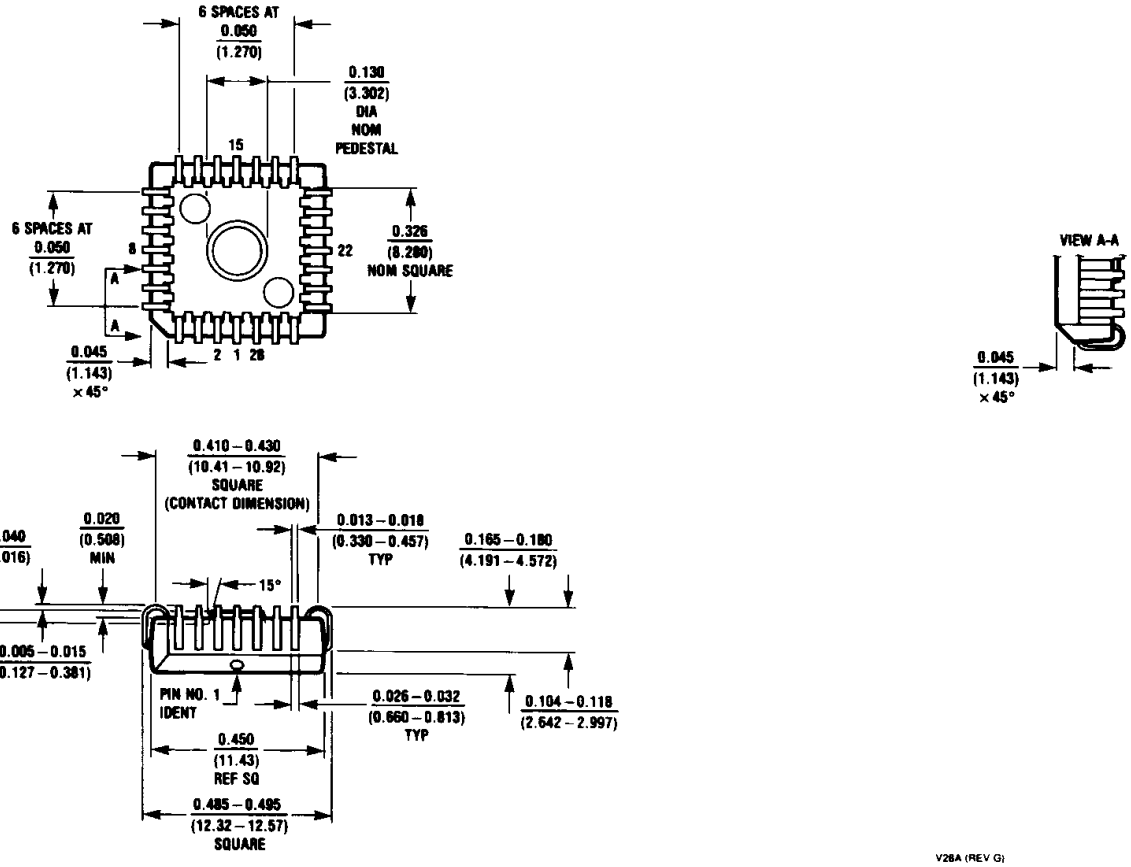
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)



24-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J24E

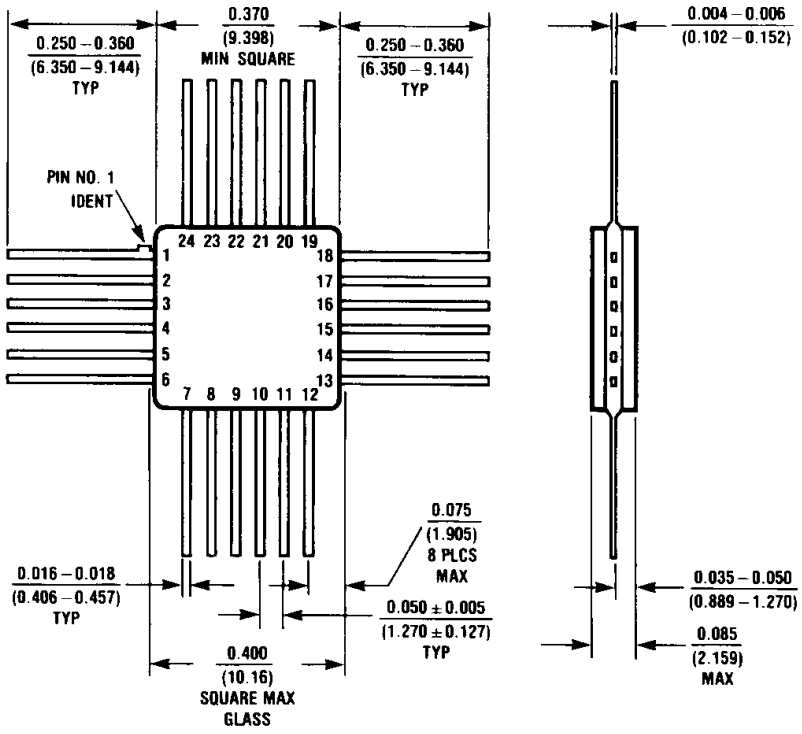


Note: Pedestal as shown on base is not available for F100K ECL products.

28-Lead Plastic Chip Carrier (Q)
NS Package Number V28A

Physical Dimensions inches (millimeters) (Continued)

Lit. # 114926



24-Lead Ceramic Flatpak (F)
NS Package Number W24B

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