F1Q28

Datasheet

Confidential / Preliminary Documentation

Revision 1.0

Bluetooth®

# List of Contents

1. General

1.1 Overview

This specification covers Bluetooth module (class-2) which complies with Bluetooth specification version 4.0 and integrates RF & Baseband controller in small package. This Module has adopted CSR's CSR8310 / CSR8311 Automotive QFN chipset.

All detailed specification including pinouts and electrical specification may be changed without notice.
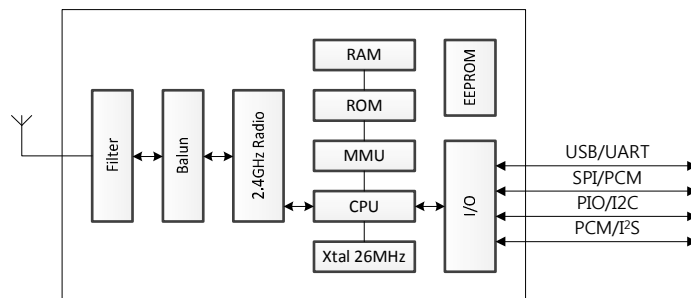

1.2 Features

- Fully Qualified Bluetooth v4.0
- Enhanced Data Rate (EDR) compliant with v2.1.E.2 of specification for both 2Mbps and 3Mbps modulation modes
- Full-speed Bluetooth Operation with Full Piconet Support and Scatternet Support
- Scatternet Support
- Low Power selectable 1.8 to 3.6V I/O
- No External regulators required for USB supply operation
- Full-Speed (12Mbps) USB 2.0 interface
- High-speed UART port (Up to 4Mbps)
- PCM/I²S digital audio interface
- Support for IEEE802.11 Co-existence
- Bluetooth low energy
- On Module SBC Encoding
- RoHS Compliant
- Integrated transcoders for A-law, u-law and linear PCM
- Standard HCI (UART and USB) support
- Integrated 16Kbit EEPROM(Option)
- Integrated 26MHz reference clock
- Operating temperature range (-40℃ ~ +85℃)

   - Automotive
- Supply voltage Range (1.8V ~ 5.7V)
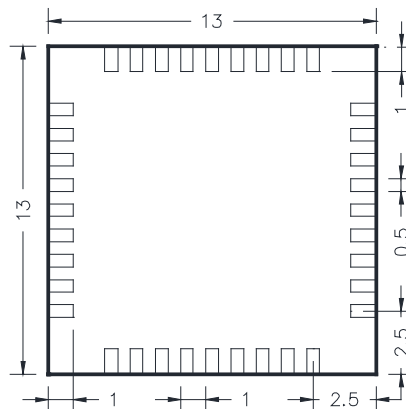- Competitive Size (13mm x 13mm x 1.7mm : QFN 36Pin)

1.3 Application

▪ Automotive Product

▪ USB Bluetooth Dongles

## 1.4 Pinout Diagram & Outline Size
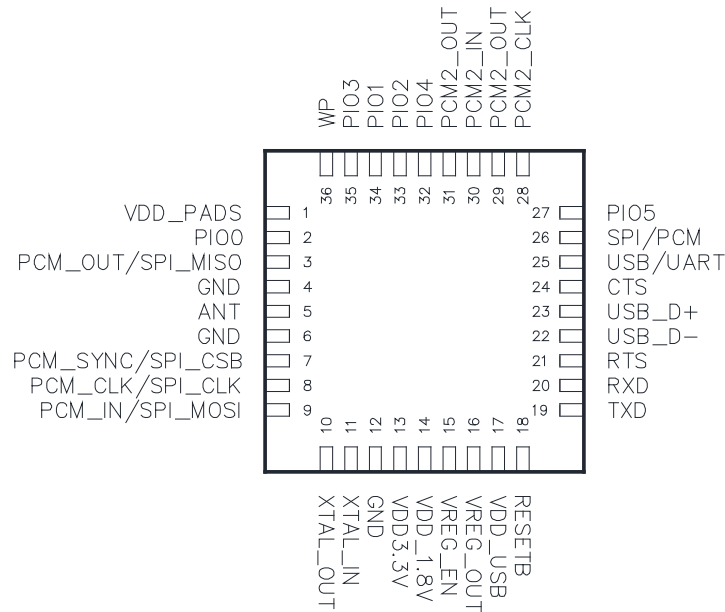
F1Q28 Pinout Diagram (Top View)

F1Q28 Size

1.5 Device Terminal Descriptions

	PIN	Name	Description
PCM/SPI	PCM OUT/SPI MISO	3	PCM1 Synchronous data output / SPI data output
	PCM IN/SPI MOSI	9	PCM1 Synchronous data input / SPI data input
	PCM CLK/SPI CLK	8	PCM1 Synchronous data clock / SPI clock
	PCM SYNC/SPI CSB	7	PCM1 Synchronous data sync / SPI chip select, active low
UART	TXD	19	UART data output, active low
	RXD	20	UART data input, active high
	CTS	24	UART clear to send, active low
	RTS	21	UART request to send, active low
USB	USB -	22	USB -
	USB +	23	USB + with selectable internal 1.5k pull-up resistor
PIO	PIO0	2	
	PIO1	34	
	PIO2	33	Programmable input/output line
	PIO3	35	
	PIO4	32	PIO 3,4 Can be used to form I2C interface
	PIO5	27	
PCM2	PCM2 OUT	31	PCM2 Serial Peripheral Interface data input
	PCM2 IN	30	PCM2 Serial Peripheral Interface clock
	PCM2 CLK	28	PCM2 Serial Peripheral Interface data output
	PCM2 Sync	29	PCM2 Chip Select for Synchronous SPI active low
Other Pins	ANT	5	RF Connection to Antenna
	GND	4,6,12	Ground
	VDD_USB	17	Input to USB Regulator. Connect to external USB bus supply.
	VDD_3V3	13	D.C input voltage for operation (3.0~3.3V)
	VDD_PADS	1	Positive supply for digital input/output pads.
	VDD_1V8	14	Output from internal high-voltage to 1.8V regulator.
	VREG_EN	15	Take high to enable internal regulator.
	VREG_OUT	16	Output to USB regulator. (Output VDD_3V3)
	SPI/PCM#	26	High : SPI Mode , Low : PCM(PIO) Mode
	USB/UART#	25	High : USB Mode , Low : UART Mode
	RESETB	18	Reset if low.
	X-Tal_IN	11	External Clock In(Option). Typical NC
	X-Tal_OUT	10	External Clock Out(Option). Typical NC
	WP	36	Internal EEPROM Write Protect.(High : Protection)

1.6 Land Pattern
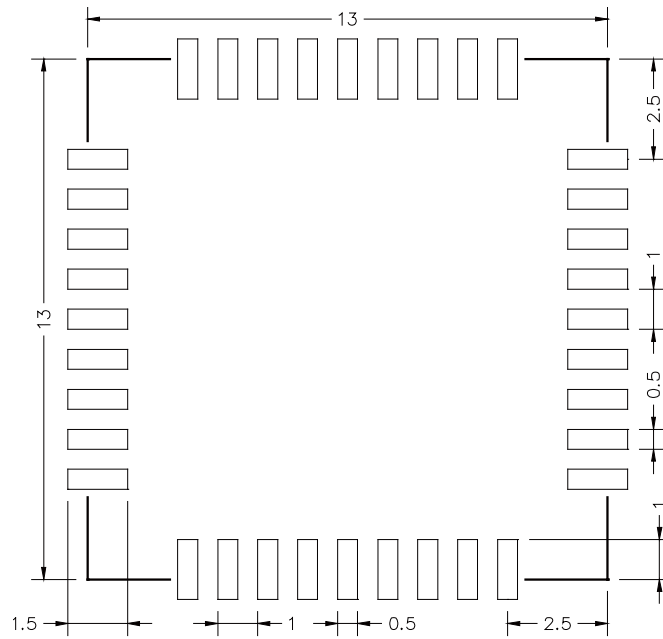
Land Pattern

2. Characteristics

2.1 Electrical Characteristics

Absolute Maximum Ratings		
Rating	Minimum	Maximum
Storage temperature	-40°C	85°C
VDD_USB	4.2V	5.75V
VDD_3V3	2.3V	4.8V
VDD_PADS	1.7V	3.6V
VREG_EN	1.2V	3.6V
VREG_OUT	3.1V	3.6V
VDD_1V8	1.7V	1.95V

Recommended Operating Temperature Conditions		
Operating Condition	Minimum	Maximum
Operating temperature range	-30°C	85°C

Recommended Operating Conditions		
Operating Condition	Typical	
VDD_USB	5V	IN
VDD_3V3	3.3V	IN
VDD_PADS	3.3V	IN
VREG_EN	3.3V	IN
VREG_OUT	3.3V	OUT
VDD_1V8	1.8V	OUT

2.2 RF Characteristics

Transmitter

Specification	Condition	Min	Typ	Max	Unit
Output transmit power	Normal	-6	1	4	dBm
Transmit power density	Normal			4	dBm
Transmit power control	Normal	2		8	dBm
Frequency Range	Normal	2400		2483.5	MHz
20dB bandwidth for modulated carrier	Normal		900	1000	KHz
Adjacent channel transmit power	±2MHz ±3MHz ±4MHz			-20 -40 -40	dBm
Modulation Characteristics	f1avg f2max f2avg / f1avg	140 115 		175 80	KHz KHz %
Initial carrier frequency tolerance	Normal	-20		20	KHz
Carrier frequency Drift	One slot packet(DH1) Three slot packet(DH3) Five slot packet(DH5)	-25 -40 -40		25 40 40	KHz

Transceiver

Specification	Condition	Min	Typ	Max	Unit
Adjacent channel transmit power	30MHz ~ 1GHz 1GHz ~12.75GHz 1.8GHz ~5.1GHz 5.1GHz ~5.3GHz			-36 -30 -47 -47	dBm

Receiver

Specification	Condition	Min	Typ	Max	Unit
Sensitivity level (0.1% BER)	Single slot packets	-70	-80		dBm
Transmit power density	Multi slot packet	-70	-80		dBm
C/I performance	co-channel 1MHz (Adjacent channel) 2MHz (2nd Adjacent channel) 3MHz (3rd Adjacent channel)			11 0 -30 -40	dB
Blocking performance	30MHz ~ 2000MHz 2000MHz ~ 2400MHz 2500MHz ~ 3000MHz 3000MHz ~ 12.75GHz	-10 -27 -27 -10			dBm
Intermodulation performance	n=5	-39			dBm
Maximum input level		-20	-10		dBm

3. Terminal Description

Host Interface Selection USB / UART# (Pin 25 Selection)
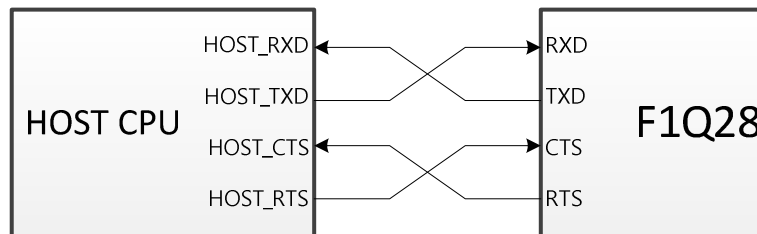
 USB Interface : 3V3 Connection

 UART Interface : GND Connection

3.1 UART

Four signals are used to implement the UART function.

UART_TX and UART_RX transfer data between the two devices.

The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active

low indicators.

3.1.1 UART Setting

User can change data format the following selection using PSKEY.

However, host shall communicate with default setting UART connection initiated at first time.

Parameter	Possible value
Baud Rate	1200 ~ 4M Baud
Flow Control	RTS/CTS or None
Parity	None, Odd or Even
Number of Stop Bits	1 or 2
Bits per channel	8

3.2 USB

F1Q28 Bluetooth Module has a full-speed (12Mbps) USB interface for communicating with other compatible digital devices. The USB

interface on the F1Q28 Bluetooth Module acts as a USB peripheral, responding to requests from a master host controller.

F1Q28 Bluetooth Module supports the Universal Serial Bus Specification,

Revision v2.0 (USB v2.0 Specification), available from http://www.usb.org.

For more information on how to integrate the USB interface on CSR8310 QFN see the Bluetooth and USB Design Considerations

Application Note .

As well as describing USB basics and architecture, the application note describes:

■ Power distribution for high and low bus-powered configurations

■ Power distribution for self-powered configuration, which includes USB VBUS monitoring

■ USB enumeration

■ Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads

■ USB suspend modes and Bluetooth low-power modes:

   ■ Global suspend

   ■ Selective suspend, includes remote wake

   ■ Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend

   ■ Suspend mode current draw

   ■ PIO status in suspend mode

   ■ Resume, detach and wake PIOs

■ Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS

voltage consideration

■ USB termination when interface is not in use

■ Internal modules, certification and non-specification compliant operation

3.3 I²C

EEPROM operation is not applicable to parts in UART mode.

F1Q28 Bluetooth Module uses an Internal I²C EEPROM to store device specific configuration information

(PS-Keys) such as Bluetooth address and USB descriptors.

Internal 16Kb EEPROM.(Option)

| EEPROM I²C Interface		
EEPROM	F1Q28	Description
SCL	PIO[3]	I²C Clock
SDA	PIO[4]	I²C Data
WP	WP	Write protect. Not driven by the CSR 8310 QFN. The Line the EEPROM WP Line active on PCB.

The I²C standard timing recommendations must be followed as regards correct pull-up and I²C bus data-line

capacitance limits. By default, the EEPROM is accessed at I²C standard (100kHz or below) rate, and switchable to fast 400kHz mode by

PS Key if the EEPROM supports fast I²C.

CSR recommends 400kHz capable EEPROM in these applications to ensure the USB bus power mode boot timing specifications are

met.

As an alternative the PS Keys are downloadable from the USB host.

This requires a 26MHz crystal operation, which enables the USB host interface to function using the default PS Key configuration.

The host must then supply all required PS Key information.
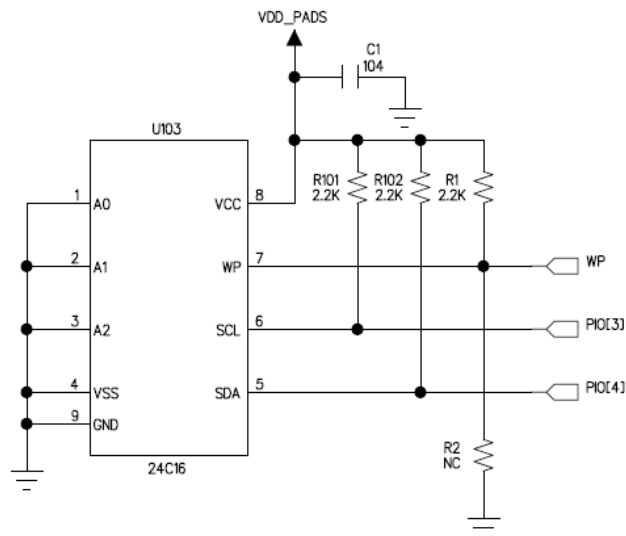
3.4 Audio Interface

SPI/PCM Selection (Pin 26 Selection)

   SPI Interface : 3V3 Connection

   PCM Interface : GND Connection

F1Q28 Bluetooth Module has a digital audio interface that can be configured as a PCM or I²S support.

3.4.1 PCM Configuration

Pulse Code Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, this module has hardware support for continual transmission and reception of PCM data, so reducing processor overhead for wireless headset applications. This module offers a bi-directional digital audio interface that route directly into the baseband layer of the on-chip firmware. It dose not pass through the HCI protocol layer.

Hardware allows the data to be sent to and received from a SCO connection. This module interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices

- OKI MSM7705 for channel A-law and u-law CODEC

- Motorola MC145481 8-bit A-law and u-law CODEC

- Motorola MC145483 13-bit linear CODEC

- STW 5093 and 5094 14-bit linear CODECs

F1Q28 has a digital audio interface that can be configured as a PCM port.

The audio PCM interface on the F1Q28 supports:

■ Continuous transmission and reception of PCM encoded audio data over Bluetooth.

■ Processor overhead reduction through hardware support for continual transmission and reception of PCM data

■ A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer.

■ Hardware on the F1Q28 for sending data to and from a SCO connection.

■ Up to 3 SCO connections on the PCM interface at any one time.

■ PCM interface master, generating PCM_SYNC and PCM_CLK.

■ PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.

■ Various clock formats including:

■ Long Frame Sync

■ Short Frame Sync

■ GCI timing environments

■ 13-bit or 16-bit linear, 8-bit μ-law or A-law commanded sample formats.

■ Receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC.

The PCM configuration options are enabled by setting the PS Key PSKEY_PCM_CONFIG32.

The PCM configuration is set using two PS keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The default for long frame sync and interface master generating 256KHz PCM_CLK with no tri-state of PCM_OUT.

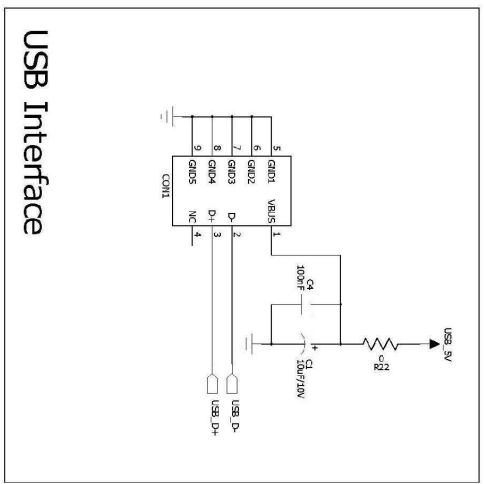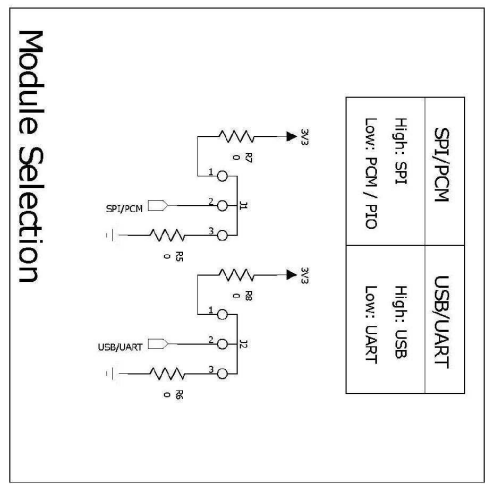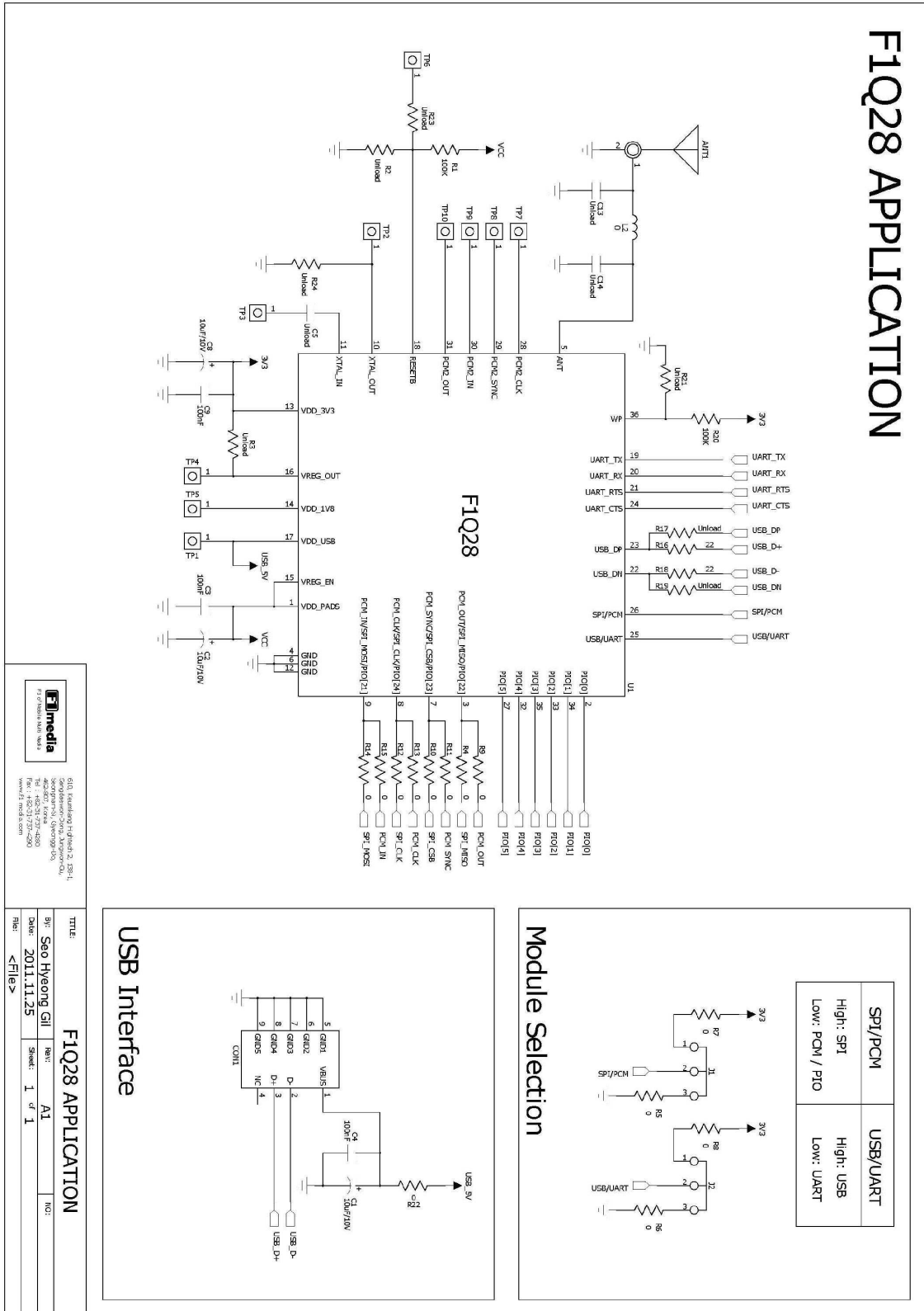| Parameter	Possible value
Mode	Slave, Master
Clock rate	Master Mode : 128,256,512,1536,2400 KHz Slave Mode : up to 2400 KHz
Sync formats	Long frame sync, Short frame sync
Data formats	13 or 16bit linear, 8-bit A-law to u-law

3.4.2 I²S Configuration

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified.

The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

4. Application Schematic

5. Revision History

Revision	Date	Change Descriptions	Issued by
Rev 1.0	2011.11.28	Initial release	J.M.KWON