

Flash

64 Mbit Serial Flash Memory  
with Dual and Quad

■ FEATURES

- Single supply voltage 2.65~3.6V
- Standard, Dual and Quad SPI
- Speed
  - Read max frequency: 50MHz
  - Fast Read max frequency: 50MHz / 86MHz / 104MHz
  - Fast Read Dual/Quad max frequency: 50MHz / 86MHz / 104MHz  
(100MHz / 172MHz / 208MHz equivalent Dual SPI;  
200MHz / 344MHz / 416MHz equivalent Quad SPI)
- Low power consumption
  - Active current: 25 mA (max.)
  - Standby current: 25 μA (max.)
  - Deep Power Down current: 10 μA (max.)
- Reliability
  - 100,000 typical program/erase cycles
  - 20 years Data Retention
- Program
  - Page programming time: 1.5 ms (typical)
- Erase
  - Chip Erase time 35 sec (typical)
  - 64K bytes Block Erase time 1 sec (typical)
  - 32K bytes Block Erase time 500 ms (typical)
  - 4K bytes Sector Erase time 120 ms (typical)
- Page Programming
  - 256 byte per programmable page
- Program / Erase Suspend and Resume
- Lockable 512 bytes OTP security sector
- SPI Serial Interface
  - SPI Compatible: Mode 0 and Mode 3
- End of program or erase detection
- Write Protect (  $\overline{WP}$  )
- Hold Pin (  $\overline{HOLD}$  )
- All Pb-free products are RoHS-Compliant

■ ORDERING INFORMATION

Product ID	Speed	Package		Comments
F25L64QA –50PAG	50MHz	8-lead SOIC	200 mil	Pb-free
F25L64QA –86PAG	86MHz			
F25L64QA –100PAG	104MHz			
F25L64QA –50PHG	50MHz	16-lead SOIC	300 mil	Pb-free
F25L64QA –86PHG	86MHz			
F25L64QA –100PHG	104MHz			
F25L64QA –50HG	50MHz	8-contact WSON	6x5 mm	Pb-free
F25L64QA –86HG	86MHz			
F25L64QA –100HG	104MHz			
F25L64QA –50VAG	50MHz	8-lead VSOP	208mil	Pb-free
F25L64QA –86VAG	86MHz			
F25L64QA –100VAG	104MHz			

■ GENERAL DESCRIPTION

The F25L64QA is a 64Megabit, 3V only CMOS Serial Flash memory device. The device supports the standard Serial Peripheral Interface (SPI), and a Dual/Quad SPI. ESMT's memory devices reliably store memory data even after 100,000 programming and erase cycles.

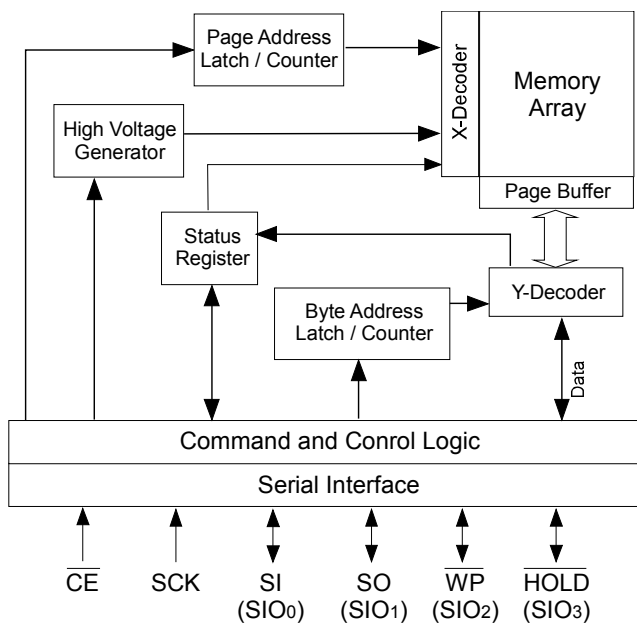
The memory array can be organized into 32,768 programmable pages of 256 byte each. 1 to 256 byte can be programmed at a time with the Page Program instruction.

The device features sector erase architecture. The memory array

is divided into 2,048 uniform sectors with 4K byte each; 256 uniform blocks with 32K byte each; 128 uniform blocks with 64K byte each. Sectors can be erased individually without affecting the data in other sectors. Blocks can be erased individually without affecting the data in other blocks. Whole chip erase capabilities provide the flexibility to revise the data in the device. The device has Sector, Block or Chip Erase but no page erase.

The sector protect/unprotect feature disables both program and erase operations in any combination of the sectors of the memory.

■ FUNCTIONAL BLOCK DIAGRAM

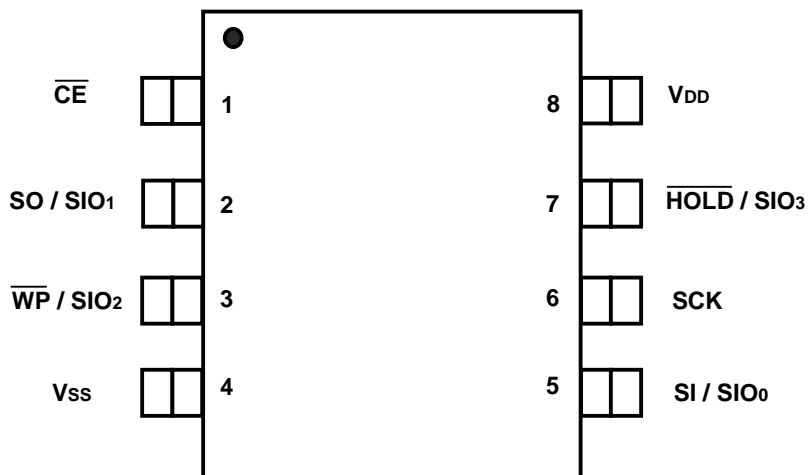


■ PIN CONFIGURATIONS

**8-Lead SOIC / 8-Lead VSOP**

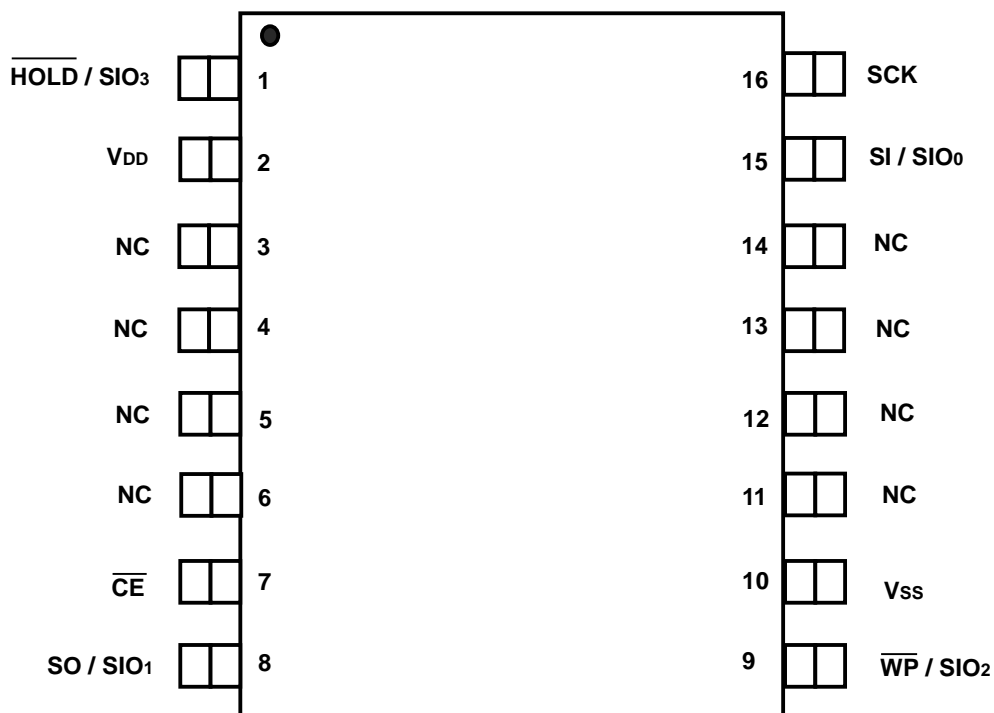
(SOIC 8L, 208mil Body, 1.27mm Pin Pitch)

(SOIC 8L, 208mil Body with thickness 1.0mm, 1.27mm Pin Pitch)



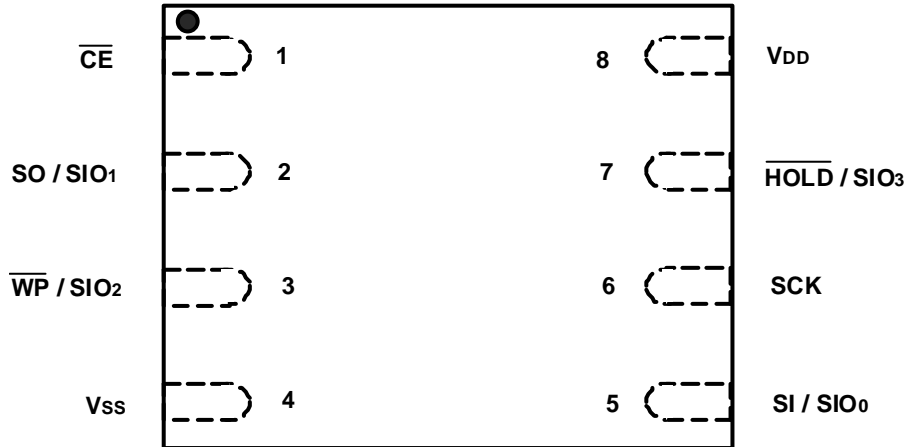
**16-Lead SOIC**

(SOIC 16L, 300mil Body, 1.27mm Pin Pitch)



**8-Contact WSON**

(WSON 8C, 6mmX5mm Body, 1.27mm Contact Pitch)



■ **PIN DESCRIPTION**

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing for serial input and output operations
SI / SIO <sub>0</sub>	Serial Data Input / Serial Data Input Output 0	To transfer commands, addresses or data serially into the device. Data is latched on the rising edge of SCK (for Standard read mode). / Bidirectional IO pin to transfer commands, addresses or data serially into the device on the rising edge of SCK and read data or status from the device on the falling edge of SCK(for Dual/Quad mode).
SO / SIO <sub>1</sub>	Serial Data Output / Serial Data Input Output 1	To transfer data serially out of the device. Data is shifted out on the falling edge of SCK (for Standard read mode). / Bidirectional IO pin to transfer commands, addresses or data serially into the device on the rising edge of SCK and read data or status from the device on the falling edge of SCK (for Dual/Quad mode).
$\overline{CE}$	Chip Enable	To activate the device when $\overline{CE}$ is low.
$\overline{WP}$ / SIO <sub>2</sub>	Write Protect / Serial Data Input Output 2	The Write Protect ( $\overline{WP}$ ) pin is used to enable/disable BPL bit in the status register. / Bidirectional IO pin to transfer commands, addresses or data serially into the device on the rising edge of SCK and read data or status from the device on the falling edge of SCK (for Quad mode).
$\overline{HOLD}$ / SIO <sub>3</sub>	Hold / Serial Data Input Output 3	To temporality stop serial communication with SPI flash memory without resetting the device. / Bidirectional IO pin to transfer commands, addresses or data serially into the device on the rising edge of SCK and read data or status from the device on the falling edge of SCK (for Quad mode).
VDD	Power Supply	To provide power.
Vss	Ground	

■ SECTOR STRUCTURE

Table 1: Sector Address Table

64KB Block	32KB Block	Sector	Sector Size (Kbytes)	Address range
127	255	2047	4KB	7FF000h – 7FFFFFFh
		:	:	:
		2040	4KB	7F8000h – 7F8FFFh
	254	2039	4KB	7F7000h – 7F7FFFh
		:	:	:
		2032	4KB	7F0000h – 7F0FFFh
126	253	2031	4KB	7EF000h – 7EFFFFh
		:	:	:
		2024	4KB	7E8000h – 7E8FFFh
	252	2023	4KB	7E7000h – 7E7FFFh
		:	:	:
		2016	4KB	7E0000h – 7E0FFFh
125	251	2015	4KB	7DF000h – 7DFFFFh
		:	:	:
		2008	4KB	7D8000h – 7D8FFFh
	250	2007	4KB	7D7000h – 7D7FFFh
		:	:	:
		2000	4KB	7D0000h – 7D0FFFh

individual  
16 sectors  
unit: 4KB

individual  
block unit:  
64KB



2	5	47	4KB	02F000h – 02FFFFh
		:	:	:
		40	4KB	028000h – 028FFFh
	4	39	4KB	027000h – 027FFFh
		:	:	:
1	3	32	4KB	020000h – 020FFFh
		31	4KB	01F000h – 01FFFFh
		:	:	:
	2	24	4KB	018000h – 018FFFh
		23	4KB	017000h – 017FFFh
		:	:	:
0	1	16	4KB	010000h – 010FFFh
		15	4KB	00F000h – 00FFFFh
		:	:	:
	0	8	4KB	008000h – 008FFFh
		7	4KB	007000h – 007FFFh
0	4KB	000000h – 000FFFh		

individual  
16 sectors  
unit: 4KB

## ■ STATUS REGISTER

The software status register provides status on whether the flash memory array is available for any Read or Write operation, whether the device is Write enabled, and the state of the memory Write protection. During an internal Erase or Program operation,

the status register may be read only to determine the completion of an operation in progress. Table 2 describes the function of each bit in the software status register.

**Table 2: Software Status Register**

Bit	Name	Function	Default at Power-up	Read/Write
<b>Status Register -1</b>				
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection (See Table 3)	0	R/W
3	BP1	Indicate current level of block write protection (See Table 3)	0	R/W
4	BP2	Indicate current level of block write protection (See Table 3)	0	R/W
5	BP3	Indicate current level of block write protection (See Table 3)	0	R/W
6	QE	1 = Quad enabled 0 = Quad disabled	0	R/W
7	BPL	1 = BP3, BP2, BP1, BP0 are read-only bits 0 = BP3, BP2, BP1, BP0 are read/writable	0	R/W

Bit	Name	Function	Default at Power-up	Read/Write
<b>Status Register -2</b>				
8	SUS	Suspend Status	0	R
9~15	Reserved	Reserved for future use	0	N/A

Note:

1. BUSY and WEL are read only.
2. BP0~3, QE and BPL bits are non-volatile.

### Write Enable Latch (WEL)

The Write-Enable-Latch bit indicates the status of the internal memory Write Enable Latch. If this bit is set to "1", it indicates the device is Write enabled. If the bit is set to "0" (reset), it indicates the device is not Write enabled and does not accept any memory Write (Program/ Erase) commands. This bit is automatically reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Page Program instruction completion
- Sector Erase instruction completion
- Block Erase instruction completion
- Chip Erase instruction completion
- Write Status Register instructions

### BUSY

The BUSY bit determines whether there is an internal Erase or Program operation in progress. A "1" for the BUSY bit indicates the device is busy with an operation in progress. A "0" indicates the device is ready for the next valid operation.

Table 3: F25L64QA Block Protection Table

Protection Level	Status Register Bit				Protected Memory Area
	BP3	BP2	BP1	BP0	64KB Block Range
0	0	0	0	0	None
Upper 1/64	0	0	0	1	Block 126~127
Upper 1/32	0	0	1	0	Block 124~127
Upper 1/16	0	0	1	1	Block 120~127
Upper 1/8	0	1	0	0	Block 112~127
Upper 1/4	0	1	0	1	Block 96~127
Upper 1/2	0	1	1	0	Block 64~127
All Blocks	0	1	1	1	Block 0~127
All Blocks	1	0	0	0	Block 0~127
Bottom 1/2	1	0	0	1	Block 0~63
Bottom 3/4	1	0	1	0	Block 0~95
Bottom 7/8	1	0	1	1	Block 0~111
Bottom 15/16	1	1	0	0	Block 0~119
Bottom 31/32	1	1	0	1	Block 0~123
Bottom 63/64	1	1	1	0	Block 0~125
All Blocks	1	1	1	1	Block 0~127

**Block Protection (BP3, BP2, BP1, BP0)**

The Block-Protection (BP3, BP2, BP1, BP0) bits define the memory area, as defined in Table 3, to be software protected against any memory Write (Program or Erase) operations. The Write Status Register (WRSR) instruction is used to program the BP3, BP2, BP1 and BP0 bits as long as  $\overline{WP}$  is high or the Block-Protection-Look (BPL) bit is 0. Chip Erase can only be executed if BP3, BP2, BP1 and BP0 bits are all 0. The factory default setting for Block Protection Bit (BP3 ~ BP0) is 0.

**Quad Enable (QE)**

When the Quad Enable bit is reset to "0" (factory default),  $\overline{WP}$  and  $\overline{HOLD}$  pins are enabled. When QE pin is set to "1", Quad SIO<sub>2</sub> and SIO<sub>3</sub> are enabled. (The QE should never be set to "1" during standard and Dual SPI operation if the  $\overline{WP}$  and  $\overline{HOLD}$  pins are tied directly to the V<sub>DD</sub> or V<sub>SS</sub>.)

**Block Protection Lock-Down (BPL)**

$\overline{WP}$  pin driven low (V<sub>IL</sub>), enables the Block-Protection-Lock-Down (BPL) bit. When BPL is set to 1, it prevents any further alteration of the BPL, BP3, BP2, BP1 and BP0 bits. When the  $\overline{WP}$  pin is driven high (V<sub>IH</sub>), the BPL bit has no effect and its value is "Don't Care".

**Program / Erase Suspend Status (SUS)**

The Suspend Status bit is a read only bit in the status register that is set to 1 after executing a Program / Erase Suspend (75H) instruction. The SUS Status bit is cleared to 0 by Program / Erase Resume (7AH) instruction as well as a power-down, power-up cycle.

■ HOLD OPERATION

$\overline{\text{HOLD}}$  pin is used to pause a serial sequence underway with the SPI flash memory without resetting the clocking sequence. To activate the  $\overline{\text{HOLD}}$  mode,  $\overline{\text{CE}}$  must be in active low state. The  $\overline{\text{HOLD}}$  mode begins when the  $\overline{\text{SCK}}$  active low state coincides with the falling edge of the  $\overline{\text{HOLD}}$  signal. The HOLD mode ends when the  $\overline{\text{HOLD}}$  signal's rising edge coincides with the  $\overline{\text{SCK}}$  active low state.

If the falling edge of the  $\overline{\text{HOLD}}$  signal does not coincide with the  $\overline{\text{SCK}}$  active low state, then the device enters Hold mode when the  $\overline{\text{SCK}}$  next reaches the active low state.

Similarly, if the rising edge of the  $\overline{\text{HOLD}}$  signal does not coincide with the  $\overline{\text{SCK}}$  active low state, then the device exits in Hold mode when the  $\overline{\text{SCK}}$  next reaches the active low state. See Figure 1 for Hold Condition waveform.

Once the device enters Hold mode,  $\text{SO}$  will be in high impedance state while  $\text{SI}$  and  $\text{SCK}$  can be  $V_{\text{IL}}$  or  $V_{\text{IH}}$ .

If  $\overline{\text{CE}}$  is driven active high during a Hold condition, it resets the internal logic of the device. As long as  $\overline{\text{HOLD}}$  signal is low, the memory remains in the Hold condition. To resume communication with the device,  $\overline{\text{HOLD}}$  must be driven active high, and  $\overline{\text{CE}}$  must be driven active low. See Figure 31 for Hold timing.

The  $\overline{\text{HOLD}}$  function is only available for Standard SPI and Dual SPI operation, not during Quad SPI because this pin is used for  $\text{SIO}_3$  when the  $\text{QE}$  bit of Status Register-1 is set for Quad I/O.

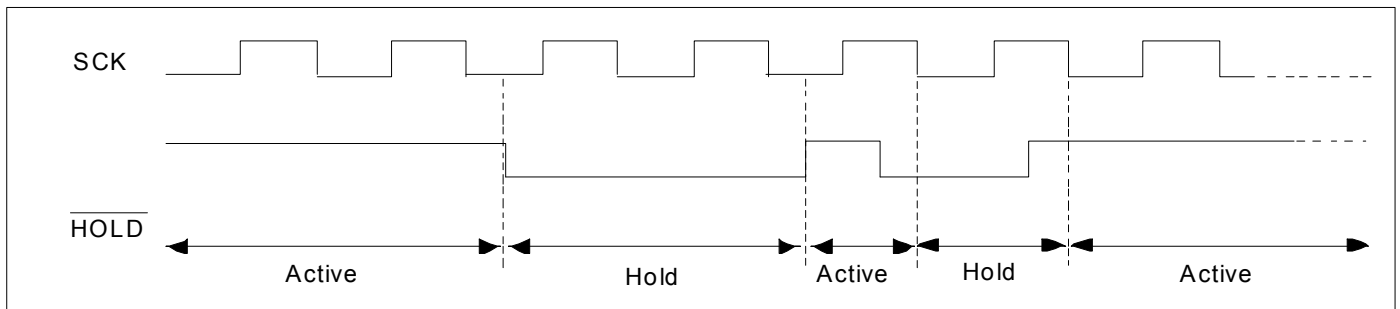


Figure 1: HOLD Condition Waveform

■ WRITE PROTECTION

The device provides software Write Protection.

The Write-Protect pin ( $\overline{\text{WP}}$ ) enables or disables the lock-down function of the status register. The Block-Protection bits ( $\text{BP}_3$ ,  $\text{BP}_2$ ,  $\text{BP}_1$ ,  $\text{BP}_0$  and  $\text{BPL}$ ) in the status register provide Write protection to the memory array and the status register. When the  $\text{QE}$  bit of Status Register-1 is set for Quad I/O, the  $\overline{\text{WP}}$  pin function is not available since this pin is used for  $\text{SIO}_2$ .

Write Protect Pin ( $\overline{\text{WP}}$ )

The Write-Protect ( $\overline{\text{WP}}$ ) pin enables the lock-down function of the  $\text{BPL}$  bit (bit 7) in the status register. When  $\overline{\text{WP}}$  is driven low, the execution of the Write Status Register ( $\text{WRSR}$ ) instruction is determined by the value of the  $\text{BPL}$  bit (see Table 4). When  $\overline{\text{WP}}$  is high, the lock-down function of the  $\text{BPL}$  bit is disabled.

Table 4: Conditions to Execute Write-Status- Register ( $\text{WRSR}$ ) Instruction

$\overline{\text{WP}}$	$\text{BPL}$	Execute $\text{WRSR}$ Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed



■ INSTRUCTIONS

Instructions are used to Read, Write (Erase and Program), and configure the F25L64QA. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. Prior to executing any Page Program, Write Status Register, Sector Erase, Block Erase, or Chip Erase instructions, the Write Enable (WREN) instruction must be executed first. The complete list of the instructions is provided in Table 5. All instructions are synchronized off a high to low transition of  $\overline{CE}$ . Inputs will be accepted on the rising edge of SCK starting with the most significant bit.  $\overline{CE}$  must be driven low before an instruction is

entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read ID, Read Status Register, Read Electronic Signature instructions). Any low to high transition on  $\overline{CE}$ , before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to the standby mode.

Instruction commands (Op Code), addresses, and data are all input from the most significant bit (MSB) first.

Table 5: Device Operation Instruction

Operation	Max. Freq	Bus Cycle <sup>1-3</sup>															
		1		2		3		4		5		6		N			
		S <sub>IN</sub>	S <sub>OUT</sub>	S <sub>IN</sub>	S <sub>OUT</sub>	S <sub>IN</sub>	S <sub>OUT</sub>	S <sub>IN</sub>	S <sub>OUT</sub>	S <sub>IN</sub>	S <sub>OUT</sub>	S <sub>IN</sub>	S <sub>OUT</sub>	S <sub>IN</sub>	S <sub>OUT</sub>		
Read	50 MHz	03H	Hi-Z	A <sub>23</sub> -A <sub>16</sub>	Hi-Z	A <sub>15</sub> -A <sub>8</sub>	Hi-Z	A <sub>7</sub> -A <sub>0</sub>	Hi-Z	X	D <sub>OUT0</sub>	X	D <sub>OUT1</sub>	X	cont.		
Fast Read	50MHz	0BH	Hi-Z	A <sub>23</sub> -A <sub>16</sub>	Hi-Z	A <sub>15</sub> -A <sub>8</sub>	Hi-Z	A <sub>7</sub> -A <sub>0</sub>	Hi-Z	X	X	X	D <sub>OUT0</sub>	X	cont.		
Fast Read Dual Output <sup>12,13</sup>		3BH		A <sub>23</sub> -A <sub>16</sub>		A <sub>15</sub> -A <sub>8</sub>		A <sub>7</sub> -A <sub>0</sub>		X		D <sub>OUT0-1</sub>			cont.		
Fast Read Dual I/O <sup>12,14</sup>		BBH		A <sub>23</sub> -A <sub>8</sub>		A <sub>7</sub> -A <sub>0</sub> , M <sub>7</sub> -M <sub>0</sub>			D <sub>OUT0-1</sub>		cont.				-		
Fast Read Quad Output <sup>12,15</sup>		6BH		A <sub>23</sub> -A <sub>16</sub>		A <sub>15</sub> -A <sub>8</sub>		A <sub>7</sub> -A <sub>0</sub>		X		D <sub>OUT0-3</sub>			cont.		
Fast Read Quad I/O <sup>12,16</sup>		EBH		A <sub>23</sub> -A <sub>0</sub> , M <sub>7</sub> -M <sub>0</sub>		X, D <sub>OUT0-1</sub>			D <sub>OUT2-6</sub>		cont.				-		
Sector Erase <sup>4</sup> (4K Byte)		20H	Hi-Z	A <sub>23</sub> -A <sub>16</sub>	Hi-Z	A <sub>15</sub> -A <sub>8</sub>	Hi-Z	A <sub>7</sub> -A <sub>0</sub>	Hi-Z	-	-	-	-	-	-	-	
Block Erase <sup>5</sup> (32K Byte)		52H	Hi-Z	A <sub>23</sub> -A <sub>16</sub>	Hi-Z	A <sub>15</sub> -A <sub>8</sub>	Hi-Z	A <sub>7</sub> -A <sub>0</sub>	Hi-Z	-	-	-	-	-	-	-	
Block Erase <sup>5</sup> (64K Byte)		D8H	Hi-Z	A <sub>23</sub> -A <sub>16</sub>	Hi-Z	A <sub>15</sub> -A <sub>8</sub>	Hi-Z	A <sub>7</sub> -A <sub>0</sub>	Hi-Z	-	-	-	-	-	-	-	
Chip Erase		60H / C7H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-	-	
Program / Erase Suspend		75H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-	-	
Program / Erase Resume		7AH	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-	-	
Page Program (PP)		104MHz	02H	Hi-Z	A <sub>23</sub> -A <sub>16</sub>	Hi-Z	A <sub>15</sub> -A <sub>8</sub>	Hi-Z	A <sub>7</sub> -A <sub>0</sub>	Hi-Z	D <sub>IN0</sub>	Hi-Z	D <sub>IN1</sub>	Hi-Z	Up to 256 bytes	Hi-Z	
Quad Page Program <sup>17</sup>			32H		A <sub>23</sub> -A <sub>16</sub>		A <sub>15</sub> -A <sub>8</sub>		A <sub>7</sub> -A <sub>0</sub>		D <sub>IN0-3</sub>		D <sub>IN4-7</sub>		Up to 256 byte		
Mode Bit Reset <sup>6</sup>			FFH	Hi-Z	FFH	Hi-Z	-	-	-	-	-	-	-	-	-	-	-
Deep Power Down (DP)			B9h	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-	-
Read Status Register-1 (RDSR-1) <sup>7</sup>			05H	Hi-Z	X	D <sub>OUT</sub> (S <sub>7</sub> -S <sub>0</sub> )	-	-	-	-	-	-	-	-	-	-	-
Read Status Register-2 (RDSR-2) <sup>7</sup>	35H		Hi-Z	X	D <sub>OUT</sub> (S <sub>15</sub> -S <sub>8</sub> )	-	-	-	-	-	-	-	-	-	-	-	
Write Status Register (WRSR) <sup>10</sup>	01H		Hi-Z	D <sub>IN</sub> (S <sub>7</sub> -S <sub>0</sub> )	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	
Write Enable (WREN) <sup>10</sup>	06H		Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-	-	
Write Disable (WRDI)/ Exit secured OTP mode	04H		Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-	-	
Enter secured OTP mode (ENSO)	B1H		Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-	-	
Release from Deep Power Down (RDP)	ABH		Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-	-	
Read Electronic Signature (RES) <sup>8</sup>	ABH		Hi-Z	X	X	X	X	X	X	X	16H	-	-	-	-	-	
RES in secured OTP mode & not lock down	ABH		Hi-Z	X	X	X	X	X	X	X	36H	-	-	-	-	-	
RES in secured OTP mode & lock down	ABH		Hi-Z	X	X	X	X	X	X	X	76H	-	-	-	-	-	

Table 5: Device Operation Instruction - Continued

Operation	Max. Freq	Bus Cycle <sup>1-3</sup>													
		1		2		3		4		5		6		N	
		S <sub>IN</sub>	S <sub>OUT</sub>	S <sub>IN</sub>	S <sub>OUT</sub>	S <sub>IN</sub>	S <sub>OUT</sub>	S <sub>IN</sub>	S <sub>OUT</sub>	S <sub>IN</sub>	S <sub>OUT</sub>	S <sub>IN</sub>	S <sub>OUT</sub>	S <sub>IN</sub>	S <sub>OUT</sub>
Jedec Read ID (JEDEC-ID) <sup>9</sup>	50MHz	9FH	Hi-Z	X	8CH	X	41H	X	17H	-	-	-	-	-	-
Read ID (RDID) <sup>11</sup>	104MHz	90H	Hi-Z	00H	Hi-Z	00H	Hi-Z	00H	Hi-Z	X	8CH	X	16H	-	-
								01H	Hi-Z	X	16H	X	8CH	-	-

Notes:

1. Operation: S<sub>IN</sub> = Serial In, S<sub>OUT</sub> = Serial Out, Bus Cycle 1 = Op Code
2. X = Dummy Input Cycles (V<sub>IL</sub> or V<sub>IH</sub>); - = Non-Applicable Cycles (Cycles are not necessary); cont. = continuous
3. One bus cycle is eight clock periods.
4. 4K byte Sector Erase addresses: use A<sub>MS</sub> -A<sub>12</sub>, remaining addresses can be V<sub>IL</sub> or V<sub>IH</sub>.
5. 32K byte Block Erase addresses: use A<sub>MS</sub> -A<sub>15</sub>, remaining addresses can be V<sub>IL</sub> or V<sub>IH</sub>  
64K byte Block Erase addresses: use A<sub>MS</sub> -A<sub>16</sub>, remaining addresses can be V<sub>IL</sub> or V<sub>IH</sub>
6. This instruction is recommended when using the Dual or Quad Mode bit feature.
7. The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on  $\overline{CE}$ .
8. The Read-Electronic-Signature is continuous with on going clock cycles until terminated by a low to high transition on  $\overline{CE}$ .
9. The JEDEC-Read-ID is output first byte 8CH as manufacture ID; second byte 41 as memory type; third byte 17H as memory capacity.
10. The Write-Enable (WREN) instruction and the Write-Status-Register (WRSR) instruction must work in conjunction of each other. The WRSR instruction must be executed immediately (very next bus cycle) after the WREN instruction to make both instructions effective. A successful WRSR can reset WREN.
11. The Manufacture ID and Device ID output will repeat continuously until  $\overline{CE}$  terminates the instruction.
12. Dual and Quad commands use bidirectional IO pins. D<sub>OUT</sub> and cont. are serial data out; others are serial data in.
13. Dual output data:  
 IO<sub>0</sub> = (D<sub>6</sub>, D<sub>4</sub>, D<sub>2</sub>, D<sub>0</sub>), (D<sub>6</sub>, D<sub>4</sub>, D<sub>2</sub>, D<sub>0</sub>)  
 IO<sub>1</sub> = (D<sub>7</sub>, D<sub>5</sub>, D<sub>3</sub>, D<sub>1</sub>), (D<sub>7</sub>, D<sub>5</sub>, D<sub>3</sub>, D<sub>1</sub>)  
 DOUT0                      DOUT1
14. M<sub>7</sub>-M<sub>0</sub>: Mode bits. Dual input address:  
 IO<sub>0</sub> = (A<sub>22</sub>, A<sub>20</sub>, A<sub>18</sub>, A<sub>16</sub>, A<sub>14</sub>, A<sub>12</sub>, A<sub>10</sub>, A<sub>8</sub>)      (A<sub>6</sub>, A<sub>4</sub>, A<sub>2</sub>, A<sub>0</sub>, M<sub>6</sub>, M<sub>4</sub>, M<sub>2</sub>, M<sub>0</sub>)  
 IO<sub>1</sub> = (A<sub>23</sub>, A<sub>21</sub>, A<sub>19</sub>, A<sub>17</sub>, A<sub>15</sub>, A<sub>13</sub>, A<sub>11</sub>, A<sub>9</sub>)      (A<sub>7</sub>, A<sub>5</sub>, A<sub>3</sub>, A<sub>1</sub>, M<sub>7</sub>, M<sub>5</sub>, M<sub>3</sub>, M<sub>1</sub>)  
 Bus Cycle-2                      Bus Cycle-3
15. Quad output data:  
 IO<sub>0</sub> = (D<sub>4</sub>, D<sub>0</sub>), (D<sub>4</sub>, D<sub>0</sub>), (D<sub>4</sub>, D<sub>0</sub>), (D<sub>4</sub>, D<sub>0</sub>)  
 IO<sub>1</sub> = (D<sub>5</sub>, D<sub>1</sub>), (D<sub>5</sub>, D<sub>1</sub>), (D<sub>5</sub>, D<sub>1</sub>), (D<sub>5</sub>, D<sub>1</sub>)  
 IO<sub>2</sub> = (D<sub>6</sub>, D<sub>2</sub>), (D<sub>6</sub>, D<sub>2</sub>), (D<sub>6</sub>, D<sub>2</sub>), (D<sub>6</sub>, D<sub>2</sub>)  
 IO<sub>3</sub> = (D<sub>7</sub>, D<sub>3</sub>), (D<sub>7</sub>, D<sub>3</sub>), (D<sub>7</sub>, D<sub>3</sub>), (D<sub>7</sub>, D<sub>3</sub>)  
 DOUT0    DOUT1    DOUT2    DOUT3

16. M<sub>7</sub>-M<sub>0</sub>: Mode bits. Quad input address:  
 IO<sub>0</sub> = (A<sub>20</sub>, A<sub>16</sub>, A<sub>12</sub>, A<sub>8</sub>, A<sub>4</sub>, A<sub>0</sub>, M<sub>4</sub>, M<sub>0</sub>)  
 IO<sub>1</sub> = (A<sub>21</sub>, A<sub>17</sub>, A<sub>13</sub>, A<sub>9</sub>, A<sub>5</sub>, A<sub>1</sub>, M<sub>5</sub>, M<sub>1</sub>)  
 IO<sub>2</sub> = (A<sub>22</sub>, A<sub>18</sub>, A<sub>14</sub>, A<sub>10</sub>, A<sub>6</sub>, A<sub>2</sub>, M<sub>6</sub>, M<sub>2</sub>)  
 IO<sub>3</sub> = (A<sub>23</sub>, A<sub>19</sub>, A<sub>15</sub>, A<sub>11</sub>, A<sub>7</sub>, A<sub>3</sub>, M<sub>7</sub>, M<sub>3</sub>)

└──────────────────────────────────┘  
 Bus Cycle-2

Fast Read Quad I/O data:  
 IO<sub>0</sub> = (X, X), (X, X), (D<sub>4</sub>, D<sub>0</sub>), (D<sub>4</sub>, D<sub>0</sub>) (D<sub>4</sub>, D<sub>0</sub>), (D<sub>4</sub>, D<sub>0</sub>), (D<sub>4</sub>, D<sub>0</sub>), (D<sub>4</sub>, D<sub>0</sub>)  
 IO<sub>1</sub> = (X, X), (X, X), (D<sub>5</sub>, D<sub>1</sub>), (D<sub>5</sub>, D<sub>1</sub>) (D<sub>5</sub>, D<sub>1</sub>), (D<sub>5</sub>, D<sub>1</sub>), (D<sub>5</sub>, D<sub>1</sub>), (D<sub>5</sub>, D<sub>1</sub>)  
 IO<sub>2</sub> = (X, X), (X, X), (D<sub>6</sub>, D<sub>2</sub>), (D<sub>6</sub>, D<sub>2</sub>) (D<sub>6</sub>, D<sub>2</sub>), (D<sub>6</sub>, D<sub>2</sub>), (D<sub>6</sub>, D<sub>2</sub>), (D<sub>6</sub>, D<sub>2</sub>)  
 IO<sub>3</sub> = (X, X), (X, X), (D<sub>7</sub>, D<sub>3</sub>), (D<sub>7</sub>, D<sub>3</sub>) (D<sub>7</sub>, D<sub>3</sub>), (D<sub>7</sub>, D<sub>3</sub>), (D<sub>7</sub>, D<sub>3</sub>), (D<sub>7</sub>, D<sub>3</sub>)

└───┘ └───┘ └───┘ └───┘ └───┘ └───┘  
 DOUT0 DOUT1 DOUT2 DOUT3 DOUT4 DOUT5

└──────────────────┘ └──────────────────┘  
 Bus Cycle-3 Bus Cycle-4

17. The instruction is initiated by executing command code, followed by address bits into SI (SIO<sub>0</sub>) before D<sub>IN</sub>, and then input data to bidirectional IO pins (SIO<sub>0</sub> ~ SIO<sub>3</sub>).  
 Quad input data:  
 IO<sub>0</sub> = (D<sub>4</sub>, D<sub>0</sub>), (D<sub>4</sub>, D<sub>0</sub>), (D<sub>4</sub>, D<sub>0</sub>), (D<sub>4</sub>, D<sub>0</sub>)  
 IO<sub>1</sub> = (D<sub>5</sub>, D<sub>1</sub>), (D<sub>5</sub>, D<sub>1</sub>), (D<sub>5</sub>, D<sub>1</sub>), (D<sub>5</sub>, D<sub>1</sub>)  
 IO<sub>2</sub> = (D<sub>6</sub>, D<sub>2</sub>), (D<sub>6</sub>, D<sub>2</sub>), (D<sub>6</sub>, D<sub>2</sub>), (D<sub>6</sub>, D<sub>2</sub>)  
 IO<sub>3</sub> = (D<sub>7</sub>, D<sub>3</sub>), (D<sub>7</sub>, D<sub>3</sub>), (D<sub>7</sub>, D<sub>3</sub>), (D<sub>7</sub>, D<sub>3</sub>)

└───┘ └───┘ └───┘ └───┘  
 DIN0 DIN1 DIN2 DIN3

**Read (50MHz)**

The Read instruction supports up to 50 MHz, it outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low to high transition on  $\overline{CE}$ . The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space, i.e. for 64Mbit density, once

the data from address location 7FFFFFFH had been read, the next output will be from address location 000000H.

The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits [A<sub>23</sub>-A<sub>0</sub>].  $\overline{CE}$  must remain active low for the duration of the Read cycle. See Figure 2 for the Read sequence.

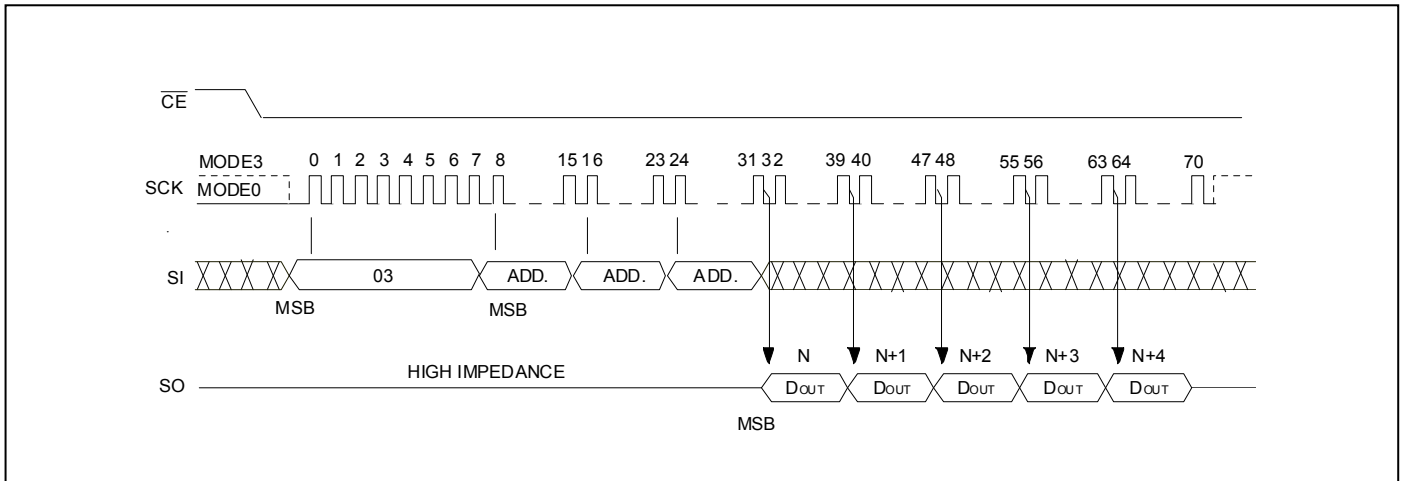


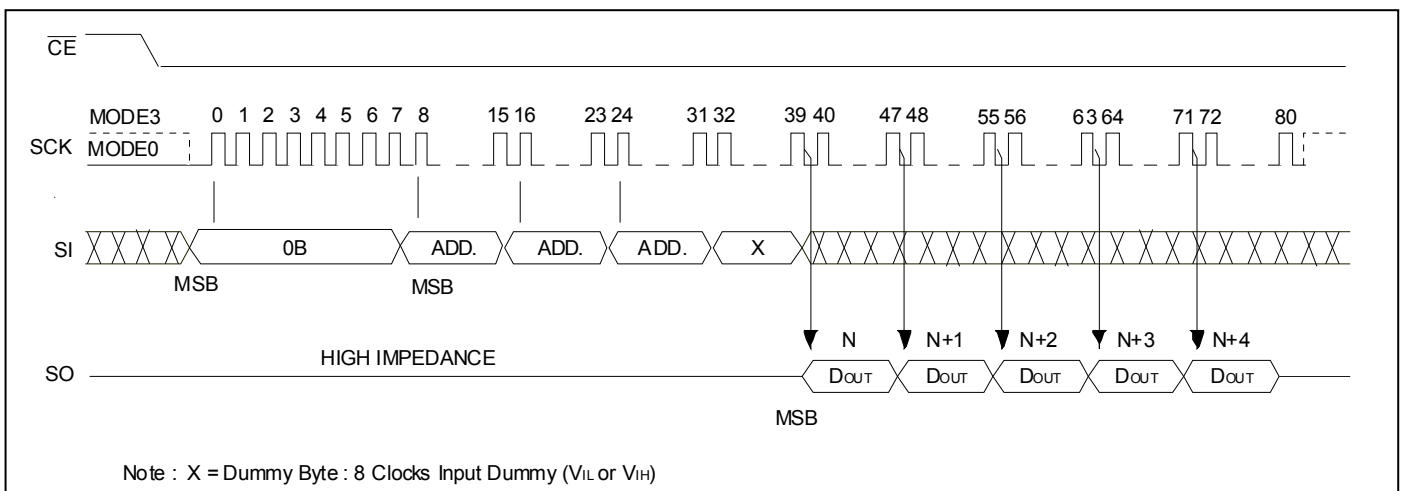
Figure 2: Read Sequence

**Fast Read (50 MHz ~ 104 MHz)**

The Fast Read instruction supporting up to 104 MHz is initiated by executing an 8-bit command, 0BH, followed by address bits [A<sub>23</sub>-A<sub>0</sub>] and a dummy byte.  $\overline{CE}$  must remain active low for the duration of the Fast Read cycle. See Figure 3 for the Fast Read sequence.

all addresses until terminated by a low to high transition on  $\overline{CE}$ . The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space, i.e. for 64Mbit density, once the data from address location 7FFFFFFH has been read, the next output will be from address location 000000H.

Following a dummy byte (8 clocks input dummy cycle), the Fast Read instruction outputs the data starting from the specified address location. The data output stream is continuous through



Note : X = Dummy Byte : 8 Clocks Input Dummy (V<sub>IL</sub> or V<sub>IH</sub>)

Figure 3: Fast Read Sequence

**Fast Read Dual Output (50 MHz ~ 104 MHz)**

The Fast Read Dual Output (3BH) instruction is similar to the standard Fast Read (0BH) instruction except the data is output on bidirectional I/O pins (SIO<sub>0</sub> and SIO<sub>1</sub>). This allows data to be transferred from the device at twice the rate of standard SPI devices. This instruction is for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

The Fast Read Dual Output instruction is initiated by executing an 8-bit command, 3BH, followed by address bits [A<sub>23</sub>-A<sub>0</sub>] and a dummy byte.  $\overline{CE}$  must remain active low for the duration of the Fast Read Dual Output cycle. See Figure 4 for the Fast Read Dual Output sequence.

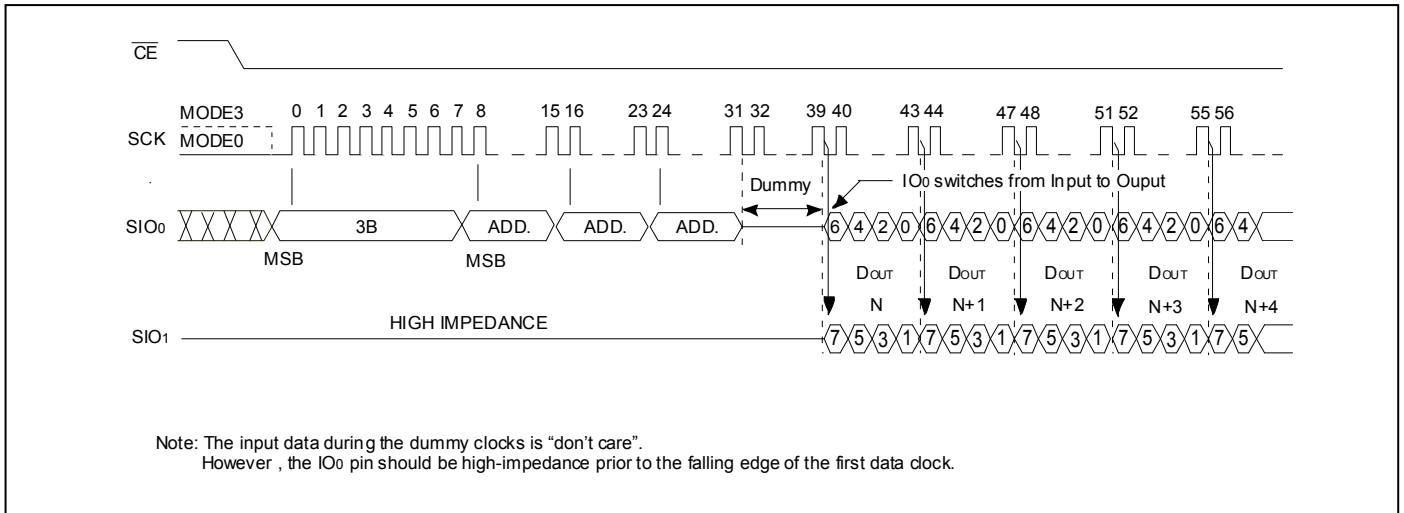


Figure 4: Fast Read Dual Output Sequence

**Fast Read Dual I/O (50 MHz ~ 104 MHz)**

The Fast Read Dual I/O (BBH) instruction is similar to the Fast Read Dual Output (3BH) instruction, but with the capability to input address bits [A<sub>23</sub>-A<sub>0</sub>] two bits per clock.

To set mode bits [M<sub>7</sub>-M<sub>0</sub>] after the address bits [A<sub>23</sub>-A<sub>0</sub>] can further reduce instruction overhead (See Figure 5). The upper mode bits [M<sub>7</sub>-M<sub>4</sub>] controls the length of next Fast Read Dual I/O instruction with/without the first byte command code (BBH). The lower mode bits [M<sub>3</sub>-M<sub>0</sub>] are “don’t care”.

If [M<sub>7</sub>-M<sub>0</sub>] = “AxH”, the next Fast Read Dual I/O instruction (after  $\overline{CE}$  is raised and the lowered) doesn’t need the command code (See Figure 6). This way let the instruction sequence reduce 8 clocks and allows to enter address immediately after  $\overline{CE}$  is asserted low. If [M<sub>7</sub>-M<sub>0</sub>] are the value other than “AxH”, the next instruction need the first byte command code, thus returning to normal operation. A Mode Bit Reset (FFH) also can be used to reset mode bits [M<sub>7</sub>-M<sub>0</sub>] before issuing normal instructions.

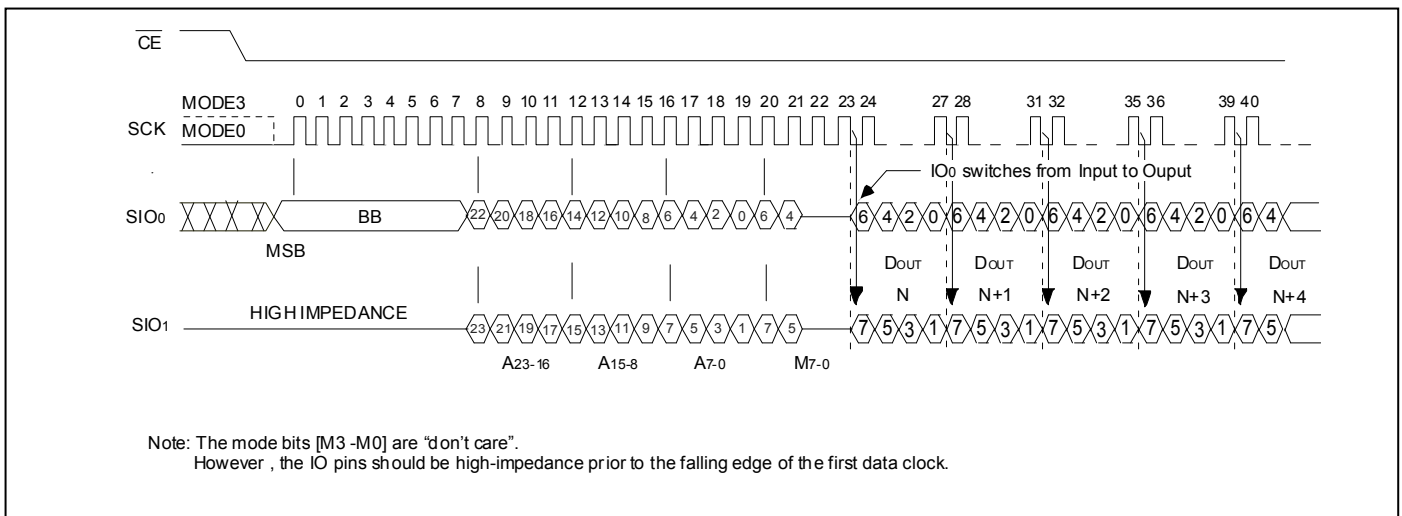


Figure 5: Fast Read Dual I/O Sequence ([M<sub>7</sub>-M<sub>0</sub>] = 0xH or NOT AxH)

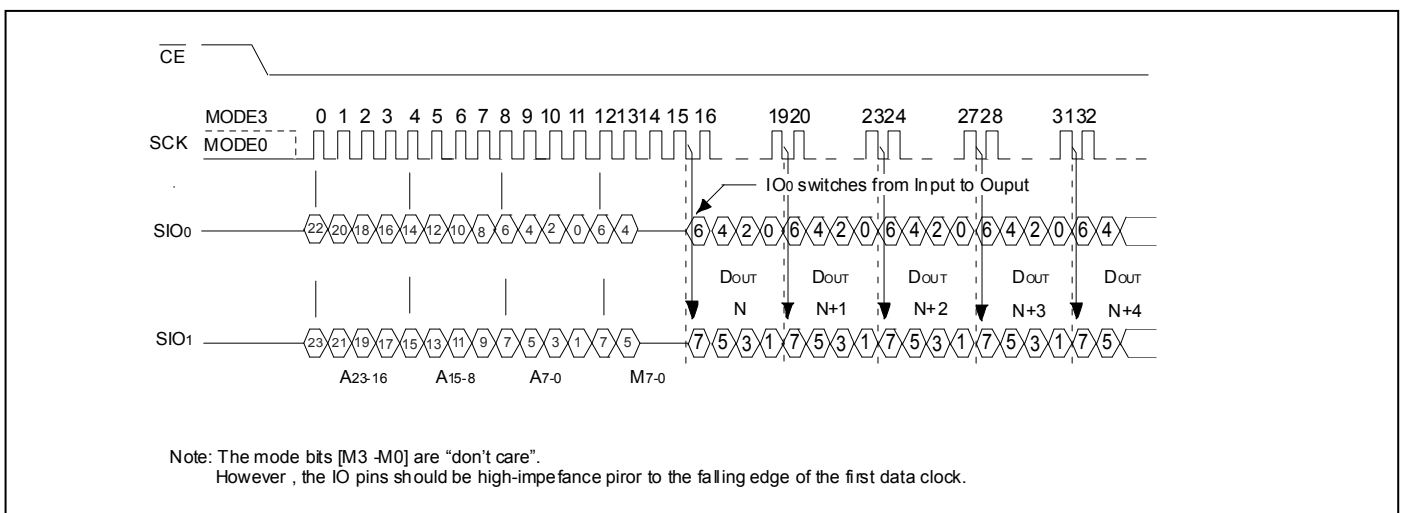


Figure 6: Fast Read Dual I/O Sequence ([M<sub>7</sub>-M<sub>0</sub>] = AxH)

**Fast Read Quad Output (50 MHz ~ 104 MHz)**

The Fast Read Quad Output (6B) instruction is similar to the Fast Read Dual Output (3BH) instruction except the data is output on bidirectional I/O pins (SIO<sub>0</sub>, SIO<sub>1</sub>, SIO<sub>2</sub> and SIO<sub>3</sub>). A Quad Enable (QE) bit of Status Register-1 must be set "1" to enable Quad function. This allows data to be transferred from the device at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction is initiated by executing an 8-bit command, 6BH, followed by address bits [A<sub>23</sub>-A<sub>0</sub>] and a dummy byte.  $\overline{CE}$  must remain active low for the duration of the Fast Read Dual Output cycle. See Figure 7 for the Fast Read Quad Output sequence.

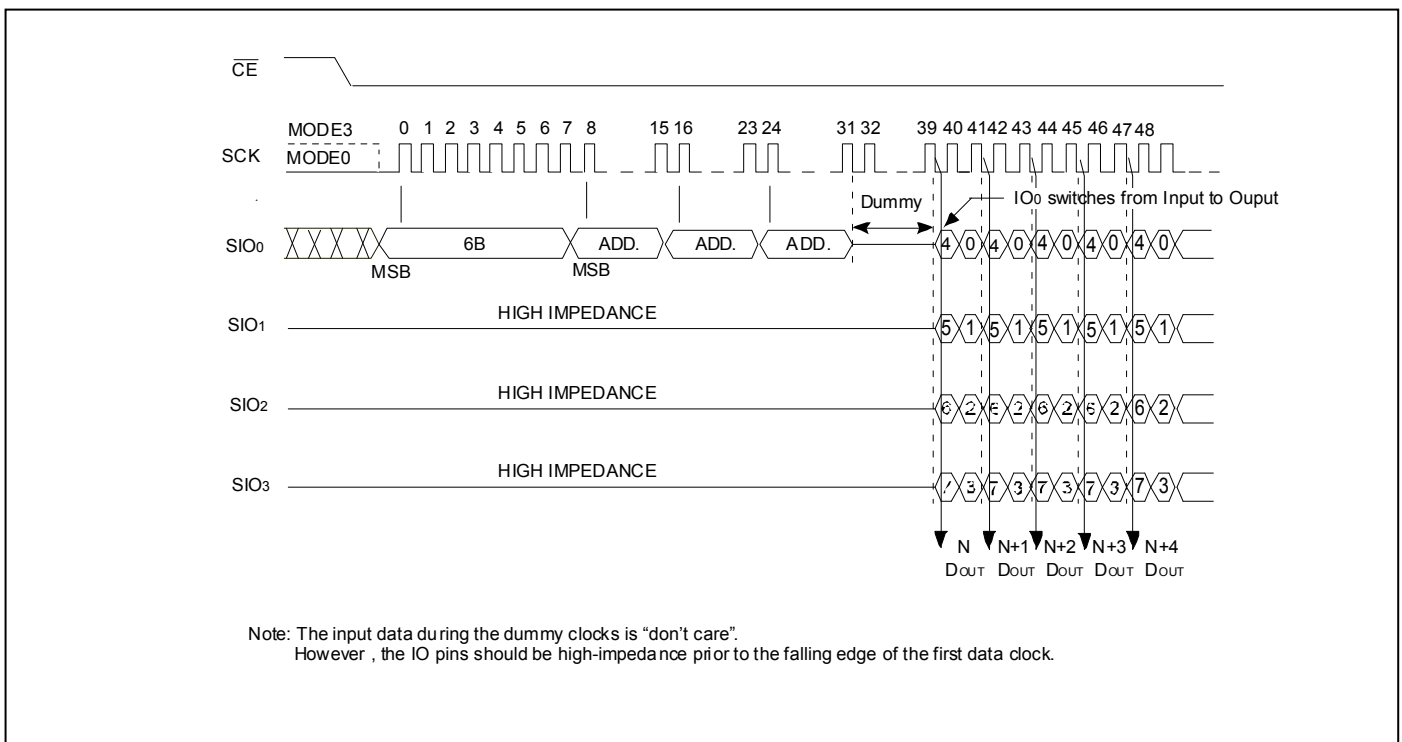


Figure 7: Fast Read Quad Output Sequence

**Fast Read Quad I/O (50 MHz ~ 104 MHz)**

The Fast Read Quad I/O (EBH) instruction is similar to the Fast Read Quad Output (6BH) instruction, but with the capability to input address bits [A<sub>23</sub>-A<sub>0</sub>] four bits per clock. A Quad Enable (QE) bit of Status Register-1 must be set "1" to enable Quad function.

To set mode bits [M<sub>7</sub>-M<sub>0</sub>] after the address bits [A<sub>23</sub>-A<sub>0</sub>] can further reduce instruction overhead (See Figure 8). The upper mode bits [M<sub>7</sub>-M<sub>4</sub>] controls the length of next Fast Read Quad I/O instruction with/without the first byte command code (EBH). The lower mode bits [M<sub>3</sub>-M<sub>0</sub>] are "don't care".

If [M<sub>7</sub>-M<sub>0</sub>] = "AxH", the next Fast Read Quad I/O instruction (after  $\overline{CE}$  is raised and the lowered) doesn't need the command code (See Figure 9). This way let the instruction sequence reduce 8 clocks and allows to enter address immediately after  $\overline{CE}$  is asserted low. If [M<sub>7</sub>-M<sub>0</sub>] are the value other than "AxH", the next instruction need the first byte command code, thus returning to normal operation. A Mode Bit Reset (FFH) also can be used to reset mode bits [M<sub>7</sub>-M<sub>0</sub>] before issuing normal instructions.

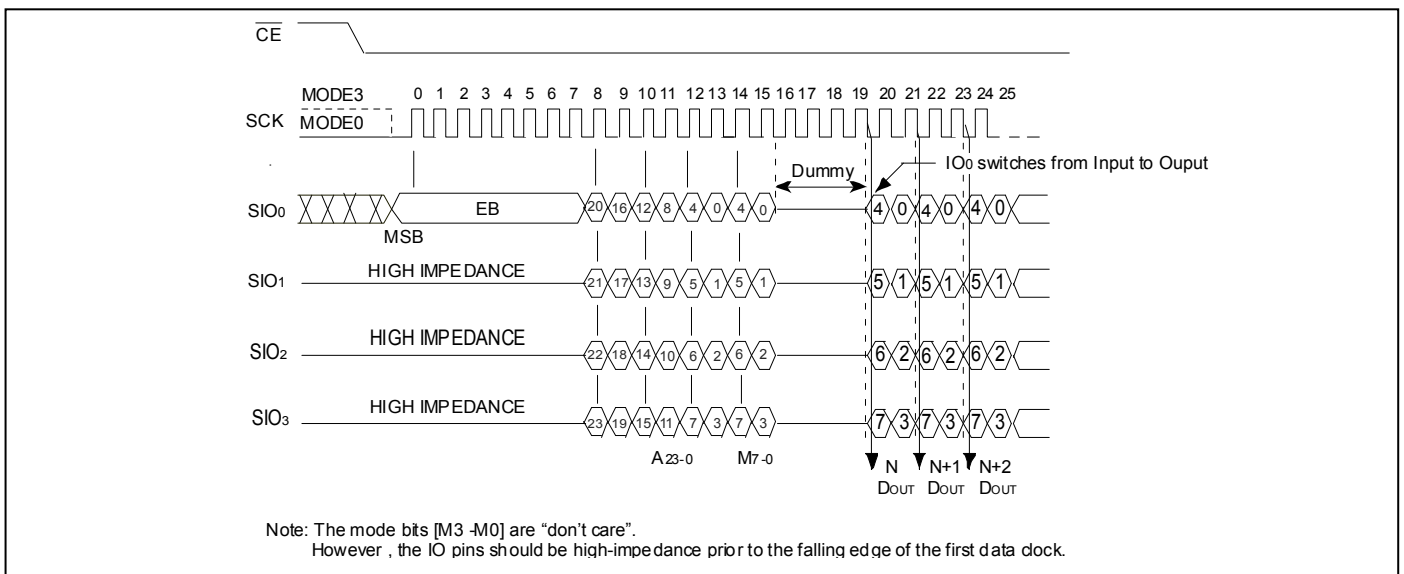


Figure 8: Fast Read Quad I/O Sequence ([M<sub>7</sub>-M<sub>0</sub>] = 0xH or NOT AxH)

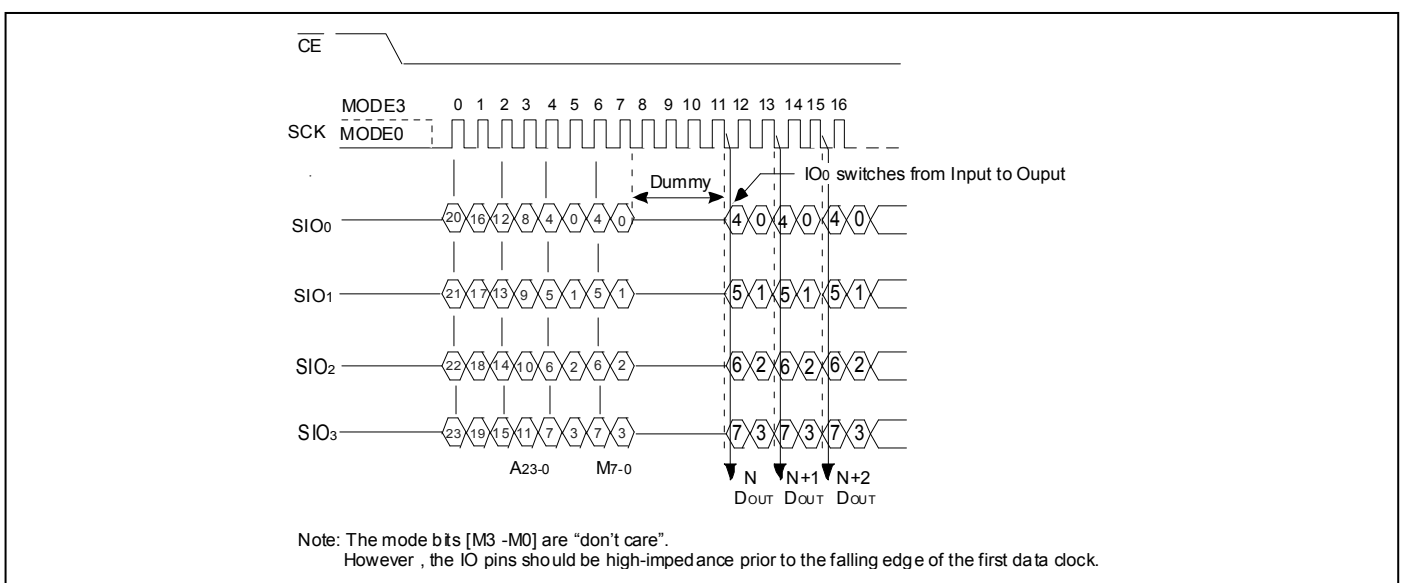


Figure 9: Fast Read Quad I/O Sequence ([M<sub>7</sub>-M<sub>0</sub>] = AxH)



**Page Program (PP)**

The Page Program instruction allows many bytes to be programmed in the memory. The bytes must be in the erased state (FFH) when initiating a Program operation. A Page Program instruction applied to a protected memory area will be ignored.

Prior to any Write operation, the Write Enable (WREN) instruction must be executed.  $\overline{CE}$  must remain active low for the duration of the Page Program instruction. The Page Program instruction is initiated by executing an 8-bit command, 02H, followed by address bits [A<sub>23</sub>-A<sub>0</sub>]. Following the address, at least one byte Data is input (the maximum of input data can be up to 256 bytes). If the 8 least significant address bits [A<sub>7</sub>-A<sub>0</sub>] are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits [A<sub>7</sub>-A<sub>0</sub>] are all zero).

If more than 256 bytes Data are sent to the device, previously

latched data are discarded and the last 256 bytes Data are guaranteed to be programmed correctly within the same page. If less than 256 bytes Data are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

$\overline{CE}$  must be driven high before the instruction is executed. The user may poll the BUSY bit in the software status register or wait T<sub>PP</sub> for the completion of the internal self-timed Page Program operation. While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished, the Write-Enable-Latch (WEL) bit in the Status Register-1 is cleared to 0. See Figure 10 for the Page Program sequence.

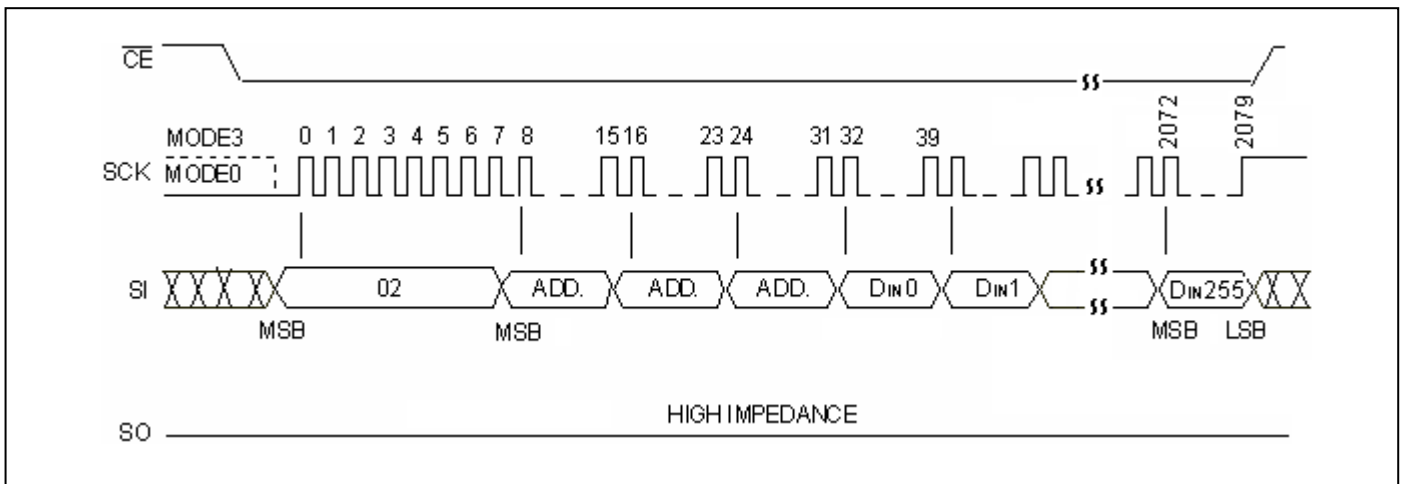


Figure 10: Page Program Sequence

**Quad Page Program**

The Quad Page Program instruction allows many bytes to be programmed in the memory by using four I/O pins (SIO0, SIO1, SIO2 and SIO3). The instruction can improve programmer performance and the effectiveness of application that have slow clock speed <20MHz. For system with faster clock, this instruction can't provide more actual favors, because the required internal page program time is far more than the time data flows in. Therefore, we suggest that user can execute this command while

the clock speed <20MHz.

Prior to Quad Page Program operation, the Write Enable (WREN) instruction must be executed and Quad Enable (QE) bit of Status Register-1 must be set "1". The other function descriptions are as same as standard Page Program. See Figure 11 for the Quad Page Program sequence.

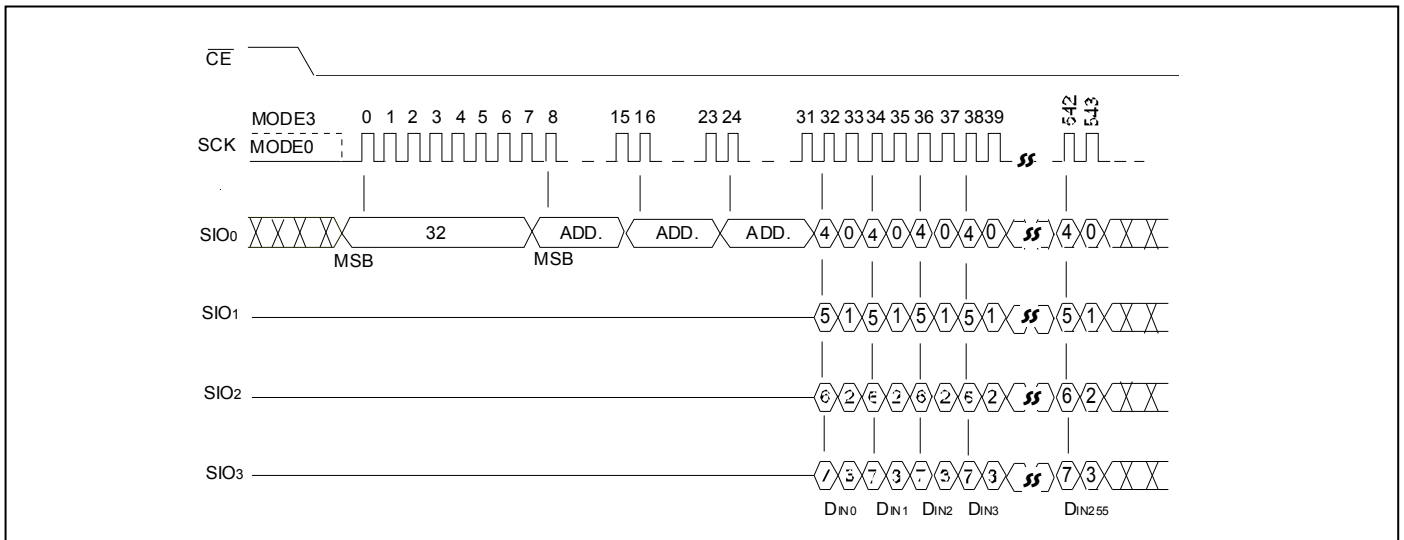


Figure 11: Quad Page Program Sequence

**Mode Bit Reset**

Mode bits [M<sub>7</sub>–M<sub>0</sub>] are issued to further reduce instruction overhead for Fast Read Dual/Quad I/O operation. If [M<sub>7</sub>–M<sub>0</sub>] = “AxH”, the next Fast Read Dual/Quad I/O instruction doesn’t need the command code.

If the system controller is reset during operation, it will send a standard instruction (such as Read ID) to the Flash memory.

However, the device doesn’t have a hardware reset pin, so if [M<sub>7</sub>–M<sub>0</sub>] = “AxH”, the device will not recognize any standard SPI instruction. After a system reset, it is recommended to issue a Mode Bit Reset instruction first to release the status of [M<sub>7</sub>–M<sub>0</sub>] = “AxH” and allow the device to recognize standard SPI instruction. See Figure 12 for the Mode Bit Reset instruction.

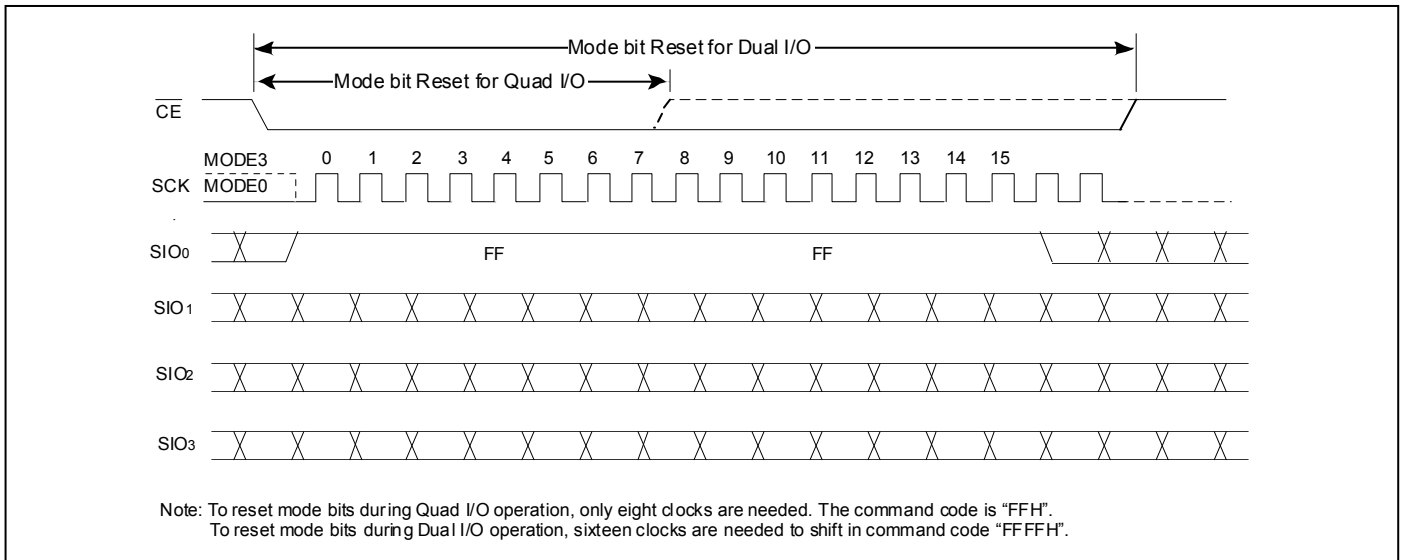


Figure 12: Mode Bit Reset Instruction

**64K Byte Block Erase**

The 64K-byte Block Erase instruction clears all bits in the selected block to FFH. A Block Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write Enable (WREN) instruction must be executed.  $\overline{CE}$  must remain active low for the duration of the any command sequence. The Block Erase instruction is initiated by executing an 8-bit command, D8H, followed by address bits [A<sub>23</sub>

-A<sub>0</sub>]. Address bits [A<sub>MS</sub>-A<sub>16</sub>] (A<sub>MS</sub> = Most Significant address) are used to determine the block address (BA<sub>x</sub>), remaining address bits can be V<sub>IL</sub> or V<sub>IH</sub>.  $\overline{CE}$  must be driven high before the instruction is executed. The user may poll the BUSY bit in the Software Status Register or wait T<sub>BE</sub> for the completion of the internal self-timed Block Erase cycle. See Figure 13 for 64K Byte Block Erase sequence.

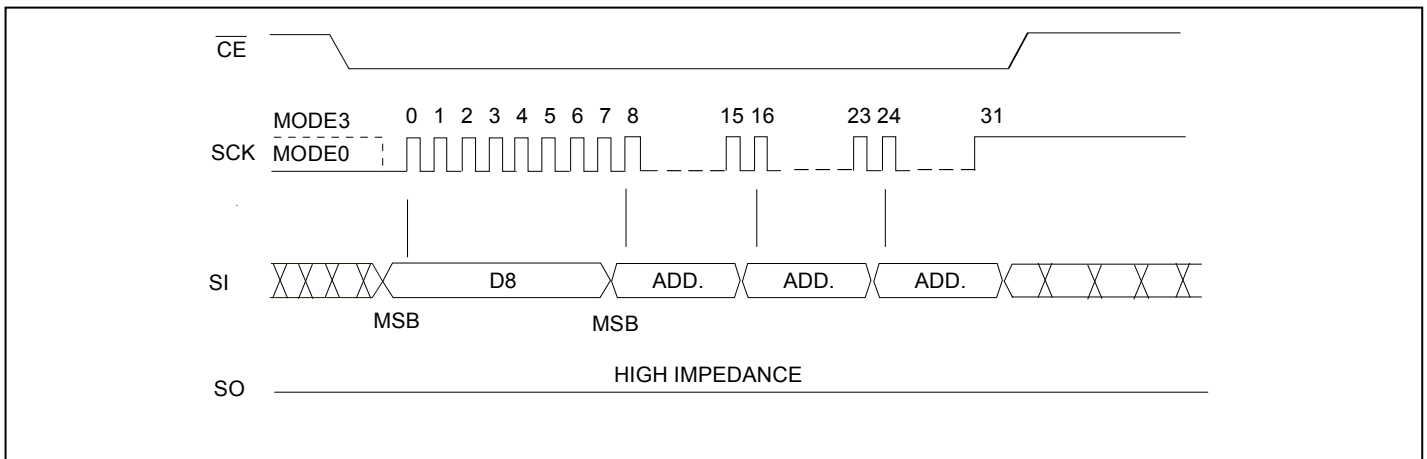


Figure 13: 64K-byte Block Erase Sequence

**32K Byte Block Erase**

The 32K-byte Block Erase instruction clears all bits in the selected block to FFH. A Block Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write Enable (WREN) instruction must be executed.  $\overline{CE}$  must remain active low for the duration of the any command sequence. The Block Erase instruction is initiated by executing an 8-bit command, 52H, followed by address bits [A<sub>23</sub>

-A<sub>0</sub>]. Address bits [A<sub>MS</sub>-A<sub>15</sub>] (A<sub>MS</sub> = Most Significant address) are used to determine the block address (BA<sub>x</sub>), remaining address bits can be V<sub>IL</sub> or V<sub>IH</sub>.  $\overline{CE}$  must be driven high before the instruction is executed. The user may poll the BUSY bit in the Software Status Register or wait T<sub>BE</sub> for the completion of the internal self-timed Block Erase cycle. See Figure 14 for 32K Byte Block Erase sequence.

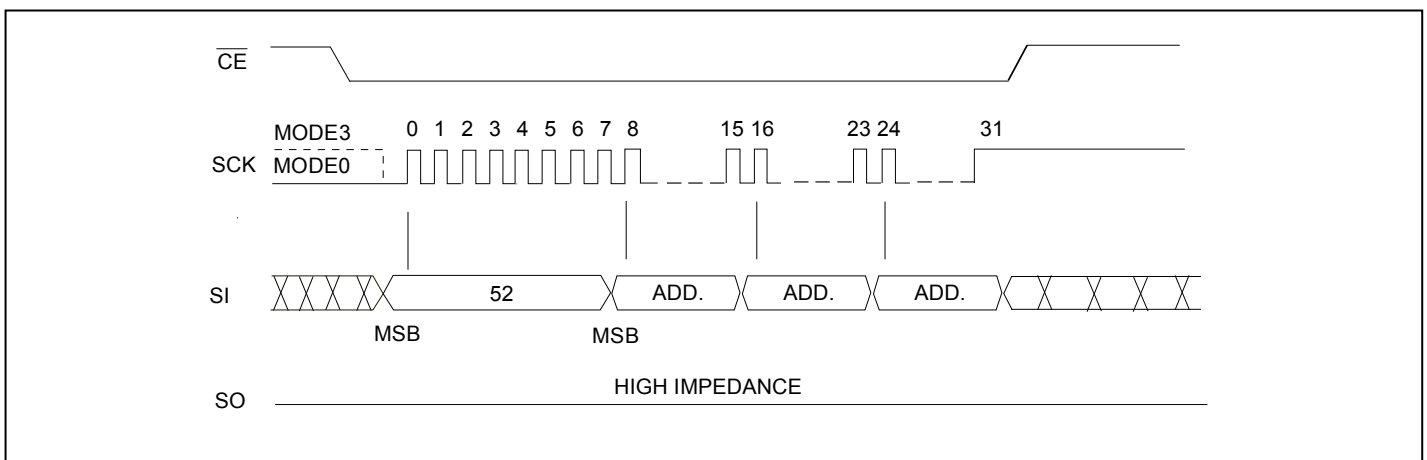


Figure 14: 32K-byte Block Erase Sequence

**4K Byte Sector Erase**

The Sector Erase instruction clears all bits in the selected sector to FFH. A Sector Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write Enable (WREN) instruction must be executed.  $\overline{CE}$  must remain active low for the duration of the any command sequence. The Sector Erase instruction is initiated by executing an 8-bit command, 20H, followed by address bits  $[A_{23}-A_0]$ . Address bits

$[A_{MS}-A_{12}]$  ( $A_{MS}$  = Most Significant address) are used to determine the sector address ( $SA_x$ ), remaining address bits can be  $V_{IL}$  or  $V_{IH}$ .  $\overline{CE}$  must be driven high before the instruction is executed. The user may poll the BUSY bit in the Software Status Register or wait  $T_{SE}$  for the completion of the internal self-timed Sector Erase cycle. See Figure 15 for the Sector Erase sequence.

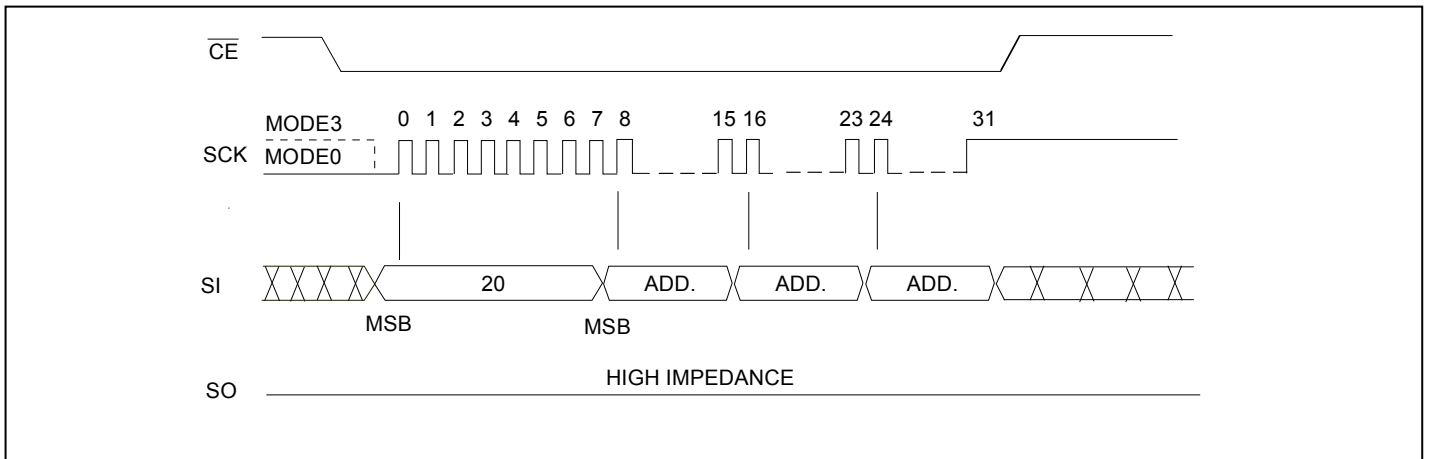


Figure 15: 4K-byte Sector Erase Sequence

**Chip Erase**

The Chip Erase instruction clears all bits in the device to FFH. A Chip Erase instruction will be ignored if any of the memory area is protected. Prior to any Write operation, the Write Enable (WREN) instruction must be executed.  $\overline{CE}$  must remain active low for the duration of the Chip Erase instruction sequence. The Chip

Erase instruction is initiated by executing an 8-bit command, 60H or C7H.  $\overline{CE}$  must be driven high before the instruction is executed. The user may poll the BUSY bit in the Software Status Register or wait  $T_{CE}$  for the completion of the internal self-timed Chip Erase cycle. See Figure 16 for the Chip Erase sequence.

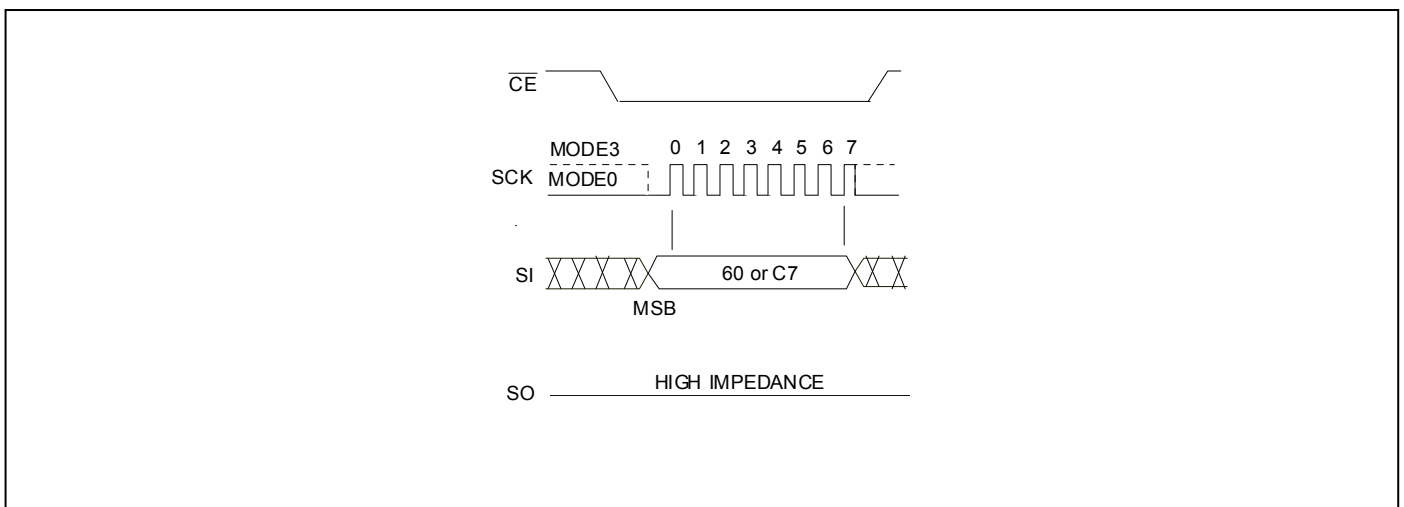


Figure 16: Chip Erase Sequence

**Program / Erase Suspend**

The Program/Erase Suspend instruction allows the system to interrupt a Sector or Block Erase and Page or Quad Page Program operation and then read from, any other sector or block.

The Write Status Register instruction and Program instruction and Sector/Block Erase instructions are not allowed during suspend. Program/Erase Suspend is valid only during the

Program and Sector or Block Erase operation. If written during the Chip Erase, the Program/Erase Suspend instruction is ignored. A maximum of  $T_{SUS}$  is required to suspend the program / erase operation. The BUSY bit in the Software Status Register will clear to "0" after Erase Suspend. A power-off during the suspend period will reset the device and release the suspend status.

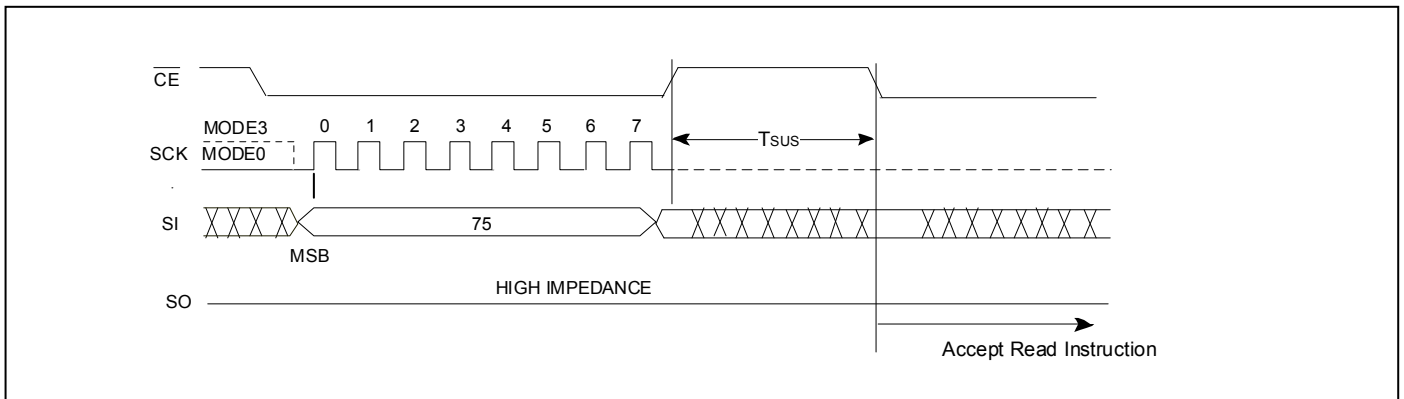


Figure 17: Program/Erase Suspend Instruction

**Program / Erase Resume**

The Program/Erase Resume instruction must be written to resume the Page or Quad Page program and Sector or Block Erase operation after Program/Erase Suspend. After issued the BUSY bit in the Software Status Register will be set to "1" and the

sector or block will complete the program/erase operation. Program/Erase Resume instruction will be ignored unless an Program/Erase Suspend operation is active.

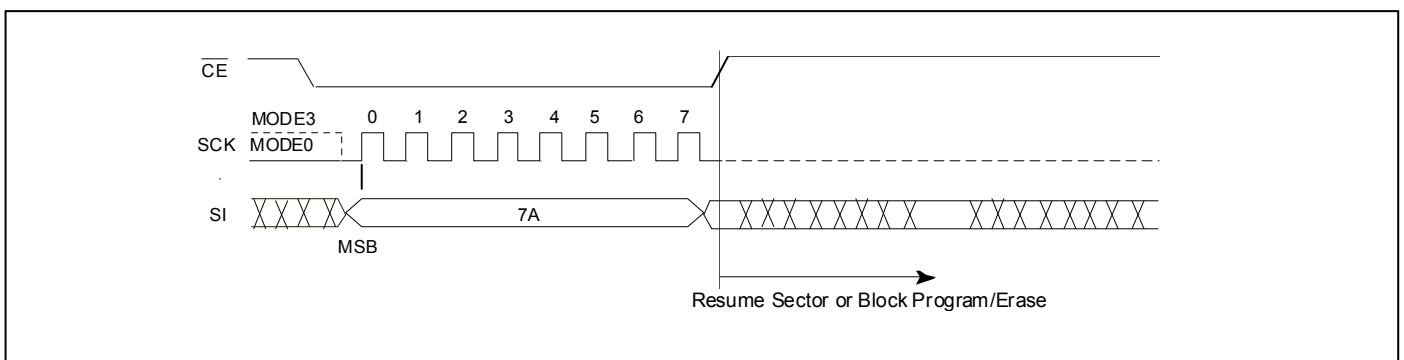


Figure 18: Program/Erase Resume Instruction

**Write Enable (WREN)**

The Write Enable (WREN) instruction sets the Write-Enable-Latch bit in the Software Status Register to 1 allowing Write operations to occur. The WREN instruction must be executed prior to any Write

(Program/Erase) operation.  $\overline{CE}$  must be driven high before the WREN instruction is executed.

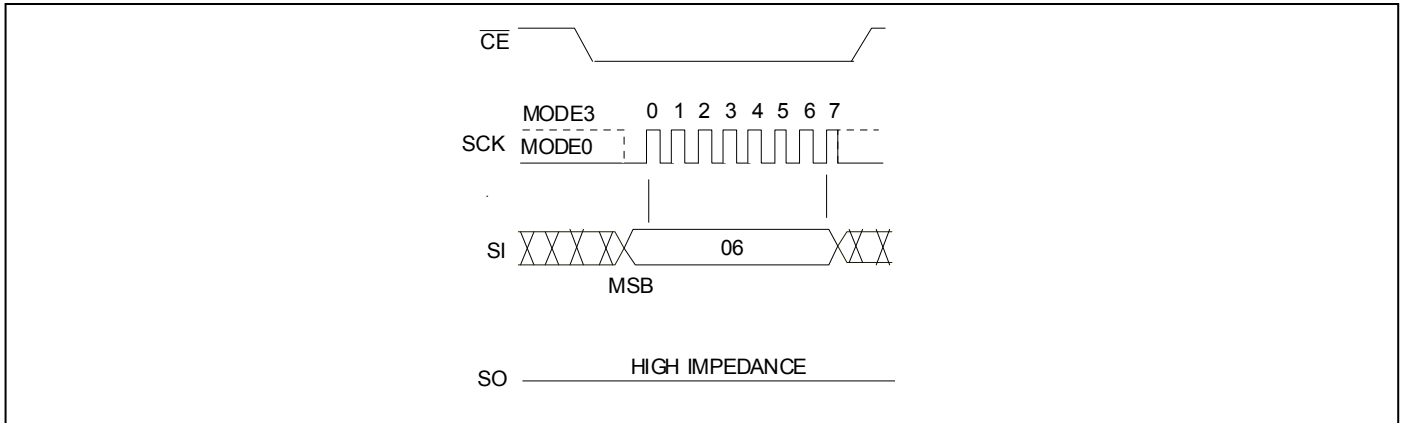


Figure 19: Write Enable (WREN) Sequence

**Write Disable (WRDI)**

The Write Disable (WRDI) instruction resets the Write-Enable-Latch bit to 0 disabling any new Write operations from occurring or exits from OTP mode to normal mode.

$\overline{CE}$  must be driven high before the WRDI instruction is executed.

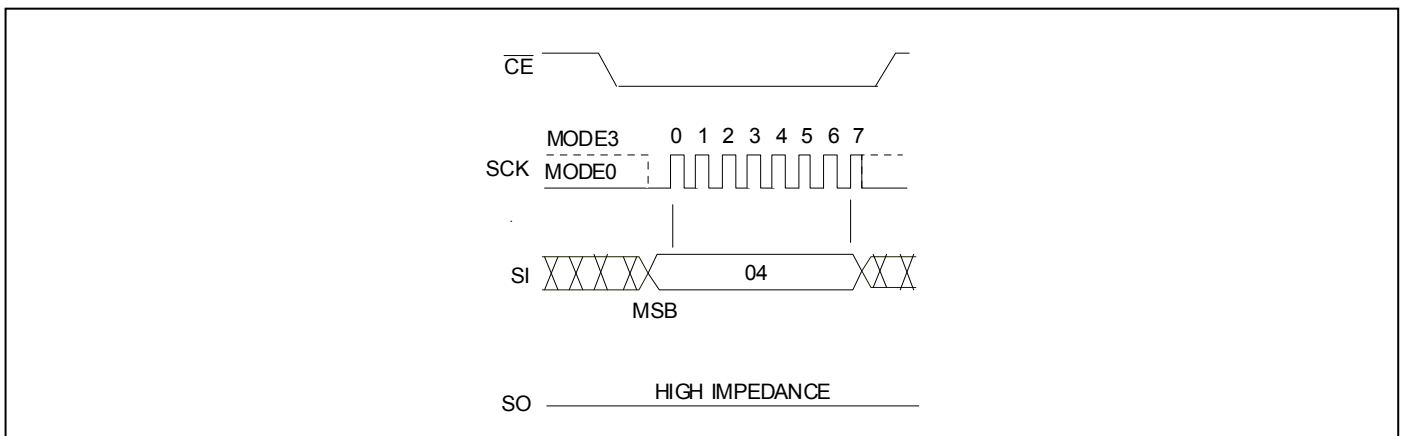


Figure 20: Write Disable (WRDI) Sequence

**Write Status Register (WRSR)**

The Write Status Register instruction writes new values to the BP3, BP2, BP1, BP0, QE and BPL (Status Register-1) and bits of the status register.  $\overline{CE}$  must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed.  $\overline{CE}$  must be driven high after the eighth bit of data that is clocked in. If it is not done, the WRSR instruction will not be issued. See Figure 21 for WREN and WRSR instruction sequences.

Executing the Write Status Register instruction will be ignored when  $\overline{WP}$  is low and BPL bit is set to "1". When the  $\overline{WP}$  is low, the BPL bit can only be set from "0" to "1" to lock down the status register, but cannot be reset from "1" to "0".

When  $\overline{WP}$  is high, the lock-down function of the BPL bit is

disabled and the BPL, BP0, BP1, BP2 and BP3 bits in the status register can all be changed. As long as BPL bit is set to 0 or  $\overline{WP}$  pin is driven high ( $V_{IH}$ ) prior to the low-to-high transition of the  $\overline{CE}$  pin at the end of the WRSR instruction, the bits in the status register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to "1" to lock down the status register as well as altering the BP0; BP1, BP2 and BP3 bits at the same time. See Table 4 for a summary description of  $\overline{WP}$  and BPL functions.

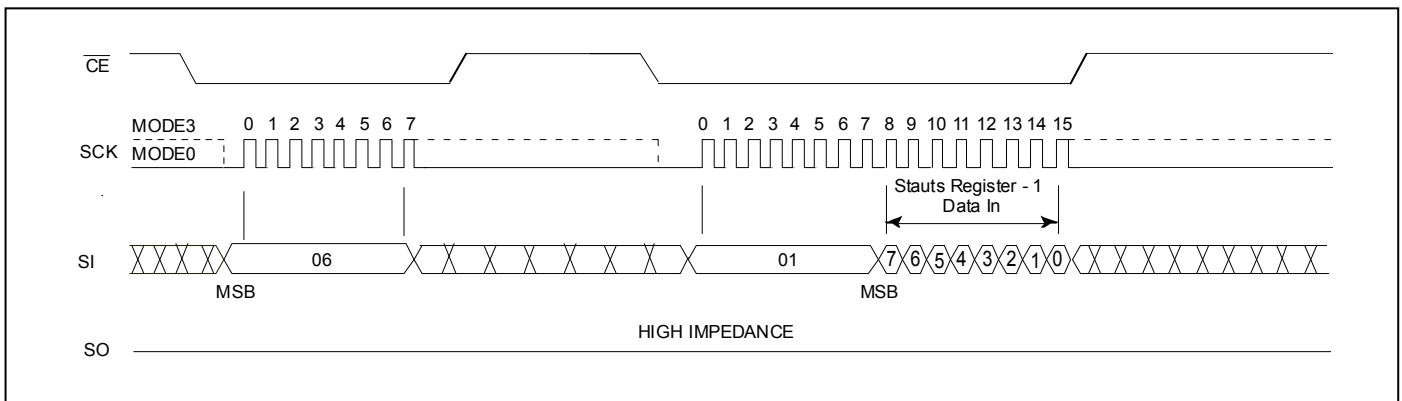


Figure 21: Write Enable (WREN) and Write Status Register (WRSR)

**Read Status Register (RDSR)**

The Read Status Register (RDSR) instruction allows reading of the status register. The status register may be read at any time even during a Write (Program/Erase) operation. When a Write operation is in progress, the BUSY bit may be checked before sending any new commands to assure that the new commands are properly received by the device.

$\overline{CE}$  must be driven low before the RDSR instruction is entered

and remain low until the status data is read. The RDSR-1 instruction code is "05H" for Status Register-1. The RDSR-2 instruction code is "35H" for Status Register-2. Read Status Register is continuous with ongoing clock cycles until it is terminated by a low to high transition of the  $\overline{CE}$ . See Figure 22 for the RDSR instruction sequence.

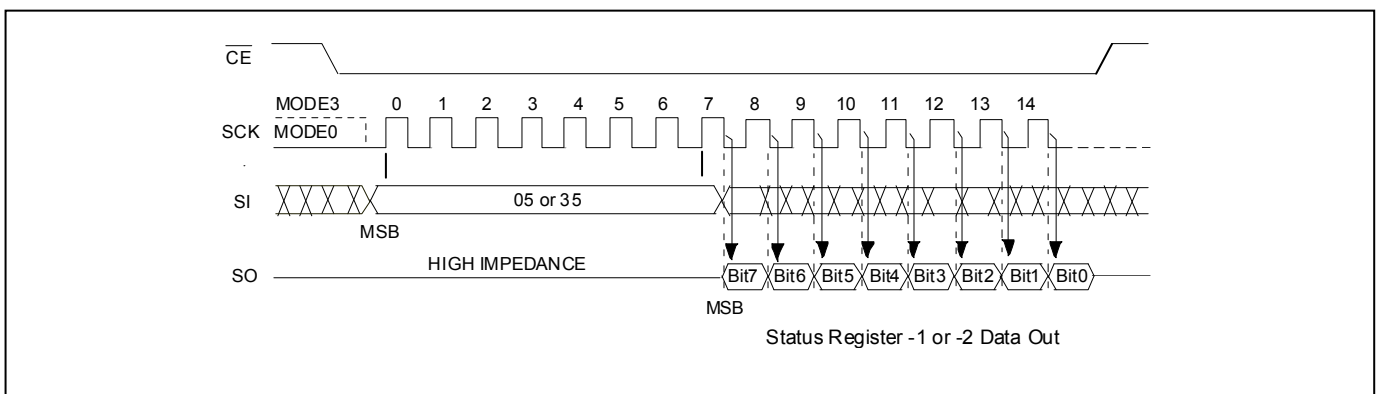


Figure 22: Read Status Register (RDSR-1 or RDSR-2) Sequence



**Enter OTP Mode (ENSO)**

The ENSO (B1H) instruction is for entering the additional 512 bytes secured OTP mode. The additional 512 bytes secured OTP sector is independent from main array, which may use to store unique serial number for system identifier. User must unprotect whole array (BP0=BP1=BP2=BP3=0), prior to any Program operation in OTP sector. After entering the secured OTP mode, only the secured OTP sector can be accessed and user can only follow the Read or Program procedure with OTP address range

(address bits [A<sub>23</sub> –A<sub>9</sub>] must be “0”). The secured OTP data cannot be updated again once it is lock down or has been programmed. In secured OTP mode, WRSR command will ignore the input data and lock down the secured OTP sector (OTP\_lock bit =1). To exit secured OTP mode, user must execute WRDI command. RES can be used to verify the secured OTP status as shown in Table 6.

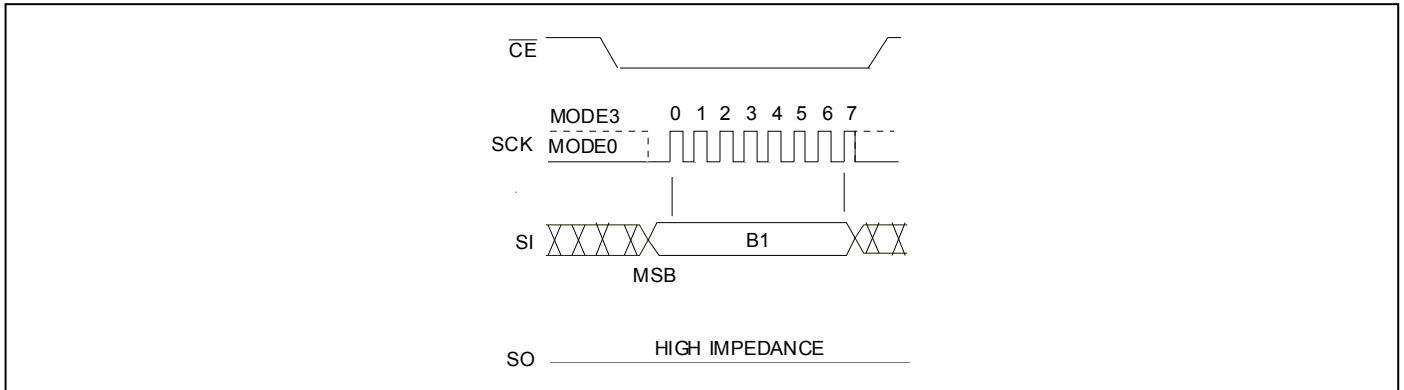


Figure 23: Enter OTP Mode (ENSO) Sequence

**OTP Sector Address**

Size	Address Range
512 bytes	000000H ~ 0001FFH

Note: The OTP sector is an independent Sector.

**Deep Power Down (DP)**

The Deep Power Down instruction is for minimizing power consumption (the standby current is reduced from  $I_{SB1}$  to  $I_{SB2}$ ).

This instruction is initiated by executing an 8-bit command, B9H, and then  $\overline{CE}$  must be driven high. After  $\overline{CE}$  is driven high, the device will enter to deep power down within the duration of  $T_{DP}$ .

Once the device is in deep power down status, all instructions will be ignored except the Release from Deep Power Down instruction (RDP) and Read Electronic Signature instruction (RES). The device always power-up in the normal operation with the standby current ( $I_{SB1}$ ). See Figure 24 for the Deep Power Down instruction.

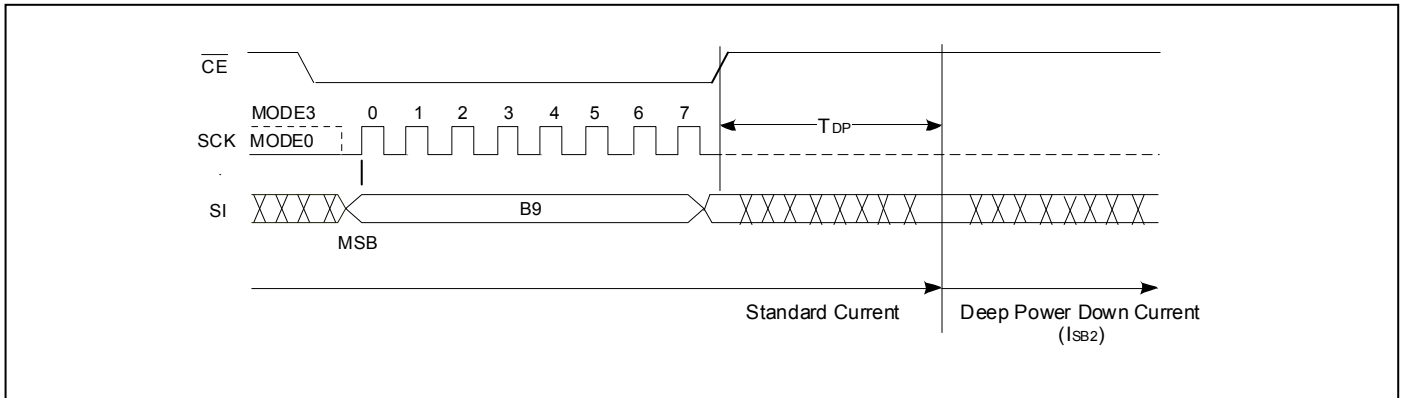


Figure 24: Deep Power Down Instruction

**Release from Deep Power Down (RDP) and Read Electronic-Signature (RES)**

The Release from Deep Power Down and Read Electronic-Signature instruction is a multi-purpose instruction.

The instruction can be used to release the device from the deep power down status. This instruction is initiated by driving  $\overline{CE}$  low and executing an 8-bit command, ABH, and then drive  $\overline{CE}$  high. See Figure 25 for RDP instruction. Release from the deep power down will take the duration of  $T_{RES1}$  before the device will resume normal operation and other instructions are accepted.  $\overline{CE}$  must remain high during  $T_{RES1}$ .

The instruction also can be used to read the 8-bit Electronic-Signature of the device on the SO pin. It is initiated by driving

$\overline{CE}$  low and executing an 8-bit command, ABH, followed by 3 dummy bytes. The Electronic-Signature byte is then output from the device. The Electronic-Signature can be read continuously until  $\overline{CE}$  go high. See Figure 26 for RES sequence. After driving  $\overline{CE}$  high, it must remain high during for the duration of  $T_{RES2}$ , and then the device will resume normal operation and other instructions are accepted.

The instruction is executed while an Erase, Program or WRSR cycle is in progress is ignored and has no effect on the cycle in progress. In OTP mode, user also can execute RES to confirm the status of OTP.

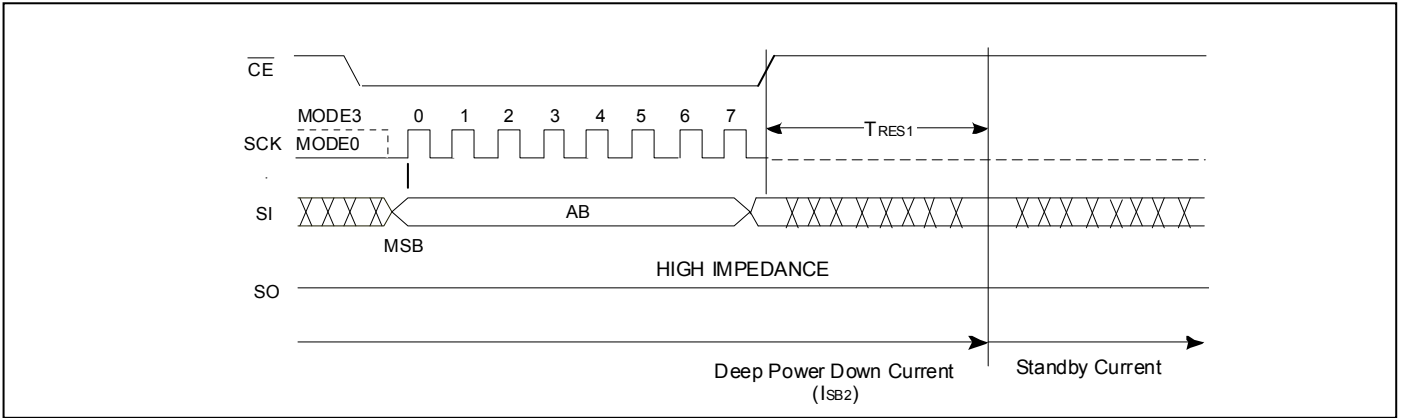


Figure 25: Release from Deep Power Down (RDP) Instruction

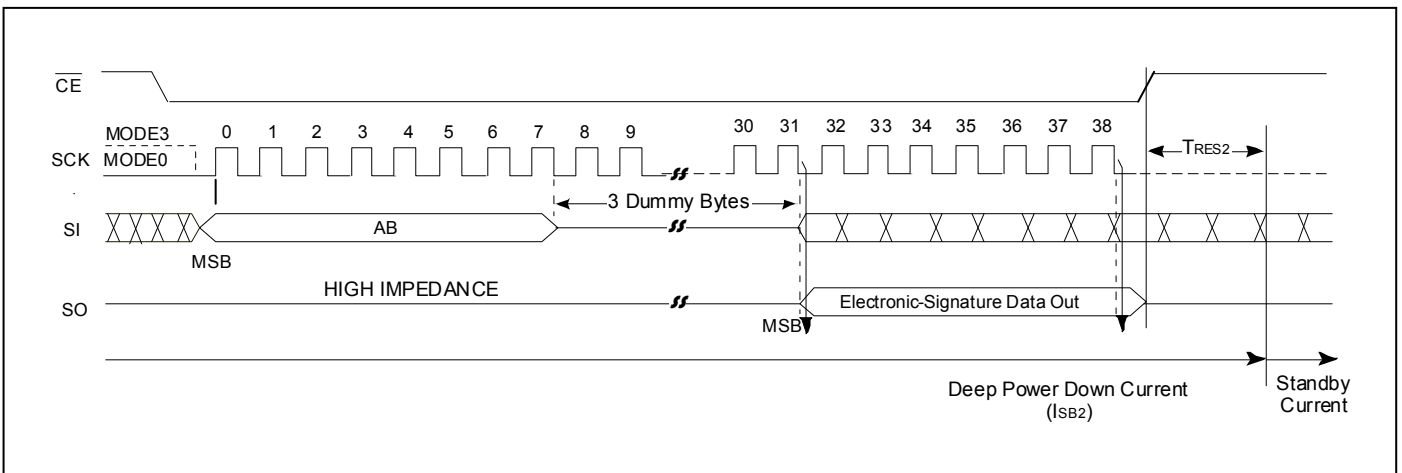


Figure 26: Read Electronic -Signature (RES) Sequence

Table 6: Electronic Signature Data

Command	Mode	Electronic Signature Data
RES	Normal	16H
	In secured OTP mode & non lock down (OTP_lock =0)	36H
	In secured OTP mode & lock down (OTP_lock =1)	76H

**JEDEC Read-ID**

The JEDEC Read-ID instruction identifies the device as F25L64QA and the manufacturer as ESMT. The device information can be read from executing the 8-bit command, 9FH. Following the JEDEC Read-ID instruction, the 8-bit manufacturer's ID, 8CH, is output from the device. After that, a 16-bit device ID is shifted out on the SO pin. Byte1, 8CH, identifies the manufacturer as ESMT. Byte2, 41H, identifies the memory type as SPI Flash. Byte3, 17H, identifies the device as

F25L64QA. The instruction sequence is shown in Figure 27. The JEDEC Read ID instruction is terminated by a low to high transition on  $\overline{CE}$  at any time during data output. If no other command is issued after executing the JEDEC Read-ID instruction, issue a 00H (NOP) command before going into Standby Mode ( $\overline{CE} = V_{IH}$ ).

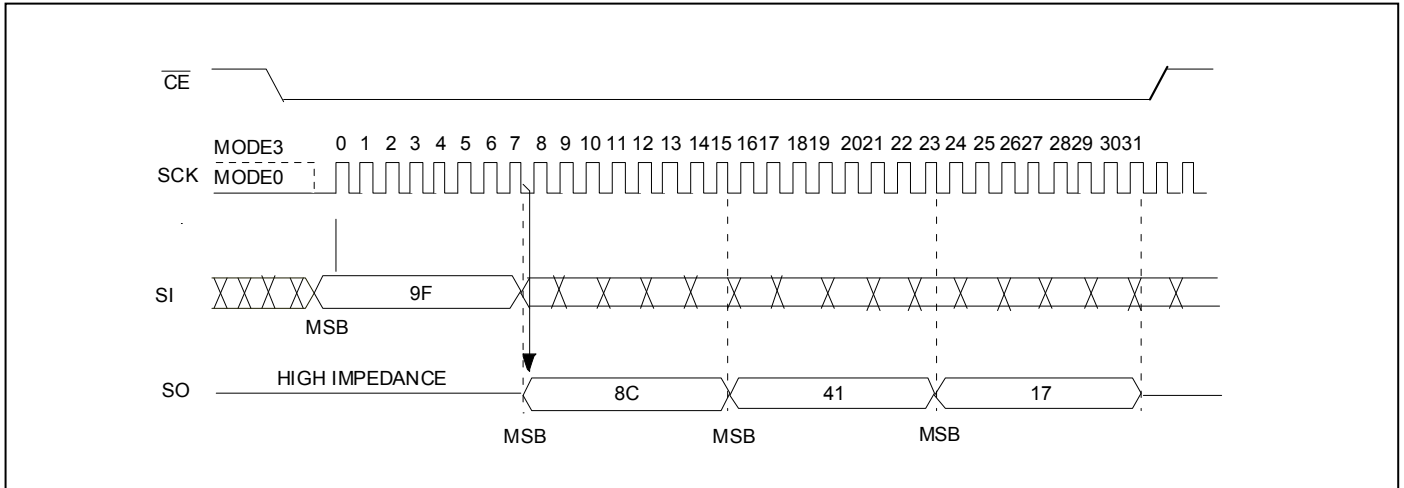


Figure 27: JEDEC Read-ID Sequence

**Table 7: JEDEC Read-ID Data**

Manufacturer's ID (Byte 1)	Device ID	
	Memory Type (Byte 2)	Memory Capacity (Byte 3)
8CH	41H	17H

**Read-ID (RDID)**

The Read-ID instruction (RDID) identifies the devices as F25L64QA and manufacturer as ESMT. This command is backward compatible to all ESMT SPI devices and should be used as default device identification when multiple versions of ESMT SPI devices are used in one design. The device information can be read from executing an 8-bit command, 90H, followed by address bits [A<sub>23</sub> -A<sub>0</sub>]. Following the Read-ID

instruction, the manufacturer's ID is located in address 000000H and the device ID is located in address 000001H. Once the device is in Read-ID mode, the manufacturer's and device ID output data toggles between address 000000H and 000001H until terminated by a low to high transition on  $\overline{CE}$ .

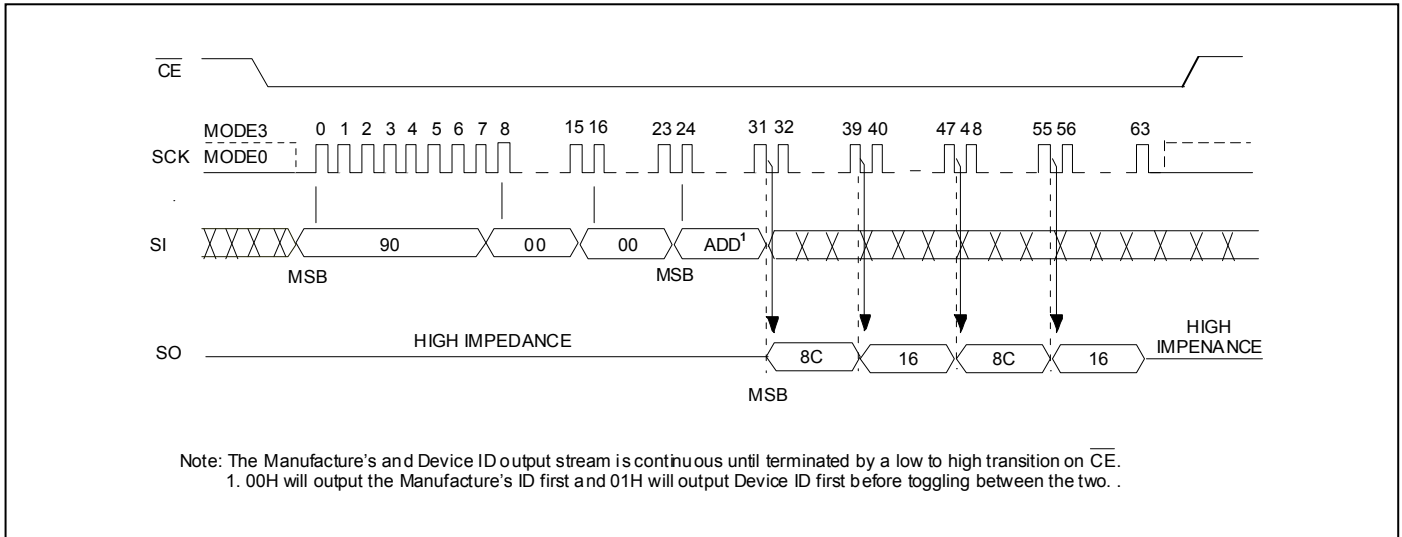


Figure 28: Read ID Sequence

**Table 8: Product ID Data**

Address	Byte1	Byte2
000000H	8CH	16H
	Manufacturer's ID	Device ID ESMT F25L64QA
000001H	16H	8CH
	Device ID ESMT F25L64QA	Manufacturer's ID

■ ELECTRICAL SPECIFICATIONS

**Absolute Maximum Stress Ratings**

(Applied conditions are greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this datasheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Storage Temperature . . . . .	-65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . .	-0.5V to VDD+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . .	-2.0V to VDD+2.0V
Package Power Dissipation Capability (T <sub>A</sub> = 25°C) . . . . .	1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . .	260°C
Output Short Circuit Current (Note 1). . . . .	50 mA

( Note 1: Output shorted for no more than one second. No more than one output shorted at a time. )

**TABLE 9: AC CONDITIONS OF TEST**

Input Rise/Fall Time . . . . .	5 ns
Output Load . . . . .	C <sub>L</sub> = 15 pF for ≥ 75MHz
. . . . .	C <sub>L</sub> = 30 pF for ≤ 50MHz
See Figures 34 and 35	

**TABLE 10: OPERATING RANGE**

Parameter	Symbol	Value	Unit
Operating Supply Voltage	V <sub>DD</sub>	2.65 ~ 3.6	V
Ambient Operating Temperature	T <sub>A</sub>	-40 ~ +85	°C

**TABLE 11: DC OPERATING CHARACTERISTICS**

Symbol	Parameter	Limits			Test Condition
		Min	Max	Unit	
I <sub>DDR1</sub>	Read Current @ 50MHz	Standard	10	mA	$\overline{CE} = 0.1 V_{DD}/0.9 V_{DD}$ , SO=open
		Dual	12		
		Quad	13.5		
I <sub>DDR2</sub>	Read Current @ 86MHz	Standard	15	mA	$\overline{CE} = 0.1 V_{DD}/0.9 V_{DD}$ , SO=open
		Dual	16.5		
		Quad	18		
I <sub>DDR3</sub>	Read Current @ 104MHz	Standard	22	mA	$\overline{CE} = 0.1 V_{DD}/0.9 V_{DD}$ , SO=open
		Dual	23.5		
		Quad	25		
I <sub>DDW</sub>	Program and Write Status Register Current		15	mA	$\overline{CE} = V_{DD}$
I <sub>DDE</sub>	Sector and Block Erase Current		15	mA	$\overline{CE} = V_{DD}$
	Chip Erase Current		20	mA	$\overline{CE} = V_{DD}$
I <sub>SB1</sub>	Standby Current		25	µA	$\overline{CE} = V_{DD}$ , V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>
I <sub>SB2</sub>	Deep Power Down Current		10	µA	$\overline{CE} = V_{DD}$ , V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>
I <sub>LI</sub>	Input Leakage Current		1	µA	V <sub>IN</sub> =GND to V <sub>DD</sub> , V <sub>DD</sub> =V <sub>DD</sub> Max
I <sub>LO</sub>	Output Leakage Current		1	µA	V <sub>OUT</sub> =GND to V <sub>DD</sub> , V <sub>DD</sub> =V <sub>DD</sub> Max
V <sub>IL</sub>	Input Low Voltage	-0.5	0.3 x V <sub>DD</sub>	V	
V <sub>IH</sub>	Input High Voltage	0.7 x V <sub>DD</sub>	V <sub>DD</sub> +0.4	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> =1.6 mA
V <sub>OH</sub>	Output High Voltage	V <sub>DD</sub> -0.2		V	I <sub>OH</sub> =-100 µA

**TABLE 12: LATCH UP CHARACTERISTIC**

Symbol	Parameter	Minimum	Unit	Test Method
$I_{LTH}^1$	Latch Up	$100 + I_{DD}$	mA	JEDEC Standard 78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 13: CAPACITANCE (TA = 25°C, f=1 MHz, other pins open)**

Parameter	Description	Test Condition	Maximum
$C_{OUT}^1$	Output Pin Capacitance	$V_{OUT} = 0V$	8 pF
$C_{IN}^1$	Input Capacitance	$V_{IN} = 0V$	6 pF

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 14: AC OPERATING CHARACTERISTICS<sup>5</sup>**

Symbol	Parameter	50 MHz		86 MHz		104 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$F_{CLK}$	Serial Clock Frequency		50		86		104	MHz
$T_{SCKH}^2$	Serial Clock High Time	9		6		4		ns
$T_{SCKL}^2$	Serial Clock Low Time	9		6		4		ns
$T_{CLCH}^3$	Clock Rise Time (Slew Rate)	0.1		0.1		0.1		V/ns
$T_{CHCL}^3$	Clock Fall Time (Slew Rate)	0.1		0.1		0.1		V/ns
$T_{CES}^1$	$\overline{CE}$ Active Setup Time	5		5		5		ns
$T_{CEH}^1$	$\overline{CE}$ Active Hold Time	5		5		5		ns
$T_{CHS}^1$	$\overline{CE}$ Not Active Setup Time	5		5		5		ns
$T_{CHH}^1$	$\overline{CE}$ Not Active Hold Time	5		5		5		ns
$T_{CPH}$	$\overline{CE}$ High Time	10		10		10		ns
$T_{CHZ}^3$	$\overline{CE}$ High to High-Z Output		7		7		7	ns
$T_{CLZ}$	SCK Low to Low-Z Output	0		0		0		ns
$T_{DS}$	Data In Setup Time	2		2		2		ns
$T_{DH}$	Data In Hold Time	1		1		1		ns
$T_{HLS}$	$\overline{HOLD}$ Low Setup Time	5		5		5		ns
$T_{HHS}$	$\overline{HOLD}$ High Setup Time	5		5		5		ns
$T_{HLH}$	$\overline{HOLD}$ Low Hold Time	5		5		5		ns
$T_{HHH}$	$\overline{HOLD}$ High Hold Time	5		5		5		ns
$T_{HZ}^3$	$\overline{HOLD}$ Low to High-Z Output		8		8		8	ns
$T_{LZ}^3$	$\overline{HOLD}$ High to Low-Z Output		8		8		8	ns

TABLE 14: AC OPERATING CHARACTERISTICS - Continued

Symbol	Parameter	50 MHz		86 MHz		104 MHz		Unit
		Min	Max	Min	Max	Min	Max	
T <sub>OH</sub>	Output Hold from SCK Change	0		0		0		ns
T <sub>V</sub>	Output Valid from SCK		8		8		8	ns
T <sub>WHSL</sub> <sup>4</sup>	Write Protect Setup Time before $\overline{CE}$ Low	20		20		20		ns
T <sub>SHWL</sub> <sup>4</sup>	Write Protect Hold Time after $\overline{CE}$ High	100		100		100		ns
T <sub>DP</sub> <sup>3</sup>	$\overline{CE}$ High to Deep Power Down Mode		3		3		3	us
T <sub>RES1</sub> <sup>3</sup>	$\overline{CE}$ High to Standby Mode ( for DP)		3		3		3	us
T <sub>RES2</sub> <sup>3</sup>	$\overline{CE}$ High to Standby Mode (for RES)		1.8		1.8		1.8	us
T <sub>SUS</sub> <sup>3</sup>	$\overline{CE}$ High to next Instruction after Suspend		20		20		20	us

Note:

1. Relative to SCK.
2. T<sub>SCKH</sub> + T<sub>SCKL</sub> must be less than or equal to 1/ F<sub>CLK</sub>.
3. Value guaranteed by design and/or characterization, not 100% tested in production.
4. Only applicable as a constraint for a Write status Register instruction when Block- Protection-Look (BPL) bit is set at 1.
5. Tested on sample basis and specified through design and characterization data. T<sub>A</sub> = 25°C, V<sub>DD</sub> = 3V, 100% driver strength.

■ TABLE 15: ERASE AND PROGRAMMING PERFORMANCE<sup>3</sup>

Parameter	Symbol	Limit		Unit
		Typ <sup>2</sup>	Max	
Sector Erase Time (4KB)	T <sub>SE</sub>	120	400	ms
Block Erase Time (32KB)	T <sub>BE1</sub>	500	1000	ms
Block Erase Time (64KB)	T <sub>BE2</sub>	1	2	s
Chip Erase Time	T <sub>CE</sub>	35	80	s
Write Status Register Time	T <sub>W</sub>	10	40	ms
Page Programming Time	T <sub>PP</sub>	1.5	5	ms
Erase/Program Cycles <sup>1</sup>		100,000	-	Cycles

Parameter	Symbol	Limit		Unit
		Typ	Max	
Data Retention		20	-	Years

Notes:

1. Not 100% Tested, Excludes external system level over head.
2. Typical program and erase time assumes the following conditions: 25°C, 3V, and all zero pattern.
3. The maximum chip programming time is evaluated under the worst conditions of 0C, V<sub>DD</sub>=3V, and 100K cycle with 90% confidence level.



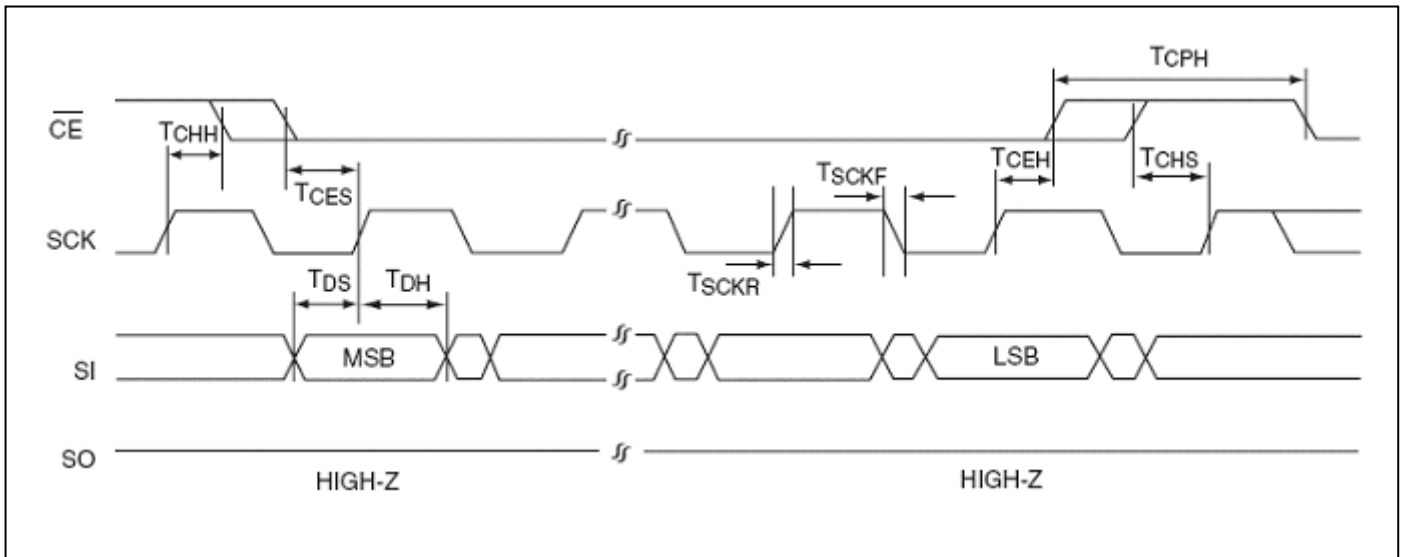


Figure 29: Serial Input Timing Diagram

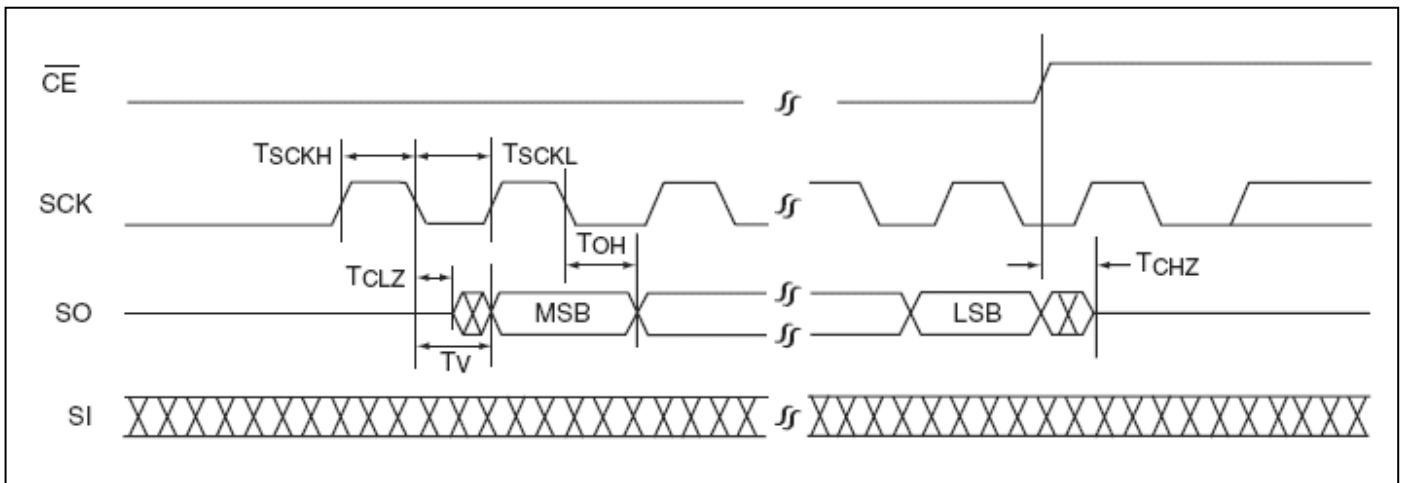


Figure 30: Serial Output Timing Diagram

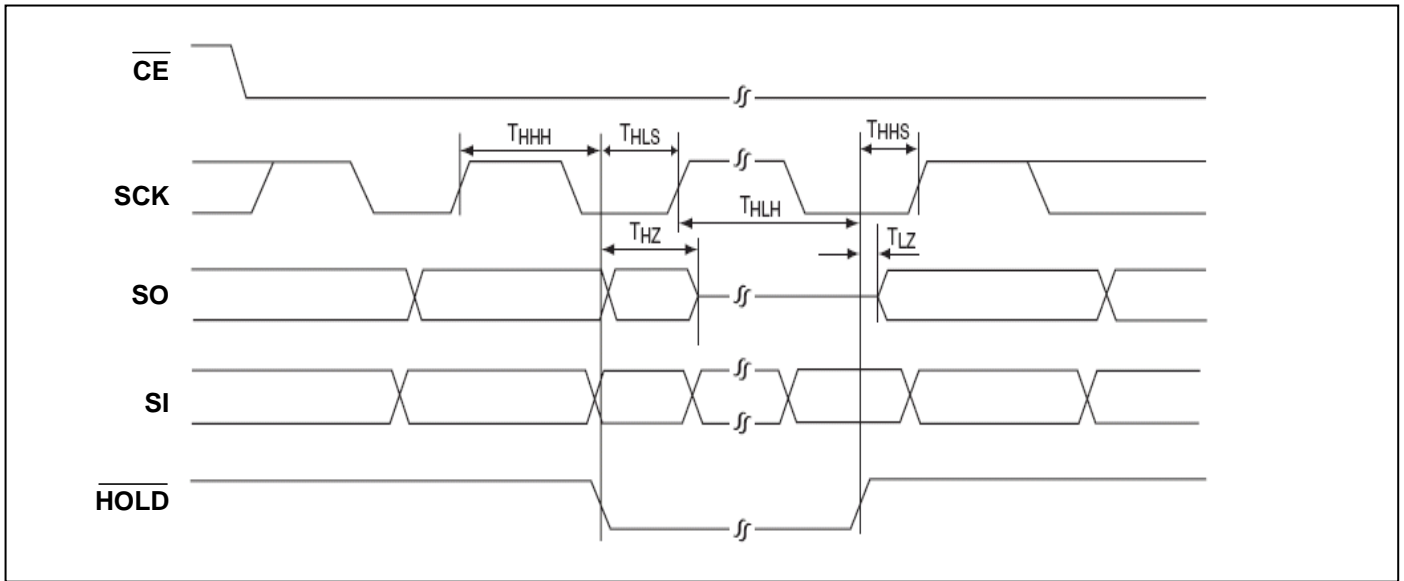


Figure 31: HOLD Timing Diagram

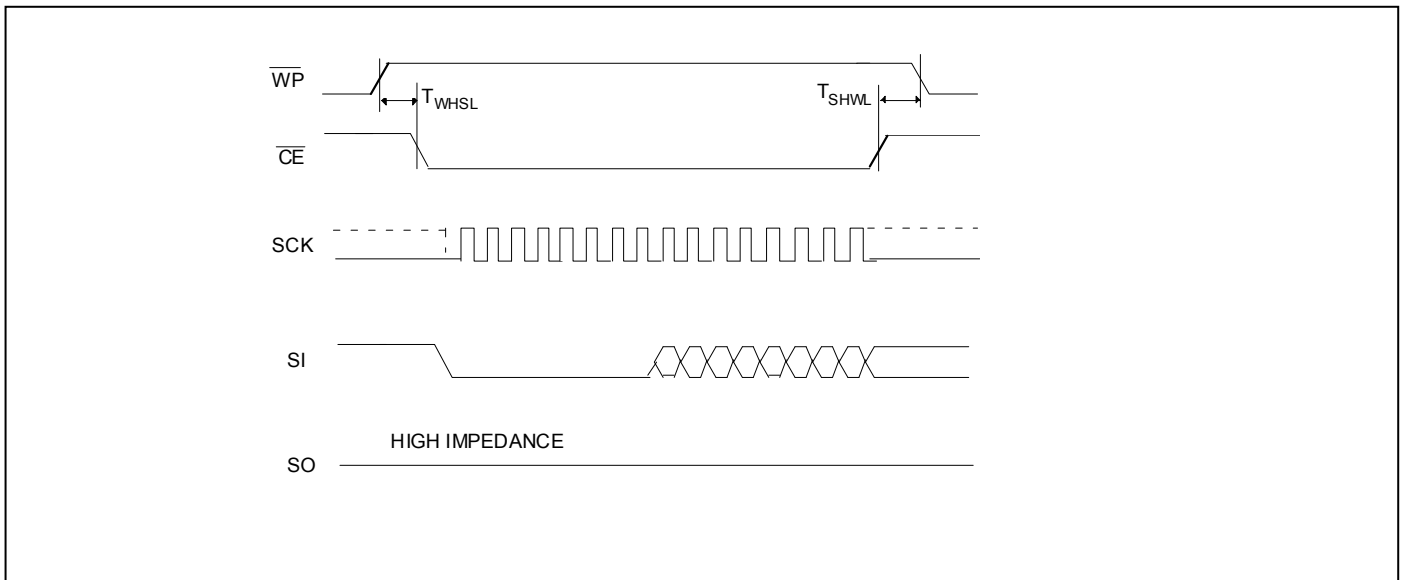


Figure 32: Write Protect setup and hold timing during WRSR when  $BPL = 1$

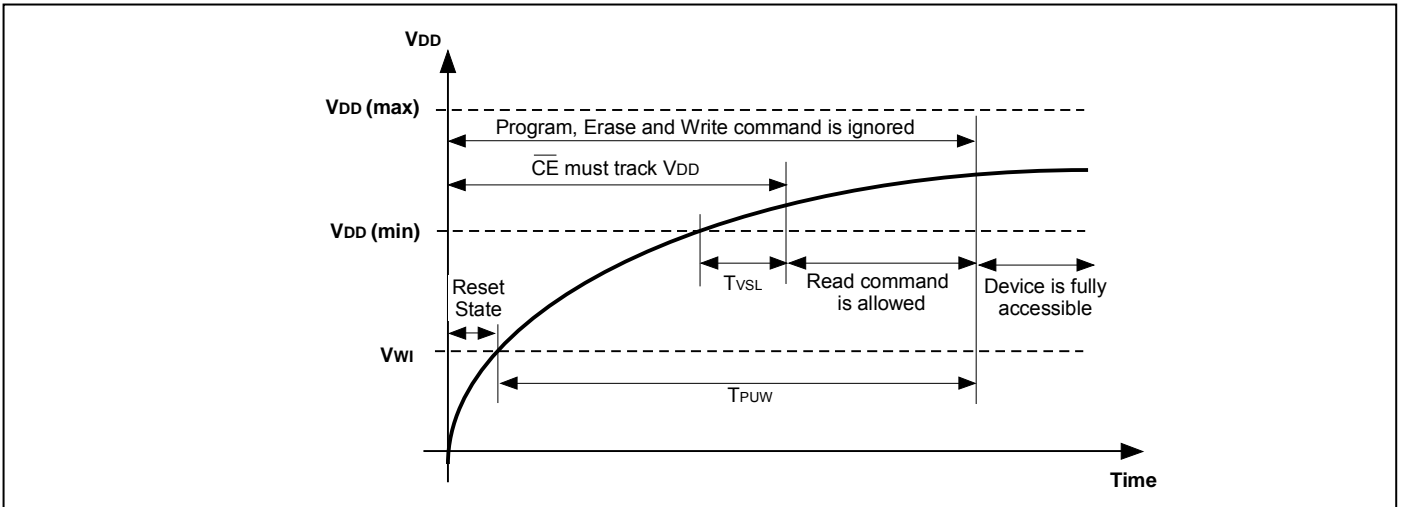


Figure 33: Power-Up Timing Diagram

Table 16: Power-Up Timing and  $V_{WI}$  Threshold

Parameter	Symbol	Min.	Max.	Unit
$V_{DD(min)}$ to $\overline{CE}$ low	$T_{VSL}$	10		us
Time Delay before Write instruction	$T_{PUW}$	1	10	ms
Write Inhibit Threshold Voltage	$V_{WI}$	1	2.5	V

Note: These parameters are characterized only.

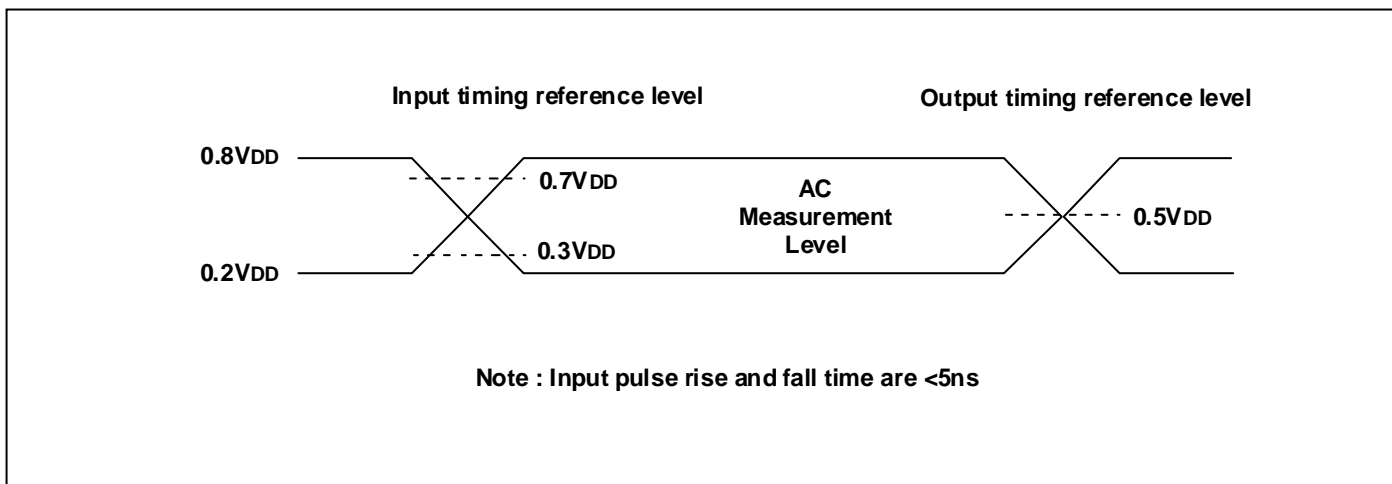


Figure 34: AC Input/Output Reference Waveforms

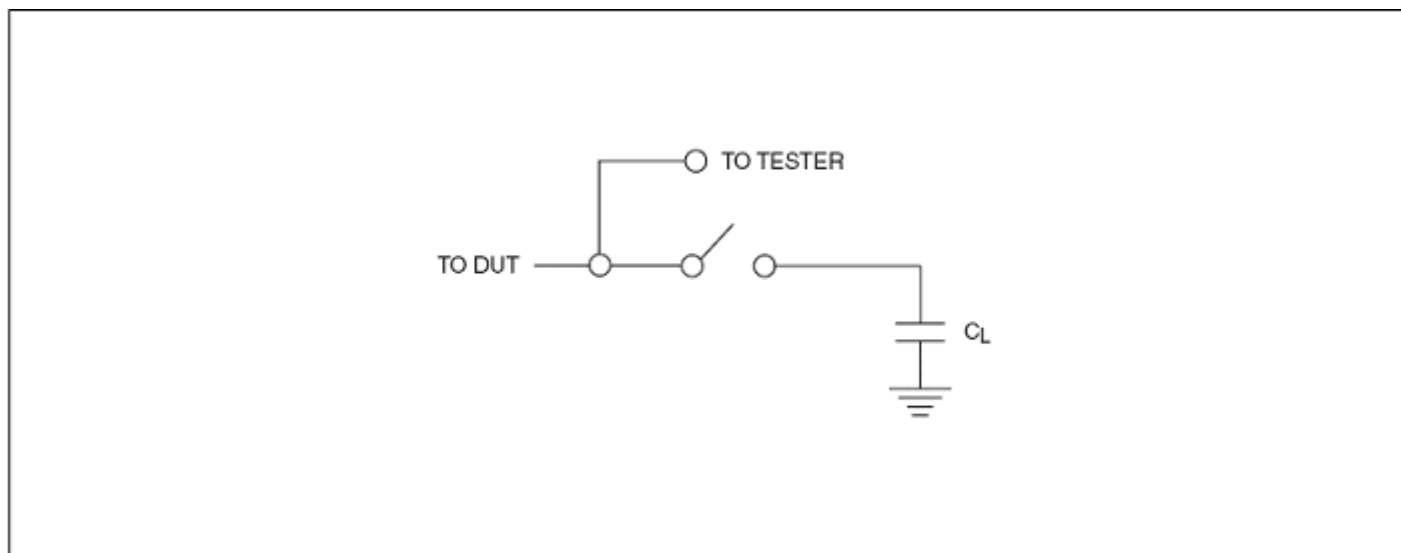
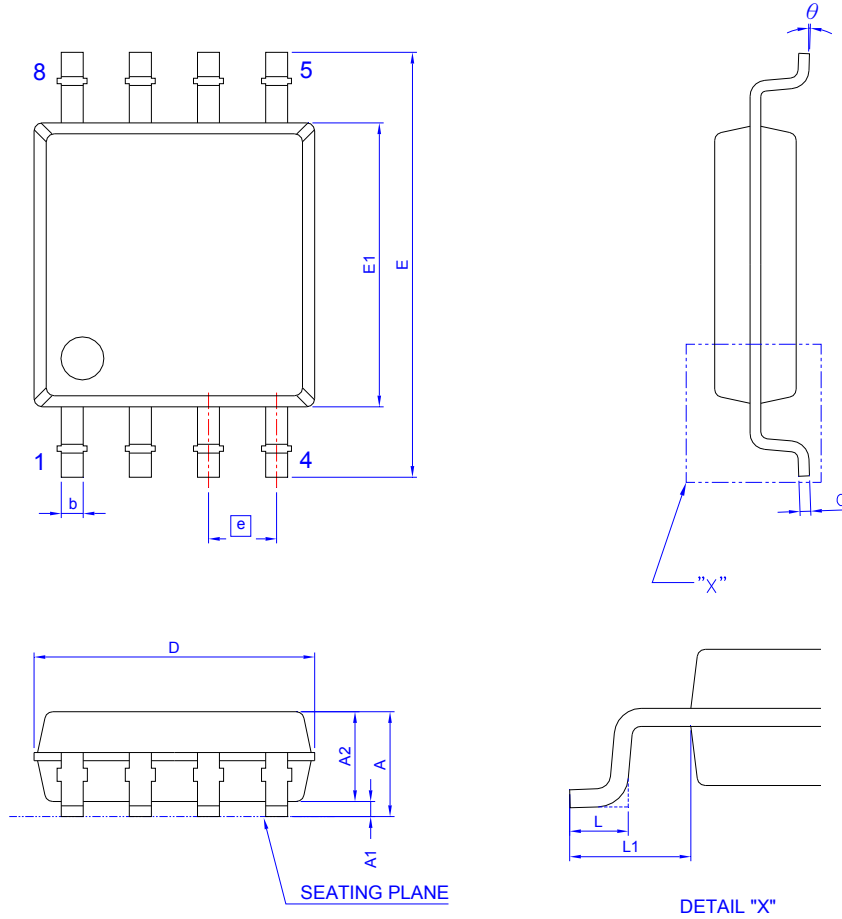


Figure 35: A Test Load Example

PACKING DIMENSIONS

8-LEAD SOIC 200 mil ( official name – 208 mil )

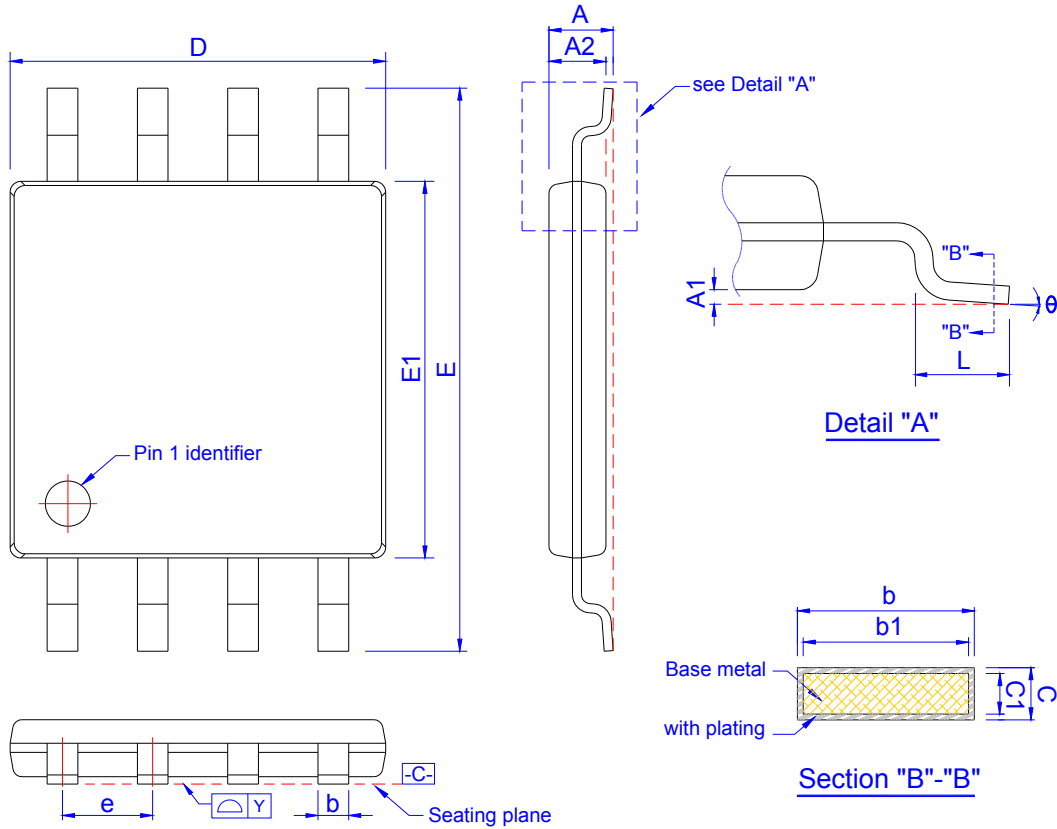


Symbol	Dimension in mm			Dimension in inch			Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max		Min	Norm	Max	Min	Norm	Max
A	---	---	2.16	---	---	0.085	E	7.70	7.90	8.10	0.303	0.311	0.319
A <sub>1</sub>	0.05	0.15	0.25	0.002	0.006	0.010	E <sub>1</sub>	5.18	5.28	5.38	0.204	0.208	0.212
A <sub>2</sub>	1.70	1.80	1.91	0.067	0.071	0.075	L	0.50	0.65	0.80	0.020	0.026	0.032
b	0.36	0.41	0.51	0.014	0.016	0.020	e	1.27 BSC			0.050 BSC		
c	0.19	0.20	0.25	0.007	0.008	0.010	L <sub>1</sub>	1.27	1.37	1.47	0.050	0.054	0.058
D	5.13	5.23	5.33	0.202	0.206	0.210	θ	0°	---	8°	0°	---	8°

Controlling dimension : millimeter

PACKING DIMENSIONS

8-LEAD VSOP 208 mil



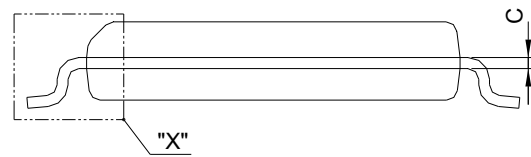
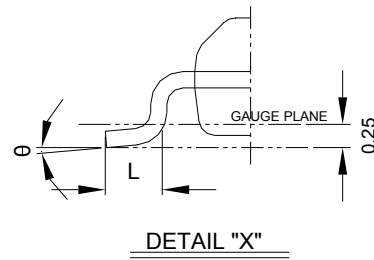
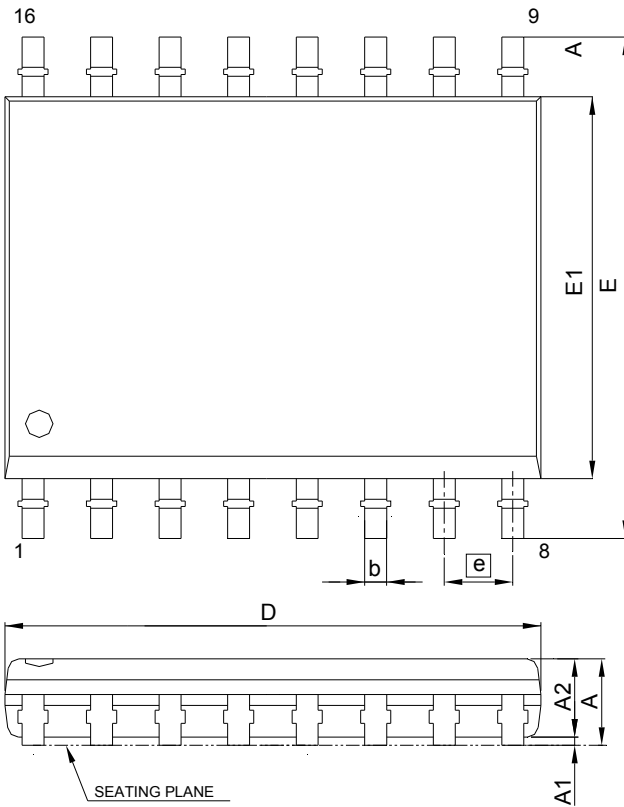
Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.00	—	—	0.039
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.75	0.80	0.85	0.030	0.031	0.033
b	0.35	0.42	0.48	0.014	0.017	0.019
b1	0.35	—	0.46	0.014	—	0.018
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.127	0.16	0.004	0.005	0.006
D	5.18	5.28	5.38	0.204	0.208	0.212
E	7.70	7.90	8.10	0.303	0.311	0.319
E1	5.18	5.28	5.38	0.204	0.208	0.212
L	0.50	0.65	0.80	0.020	0.026	0.031
e	1.27 BSC			0.050 BSC		
Y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°

Controlling dimension : Millimeter

(Revision date : Jul 27 2012)

PACKING DIMENSIONS

16-LEAD SOIC ( 300 mil )

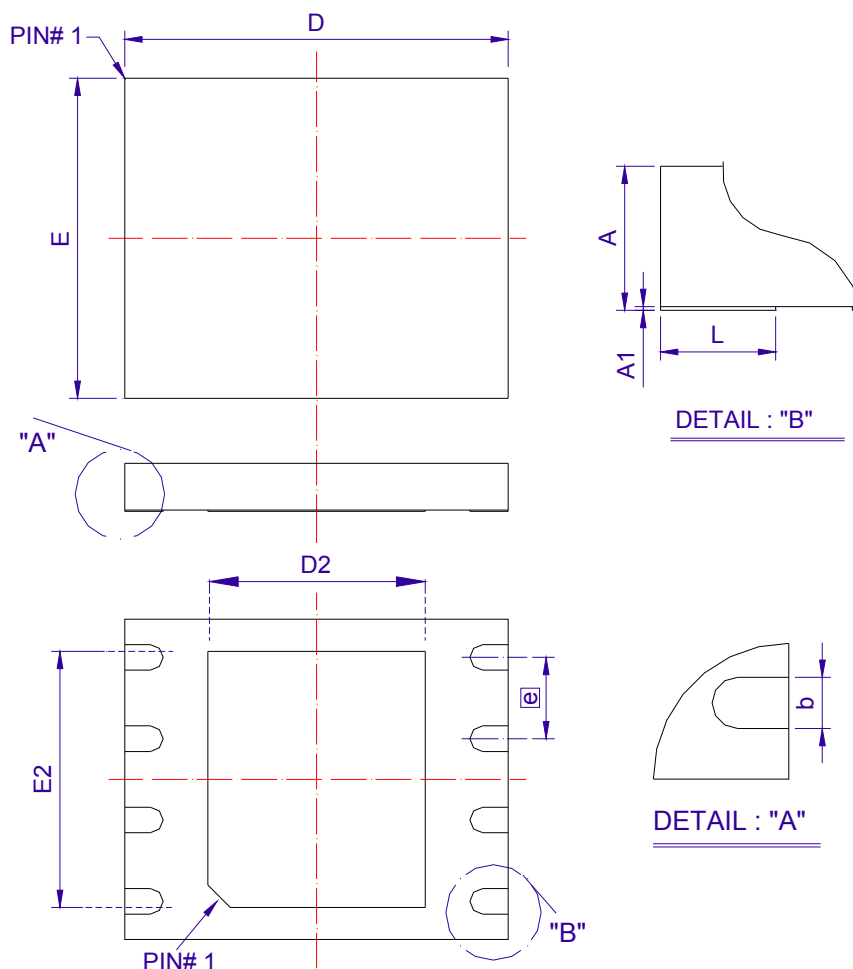


Symbol	Dimension in mm			Dimension in inch			Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max		Min	Norm	Max	Min	Norm	Max
A	---	---	2.65	---	---	0.104	E	10.30 BSC			0.406 BSC		
A <sub>1</sub>	0.1	---	0.3	0.004	---	0.012	E <sub>1</sub>	7.50 BSC			0.295 BSC		
A <sub>2</sub>	2.05	---	---	0.081	---	---	L	0.40	---	1.27	0.016	---	0.050
b	0.31	---	0.51	0.012	---	0.020	$\theta$	1.27 BSC			0.050 BSC		
c	0.20	---	0.33	0.008	---	0.013	$\theta$	0°	---	8°	0°	---	8°
D	10.10	10.30	10.50	0.400	0.406	0.413							

Controlling dimension : millimeter

PACKING DIMENSIONS

8-CONTACT WSON ( 6x5 mm )



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
D	5.90	6.00	6.10	0.232	0.236	0.240
D2	3.30	3.40	3.50	0.130	0.134	0.138
E	4.90	5.00	5.10	0.193	0.197	0.201
E2	3.90	4.00	4.10	0.154	0.157	0.161
e	1.27 BSC			0.050 BSC		
L	0.55	0.60	0.65	0.022	0.024	0.026

Controlling dimension : millimeter



## Revision History

Revision	Date	Description
0.1	2011.08.16	Original
0.2	2011.09.14	Correct WRSR command
0.3	2011.09.15	Correct Status Register-2 in Software Status Register table
0.4	2011.10.13	Modify minimum voltage from 2.7V to 2.65V
0.5	2011.12.13	Modify the specification of $T_{CE}$
0.6	2012.04.10	Correct D2 and E2 value of WSON packing dimensions
0.7	2012.04.18	Modify the range of $T_A$
1.0	2012.07.17	1. Delete "Preliminary" 2. Modify 100MHz to 104MHz for speed grade -100
1.1	2012.08.01	1. Add VSOP and BGA package 2. Modify Ambient Operating Temperature
1.2	2012.12.19	Modify the block range of BP3~BP0= 0111 in Block Protection Table
1.3	2013.01.14	1. Modify Product ID of VSOP (208mil) 2. Correct the description of Block Protection, Block Protection Lock-Down 3. Return the block range of BP3~BP0= 0111 in Block Protection Table 4. Delete BGA package
1.4	2013.03.28	Modify normal read from 33MHz to 50MHz
1.5	2013.12.26	1. Correct max. value of $T_{WHSL}$ and $T_{SHWL}$ to min. value 2. Modify the specification of $T_W(\max)$ 3. Add notes for AC OPERATING CHARACTERISTICS and ERASE AND PROGRAMMING PERFORMANCE
1.6	2014.09.16	1. Modify max. value of $t_{SE}$ and $t_{CE}$ 2. Correct the figure of Program/Erase Suspend Instruction

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