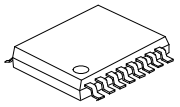
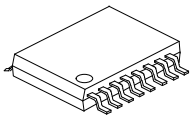
F2867 *LINEAR INTEGRATED CIRCUIT*

# VARIABLE SPEED SINGLE-PHASE FULL-WAVE PRE-DRIVER



SSOP-16



TSSOP-16

## ■ DESCRIPTION

The UTC **F2867** is a single-phase bipolar variable speed driving motor pre-driver that works with external PWM signal. A highly efficient, highly silent and low power consumption motor driver circuit can be achieved with a few external parts. This product is optimal for driving large scale fan motors requiring large air flow and large current such as servers and consumer appliances. UTC **F2867-R** is with RD option and UTC **F2867-F** with FG.

## ■ FEATURES

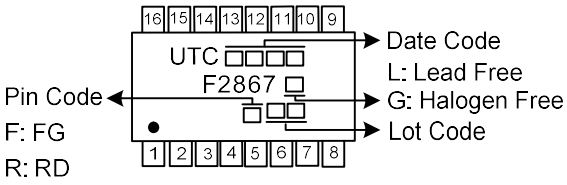
* Pre-driver for single-phase full-wave drive
  Low-saturation drive using external PMOS-NMOS enables high-efficiency low power-consumption drive.
* External PWM input enabling variable speed control
  Separately-excited upper direct PWM (f=30kHz) control method enabling highly silent speed control.
* Current limiting circuit incorporated
  Chopper type current limit at start.
* Reactive current cut circuit incorporated
  Reactive current before phase change is cut to enable silent and low power-consumption drive.
* Minimum speed setting pin
  Minimum speed can be set by set with external resistor.
* Soft start setting pin
* Lock protection and automatic reset functions incorporated
* Thermal shutdown circuit incorporated
* FG (rotation speed detection) output (**F2867-F**)
* RD(latch-type lockup detection) output (**F2867-R**)

## ■ ORDERING INFORMATION

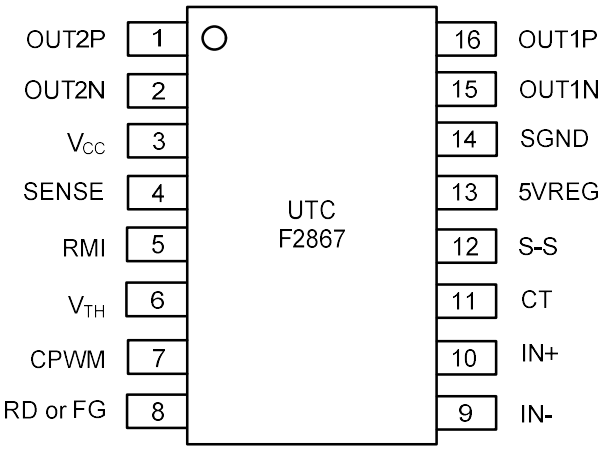
| Ordering Number | | Package | Packing |
|---|---|---|---|
| Lead Free | Halogen Free | | |
| F2867L-R16-F-R | F2867G-R16-F-R | SSOP-16 | Tape Reel |
| F2867L-R16-R-R | F2867G-R16-R-R | SSOP-16 | Tape Reel |
| F2867L-P16-F-R | F2867G-P16-F-R | TSSOP-16 | Tape Reel |
| F2867L-P16-R-R | F2867G-P16-R-R | TSSOP-16 | Tape Reel |

| | |
|---|---|
| F2867G-R16-F-R<br>(1)Packing Type<br>(2)Pin Code<br>(3)Package Type<br>(4)Green Package | (1) R: Tape Reel<br>(2) F: FG, R: RD<br>(3) R16: SSOP-16, P16: TSSOP-16<br>(4) G: Halogen Free and Lead Free, L: Lead Free |

## ■ MARKING



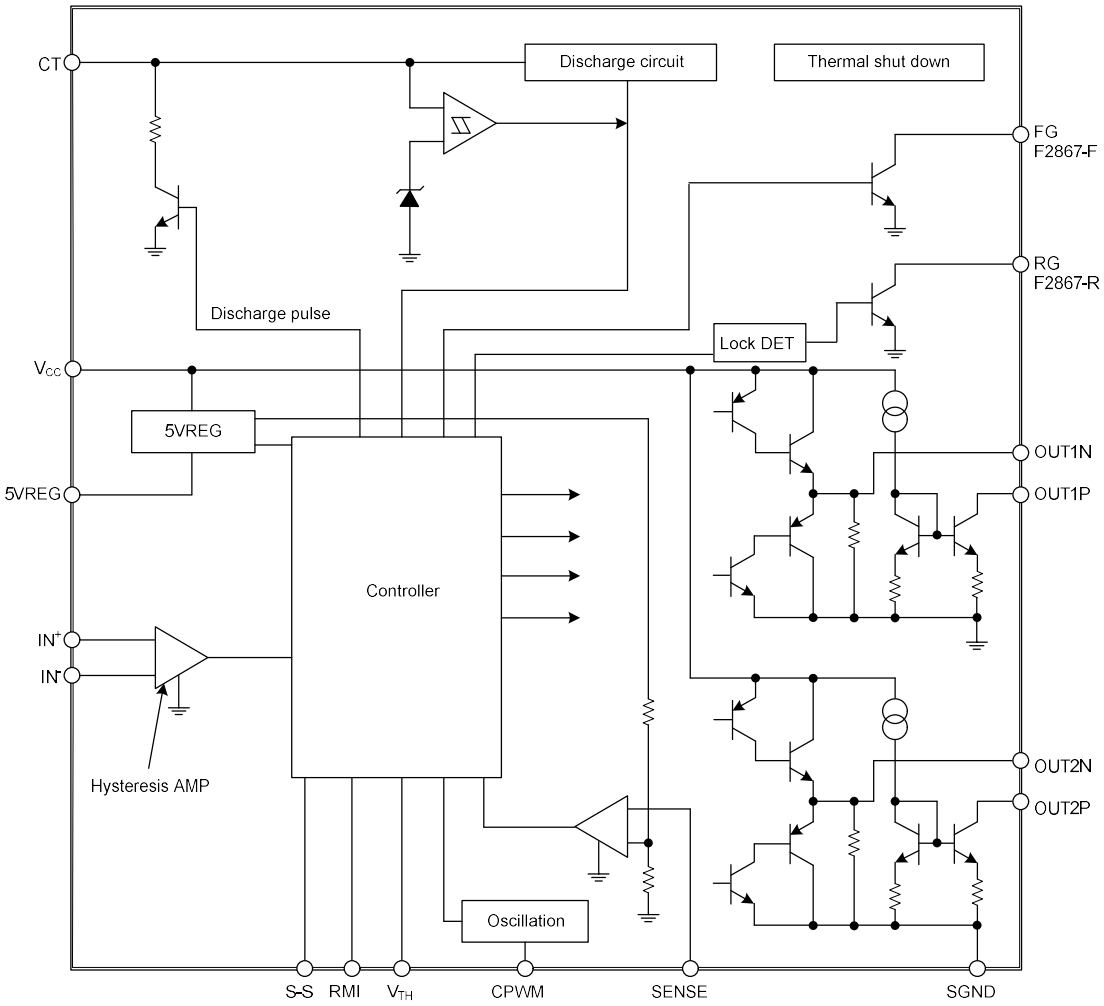
## ■ PIN CONFIGURATION




## ■ PIN DESCRIPTION

| PIN NO. | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | OUT2P | Output2 PMOS drive |
| 2 | OUT2N | Output2 NMOS drive |
| 3 | $V_{CC}$ | Power supply |
| 4 | SENSE | Current limiting detection pin |
| 5 | RMI | Minimum speed setting pin |
| 6 | $V_{TH}$ | Speed control pin |
| 7 | CPWM | Pin to connect the capacitor for generation of the PWM basic frequency |
| 8 | FG or RD | Rotation speed detection pin/latch-type lockup detection pin |
| 9 | $IN^-$ | Hall signal input |
| 10 | $IN^+$ | Hall signal input |
| 11 | CT | Pin to connect the lock detection capacitor |
| 12 | S-S | Pin to connect the soft-start setting capacitor |
| 13 | 5VREG | 5V reference voltage |
| 14 | SGND | Power-GND |
| 15 | OUT1N | Output1 NMOS drive |
| 16 | OUT1P | Output1 PMOS drive |

## ■ BLOCK DIAGRAM




## ■ TRUTH TABLE

**Table 1.DRIVE LOCK CPWM = H VTH, RMI, S−S = L**

| IN- | IN+ | CT | OUT1P | OUT1N | OUT2P | OUT2N | FG | RD | MODE |
|---|---|---|---|---|---|---|---|---|---|
| H | L | L | L | L | OFF | H | L | ON | OUT1→2 drive |
| L | H | | OFF | H | L | L | OFF | | OUT2→1 drive |
| H | L | H | OFF | L | OFF | H | L | OFF | Lock protection |
| L | H | | OFF | H | OFF | L | OFF | | |

**Table 2.SPEED CONTROL CT, S−S = L**

| $V_{TH}$, RMI | CPWM | IN- | IN+ | OUT1P | OUT1N | OUT2P | OUT2N | MODE |
|---|---|---|---|---|---|---|---|---|
| L | H | H | L | L | L | OFF | H | OUT1→2 drive |
| | | L | H | OFF | H | L | L | OUT2→1 drive |
| H | L | H | L | OFF | L | OFF | H | Regeneration mode |
| | | L | H | OFF | H | OFF | L | |

Note: For $V_{TH}$, RMI, and S-S pins, refer to the timing chart.

## ■ ABSOLUTE MAXIMUM RATING ($T_A$=25°C unless otherwise specified)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| $V_{CC}$ Pin Maximum Supply Voltage | $V_{CC}$ | 18 | V |
| OUTN Pin Maximum Output Current | $I_{OUTN}$ | 20 | mA |
| OUTP Pin Maximum Sink Current | $I_{OUTP}$ | 20 | mA |
| OUT Pin Output Withstand Voltage | $V_{OUT}$ | 18 | V |
| $V_{TH}$, RMI Pins Withstand Voltage | $V_{VTH}$, $V_{RMI}$ | 7 | V |
| S-S Pin Withstand Voltage | $V_{S-S}$ | 7 | V |
| FG/RD Output Pin Withstand Voltage | $V_{FG}$ / $V_{RD}$ | 19 | V |
| FG/RD Pin Maximum Output Current | $I_{FG}$ / $I_{RD}$ | 10 | mA |
| 5VREG Pin Maximum Output Current | $I5V_{REG}$ | 20 | mA |
| Allowable Power Dissipation (with specified substrate (Note 2)) | $P_D$ | 800 | mW |
| Junction Temperature | $T_J$ | +150 | °C |
| Operating Temperature (Note 3) | $T_{OPR}$ | -30 ~ +95 | °C |
| Storage Temperature | $T_{STG}$ | -55 ~ +150 | °C |

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Specified substrate: 114.3mm×76.1mm×1.6mm, glass epoxy board.

## ■ RECOMMENDED OPERATING CONDITIONS ($T_A$=25°C unless otherwise specified)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| $V_{CC}$ Supply Voltage | $V_{CC}$ | 5.5 ~ 16 | V |
| $V_{TH}$, RMI Input Voltage Range | $V_{TH}$, $R_{MI}$ | 0 ~ 5 | V |
| Hall Input Common-Phase Input Voltage Range | $V_{ICM}$ | 0.2 ~ 3 | V |

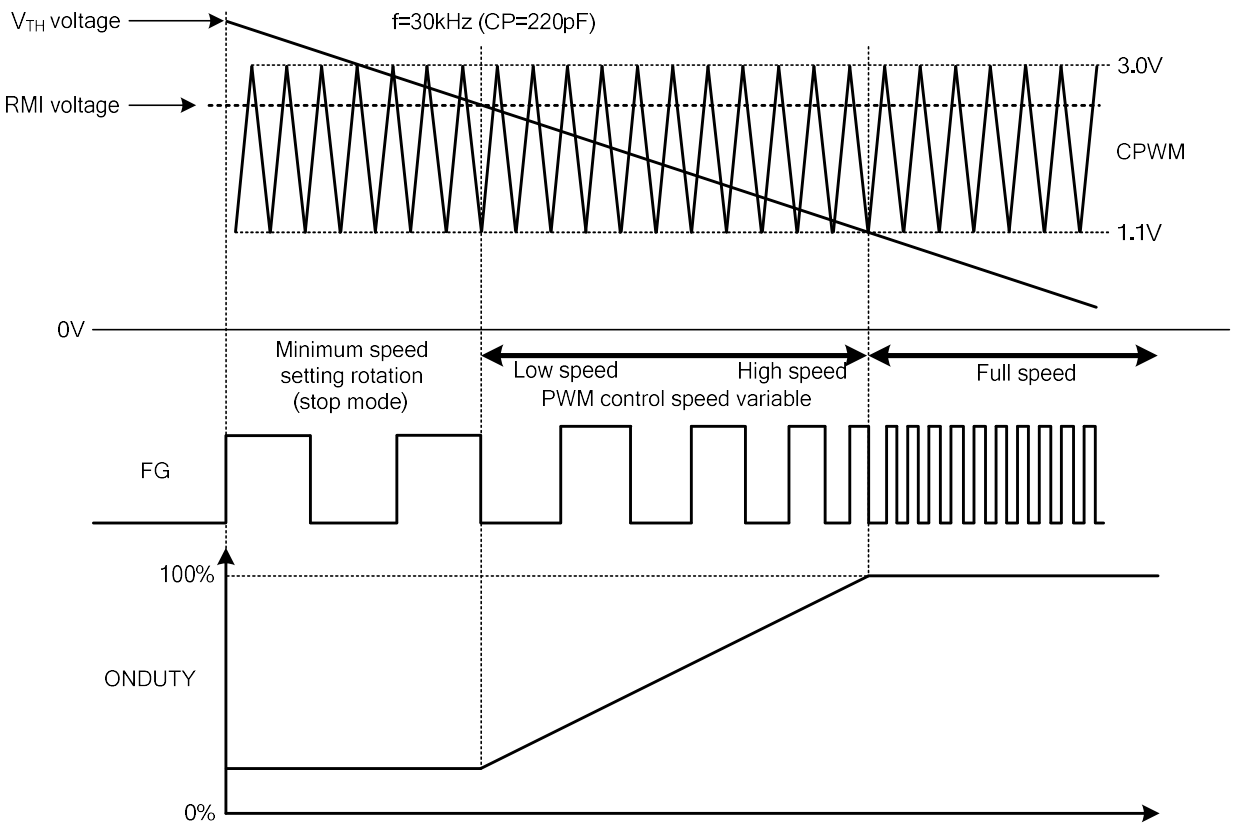
## ■ ELECTRICAL CHARACTERISTICS ($V_{CC}$=12V, $T_A$=25°C unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Circuit Current | $I_{CC1}$ | During drive | 5.5 | 7.5 | 9.5 | mA |
| | $I_{CC2}$ | During lock protection | 5.5 | 7.5 | 9.5 | mA |
| 5VREG Voltage | $5V_{REG}$ | I5VREG = 5mA | 4.80 | 4.95 | 5.10 | V |
| Current Limiting Voltage | $V_{LIM}$ | | 185 | 200 | 215 | mV |
| CPWM Pin “h” Level Voltage | $V_{CPWM\_H}$ | | 2.8 | 3.0 | 3.2 | V |
| CPWM Pin “L” Level Voltage | $V_{CPWM\_L}$ | | 0.9 | 1.1 | 1.3 | V |
| CPWM Pin Charge Current | $I_{CPWM1}$ | $V_{CPWM}$=0.5V | 24 | 30 | 36 | μA |
| CPWM Pin Discharge Current | $I_{CPWM2}$ | $V_{CPWM}$=3.5V | 21 | 27 | 33 | μA |
| CPWM Oscillation Frequency | $F_{PWM}$ | C=220PF | | 30 | | kHz |
| CT Pin “H” Level Voltage | $V_{CTH}$ | | 2.8 | 3.0 | 3.2 | V |
| CT Pin “L” Level Voltage | $V_{CTL}$ | | 0.9 | 1.1 | 1.3 | V |
| CT Pin Charge Current | $I_{CT1}$ | $V_{CT}$=0.5V | 1.6 | 2.0 | 2.5 | μA |
| CT Pin Discharge Current | $I_{CT2}$ | $V_{CT}$=3.5V | 0.16 | 0.20 | 0.25 | μA |
| CT Pin Charge/Discharge Ratio | $R_{CT}$ | $I_{CT}1/I_{CT}2$ | 8 | 10 | 12 | times |
| S-S Pin Discharge Current | $I_{S-S}$ | $V_{S-S}$=1V | 0.4 | 0.5 | 0.6 | μA |
| OUTN Output H-level Voltage | $V_{ONH}$ | $I_O$=10mA | | $V_{CC}$-0.85 | $V_{CC}$-1.00 | V |
| OUTN Output L-level Voltage | $V_{ONL}$ | $I_O$=10mA | | 0.9 | 1.2 | V |
| OUTP Output L-level Voltage | $V_{OPL}$ | $I_O$=10mA | | 0.5 | 0.65 | V |
| Hall Input Sensitivity | $V_{HN}$ | $IN^+$, $IN^-$ differential voltage (including offset and hysteresis) | | ±10 | ±20 | mV |

## ■ ELECTRICAL CHARACTERISTICS (Cont.)

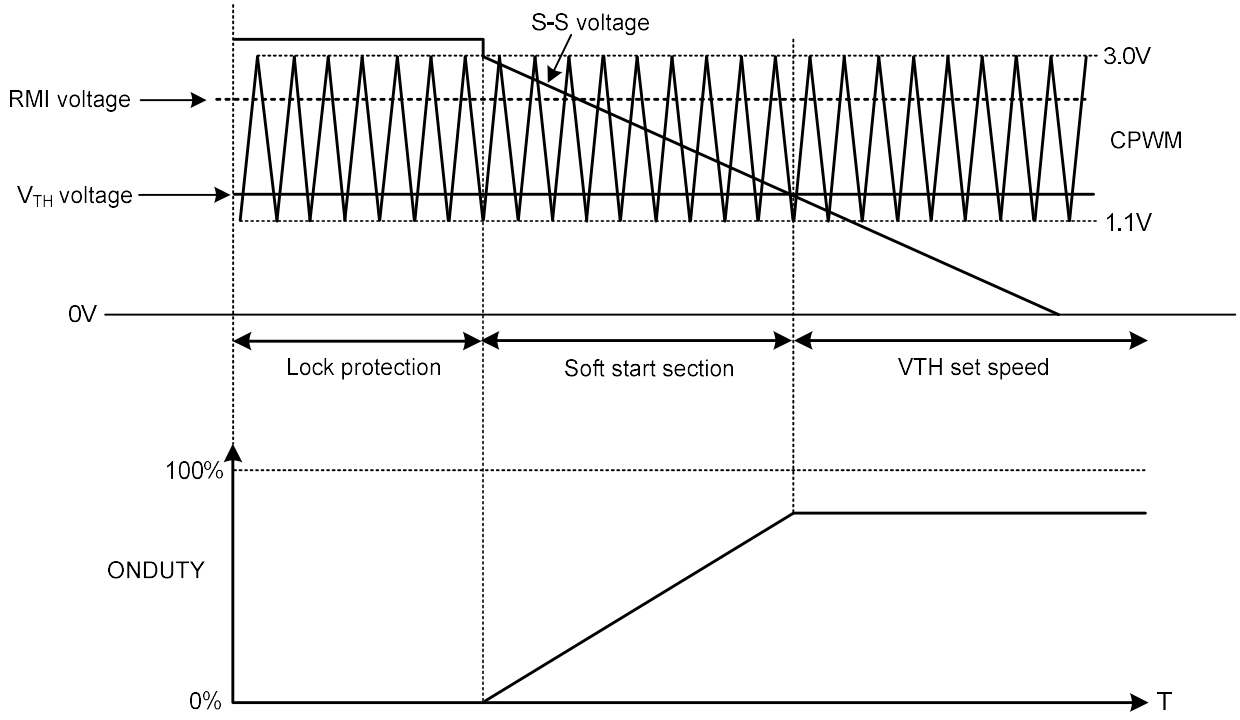
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| FG Output L-level Voltage | $V_{FGL}$ | $I_{FG}$=5mA | | 0.15 | 0.40 | V |
| FG Pin Leakage Current | $I_{FGL}$ | $V_{FG}$=19V | | | 20 | μA |
| RD Output L-level Voltage | $V_{FGL}$ | $I_{FG}$=5mA | | 0.15 | 0.40 | V |
| RD Pin Leakage Current | $I_{FGL}$ | $V_{FG}$=19V | | | 20 | μA |
| $V_{TH}$/RMI Pin Bias Current | $I_{VTH}/I_{RMI}$ | CPWM=$V_{TH}$/RMI=2V | | | 0.2 | μA |

## ■ CONTROL TIMING CHART (Speed Control)

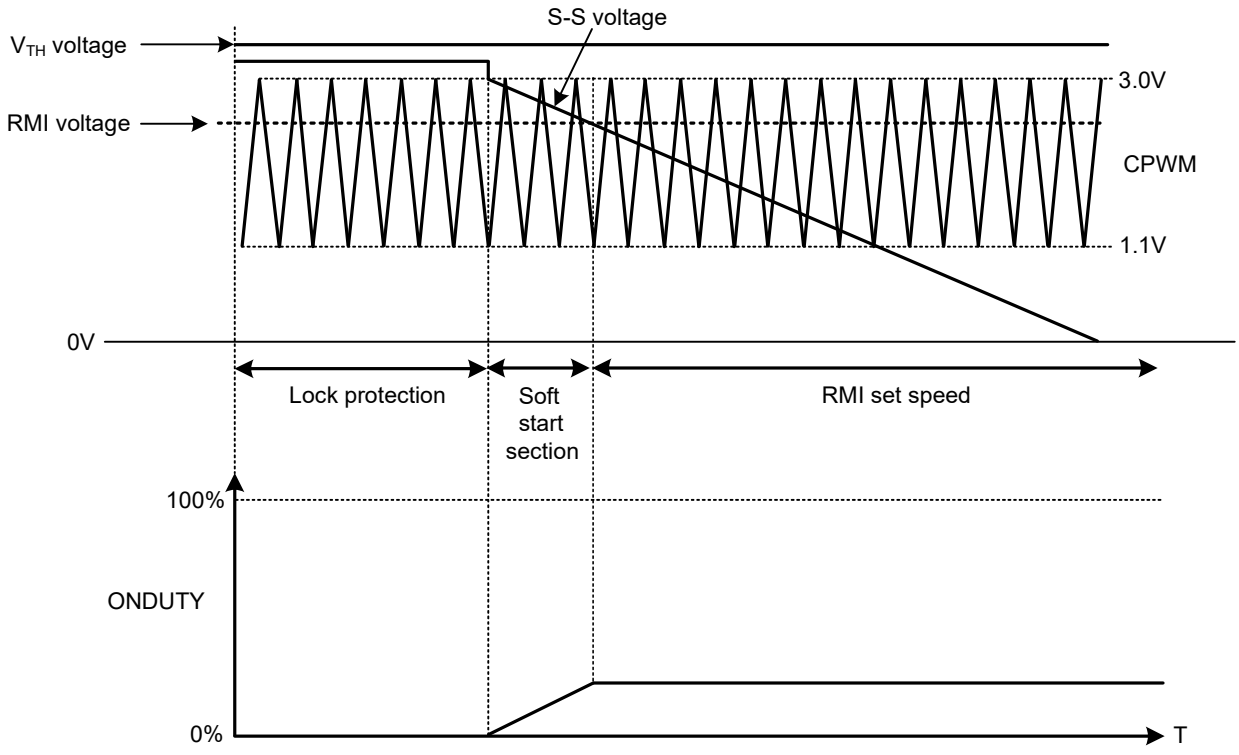


## ■ CONTROL TIMING CHART (Cont.) (Soft start)

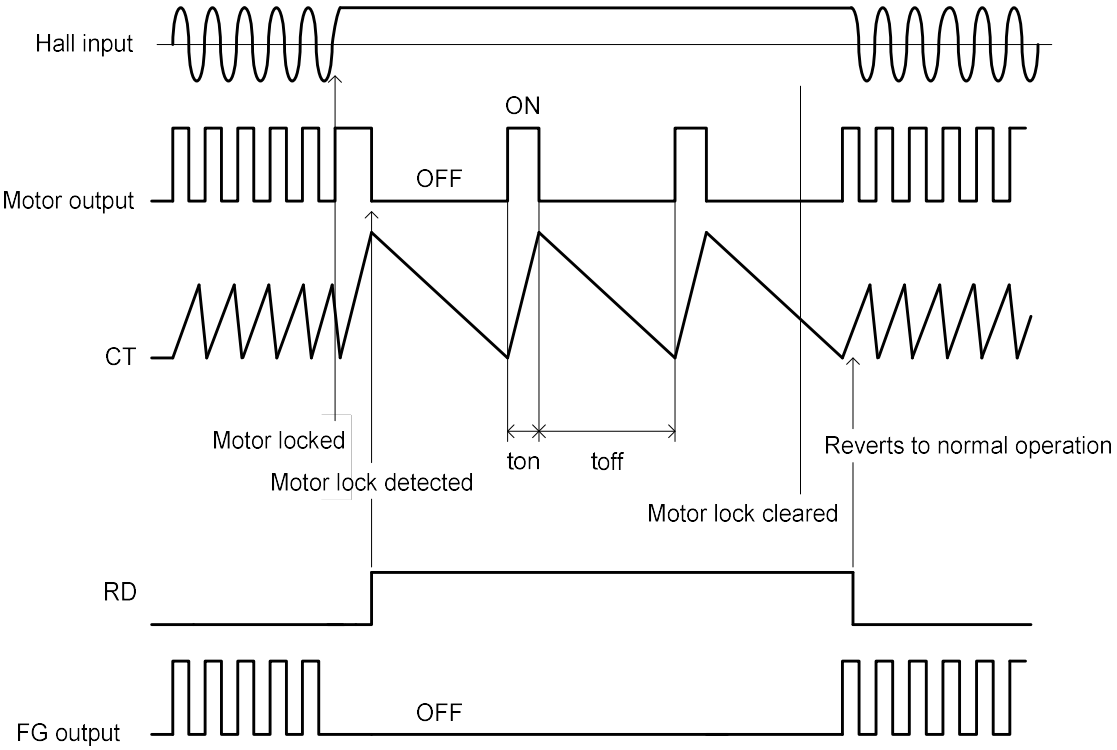
(1) At $V_{TH}$ < RMI voltage



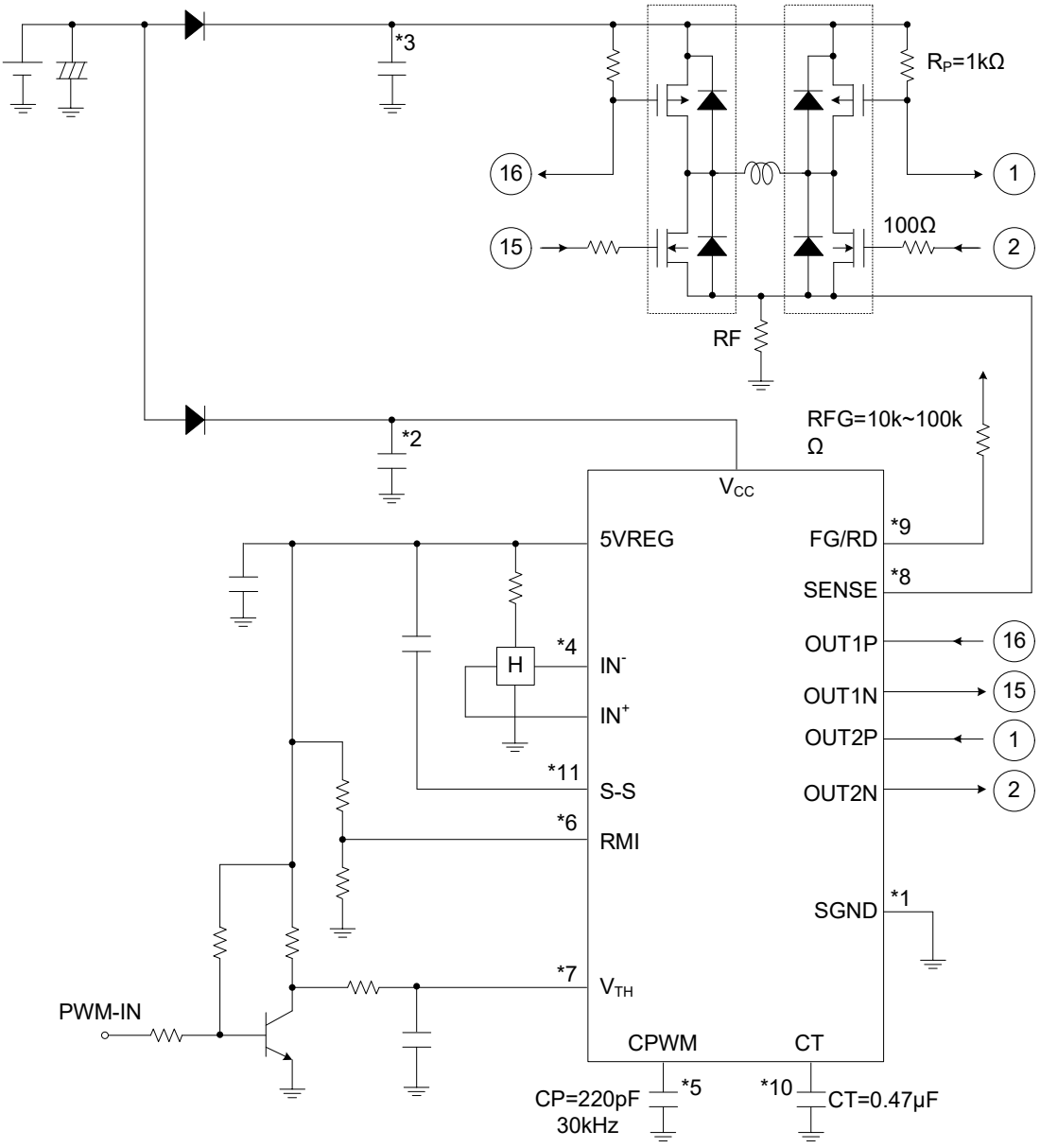

(2) At $V_{TH}$ > RMI voltage



## ■ LOCKUP PROTECTION / AUTOMATIC RECOVERY



## ■ TYPICAL APPLICATION CIRCUIT




Notes: *1. Power−GND wiring

SGND is connected to the control circuit power supply system.

*2. Power stabilization capacitor

For the power stabilization capacitor on the signal side, use the capacitance of 1μF or more.

Connect $V_{CC}$ and GND with a thick and shortest pattern.

*3. Power stabilization capacitor on the power side

For the power stabilization capacitor on the power side, use the capacitance of 1μF or more.

Connect the power supply on the power side and GND with a thick and shortest pattern.

*4. $IN^+$, $IN^-$ pins

Hall signal input pin.

Wiring should be short to prevent carrying of noise.

If noise is carried, insert the capacitor between IN+ and IN- pins.

The Hall input circuit functions as a comparator with hysteresis (15mV).

This also has a soft switch section with ±30mV (input signal differential voltage).

It is also recommended that the Hall input level is minimum 100mV (p-p).

## ■ TYPICAL APPLICATION CIRCUIT (Cont.)

Notes: *5. CPWM pin
Pin to connect the capacitor for generation of the PWM basic frequency
The use of CP=220pF causes oscillation at f=30kHz, which is the basic frequency of PWM.
As this is used also for the current limiting canceling signal, be sure to connect the capacitor even when the speed control is not made.

*6. RMI pin
Minimum speed setting pin.
Perform pull-up with 5VREG when this pin is not to be used.
If the IC power supply is likely to be turned OFF first when the pin is used with external power supply, be sure to insert the current limiting resistor to prevent inflow of large current. (The same applies to the $V_{TH}$ pin.)

*7. $V_{TH}$ pin
Speed control pin.
Connect this pin to GND when it is not used (at full speed).
For the control method, refer to the timing chart.
For control with pulse input, insert the current limiting resistor and use the pin with the frequency of 20k~100kHz (20kHz~50kHz recommended).

*8. SENSE pin
Current limiting detection pin.
When the pin voltage exceeds 0.2V, the current is limited and the operation enters the lower regeneration mode.
Connect this pin to GND when it is not to be used.

*9. FG/RD pin
"FG" means pin 8 is an output pin of FG signal which is used for detecting rotation speed. "RD" means pin 8 is an output pin of RD signal, and is used for detecting fan rotate-stop state. "FG" and "RD" can be selected according to the requirement. This pin need to be connected with pull-up resistor when used. A new pulse will be generated once input signal changed. Keep this pin open when it is not to be used.

*10. CT pin
Pin to connect the lock detection capacitor.
The constant-current charge and discharge circuits incorporated cause locking when the pin voltage becomes 3.0V and unlocking when it is 1.1V. Connect the pin to GND when it is not to be used (locking not necessary).

*11. S-S pin
Pin to connect the soft-start setting capacitor.
Connect the capacitor between 5VREG and S-S pin.
This pin enables setting of the soft start time according to the capacity of the capacitor.
See the timing char.
Connect the pin to GND when it is not to be used.