F38C70 Single-Chip Microcomputer

T-49-19-08

Microprocessor Product

Description

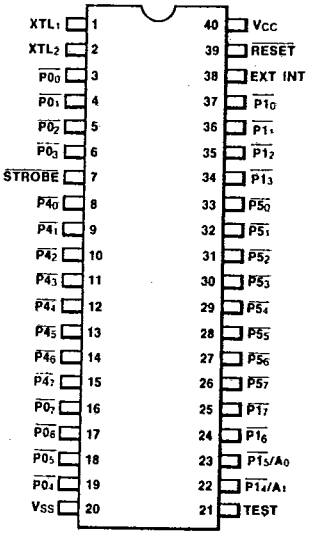
The Fairchild F38C70 8-bit single-chip microcomputer is a member of the F387X series; it executes all of the F8 instruction set and is software-compatible with the F3870. Additional power-save instructions provide two different power-save modes.

Implemented in ion-implanted CMOS doublepoly silicon-gate technology, the F38C70 offers maximum cost effectiveness in a wide range of applications requiring very low power consumption.

More than 70 commands of the F8 instruction set are executed by the single-chip microcomputer, which features 2048 bytes of ROM, 64 bytes of scratchpad RAM, a programmable timer, 32 bits of I/O, and a single +5 V power supply.

- **Single CMOS Integrated Circuit**
- **Software-Compatible with F8 and F3870**
- **2048-Byte Mask Programmable ROM**
- **64-Byte Scratchpad RAM**
- **32-Bit I/O with Four Options**
- **8-Bit Programmable Timer with 16-Bit Programmable Prescaler**
- **External Interrupt**
- **Crystal, LC, RC, or External Clock**
- **Single +5 V (±10%) Power Supply**
- **Power-Save (PS) and Power-Save All (PSA) Modes**
- **Option for all Short Machine Cycles**
- **Direct Replacement for F3870**
- **Low Power (50 mW typ., 5 mW in PS mode, 0.5 mW in PSA mode)**

Connection Diagram
40-Pin DIP



(Top View)

Signal Functions

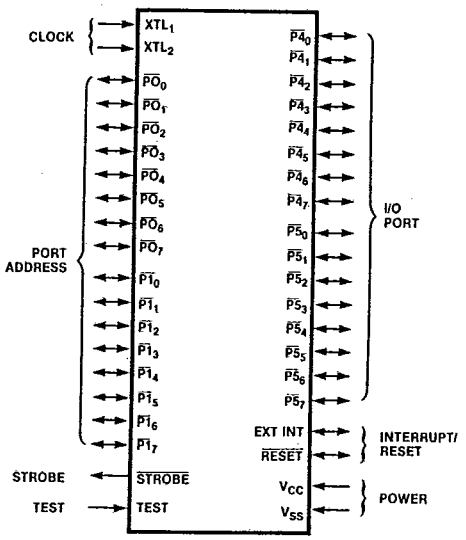
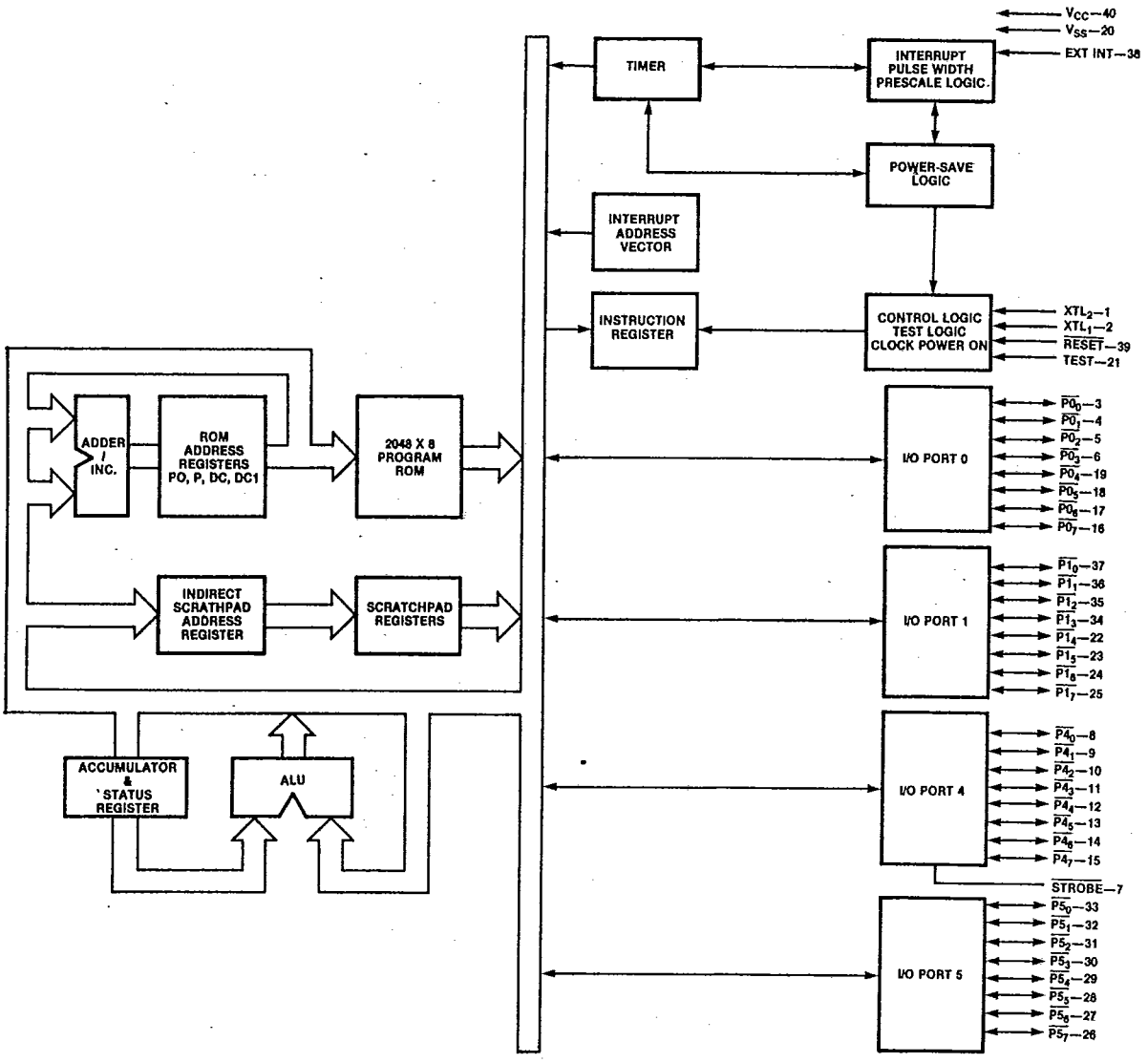


Figure 1 Block Diagram



Main Control Logic

The instruction register (IR) receives the operation code (OP code) of the instruction to be executed from the program ROM through the data bus. Eight bits are latched into the IR during all OP code fetches. Some instructions are completely specified by the upper four bits of the OP code; in these instructions, the lower four bits are an immediate register address or an immediate 4-bit operand. Once latched into the IR, the main control logic decodes the instruction and provides the necessary control gating signals to all circuit elements.

ROM Address Registers

Four 12-bit registers are associated with the program ROM: program counter PO, stack register P, data counter DC0, and auxiliary data counter DC1. The program counter is used to address instructions or immediate operands; the stack register is used to save the contents of PO during an interrupt or subroutine call. Thus, P contains the return address at which processing is to resume upon completion of the subroutine or the interrupt routine.

The data counter is used to address data tables. This register is autoincrementing. Of the two data counters, only DC0 can access the ROM; however, the XDC instruction allows DC0 and DC1 to be exchanged.

Associated with the address registers is a 12-bit adder/incrementer. This logic element is used to increment PO or DC when required and to add displacements to PO on relative branches or to add the data bus contents to DC0 in the add data counter (ADC) instruction.

Program ROM

The microcomputer program and data constants are stored in the 2048 X 8 byte program ROM. When a ROM access is required, the appropriate address register (PO or DC0) is gated onto the ROM address bus and the ROM output is gated onto the main data bus. The first byte in the ROM is location zero.

Scratchpad and ISAR

The scratchpad provides 64 8-bit registers that can be used as general purpose RAM memory. The indirect scratchpad address register (ISAR) is a 6-bit register used to address the 64 registers. All 64 registers can be accessed using the ISAR. In addition, the lower order 12 registers can also be directly addressed.

The ISAR can be visualized as holding two octal digits. This division of the ISAR is important, since a number of instructions increment or decrement only the least significant three bits of the ISAR when referencing scratchpad bytes through the ISAR. This simplifies referencing a buffer of contiguous scratchpad bytes. For example, when the low-order octal digit is incremented or decremented, the ISAR is incremented from octal 27 (0'27) to 0'20' or is decremented from 0'20' to 0'27'. This feature of the ISAR is very useful in many program sequences.

All six bits of the ISAR can be loaded at one time, or either half can be loaded independently.

The decimal scratchpad registers (9 through 15) are given mnemonic names (J, H, K, and Q) because of special linkages between these and other registers, such as the stack register. These special linkages simplify the performance of multi-level interrupts and subroutine nesting. For example, the instruction LR K,P stores the lower eight bits of the stack register into register 13 (K lower, or KL) and stores the upper three bits of P into register 12 (K upper, or KU).

Arithmetic and Logic Unit (ALU)

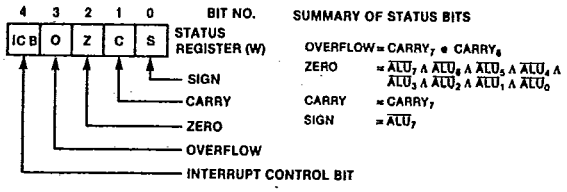
After receiving commands from the main control logic, the ALU performs the required arithmetic or logic operations (using the data presented on the two input buses) and provides the result on the result bus. The arithmetic operations performed in the ALU are binary add, decimal adjust, add with carry, decrement, and increment. The logic operations performed are AND, OR, exclusive-OR, ones complement, shift right, and shift left. The ALU also provides four signals presenting the status of the result. These signals, stored in status register W, represent the carry, overflow, sign, and zero condition of the operation.

Accumulator

The accumulator (ACC) is the prinicpal register for data manipulation within the F38C70. The ACC serves as one input to the ALU for arithmetic or logic operations; the results of ALU operations are stored in the ACC.

Status Register

The status (W) register holds five status flags:



Interrupt Control Bit

The interrupt control bit (ICB) is used to allow or disallow interrupts in the F38C70. (This bit is not the same as the two interrupt enable bits in the interrupt control port.) If the ICB is set and the F38C70 interrupt logic communicates an interrupt request to the CPU section, the interrupt is acknowledged and processed upon completion of the first non-privileged instruction. If the ICB is cleared, an interrupt request is not acknowledged or processed until the ICB is set again.

I/O Ports

The F38C70 provides four complete bidirectional input/output ports: 0, 1, 4, and 5. In addition, the interrupt control port is addressed as port 6, and the binary timer is addressed as port 7. Ports 8 and 9 are the 16-bit holding register for the timer prescaler.

An output instruction (OUT or OUTS) causes the contents of the ACC to be latched into the addressed port. An input instruction (IN or INS) transfers the contents of the port to the ACC (port 6, an exception, is described in the "Timer and Interrupt Control Port") section. The I/O buffers on the F38C70 are logically inverted.

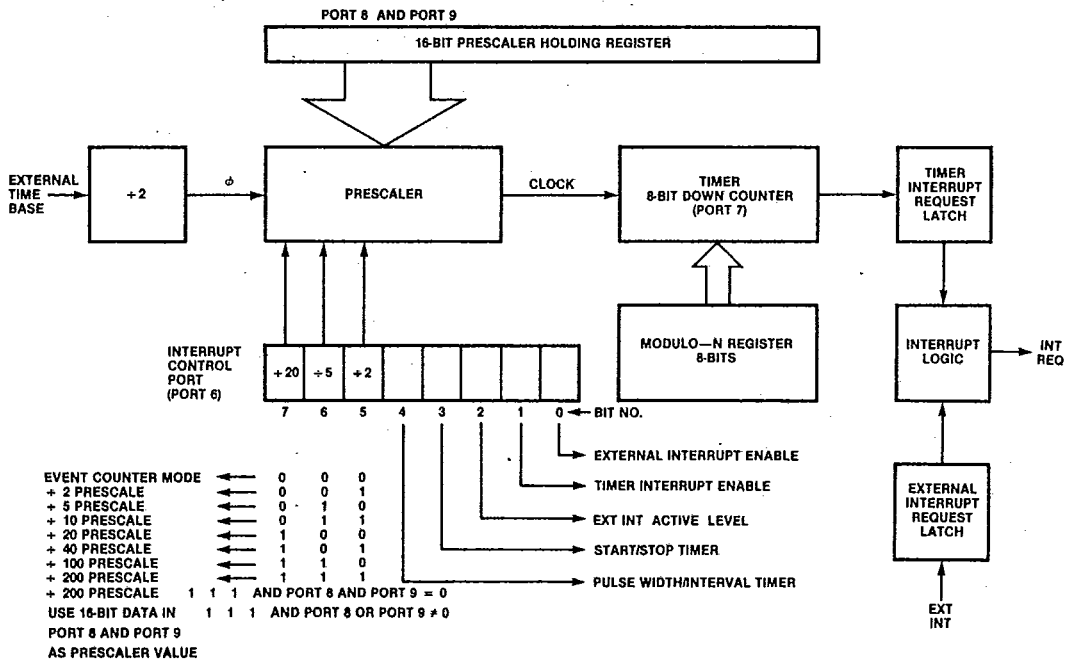
An output ready strobe is associated with port 4. This flag is used to signal a peripheral device that the F38C70 has just completed an output of new data to port 4. Because the strobe provides a single low pulse shortly after the output operation is complete, either edge can be used to signal the peripheral. The STROBE signal is also used to request new input information from a peripheral by performing a dummy output of H'00' to port 4 after completing the input operation.

Four output drive options are available for the F38C70 I/O ports. Individual bits of the four I/O ports are configured as

1. Open drain
2. CMOS 3-state push-pull buffer
3. TTL-compatible
4. CMOS push-pull buffer

For the 3-state push-pull buffer, the I/O pin goes 3-state when executing an INS instruction to that port and remains in 3-state until an OUTS instruction is executed to that port.

Figure 2. Timer and Interrupt Control Port Block Diagram



Timer and Interrupt Control Port
The timer is an 8-bit binary down counter that is software-programmable to operate in one of three modes: interval timer, pulse width measurement, or event counter. As shown in figure 2, an 8-bit register (interrupt control port), a programmable 16-bit prescaler, and an 8-bit modulo-N register are associated with the timer.

The timer mode, prescale value, timer start and stop, active level of the EXT INT pin, and interrupt local enable/disable are selected by the proper bit configuration output from the accumulator to interrupt control port 6 with an OUT or OUTS instruction. Bits within the interrupt control port are defined as follows:

Bit 0 = External interrupt enable
Bit 1 = Timer interrupt enable
Bit 2 = EXT INT active level
Bit 3 = Start/stop timer
Bit 4 = Pulse width/internal timer
Bit 5 = ÷2 Prescaler control
Bit 6 = ÷5 Prescaler control
Bit 7 = ÷20 Prescaler control

Timer

The F38C70 timer, like the F3870, is an 8-bit programmable down counter. However, the F38C70 has two additional 8-bit registers (ports 8 and 9) that can be accessed by output instructions. These registers can be used to generate very long interval timer interrupts or any desired prescaler value.

A special situation exists when reading the interrupt control port with an IN or INS instruction). The accumulator is *not* loaded with the content of the ICP; instead, accumulator bits 0 through 6 are loaded with zeros, and bit 7 is loaded with the logic level being applied to the EXT INT pin. Thus, the status of EXT INT can be determined without needing to service an external interrupt request. This capability is useful in establishing a high-speed polled handshake procedure or for using EXT INT as an extra input pin if external interrupts are not required and the timer is used only in the interval timer mode.

The rate at which the timer is clocked in the interval timer mode is determined by the frequency of an internal Φ clock and by the division value selected for the prescaler. (The internal Φ clock operates at one-half the external time base frequency.) Assuming ports 8 and 9 have been loaded with zeros, if ICP bit 5 is set and bits 6 and 7 are cleared, the prescaler divides Φ by two. In the same manner, if bit 6 or 7 is individually set, the prescaler divides Φ by 5 or 20, respectively. Combinations of bits 5, 6, and 7 may also be selected. For example, if bits 5 and 7 are set, while 6 is cleared, the prescaler will divide by 40. Thus, possible prescaler values are ÷2, ÷5, ÷10, ÷20, ÷40, ÷100, and ÷200. If bits 5, 6, and 7 of the interrupt control port are set, and the contents of either of the two prescaler registers are not zero, the timer uses the value that is held in the two registers as a 16-bit prescaler value.

Any of three conditions will cause the prescaler to be reset:

1. When the timer is stopped by clearing ICP bit 3
2. When an output instruction to port 7 (the timer is assigned Port Address 7) is executed
3. On the trailing edge transition of the EXT INT pin when in the pulse width measurement mode

An OUT or OUTS instruction to port 7 loads the contents of the accumulator to both the timer and the 8-bit modulo-N register, resets the prescaler, and clears any previously stored timer interrupt request. The timer is an 8-bit down-counter clocked by the prescaler in both the interval timer mode and the pulse width measurement mode. The prescaler is not used in the event counter mode. The modulo-N register is used as a buffer in all three timer modes. Its function is to save the value that was most recently output to port 7.

Interval Timer Mode
When ICP bit 4 is cleared (logic 0) and at least one prescale bit is set, the timer operates in the interval timer mode. When bit 3 of the ICP is set, the timer starts counting down from the modulo-N value. After counting down to H'01', the timer returns to the modulo-N value at the next count. On the transition from H'01' to H'N', the timer sets a timer interrupt request latch. Note that the interrupt request latch is set by the transition of H'N' in the timer, thus allowing a full 256 counts if the modulo-N register is preset to H'00'.

If bit 1 of the ICP is set, the interrupt request is passed on to the CPU section of the F38C70. However, if bit 1 of the ICP is a logic 0, the interrupt request is not passed on the the CPU section, although the interrupt request latch remains set. If ICP bit 1 is subsequently set, the interrupt request is then passed on to the CPU section. (The interrupt request is acknowledged by the CPU section only if ICB is set.) Only two events reset the timer interrupt request latch: the timer interrupt request is acknowledged by the CPU section, or a new load of the modulo-N register is performed.

If the modulo-N register is loaded with H'64' (decimal 100), the timer interrupt request latch is set at the 100th count following the timer start and the latch is repeatedly set on precise 100-count intervals. If the prescaler is set at ÷40, the timer interrupt request latch is set every 4000 Φ clock

periods. For a 2-mHz Φ clock (4-mHz time base frequency), this produces 2 ms intervals.

If ports 8 and 9 are loaded with zeros, the range of possible intervals is from 2 to 51,200 Φ clock periods (1 μs to 25.6 ms for a 2-mHz Φ clock). However, approximately 50 Φ periods is a practical minimum, because the time between setting the interrupt request latch and the execution of the first instruction of the interrupt service routine is at least 29 Φ periods (the response time is dependent on how many privileged instructions are encountered when the request occurs).

To establish time intervals greater than 51,200 Φ clock periods, the 16-bit prescaler or the timer interrupt service routine can be used to count the number of interrupts, saving the result in one or more of the scratchpad registers until the desired interval is achieved. Virtually any time interval, or several time intervals, can be generated using this technique.

The timer is read at any time and in any mode, using an input instruction (IN 7 or INS 7), and can take place "on-the-fly" without interfering in normal timer operation. Also, the timer can be stopped at any time by clearing bit 3 of the ICP. The timer holds its current contents indefinitely and resumes counting when bit 3 is set again. The prescaler is reset whenever the timer is stopped; thus, a series of starting and stopping results in a cumulative truncation error.

For a free-running timer in the interval timer mode, the time interval between any two interrupt requests can be in error by ±6 Φ clock periods, although the cumulative error over many intervals is zero. The prescaler and timer generate precise intervals for setting the timer interrupt request latch, but the time out can occur at any time within a machine cycle. (There are two machine cycle types: short, which consist of 4 Φ clock periods, and long, which consist of 6 Φ clock periods.) The Fairchild multi-chip F8 family has a write clock signal that corresponds to a machine cycle. Interrupt requests are synchronized with the internal write clock, thus providing the possible ±6 Φ error. Additional errors may arise if the interrupt request occurs while a privileged instruction or multi-cycle instruction is being executed. Nevertheless, for most applications, all the above errors are negligible, especially if the desired time interval is greater than one ms.

Pulse Width Measurement Mode

When ICP bit 4 is set (logic 1) and at least one prescale bit is set, the timer operates in the pulse width measurement mode. This mode is used to accurately measure the duration of a pulse applied to the EXT INT pin. The timer is stopped and the prescaler is reset whenever EXT INT is at its inactive level. The active level of EXT INT is defined by ICP bit 2: if cleared, EXT INT is active low; if set, EXT INT is active high.

If ICP bit 3 is set, the prescaler and timer start counting when EXT INT transfers to the active level. When EXT INT returns to the inactive level, the timer stops, the prescaler resets, and, if ICP bit 0 is set, an external interrupt request latch is set. (Unlike timer interrupts, external interrupts are not latched if the ICP interrupt enable bit is not set.)

As in the interval timer mode, the timer can be read at any time and can be stopped at any time by clearing ICP bit 3 (the prescaler and ICP bit 1 function as described in the interval timer mode section). The timer still functions as an 8-bit binary down counter with the interrupt request latch set on the timer's transition from H'01' to H'N' (modulo-N value). Note that the EXT INT pin has nothing to do with loading the timer; its action is that of automatically starting and stopping the timer and of generating external interrupts. Pulse widths longer than the prescale value times the modulo-N value are easily measured by using the timer interrupt service routine to store the number of timer interrupts in one or more scratchpad registers.

The actual pulse duration is typically slightly longer than the measured value, because the prescaler status is not readable and is reset when the timer is stopped. Thus, for maximum accuracy, it is advisable to use a small division setting for the prescaler.

Event Counter Mode

When ICP bit 4 is cleared and all prescale bits (ICP bits 5, 6, and 7) are cleared, the timer operates in the event counter mode. This mode is used for counting pulses applied to the EXT INT pin. If ICP bit 3 is set, the timer will decrement on each transition from the inactive level to the active level of the EXT INT pin. The prescaler is not used in this mode. As in the other two timer modes, the timer can be read at any time and can be stopped at any time by clearing ICP bit 3, ICP bit 1 functions as previously described, and the timer interrupt request latch is set on the timer's transition from H'01' to H'N' (modulo-N value).

Normally, ICP bit 0 should be kept cleared in the event counter mode; otherwise, external interrupts are generated on the transition from the inactive level to the active level of the EXT INT pin.

For the event counter mode, the minimum pulse width required on EXT INT is 2 Φ clock periods and the minimum inactive time is 2 Φ clock periods; therefore, the maximum repetition rate is 500 Hz.

External Interrupts

When the timer is in the interval timer mode, the EXT INT pin is available for non-timer related interrupts. If ICP bit 0 is set, an external interrupt request latch is set for a transition from the inactive level to the active level of EXT INT. (The EXT INT signal is an edge-triggered input.) The interrupt request is latched either until acknowledged by the CPU section or until ICP bit 0 is cleared (unlike timer interrupt requests that remain latched even when ICP bit 1 is cleared).

External interrupts are handled in the same fashion when the timer is in the pulse width measurement mode or in the event counter mode, except that when in the pulse width measurement mode, the external interrupt request latch is set on the trailing edge of EXT INT (that is, on the transition from the active level to the inactive level).

Interrupt Handling

When either a timer or an external interrupt request is communicated to the CPU section of the F38C70, it is acknowledged and processed at the completion of the first non-privileged instruction if the interrupt control bit of the status register is set. If the interrupt control bit is not set, the interrupt request continues either until the interrupt control bit is set and the CPU section acknowledges the interrupt or until the interrupt request is cleared (as previously described).

If a timer interrupt request and an external interrupt request occur simultaneously, when the CPU section starts to process the requests, the timer interrupt is handled first.

When an interrupt is allowed, the CPU section requests that the interrupting element pass its interrupt vector address to the program counter through the data bus. The vector address for a timer interrupt is H'020'. The vector address for external interrupts is H'0A0'. After the vector address is passed to the program counter, the CPU section sends an acknowledge signal to the appropriate interrupt request latch, which clears that latch. The interrupt service routine executes; the return address of the original program is automatically stored in stack register P.

Power-On Clear

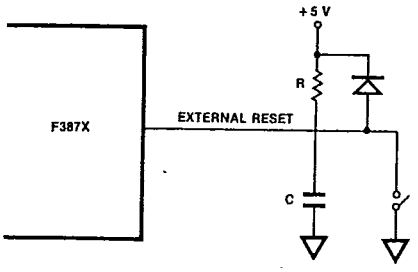
The F38C70 contains power-on clear circuitry to automatically reset the internal logic following the application of external power. Since many variations of power supply circuitry exist, Fairchild cannot guarantee that the power-on clear will operate under every power-up condition.

The power-on clear circuitry contains on-chip sensors to monitor various conditions. The following conditions must be satisfied before the power-reset sequence is allowed to start:

1. Supply voltage must be above a certain value, typically +3 V to +4 V.
2. The clocks of the device must be functioning.
3. The substrate bias must reach a certain level.

All three conditions must be met before the power-on clear circuitry initiates a reset cycle. However, these conditions can be satisfied even with a supply voltage of as low as 3 volts. The latest versions of the F38C70 have a modified delay circuit that gives a typical delay of 500 μs (with a 4 mHz crystal) after the above conditions are met. This is an improvement over the earlier F38C70 versions.

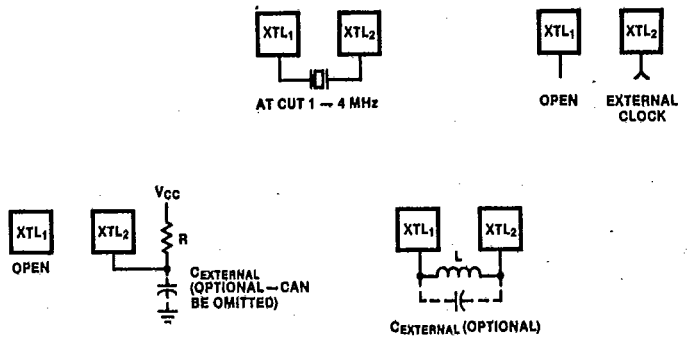
Since the F38C70 is only guaranteed to operate at a supply voltage of 4.5 V or greater, the user must ensure that the supply voltage is at least 4.5 V when the F38C70 initiates the reset cycle. For power supplies having a slow rise time, an external RC network can be converted to the external reset input of the F38C70 to hold the device in a reset state long enough to allow the power supply to reach a voltage of 4.5 V. For example:



External Reset

When the RESET signal is taken low, the contents of the program counter are pushed to the stack register and the program counter and the ICB of the status register are cleared. The original stack register contents are lost. As with power-on clear, ports 4, 5, 6, and 7 are loaded with H'00'. The contents of all other registers and ports are unchanged. When the RESET signal is taken high, the first program instruction is fetched from ROM location H'0000'.

Figure 3 Clock Configurations



Minimum R = 4kΩ

$C = 20.5\ pF \pm 2.5\ pF + C_{EXTERNAL}$

$f_{MIN} \cong \frac{1}{1.1\,RC + 65\ ns}$

$f_{MAX} \cong \frac{1}{1.0\,RC + 15\ ns}$

Example with $C_{EXTERNAL} = 0$

$R = 15\ k\Omega \pm 5\%$

$f \cong 2.9\ MHz \pm 26\%$

Minimum L = 0.1 mH

Minimum Q = 40

Maximum $C_{EXTERNAL} = 30\ pF$

$f \cong 3.0\ MHz \pm 10\%$

$C = 10\ pF \pm 1.3\ pF + C_{EXTERNAL}$

$f \cong \frac{1}{2\pi\sqrt{LC}}$

Example with $C_{EXTERNAL} = 0$

$L = 0.3\ mH \pm 10\%$

Test Logic

Special test logic is implemented to allow access to the internal main data bus for test purposes. In normal operation, the TEST pin must be connected to ground. When the TEST signal is set to V_{DD}, port 4 becomes an output of the internal data bus and port 5 becomes a wired-OR input to the internal data bus. The data appearing on the port 4 pins is logically true, whereas input data forced on port 5 must be logically false. When the TEST signal is set to one-half the level of V_{CC} ($V_{CC}/2$), the ports act as above and the 2K X 8 program ROM is prevented from driving the data bus. In this mode, operands and instructions are forced externally through port 5 instead of being accessed from the program ROM. When the TEST signal is in either the $V_{DD}/2$ or the high state, the STROBE signal ceases its normal function and becomes a cycle clock (identical to the F8 multi-chip system write clock, except inverted).

The TEST pin capabilities are impractical for user applications because of timing complexities; however these capabilities are sufficient to enable Fairchild to implement rapid methods for thoroughly testing the F38C70.

Clocks

The time bases for the F38C70 originate from one of four external sources by mask options. These four configurations are illustrated in figure 3. External capacitors are not required. In all external clock modes, the external time base frequency is divided by two to form the internal Φ clock. The selection of clock configurations is by mask options.

Figure 4 F38C70 Programmable Registers and Ports

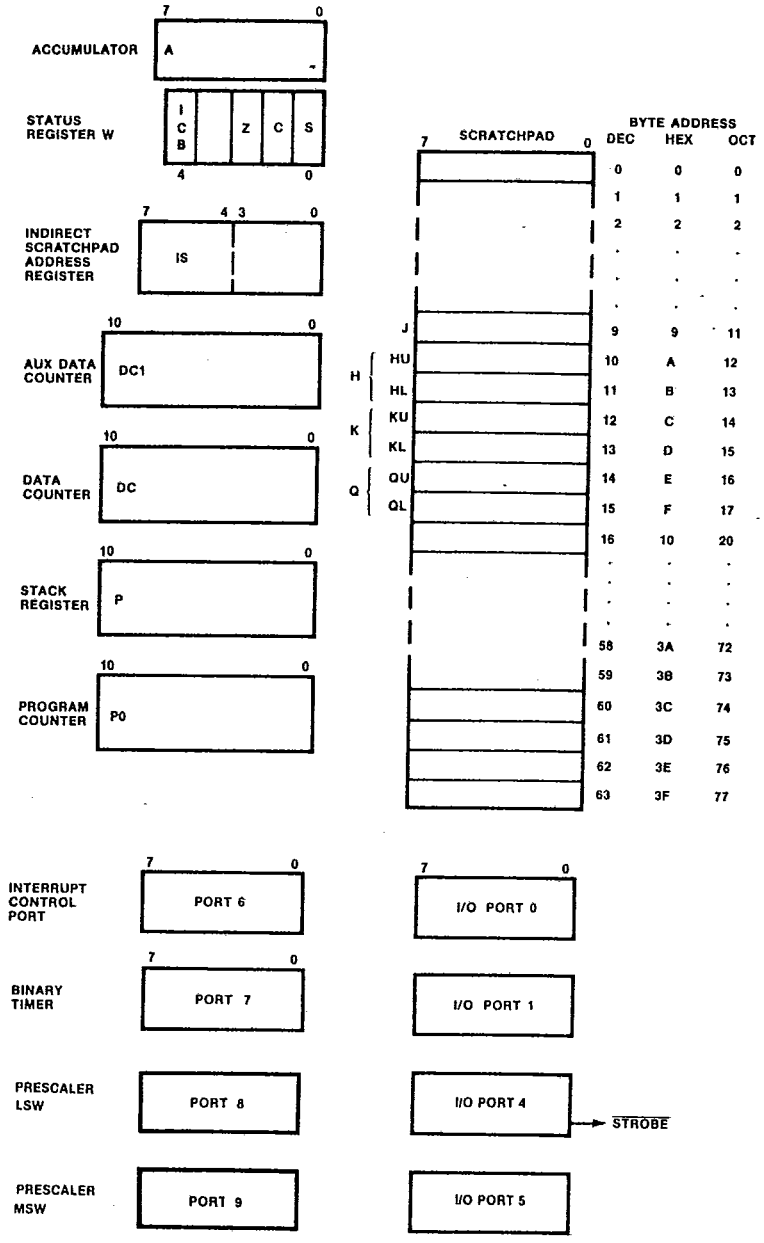


Figure 5 PS Instruction

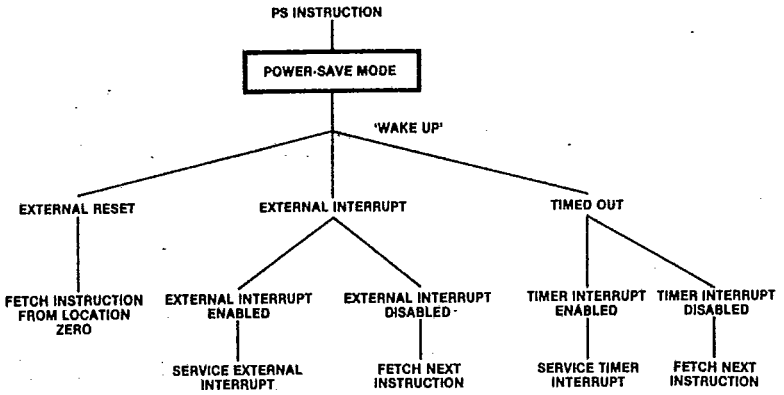
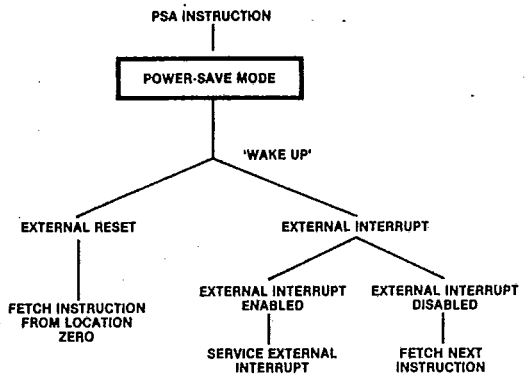


Figure 6 PSA Instruction



Instruction Set

The F38C70 executes the entire instruction set of the F3870 family. In addition, two instructions exclusive to the F38C70 allow the F38C70 to further reduce its power consumption by entering into one of two power-save modes.

A summary of programmable registers and ports is shown in *Figure 4*. *Table 1* lists the F38C70 instruction set and F8-compatible instructions.

Power-Save Mode

When the power-save instruction (mnemonic PS, OP code 2D) is executed, the F38C70 halts all its operations except the timer and interrupts. The microcomputer is returned to the operating status by an external reset, an external interrupt, or a timer interrupt (as the timer is timed out).

Power-Save All Mode

When the power-save all instruction (mnemonic PSA, Op code 2F) is executed, the F38C70 halts all its operations and goes into a power-save mode (refer to Figures 5 and 6). The microcomputer is returned to the previous operating status by an external reset or an external interrupt. Both the timer and prescaler are reset when PSA is executed, except in the event counter mode.

In returning from either power-save mode, the microcomputer exercises the interrupt routine or continues with the next instruction, depending on whether the interrupt is enabled.

If the return is by an external reset, the microcomputer restarts from the reset mode.

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Table 1 F38C70 Instruction Set and F8-Compatible Instructions

Accumulator Group Instructions

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF	Zero	CRY	Sign
Add Carry	LNK		ACC ← (ACC) + CRY	19	1	1	1/0	1/0	1/0	1/0
Add Immediate	AI	ii	ACC ← (ACC) H 'ii'	24ii	2	2.5	1/0	1/0	1/0	1/0
And Immediate	NI	ii	ACC → (ACC) H 'ii'	21ii	2	2.5	0	1/0	0	1/0
Clear	CLR		ACC → H'00'	70	1	1				
Compare Immediate	CI	ii	H 'ii'	25ii	2	2.5	1/0	1/0	1/0	1/0
Complement	COM		ACC → (ACC) ⊕H'FF'	18	1	1	0	1/0	0	1/0
Exclusive or Immediate	XI	ii	ACC → (ACC) ⊕ H ii	23 ii	2	2.5	0	1/0	0	1/0
Increment	INC		ACC → (ACC) + 1	1F	1	1	1/0	1/0	1/0	1/0
Load Immediate	LI	ii	ACC → H 'ii'	20 ii	2	2.5	—	—	—	—
Load Immediate Short	LIS	i	ACC → H'0i'	7i	1	1	—	—	—	—
Or Immediate	OI	ii	ACC → (ACC) V H 'ii'	22ii	2	2.5	0	1/0	0	1/0
Shift Left One	SL	1	Shift Left 1	13	1	1	0	1/0	0	1/0
Shift Left Four	SL	4	Shift Left 4	15	1	1	0	1/0	0	1/0
Shift Right One	SR	1	Shift Right 1	12	1	1	0	1/0	0	1/0
Shift Right Four	SR	4	Shift Right 4	14	1	1	0	1/0	0	1/0

Table 1 F38C70 Instruction Set and F8-Compatible Instructions (Continued)

Branch Instructions (In all conditional branches, PO (PO) + 2 if the test conditions are not met. Execution is complete in 30 cycles.)

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF Zero CRY Sign
Branch on Carry	BC	aa	PO ← [(PO) + 1] + H'aa' if CRY = 1	82 aa	2	3.5	— — — —
Branch on Positive	BP	aa	PO→ [(PO) + 1] + H'aa' if	81aa	2	3.5	— — — —
Branch on Zero	BZ	aa	PO → [(PO) + 1] + H'aa' if Zero = 1	84aa	2	3.5	— — — —
Branch on True	BT	t,aa	PO ← [(PO) + 1] + H'aa' if any test is true	8t aa	2	3.5	— — — —

1 - TEST CONDITION

2^2	2^1	2^0
ZERO	CRY	SIGN

Branch if Negative	BM	aa	PO ← [(PO) + 1] + H'aa' if Sign = 0	91aa	2	3.5	— — — —
Branch if No Carry	BNC	aa	PO ← [(PO) + 1] + H'aa' if Carry ≠ 0	92 aa	2	3.5	— — — —
Branch if No Overflow	BNO	aa	PO ← [(PO)i + 1] + H'aa' if OVF = 0	98 aa	2	3.5	— — — —
Branch if Not Zero	BNZ	aa	PO ← [(PO) + 1] + H'aa' if Zero = 0	94 aa	2	3.5	— — — —
Branch if False Test	BF	t.aa	PO ← [(PO) + 1] + H'aa' if all false test bits	9t aa	2	3.5	— — — —

1 = TEST CONDITION

2^3	2^2	2^1	2^0
OVF	ZERO	CRY	SIGN

Branch If ISAR(Lower)7	BR7	aa	PO← [(PO)+1]+H'aa' If ISARL ≅ 7	8Faa	2	2.5	— — — —
			PO ← (PO) + 2 if ISARL = 7	2.0	— —	— —	
Branch Relative	BR	aa	PO ← [(PO) + 1] + H'aa'	90 aa	2	3.5	— — — —
Jump*	JMP	aaaa	PO ← H'aaa'	29 aaa	3	5.5	— — — —

* Privileged Instruction

Note
JMP and P1 change accumulator contents to the high byte address.

Table 1 F38C70 Instruction Set and F8-Compatible Instructions (Continued)

Memory Reference Instructions (In all memory reference instructions, the data counter is incremented DC←DC — 1.)

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF Zero CRY Sign
Add Binary	AM		ACC←(ACC) + [(DC)]	88	1	2.5	1/0 1/0 1/0 1/0
Add Decimal	AMD		ACC←(ACC) + [(DC)]	89	1	2.5	1/0 1/0 1/0 1/0
AND	NM		ACC←(ACC)∧[(DC)]	8A	1	2.5	0 1/0 0 1/0
COMPARE	CM		[(DC)] + (ACC) + 1	8D	1	2.5	1/0 1/0 1/0 1/0
EXCLUSIVE OR	XM		ACC←(ACC) ⊕ [(DC)]	8C	1	2.5	0 1/0 0 1/0
LOAD	LM		ACC←[(DC)]	16	1	2.5	— — — —
LOGICAL OR	OM		ACC←(ACC) ∨[(DC)]	8B	1	2.5	0 1/0 0 1/0
STORE	ST		(DC)←(ACC)	17	1	2.5	— — — —

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Address Register Group Instructions

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF Zero CRY Sign
Add to Data Counter	ADC		DC←(DC) + (ACC)	8E	1	2.5	— — — —
Call to Subroutine	PK		P←(PO)ΦPOU←(r12)+ PL←(r13)	DC	1	4	— — — —
Call to Subroutine Immediate	PI	aaaa	P←(P)PO←H'aaaa' ‡	28aaaa	3	6.5	— — — —
Exchange DC	XDC		DC‡DC1	2C	1	2	— — — —
Load Data Counter	LR	DC,Q	DCU←(r14), DCL←(r15)	0F	1	4	— — — —
Load Data Counter	LR	DC,H	DCU←(r10), DCL←(r11)	10	1	4	— — — —
Load DC Immediate	DCI	aaaa	DC←H'aaaa'	2Aaaaa	3	6	— — — —
Load Program Counter	LR	PO,Q	POU←(r14), POL←(r15)	0D	1	4	— — — —
Load Stack Register	LR	P,K	PU←(r12), PL←(r13)	09	1	4	— — — —
Return From Subroutine	POP		PO\P	1C	1	2	— — — —
Store Data Counter	LR	Q,DC	r14←(DCU), r15←(DCL)	0E	1	4	— — — —
Store Data Counter	LR	H,DC	r10←(DCU), r11←(DCL)	11	1	4	— — — —
Store Stack Register	LR	K,P	r12←(PU), r13←P	08	1	4	— — — —

Table 1 F38C70 Instruction Set and F8-Compatible Instructions (Continued)

Scratchpad Register Instructions (refer to scratchpad addressing modes.)

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF Zero CRY Sign
Add Binary	AS	r	ACC(ACC) + (r)	Cr	1	1	1/0 1/0 1/0 1/0
Add Decimal	ASD	r	ACC←(ACC) + (r)	Dr	1	2	1/0 1/0 1/0 1/0
Decrement	DS	r	r←(r) + H'FF'	3r	1	1.5	1/0 1/0 1/0 1/0
Load	LR	A,r	ACC←(r)	4r	1	1	— — — —
Load	LR	A,KU	AC←(r12)	00	1	1	— — — —
Load	LR	A,KL	ACC←(r13)	01	1	1	— — — —
Load	LR	A,QU	ACC←(r14)	02	1	1	— — — —
Load	LR	A,QL	ACC←(r15)	03	1	1	— — — —
Load	LR	r,A	r←(ACC)	5r	1	1	— — — —
Load	LR	KU,A	r12←(ACC)	04	1	1	— — — —
Load	LR	KL,A	r13←(ACC)	05	1	1	— — — —
Load	LR	QU,A	r14←(ACC)	06	1	1	— — — —
Load	LR	QL,A	r15←(ACC)	07	1	1	— — — —
And	NS	r	ACC←(ACC)∧(r)	Fr	1	1	0 1/0 0 1/0
Exclusive Or	XS	r	ACC←(ACC)⊕(r)	Er	1	1	0 1/0 0 1/0

Table 1 F38C70 Instruction Set and F8-Compatible Instructions (Continued)

Miscellaneous Instructions

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF	Zero	CRY	Sign
Disable Interrupt	DI		Reset ICB	1A	1	2	—	—	—	—
Enable Interrupt*	EI		SET ICB	1B	1	2	—	—	—	—
Input	IN	aa	ACC ← (Input PORT aa)	26aa	2	4	0	1/0	0	1/0
Input Short	INS	a	ACC ← (Input PORT a)	Aa	1	4***	0	1/0	0	1/0
Load ISAR	LR	IS.A	ISAR ← (ACC)	0B	1	1	—	—	—	—
Load ISAR Lower	LISL	a	ISARL ← a	01101a**	1	1	—	—	—	—
Load ISAR Upper	LISU	a	ISARU ← a	01100**	1	1	—	—	—	—
Load statusregister	LR	W,J	W ← (r9)	1D	1	2	1/0	1/0	1/0	1/0
No-Operation	Nop		P0 ← (P0) + 1	2B	1	1	—	—	—	—
OUTPUT	OUT	aa	OUTPUT PORT aa ← (ACC)	27 aa	2	4	—	—	—	—
OUTPUT Short	OUTS	a	OUTPUT PORT a ← (ACC)	Ba	1	4***	—	—	—	—
Store ISAR	LR	A.15	ACC ← (ISAR)	0A	1	1	—	—	—	—
Store Status Reg	LR	J,W	r9 ← (W)	1E	1	1	—	—	—	—
Power Save	PS		Halt Internal Clock	2D	1	3	—	—	—	—
Power Save All	PSA		Halt Internal Clock and Timer	2F	1	3	—	—	—	—

*Privileged instruction
**3-bit octal digit
***Two machine cycles for CPU ports

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Notes
Each lower case character represents a hexadecimal digit.
Each cycle equals four machine clock periods.
Lower case denotes variables specified by programmer.

Function definitions

←	is replaced by
( )	the contents of
(-)	binary ones complement of
+	arithmetic add (binary or decimal)
•	logical OR exclusive
	logical AND
	logical OR inclusive
H'#	hexadecimal digit

Register Names

a	address variable
	A accumulator
DC	data counter (indirect address register)
DCI	data counter #1 (auxiliary data counter)
DCL	least significant eight bits of data counter addressed
DCU	most significant eight bits of data counter addressed
H	scratchpad register #10 and #11
I and II	immediate operand
ICB	interrupt control bit
IS	indirect scratchpad address register
ISAR	indirect scratchpad address register
ISARL	least significant three bits of ISAR
ISARU	most significant three bits of ISAR
J	scratchpad register #
K	registers #12 and #13
KL	register #13
KU	register #12
P0	program counter
P0L	least significant eight bits of program counter
P0U	most significant eight bits of program counter
P	stack register
PL	least significant eight bits of program counter
PU	most significant eight bits of active stack register
Q	registers #14 and #15
QL	register #15
QU	register #14
r	scratchpad/register (any address through 11)
W	status register

Scratchpad Addressing Modes (Machine Code Format)

r = C	(hexadecimal) register addressed by ISAR (unmodified)
r = D	(hexadecimal) register addressed by ISAR, ISARL incremented
r = E	(hexadecimal) Register addressed by ISAR, ISARL decremented
r = F	(no operation performed)
r = 0-B	(hexadecimal) register 0 through 11 addressed directly from the instruction

Status Register

.	no change in condition
1/10	is set to 1 or 0 depending on conditions
CRY	carry flag

Supplementary Notes

The interrupt control bit of the status register is automatically reset when an interrupt request is acknowledged. It is then the programmer's responsibility to determine when ICB will again be set (by executing an EI instruction). This action prevents an interrupt service routine from being interrupted, unless the programmer so desires.

When reading the interrupt control port (port 6), bit 7 of the accumulator 1, loaded with the actual logic level being applied to the EXT INT pin, regardless of the status of ICP bit 2 (the EXT INT active level bit); that is, if EXT INT is at +5 V, bit 7 of the accumulator is set to a logic 1, but if EXT INT is at V_{SS}, the accumulator bit 7 is reset to logic 0.

In the instruction set summary (table 1), the number of cycles shown are nominal machine cycles. A nominal cycle is defined as 4 Φ clock periods, thus requiring 2 μs for a 2-mHz clock frequency (4-mHz external time base frequency). When desired, the long machine cycles can be altered to short machine cycles by mask option.

The following nomenclature for register names is used for consistency with the assembly language mnemonics:

F8	F38C70	Register
PC_0	PO	program counter
PC_1	P	stack register
DC_0	DC	data counter
DC_1	DC1	auxiliary data counter

For the F38C70, execution of an INS or OUTS instruction requires two machine cycles for ports 0 and 1, whereas ports 4 an 5 require four machine cycles. When an external reset of the F38C70 occurs, PO is stored in P and the old contents of P are lost. Note that an external reset is recognized at the start of the machine cycle and not necessarily at the end of an instruction. Thus, if the F38C70 is executing a multi-cycle instruction, that instruction is not completed, and the contents of P, upon reset, may not necessarily be the address of the instruction that would have been executed next. They may, for example, point to an immediate operand, if the reset occurred during the second cycle of an LI or CI instruction. Additionally, several instructions (JMP, PI, PK, LR, PO, Q) as well as the interrupt acknowledge sequence, modify PO in parts. That is, they alter PO by first loading one part, then the other part, and the entire operation takes more than one cycle. Should reset occur during this modification process, the value stored in P becomes part of the old PO (the not yet modified part), and part of the new PO (already modified part). Thus, care should be taken (perhaps by external gating) to ensure that reset does not occur at an undesirable time, if any significance is to be given to the contents of P after a reset occurs.

If desired, the F38C70 can execute all instructions in short cycles via mask options to improve the execution speed of the device.

Signal Descriptions

The F38C70 input and output signals are described in Table 2.

Table 2 F38C70 Signal Descriptions

Mnemonic	Pin No.	Name	Description
Clock			
XTL_1 XTL_2	1	Clock	The time base inputs to which a crystal (1 to 4 mHz), LC network, RC network, or an external single-phase clock is connected.
I/O Ports			
$\overline{PO}_0 - \overline{PO}_7$	3, 4, 5, 6, 19, 18 17, 16	Port Address	The 32 ports are individually used as either TTL-compatible inputs or as latched outputs.
$\overline{P1}_0 - \overline{PO}_7$	37, 36, 35, 34, 22, 23, 24, 25	Port Address	
$\overline{P4}_0 - \overline{P4}_7$	8, 9, 10, 11, 12, 13, 14, 15,	I/O Port	
$\overline{P5}_0 - \overline{P5}_7$	33, 32, 31, 30, 29, 28, 27, 26	I/O Port	
Interrupt/Reset			
EXT INT	38	External Interrupt	The active state of the external interrupt signal is software programmable; it is also used in conjunction with the timer for pulse width measurement and event counting.
RESET	39	Reset	This input signal is used to reset the F38C70 externally. When the signal is allowed to go low, the F38C70 resets. When subsequently allowed to go high, the F38C70 begins program execution at location H'0000'.
Strobe			
$\overline{STROBE}$	7	Strobe	This output pin, which is normally high, provides a single low pulse after valid data is present on the $P4_0 - P4_7$ pins during an output instruction.
Test			
TEST	21	Test	An input signal used only in testing the F38C70. For normal circuit function, this pin must be connected to ground.
Power			
V_{SS}	20	Ground	Common power and signal return
V_{CC}	40	Power Supply	Power supply input signal, +5 (±10%) V

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DC Characteristics

The characteristics of the F38C70 are provided in table 3.

Table 3 F38C70 DC Charateristics $T_A = 0°$ to 70°C, $V_{CC} = 5V \pm 10\%$, I/O Power Dissipation ≤ mW

Symbol	Parameter	Min	Max	Unit	Test Conditions
I_{CC}	Power Supply Current		TBD	mA	Outputs Open
P_D	Power Dissipation		TBD	mW	Outputs Open
V_{IHEX}	External Clock Input High Voltage	2.4	5.8	V	
V_{ILHEX}	External Clock Input Low Voltage	−0.3	0.6	V	
I_{HEX}	External Clock Input High Current		100	μA	V_{IHEX} = 2.4 V
I_{LEX}	External Clock Input Low Current		−100	μA	V_{ILEX} = 0.6 V
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{IL}	Input Low Voltage	−0.3	0.8	V	
I_{IH}	Input High Current (except 3-state option)		100	μA	V_{IH} = 2.4 V, internal pull-up
I_{IL}	Input Low Current (except open drain and direct drive ports)		−1.6	mA	V_{IL} = 0.4 V
I_{LOD}	Leakage Current		±10	μA	$0 \leq V_{IN} \leq V_{CC}$
I_{OH}	Output High Current (except open drain and direct drive ports) std.	−100		μA	V_{OH} = 2.4 V
I_{OHDD}	Output Drive Current (push-pull)	−1.5	TBD	mA	V_{OH} = 0.7 V to 1.5 V
I_{OL}	Output Low Current	1.8		mA	V_{OL} = 0.4 V
I_{OHS}	Output High Current (STROBE Output)	−300		μA	V_{OH} = 2.4 V
I_{OLS}	Output Low Current (STROBE Output)	5.0		mA	V_{OL} = 0.4 V

Absolute Maximum Ratings

These are stress ratings only, and functional operation at these ratings, or under any conditions above those indicated in this data sheet, is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect device reliability, and exposure to stresses greater than those listed may cause permanent damage to the device.

Temperature (Ambient) Under Bias	0°C, +70°C
Storage Temperature	−55°C, +150°C
Voltage on Any Pin with Respect to Ground (Except Open Drain Pins)	−0.3 V, V_{CC} + 0.3 V
Power Dissipation	1 W

Ordering Information

Part Number	Temperature Package	Range*
F38C70DC	Ceramic	C
F38C70DL	Ceramic	L
F38C70DM	Ceramic	M
F38C70PC	Plastic	C
F38C70PL	Plastic	L
F38C70PM	Plastic	M

*C = Commercial Temperature Range 0°C to +70°C
L = Limited Temperature Range −40°C to +85°C
M = Military Temperature Range −55°C to + 125°C