Flash

3.3V 1 Gbit SPI-NAND Flash Memory

PRODUCT LIST

Parameters	Values
V_{CC}	3.3V
Width	x1, x2[1], x4
Frequency	104MHz
Internal ECC Correction	1 bit
Power-up Ready Time	1ms (maximum value)
Max Reset Busy Time	1ms (maximum value)

Note: 1. x2 PROGRAM operation is not defined.

FEATURES

- Voltage Supply: 3.3V (2.7V~3.6V)
- Organization
  - Memory Cell Array: (128M + 4M) x 8bit
  - Data Register: (2K + 64) x 8bit
- Automatic Program and Erase
  - Page Program: (2K + 64) Byte
  - Block Erase: (128K + 4K) Byte
- Page Read Operation
  - Page Size: (2K + 64) Byte
  - Read from Cell to Register with Internal ECC: 100us
- Memory Cell: 1bit/Memory Cell
- Support SPI-Mode 0 and SPI-Mode 3[1]
- Fast Write Cycle Time
  - Program time: 400us
  - Block Erase time: 4ms
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating Gate Technology
  - Internal ECC Requirement: 1bit/512Byte
  - Endurance: 100K Program/Erase cycles
  - Data Retention: 10 years
- Command Register Operation
- NOP: 4 cycles
- OTP Operation
- Bad-Block-Protect
- Read parameter page operation
- One Time Program (OTP) Operation
- Read Unique ID
- CASN page supported

Note: 1. Mode 0: CPOL = 0, CPHA = 0; Mode 3: CPOL = 1, CPHA = 1

ORDERING INFORMATION

Product ID	Speed	Package		Comments
F50L1G41LC-104YIG2P	104MHz	8-contact WSON	8x6mm	Pb-free
F50L1G41LC-104WIG2P			6x5mm	

GENERAL DESCRIPTION

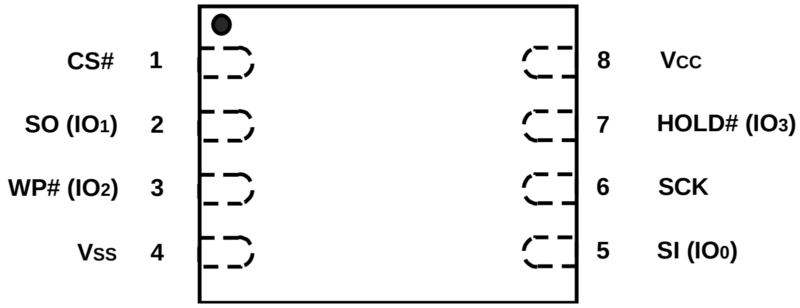
Serial peripheral interface (SPI) NAND is an SLC NAND Flash memory device that provides a cost-effective nonvolatile memory storage solution where pin count must be kept to a minimum. It is also an alternative solution to SPI NOR, offering superior writes performance and cost per bit over SPI NOR. The hardware interface creates a low pincount device with a standard pinout that remains the same from one density to another and supports future upgrades to higher densities without board redesign.
The serial electrical interface follows the industry-standard serial peripheral interface.
New command protocols and registers are defined for SPI operation. The command set resembles common SPI-NOR command sets, modified to handle NAND specific functions and additional new features.

New features include user-selectable internal ECC and first page auto-load on power-up. SPI NAND Flash devices have six signal lines plus V_{CC} and ground (GND). The signal lines are SCK (serial clock), SI, SO (for command/response and data input/output), and control signals CS, HOLD#, WP#. This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, supporting future upgrades to higher densities without board redesign.

Each block of the serial NAND Flash device is divided into 64 programmable pages, each page consisting of 2112 bytes. Each page is further divided into a 2048-byte data storage region and a 64-byte spare area. The 64-byte area is typically used for memory and error management functions.
With internal ECC enabled as the default after power on, ECC code is generated internally when a page is written to the memory core. The ECC code is stored in the spare area of each page. When a page is read to the cache register, the ECC code is calculated again and compared with the stored value. Errors are corrected if necessary. The device either outputs corrected data or returns an ECC error status.
The first block is valid when shipped from factory. Security functions are also provided including software block protection: Lock tight and hardware protection modes avoid array data corruption.

PIN CONFIGURATION (TOP VIEW)

8-Contact WSON

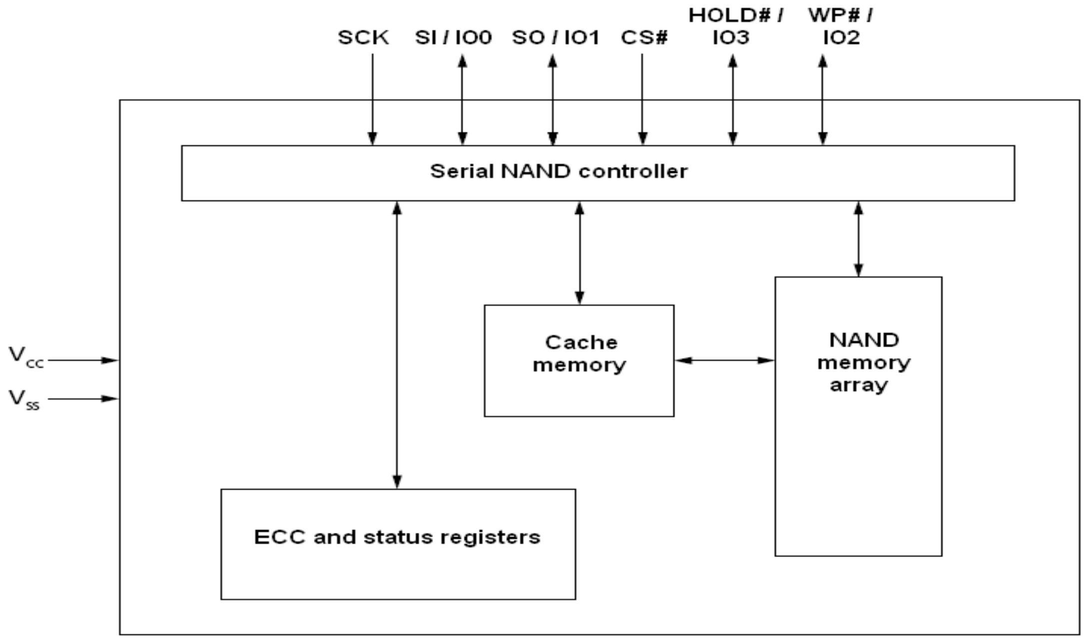


Pin Description

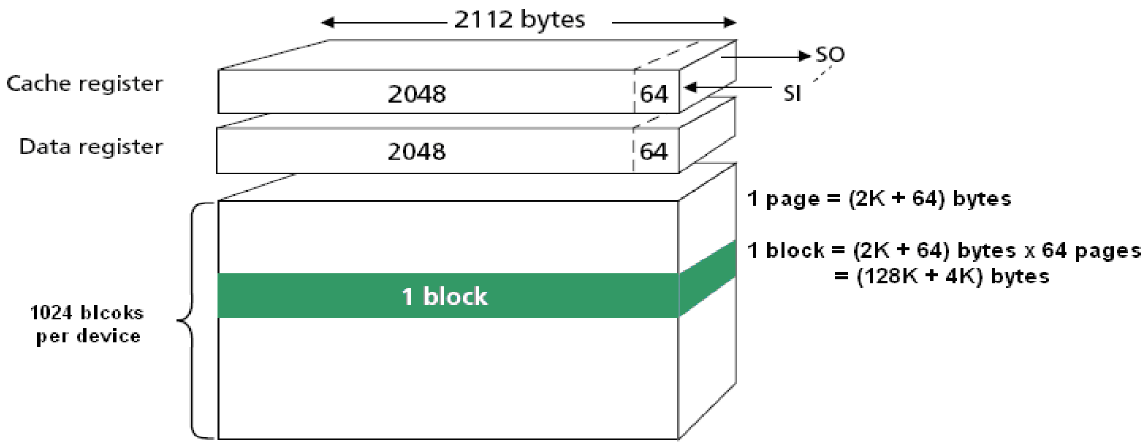
Pin Name	Functions
CS#	**Chip Select (Input)** The device is activated[1]/deactivated[2] as CS# is driven LOW/HIGH. After power-on, the device requires a falling-edge on CS# before any command can be written. The device goes to standby mode when no PROGRAM, ERASE, or WRITE STATUS REGISTER operation is in progress.
HOLD# / IO_3	**Hold (Input) / IO_3 (Input/Output)** Hold pauses any serial communication with the device without deselecting it [3]. When driven LOW, SO is at high impedance (Hi-Z), and all inputs in SI and SCK are ignored; CS# also should be driven LOW. HOLD# must not be driven during x4 operation; it means HOLD function is only available for standard and x2 SPI.
WP# / IO_2	**Write Protect (Input) / IO_2 (Input/Output)** WP# is driven LOW to prevent writing the Feature Registers. The WP-E bit in Protection Register controls the function of WP#, and the other bits in Register can protect a specific portion by hardware. When WP-E=1, the device is in the Hardware-protection mode that WP# functions as a dedicated active low input pin for the Write Protect of the device. If WP-E=1 and WP# goes LOW, the device will become READ-only. When WP-E=0, the device is in the Software-protection mode that only Protection Register can be protected. WP# functions as a data I/O pin. WP# must not be driven during x4 operation; it means Write Protect function is only available for standard and x2 SPI.
SCK	**Serial Clock (Input)** SCK provides serial interface timing. Address, commands, and data in SI are latched on the rising edge of SCK. Output (data in SO) is triggered after the falling-edge of SCK. The clock is valid only when the device is active.[4]
SI / IO_0	**Serial Data Input (Input) / IO_0 (Input/Output)** SI transfers data serially into the device. Device latches addresses, commands, and program data in SI on the rising-edge of SCK. SI must not be driven during x2 or x4 READ operation.
SO / IO_1	**Serial Data Output (Output) / IO_1 (Input/Output)** SO transfers data serially out of the device on the falling-edge of SCK. SO must not be driven during x2 or x4 PROGRAM operation.
V_{CC} [5]	**Power** V_{CC} is the power supply for device.
V_{SS} [5]	**Ground**
NC	**No Connection** Not internally connected.

Note:
1. CS# places the device in active power mode.
2. CS# deselects the device and places SO at high impedance.
3. It means HOLD# input doesn't terminate any READ, PROGRAM, or ERASE operation currently in progress.
4. SI and SO can be triggered only when the clock is valid.
5. Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs. Do not leave V_{CC} or V_{SS} disconnected.

BLOCK DIAGRAM



ARRAY ORGANIZATION



Array Address

Data Bits	0	1	2	3	4	5	6	7	Address
1st byte	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	Column Address
2nd byte	A_8	A_9	A_{10}	A_{11}	X	X	X	X	Column Address
3rd byte	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	Row Address
4th byte	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	Row Address
5th byte	X	X	X	X	X	X	X	X	Dummy Address

Note:
1. Column Address: Starting Address of the Register.
2. X = don't care.
3. The device ignores any additional input of address cycles than required.

COMMAND SET

Function	Op Code	Address Byte	Dummy Byte	Data Bytes
BLOCK ERASE	D8h	3	0	0
GET FEATURE [(1)]	0Fh	1	0	1
SET FEATURE	1Fh	1	0	1
WRITE DISABLE	04h	0	0	0
WRITE ENABLE	06h	0	0	0
PROGRAM LOAD	02h	2	0	1 to 2112
PROGRAM LOAD x4 [(2)]	32h	2	0	1 to 2112
PROGRAM LOAD RANDOM DATA	84h	2	0	1 to 2112
PROGRAM LOAD RANDOM DATA x4 [(2)]	34h	2	0	1 to 2112
PROGRAM EXECUTE	10h	3	0	0
PAGE READ	13h	3	0	0
READ FROM CACHE	03h, 0Bh	2	1	1 to 2112
READ FROM CACHE with 4Byte Address	0Ch	2	3	1 to 2112
READ FROM CACHE x2	3Bh	2	1	1 to 2112
READ FROM CACHE x2 with 4Byte Address	3Ch	2	3	1 to 2112
READ FROM CACHE x4 [(2)]	6Bh	2	1	1 to 2112
READ FROM CACHE x4 with 4Byte Address [(2)]	6Ch	2	3	1 to 2112
FAST READ X2 IO	BBh	2	1	1 to 2112
FAST READ X2 IO with 4Byte Address	BCh	2	3	1 to 2112
FAST READ X4 IO	EBh	2	2	1 to 2112
FAST READ X4 IO with 4Byte Address	ECh	2	5	1 to 2112
READ ID [(3)]	9Fh	0	1	2
RESET	FFh	0	0	0

Note:
1. Refer to Feature Register.
2. Command/Address is 1-bit input per clock period, data is 4-bit input/output per clock period.
3. Address is 00h to get JEDEC ID

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{CC}	-0.6 to +4.6	V
	V_{IN}	-0.6 to +4.6	
	$V_{I/O}$	-0.6 to V_{CC} + 0.3 (< 4.6)	
Temperature Under Bias	T_{BIAS}	-40 to +125	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Short Circuit Current	I_{OS}	5	mA

Note:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

(Voltage reference to GND, T_A = -40 to 85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC and Operation Conditions

(Recommended operating conditions otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.[2]	Max.	Unit
Operating Current	Page Read with Serial Access	I_{CC1}	CS#=V_{IL}, I_{OUT}=0mA	-	16	20	mA
	Program	I_{CC2}	-	-	16		
	Erase	I_{CC3}	-	-	16		
Stand-by Current (TTL)		I_{SB1}	CS#=V_{IH}, WP#=0V/V_{CC}	-	-	1	mA
Stand-by Current (CMOS)		I_{SB2}	CS#= V_{CC} -0.2, WP#=0V/ V_{CC}	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to V_{CC} (max)	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to V_{CC} (max)	-	-	±10	uA
Input High Voltage		V_{IH}[1]	-	0.8 x V_{CC}	-	V_{CC} +0.3	V
Input Low Voltage, All inputs		V_{IL}[1]	-	-0.3	-	0.2 x V_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH}=-20uA	0.7 x V_{CC}	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL}=1mA	-	-	0.15 x V_{CC}	V

Note:
1. V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to V_{CC}+0.4V for durations of 20ns or less.
2. Typical value are measured at V_{CC} =3.3V, T_A=25℃. Not 100% tested.

Valid Block and Error Management

Description	Requirement
Minimum / Maximum number of valid block number of block	1004 / 1024
Bad block mark	Non FFh
Mark location	Column 2048 of page 0 and page 1

Note:

1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

AC Test Condition

(T_A=-40 to 85℃, V_{CC}=2.7V~3.6V)

Parameter	Condition
Input Pulse Levels	0.2V_{CC} to 0.8V_{CC}
Input Rise and Fall Times	Max: 2.4ns
Input and Output Timing Levels	V_{CC} /2
Output Load	1 TTL Gate and C_L=30pF

Capacitance

(T_A=25℃, V_{CC}=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL} = 0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	8	pF

Note: Capacitance is periodically sampled and not 100% tested.

Read / Program / Erase Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Average Program Time with ECC ON	t_{PROG}	-	400	900	us
Number of Partial Program Cycles in the Same Page	NOP	-	-	4	Cycle
Block Erase Time	t_{BERS}	-	4	10	ms
Read Page Time with ECC ON	t_{RD}	-	-	100	us
Power-on reset time from Vcc Min	t_{POR}	-	-	1	Ms
Write inhibit voltage	V_{WI}	-	-	2.5	V

General Timing Characteristic

Parameter	Symbol	Min.	Max.
Clock frequency	f_C		104MHz
Hold# non-active hold time relative to SCK	t_{CD}	4.5ns	
Hold# hold time relative to SCK	t_{CH}	4.5ns	
Command deselect time	t_{CS}	80ns	
CS# Setup Time	t_{CSS}	5ns	
CS# Hold Time	t_{CSH}	5ns	
The last valid Clock low to CS# high	t_{CSCL}	5ns	
Output disable time	t_{DIS}		20ns
Hold# non-active setup time relative to SCK	t_{HC}	4.5ns	
Hold# setup time relative to SCK	t_{HD}	4.5ns	
Data input setup time	t_{SUDAT}	2ns	
Data input hold time	t_{HDDAT}	3ns	
Output hold time	t_{HO}	1.5ns	
Hold# to output Hi-Z	t_{HZ}		7ns
Hold# to output Low-Z	t_{LZ}		7ns
Clock low to output valid	t_V		8ns
Clock high time	t_{WH}	4ns	
Clock low time	t_{WL}	4ns	
Clock rise time (slew rate)	t_{CRT}	0.1V/ns	
Clock fall time (slew rate)	t_{CFT}	0.1V/ns	
WP# setup time	t_{WPS}	20ns	
WP# hold time	t_{WPH}	100ns	
Resetting time during Idle/Read/Program/Erase	t_{RST}		5/5/10/500us

Note:
1. For first RESET condition after power up, t_{RST} will be 1ms MAX.

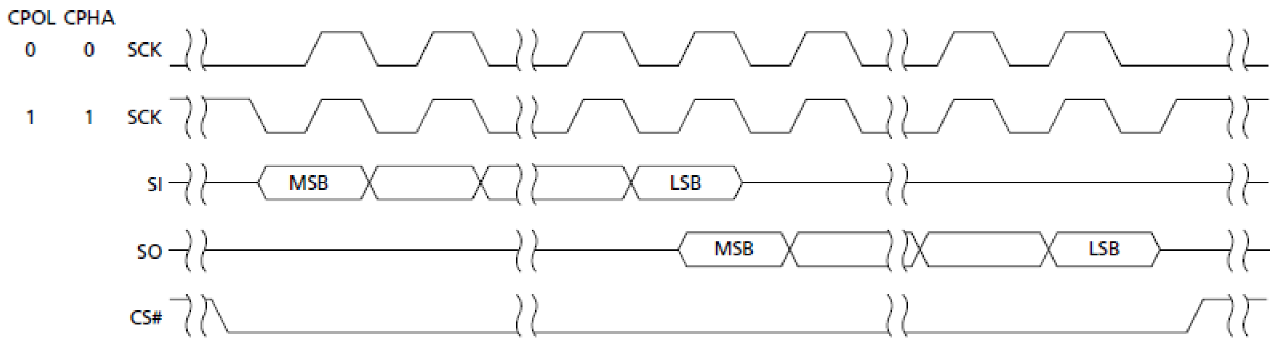
Technical Notes

Bus Operation

SPI NAND supports two SPI modes:
(Mode 0) CPOL (clock polarity) = 0, CPHA (clock phase) = 0
(Mode 3) CPOL=1, CPHA=1

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes. When CS# is high, keep SCK at V_{CC} (Mode 0) or V_{SS} (Mode 3). Do not begin toggling SCK until after CS# is driven LOW.

SPI Modes Timing



Note:

1. All timing diagrams shown in this data sheet are mode 0.

Feature Operations

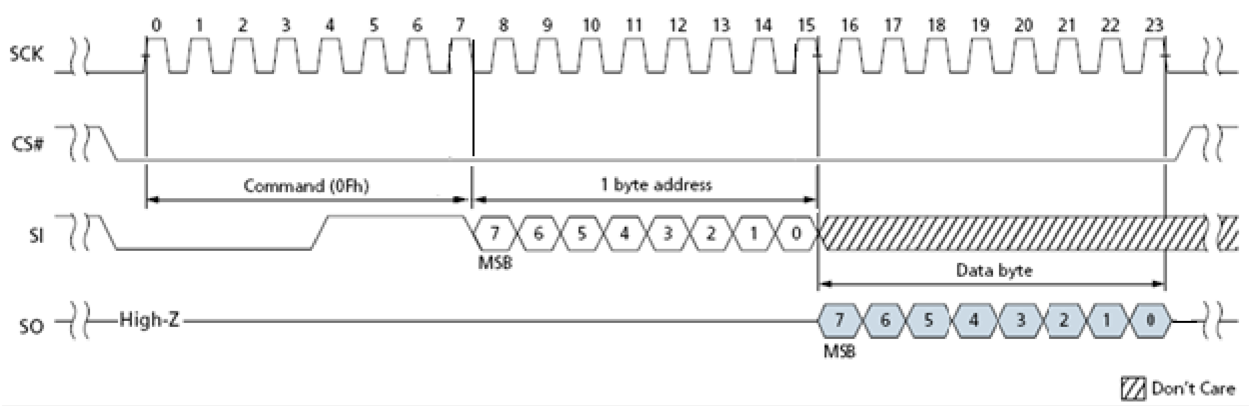
The GET FEATURE (0Fh) and SET FEATURE (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-Byte feature address to determine which feature is to be read or modified.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in Feature Setting Table, once the device is set, it remains set, even if a RESET (FFh) command is issued.

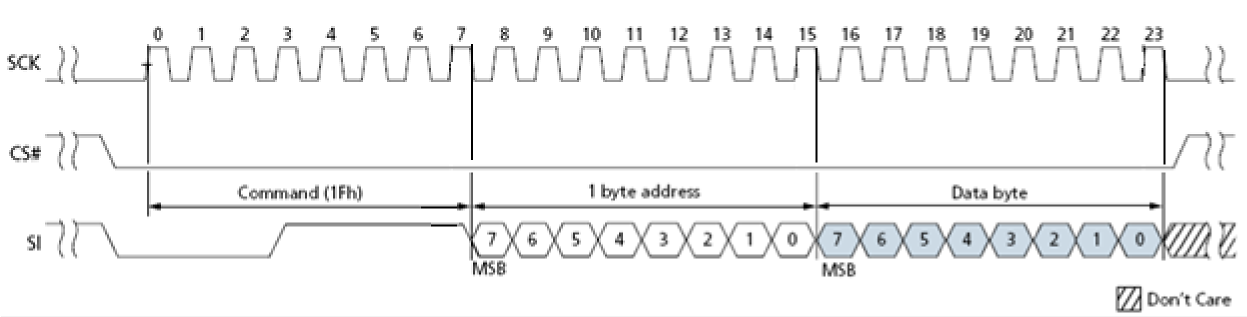
Feature Settings Table

Register	Acronym	Address	Data Bits							
			7	6	5	4	3	2	1	0
Protection Register	PR	A0h	PRP0	BP3	BP2	BP1	BP0	T/BP	WPE	PRP1
Configuration Register	CR	B0h	CFG2	CFG1	Reserved	ECC-E	Reserved	Reserved	CFG0	HD
Status Register	SR	C0h	Reserved	Reserved	ECC_S1	ECC_S0	P_Fail	E_Fail	WEL	OIP
Output Driver Register	ODR	D0h	Reserved	DRV_S1	DRV_S0	Reserved	Reserved	Reserved	Reserved	Reserved

GET FEATURE (0Fh) Timing



SET FEATURE (1Fh) Timing



Protection Register

Protection Register Setting Table

A0h	Data Bits							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Definition	Protection Register Protect 0	Block Protect 3	Block Protect 2	Block Protect 1	Block Protect 0	Top / Bottom Protect	WP# Enable	Protection Register Protect 1
Shipment default	0	1	1	1	1	1	0	0

Note:

1. All bits in A0h are volatile writable.
2. Once BP[3:0], T/B-P, and WPE bits are set correctly.

Related Protection Bits of Protection Register Table

Software Protection (Controller, X4 Program/ Read is enable)				
PRP0 (7)	**WPE (1)**	**PRP1 (0)**	**WP# IO2**	**Description**
0	0	0	X	No WP# functionality, and WP# pin will always function as IO2
1	0	0	0	PR(1) cannot be changed, and WP# pin will function as IO2 for X4 operation
1	0	0	1	PR can be changed, and WP# pin will function as IO2 for X4 operation
X	0	1	X	Power Lock Down(2) PR, and WP# pin will always function as IO2
Hardware Protection (System Circuit/ PCB layout, X4 Program/ Read is disable)				
PRP0 (7)	**WPE (1)**	**PRP1 (0)**	**WP# IO2**	**Description**
X	1	0	VCC	PR can be changed
X	1	1	VCC	Power Lock Down PR
X	1	X	GND	All Write operations are blocked, and entire device (Register, Array, and OTP area) is Read-only

Note:

1. PR means Protection Register [7:0].
2. When PRP1 = "1", PR cannot be changed during the current power cycle. Only after power cycle can reset the state to PRP1 = "0" and PRP0 = "0"

Block Protect Bits of Protection Register Table

BP3 (6)	BP2 (5)	BP1 (4)	BP0 (3)	T/BP (2)	Protected Rows
0	0	0	0	X	None; all unlocked
0	0	0	1	0	Upper 1/512 locked (BLK1022 & 1023)
0	0	1	0	0	Upper 1/256 locked
0	0	1	1	0	Upper 1/128 locked
0	1	0	0	0	Upper 1/64 locked
0	1	0	1	0	Upper 1/32 locked
0	1	1	0	0	Upper 1/16 locked
0	1	1	1	0	Upper 1/8 locked
1	0	0	0	0	Upper 1/4 locked
1	0	0	1	0	Upper 1/2 locked
0	0	0	1	1	Lower 1/512 locked (BLK0 & 1)
0	0	1	0	1	Lower 1/256 locked
0	0	1	1	1	Lower 1/128 locked
0	1	0	0	1	Lower 1/64 locked
0	1	0	1	1	Lower 1/32 locked
0	1	1	0	1	Lower 1/16 locked
0	1	1	1	1	Lower 1/8 locked
1	0	0	0	1	Lower 1/4 locked
1	0	0	1	1	Lower 1/2 locked
1	0	1	X	X	All locked
1	1	X	X	X	All locked

Note:
1. X = don’t care
2. Any Erase or Program command for the protected area will be ignored.

Configuration Register

Configuration Register Setting Table

B0h	Data Bits							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Definition	CFG2	CFG1	Reserved	ECC Enable[(2)]	Reserved	Reserved	CFG0	HD
Shipment default	0	0	0	1	0	0	0	0

Note:

1. Internal ECC for all READ and PROGRAM operations can be enabled (ECC enable = 1)
2. Bit7, Bit6, Bit4 and Bit1 are volatile writable.

OTP State Bits of Configuration Register Table

CFG2	CFG1	CFG0	State
0	0	0	Normal operation (read array)
0	1	0	Access OTP area/Parameter/Unique ID
1	0	0	Not applicable
1	1	0	Lock the OTP area
X	X	1	Not applicable

Hold Disable Bit (HD)

When WP-E is “0”, during the x4 operation, to prevent accidental operation from host to place the Hold Input (drive Hold# low), Hold Disable (HD) can be set by SET Feature (B0h, 0Bit).

While HD bit is "0" (default), during the x4 operation, HOLD# function still can be enabled before the x4 operation command. When the x4 operation command is issued, HOLD# pin will become a data I/O pin for the x4 operations and no HOLD# function is available until the current x4 operation finishes.
HD bit is allowed to be set “1” only when WP-E bit is “0”. While WP-E bit is “0” and HD bit is set "1", Hold# function as well as WP# control function is disabled. HD bit returns to “0” after next power cycle.

Status Register

Software can read status register during the NAND device operation by issuing GET FEATURE (0Fh) command, followed by the feature address C0h. The status register will output the status of the operation, refer to Status Register Setting Table, Bits of Status Register Table and ECC Status Bits of Status Register Table.

Status Register Setting Table

C0h	Data Bits							
Bit	7	6	5	4	3	2	1	0
Definition	Reserved	Reserved	ECC_Status1	ECC_Status0	Program_Fail	Erase_Fail	Write Enable Latch	Operation In Progress
Shipment default	0	0	0	0	0	0	0	0

Status Register Bit Descriptions

Bit Name	Mode	Description
ECC_status1 (Bit 5) ECC_status0 (Bit 4)	R	ECC Status Bits of Status Register Table shows the ECCS definitions. ECC_S is set to 00h either following a RESET, or at the beginning of the READ. It is then updated after the device completes a valid READ operation. ECC_S is invalid if ECC is disabled (via a SET FEATURE command to get access the configuration register). After power-up RESET, ECC_S is set to reflect the contents of block 0, page 0.
Program fail (Bit 3)	R	P_Fail is set to 1 as a program failure has occurred. P_Fail = 1 will also be set if the user attempts to program an invalid address or a locked region. P_Fail is set to 0 during the PROGRAM EXECUTE command sequence or the RESET command.
Erase fail (Bit 2)	R	E_Fail is set to 1 as an erase failure has occurred. E_Fail = 1 will also be set if the user attempts to erase a locked region, or if ERASE operation fails. E_Fail is set to 0 at the start of the BLOCK ERASE command sequence or the RESET command.
Write enable latch (Bit 1)	W	WEL must be set to 1 to indicate the current status of the write enable latch, prior to issuing PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing WRITE ENABLE command. WEL can also be cleared (WEL=0) by issuing the WRITE DISABLE command or RESET command or after a successful PROGRAM/ERASE operation.
Operation in progress (Bit 0)	R	OIP is set to 1 when the device is busy; it means a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE or RESET command is executing. OIP is cleared to 0 as the interface is in ready state.

ECC Status Register Bit Descriptions

ECCS1 (5)	ECCS0 (4)	Description
0	0	No errors
0	1	1 bit errors detected and corrected
1	0	2 bit errors detected and not corrected
1	1	Reserved

ECC Protection

ECC is enabled after device power-up, so the default PROGRAM and READ commands operate with internal ECC in the active state. During a PROGRAM operation, the device calculates an ECC code on the 2KB page in the cache register, before the page is written to the NAND Flash array. The ECC code is stored in the spare area of the page in array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If a single-bit data error is discovered, the error is corrected in the cache register and only the corrected data is on the output bus.

ECC Protection Table

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh (511)	000h (0)	Yes	Main 0	User data 0[1]
3FFh (1023)	200h (512)	Yes	Main 1	User data 1[1]
5FFh (1535)	400h (1024)	Yes	Main 2	User data 2[1]
7FFh (2047)	600h (1536)	Yes	Main 3	User data 3[1]
801h (2049)	800h (2048)	No		Reserved (Bad Block Marker)
803h (2051)	802h (2050)	No	Spare 0	User Data II
807h (2055)	804h (2052)	Yes	Spare 0	User Data I
80Dh (2061)	808h (2056)	Yes		ECC for Main 0
80Fh (2063)	80Eh (2062)	No		ECC for Spare 0
811h	810h	No		Reserved
813h	812h	No	Spare 1	User Data II
817h	814h	Yes	Spare 1	User Data I
81Dh	818h	Yes		ECC for Main 1
81Fh	81Eh	No		ECC for Spare 1
821h	820h	No		Reserved
823h	822h	No	Spare 2	User Data II
827h	824h	Yes	Spare 2	User Data I
82Dh	828h	Yes		ECC for Main 2
82Fh	82Eh	No		ECC for Spare 2
831h	830h	No		Reserved
833h	832h	No	Spare 3	User Data II
837h	834h	Yes	Spare 3	User Data I
83Dh	838h	Yes		ECC for Main 3
83Fh	83Eh	No		ECC for Spare 3

Note:
1. The user areas must be programmed within a single partial-page programming operation so the NAND Flash device can calculate the proper ECC bytes.
2. When internal ECC is enabled, these areas are prohibited to be programming.

Output Driver Register

Output Driver Register Setting Table

D0h	Data Bits							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Definition	Reserved	Driver_Strength1	Deiver_Strength0	Reserved	Reserved	Reserved	Reserved	Reserved
Shipment default	0	0	1	0	0	0	0	0

Driver Strength Bits of Output Driver Register Table

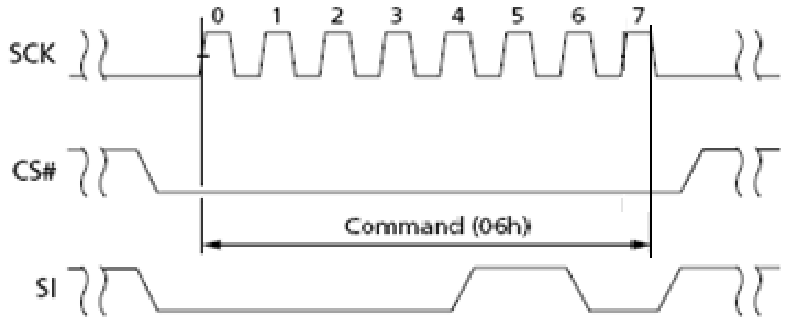
DRV_S1 (6)	DRV_S0 (5)	Driver Strength
0	0	100 %
0	1	75 %
1	0	50 %
1	1	25%

Array Write Enable / Disable

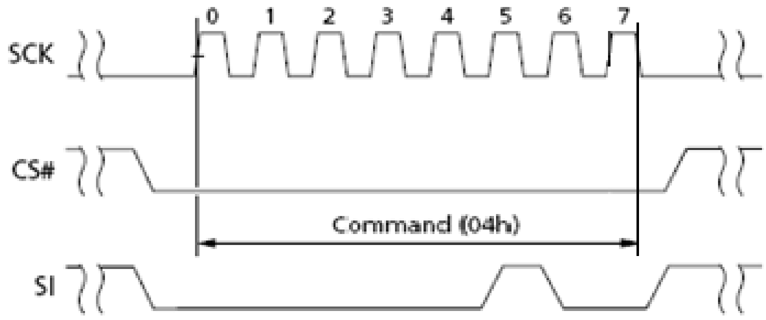
The WRITE ENABLE (06h) command sets the WEL bit (in status register) to 1. This is required in the following WRITE operations that change the contents of the memory array: PAGE PROGRAM, BLOCK ERASE, and OTP PROGRAM.

Contrarily, the WRITE DISABLE (04h) command sets the WEL bit to 0. This disables PAGE PROGRAM, BLOCK ERASE, and OTP PROGRAM.

WRITE ENABLE (06h) Timing



WRITE DISABLE (04h) Timing



Error Management

Mask Out Initial Invalid Blocks

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by ESMT. The information regarding the initial invalid blocks is called the initial invalid block information. Devices with initial invalid blocks have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block does not affect the performance of valid blocks because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid blocks via address mapping.

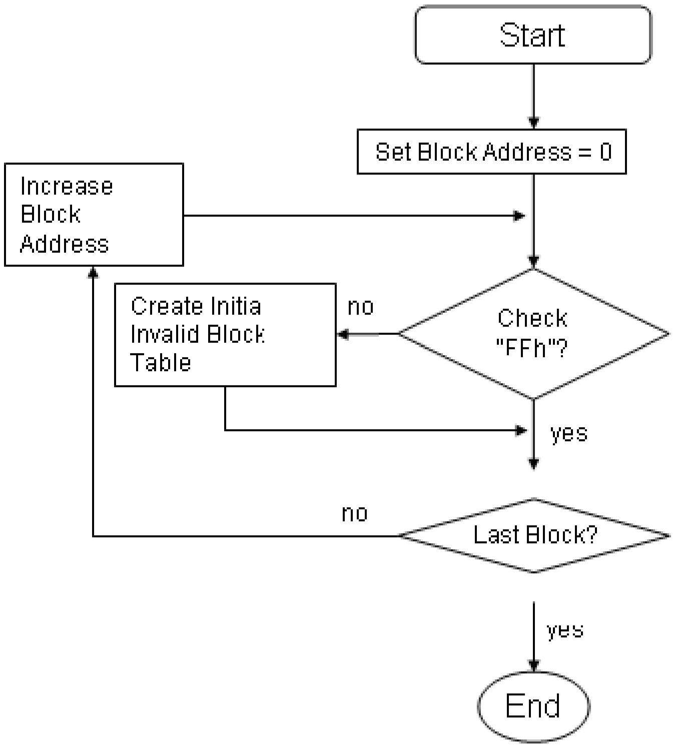
The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

Identifying Initial invalid Blocks

All device locations are erased (FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. ESMT makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the 1st byte column address in the spare area.

Do not erase or program factory-marked bad blocks. The host controller must be able to recognize the initial invalid block information and to create a corresponding table to manage block replacement upon erase or program error when additional invalid blocks develop with Flash memory usage.

Algorithm for Bad Block Scanning



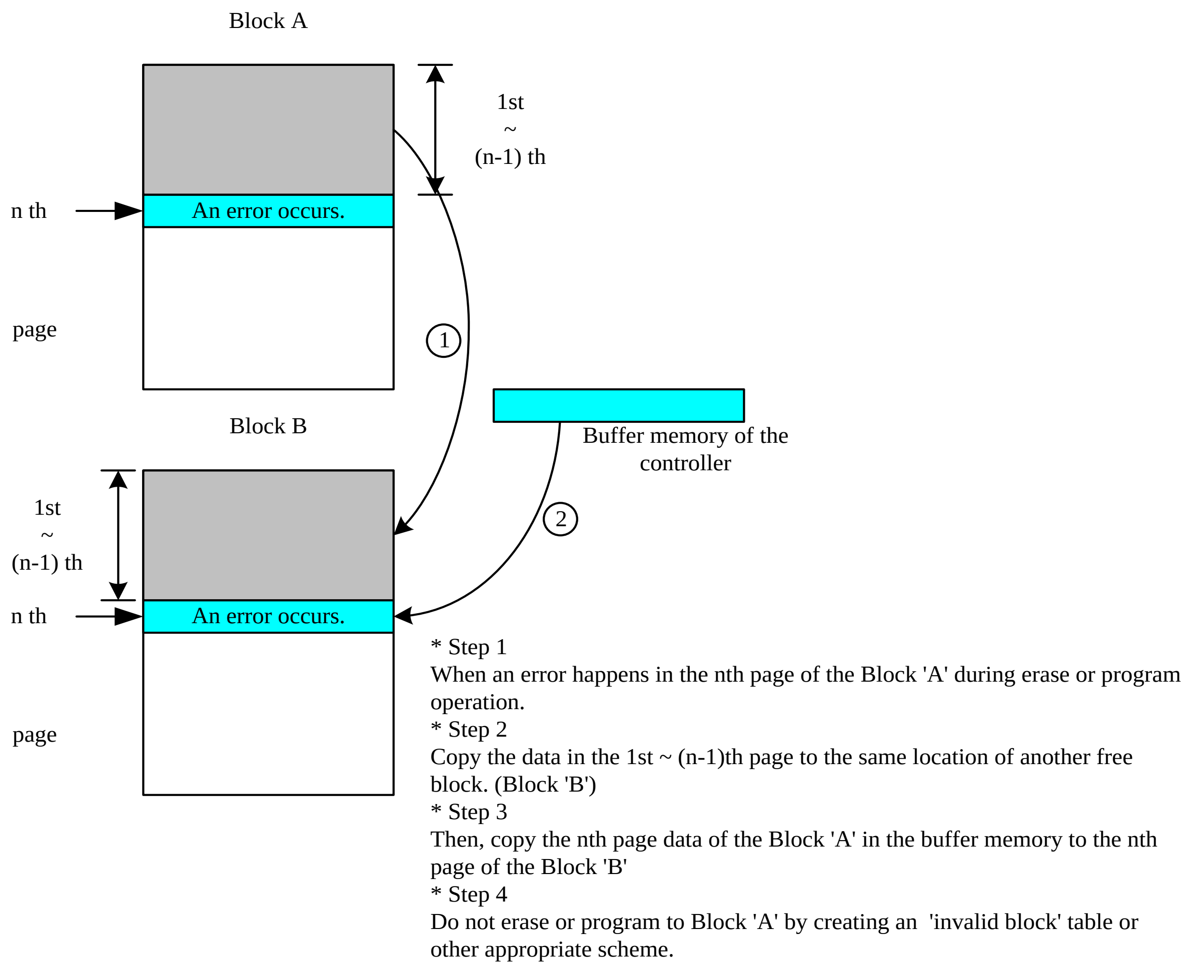
Check “FFh” at the 1st Byte column address in the spare area of the 1st and 2nd page in the block.

```
For (i=0; i<Num_of_LUs; i++)
{
        For (j=0; j<Blocks_Per_LU; j++)
        {
                Defect_Block_Found=False;

                Read_Page(lu=i, block=j, page=0);
                If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)    Defect_Block_Found=True;

                Read_Page(lu=i, block=j, page=1);
                If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)    Defect_Block_Found=True;

                If (Defect_Block_Found)        Mark_Block_as_Defective(lu=i, block=j);
        }

}
```

Block Replacement

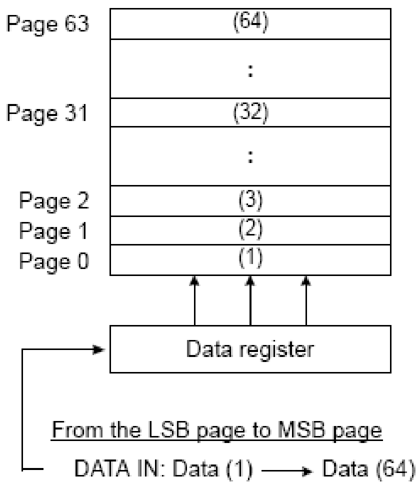
Within its lifetime, number of invalid blocks may increase with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of failure after ERASE or PROGRAM in status register, block replacement should be done. Because PROGRAM status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block.

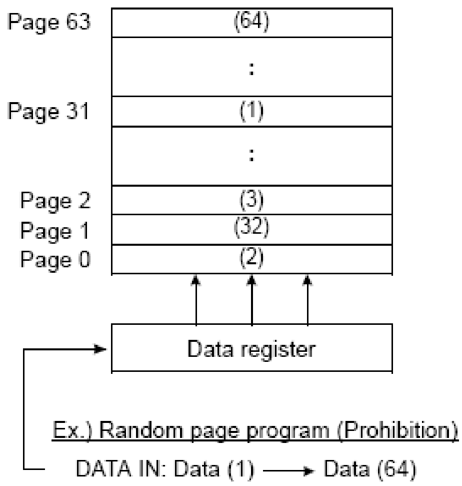
In case of READ, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The additional block failure rate does not include those reclaimed blocks.



Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.





Operations and Timing Diagrams

Read Operations and Serial Output

The command sequence is follows:

- 13h (PAGE READ to cache)
- 0Fh (GET FEATURE command to read the status)
- 0Bh or 03h (READ FROM CACHE x1); 0Ch (x1) / 3Bh (x2); 3Ch (x2) / 6Bh (x4); 6Ch (x4)
- BBh (x2); BCh (x2) / EBh (x4); ECh (x4)

PAGE READ command requires 24-bit address with 8 dummy and a 16-bit row address. After row address is registered, the device starts the transfer from the main array to the cache register, and is busy for t_R time. During this time, GET FEATURE command can be issued to monitor the status of the operation(1). Following a status of successful completion, READ FROM CACHE command must be issued to read the data out of the cache.

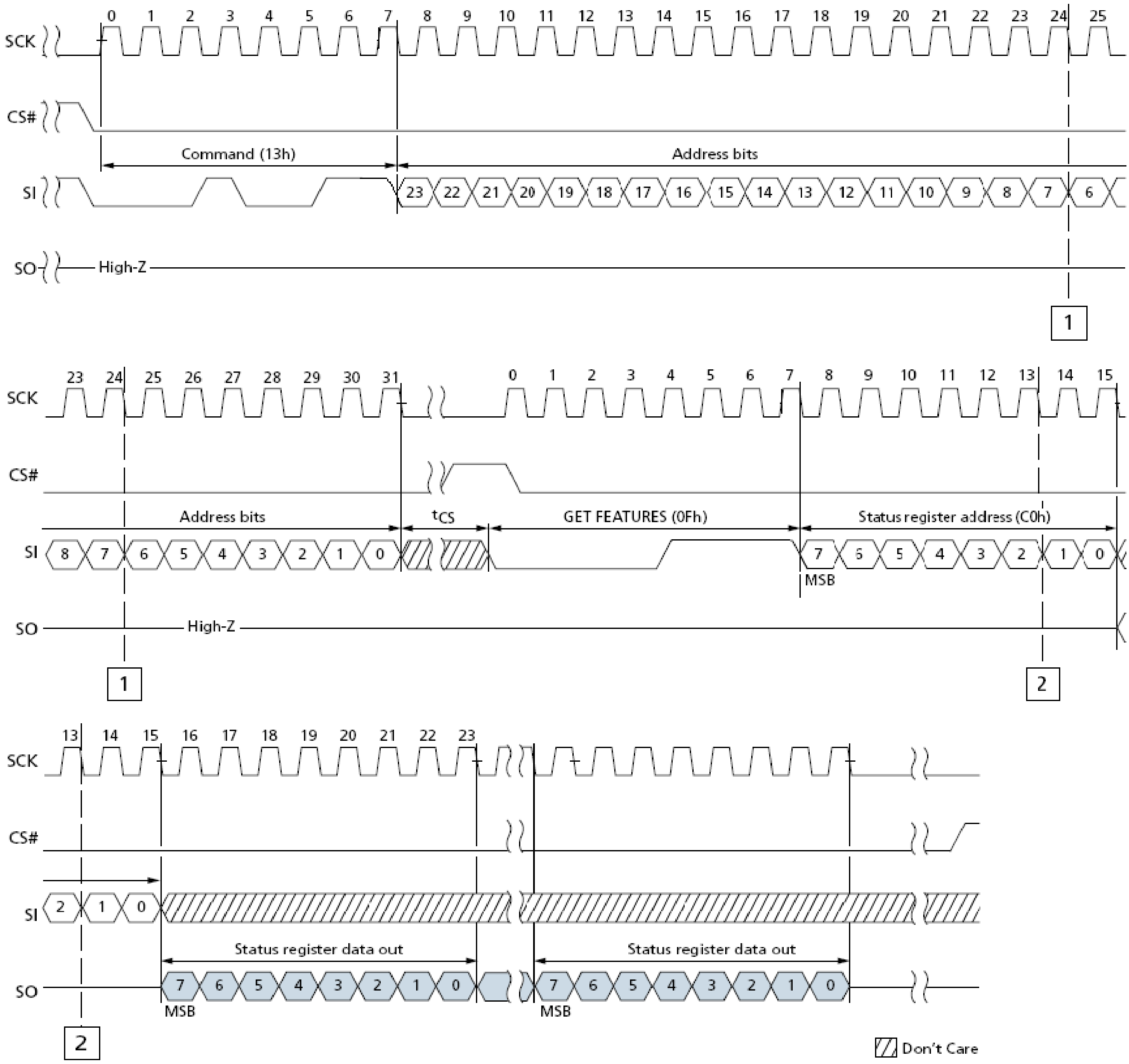
READ FROM CACHE command requires 16-bit address with 4 dummy bits and a 12-bit column address for the starting byte. The starting byte can be 0 to 2011, but after the end of the cache register is reached, the data does not wrap around and SO goes to a Hi-Z state.

BBh and BCh command allow for improved random access while maintaining two IO pins: SI and SO. It is similar to 3Bh command but with the capability to input Column Address or dummy clocks two bits per clock.

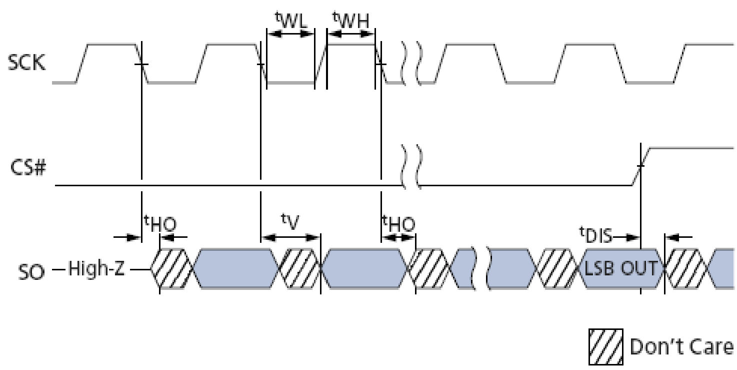
The data output sequence will start from the location specified by the Column Address input and continue to the end of the Page. Once the last byte of data is output, both SI (SO0) and SO (SO1) will become Hi-Z.

Note1：If the status is not ready (OIP=1), the IO pins will keep on a Hi-Z state after READ FROM CACHE command.

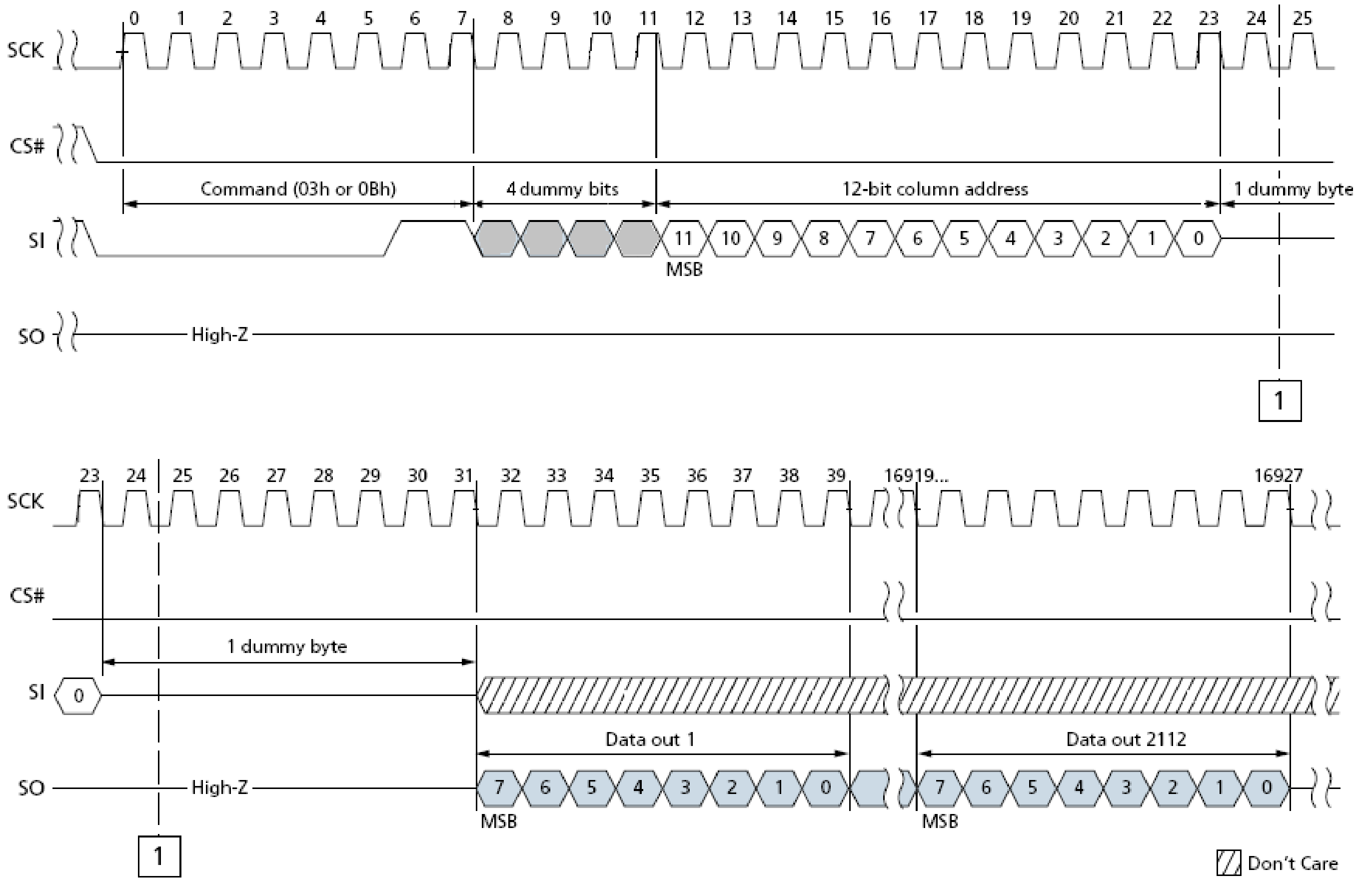
PAGE READ (13h) Timing



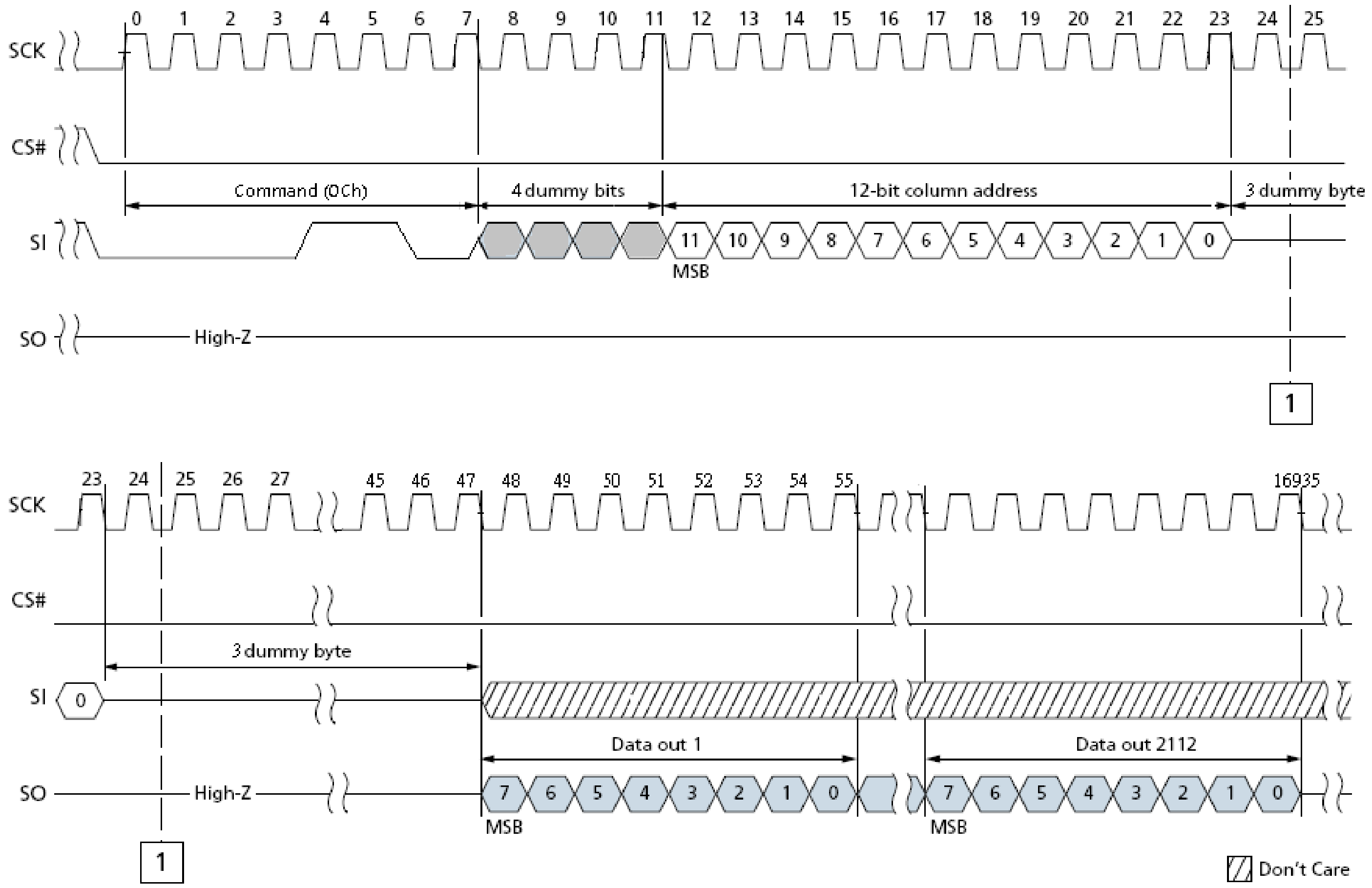
Serial Output Timing



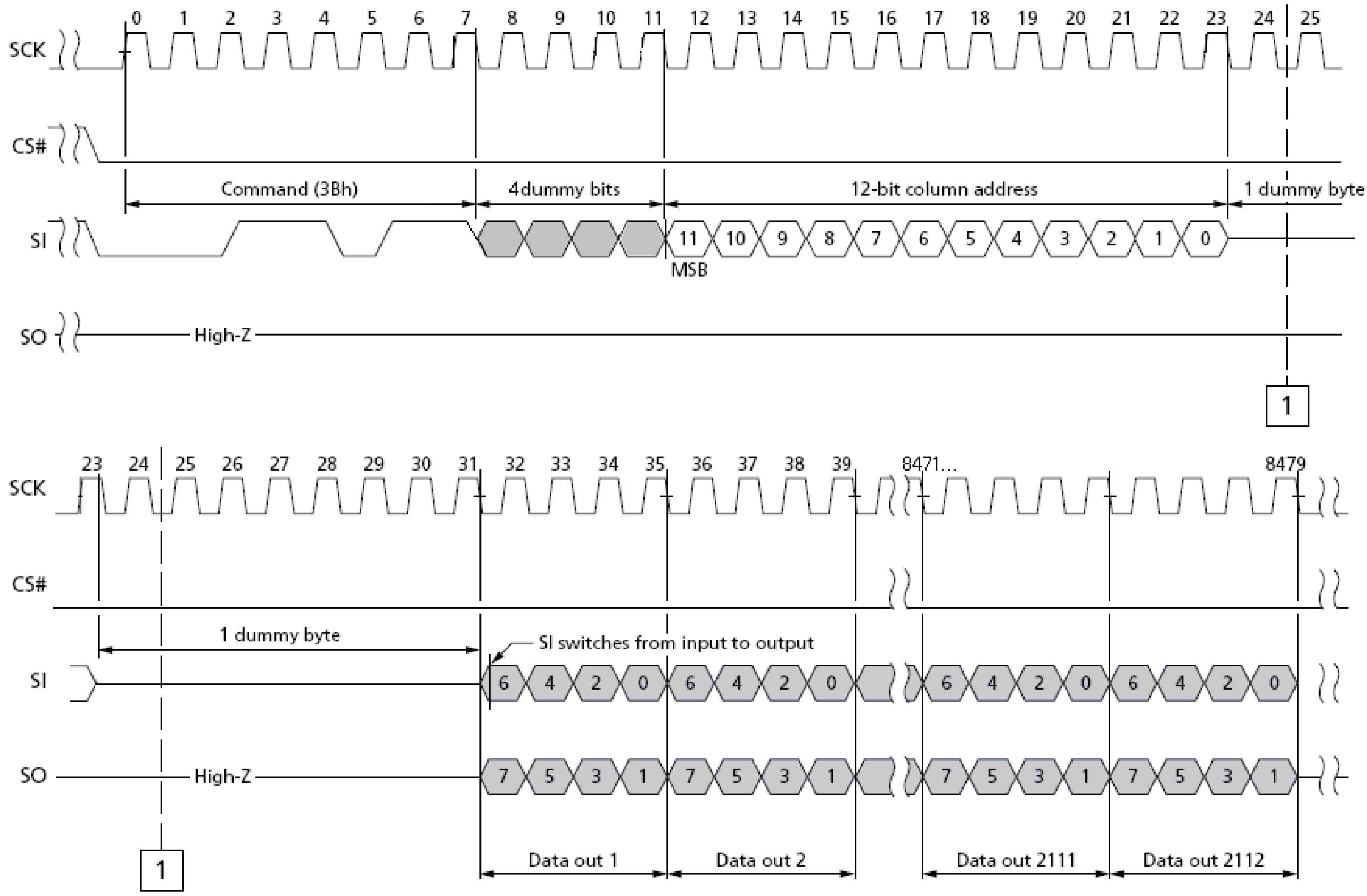
READ FROM CACHE (03h or 0Bh) Timing



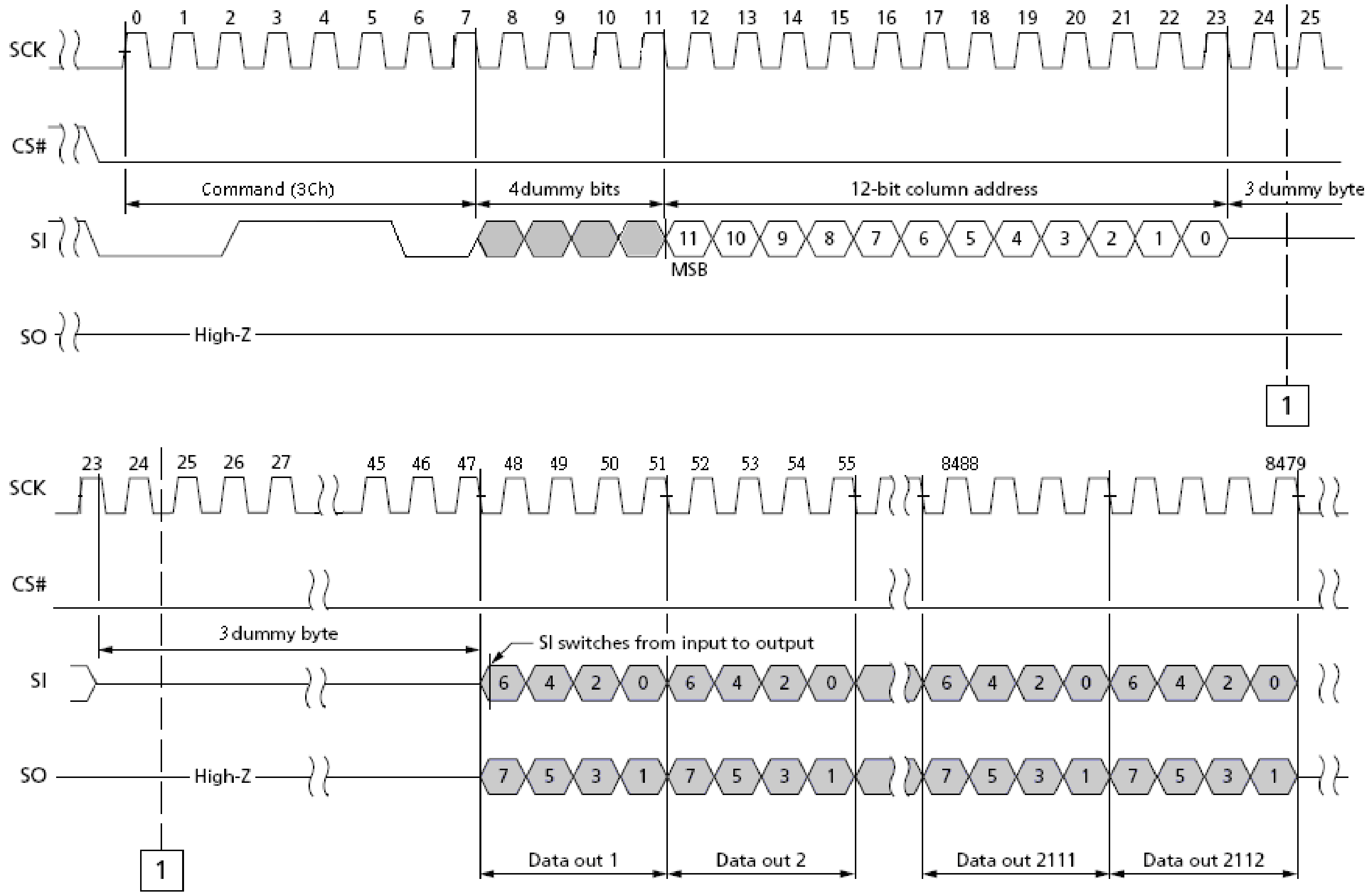
READ FROM CACHE with 4-Byte Address (0Ch) Timing



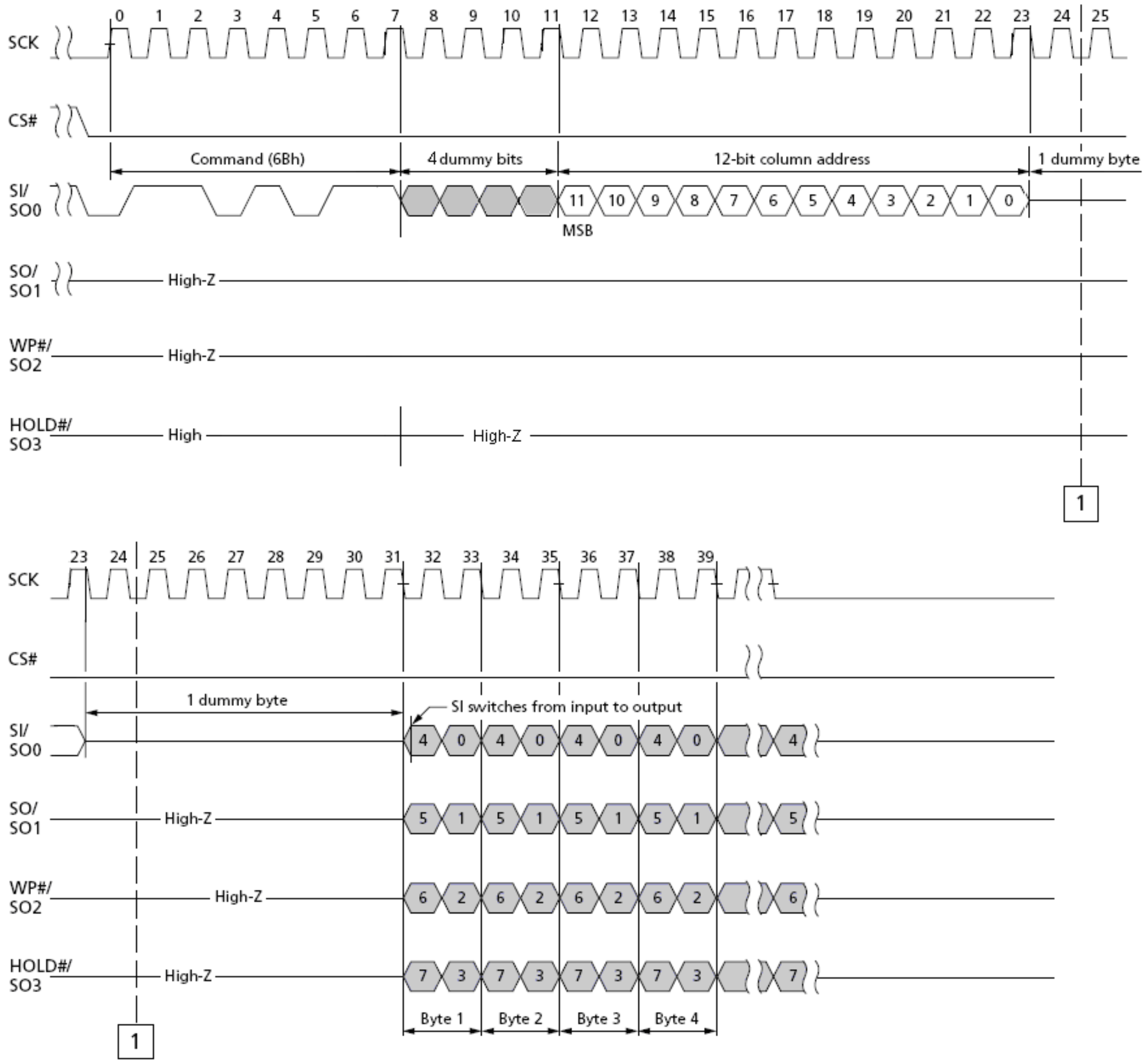
READ FROM CACHE x2 (3Bh) Timing



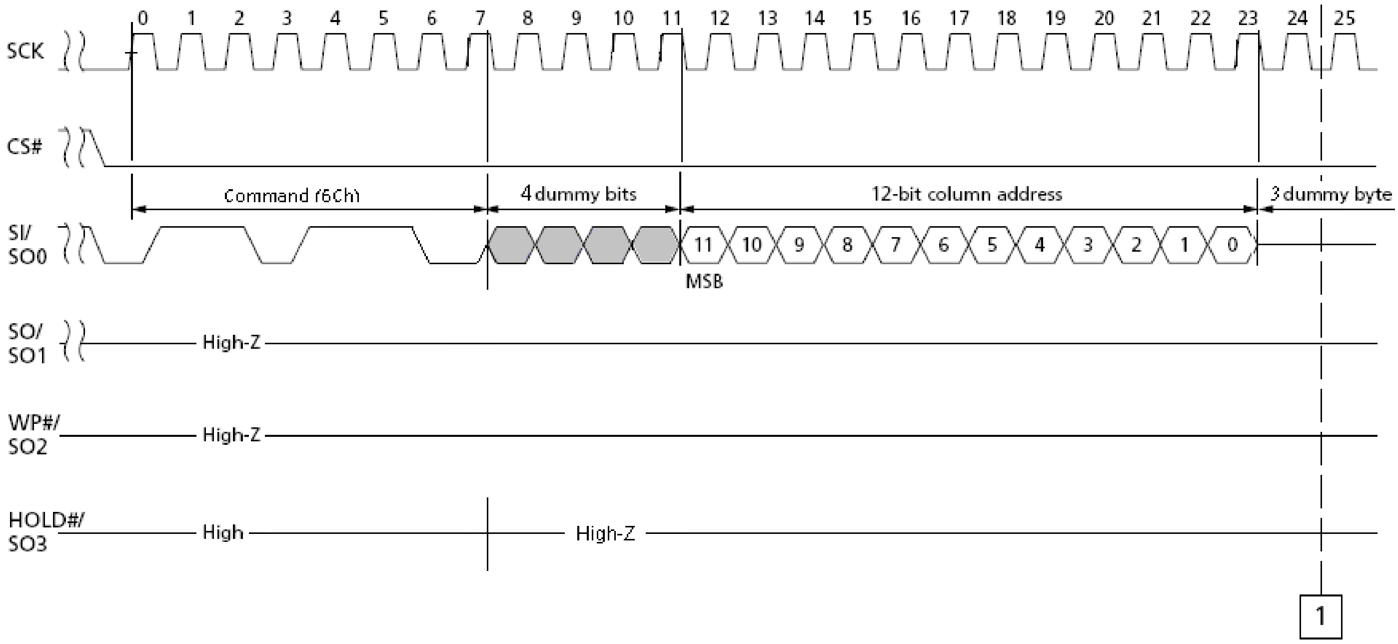
READ FROM CACHE x2 with 4-Byte Address (3Ch) Timing

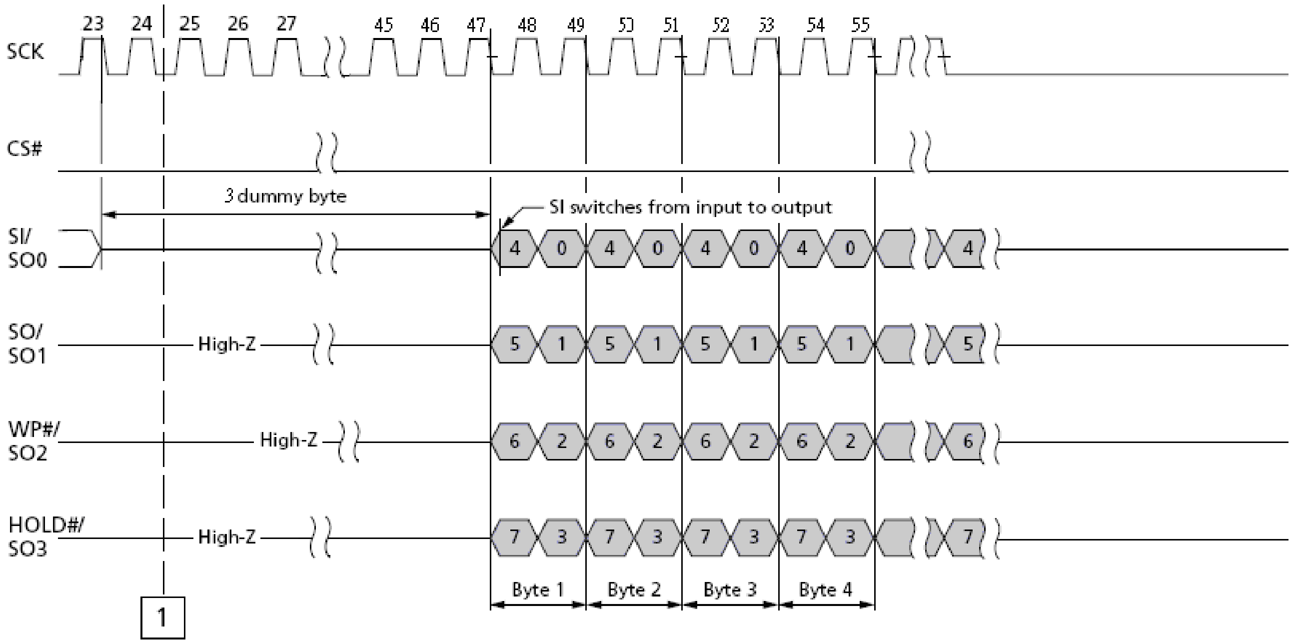


READ FROM CACHE x4 (6Bh) Timing

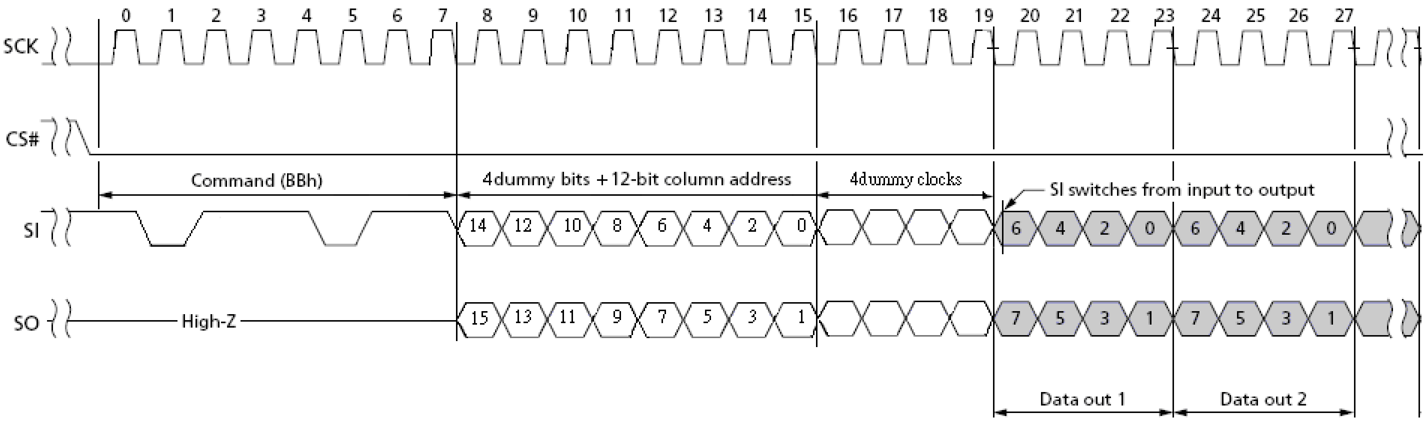


READ FROM CACHE x4 with 4-Byte Address (6Ch) Timing

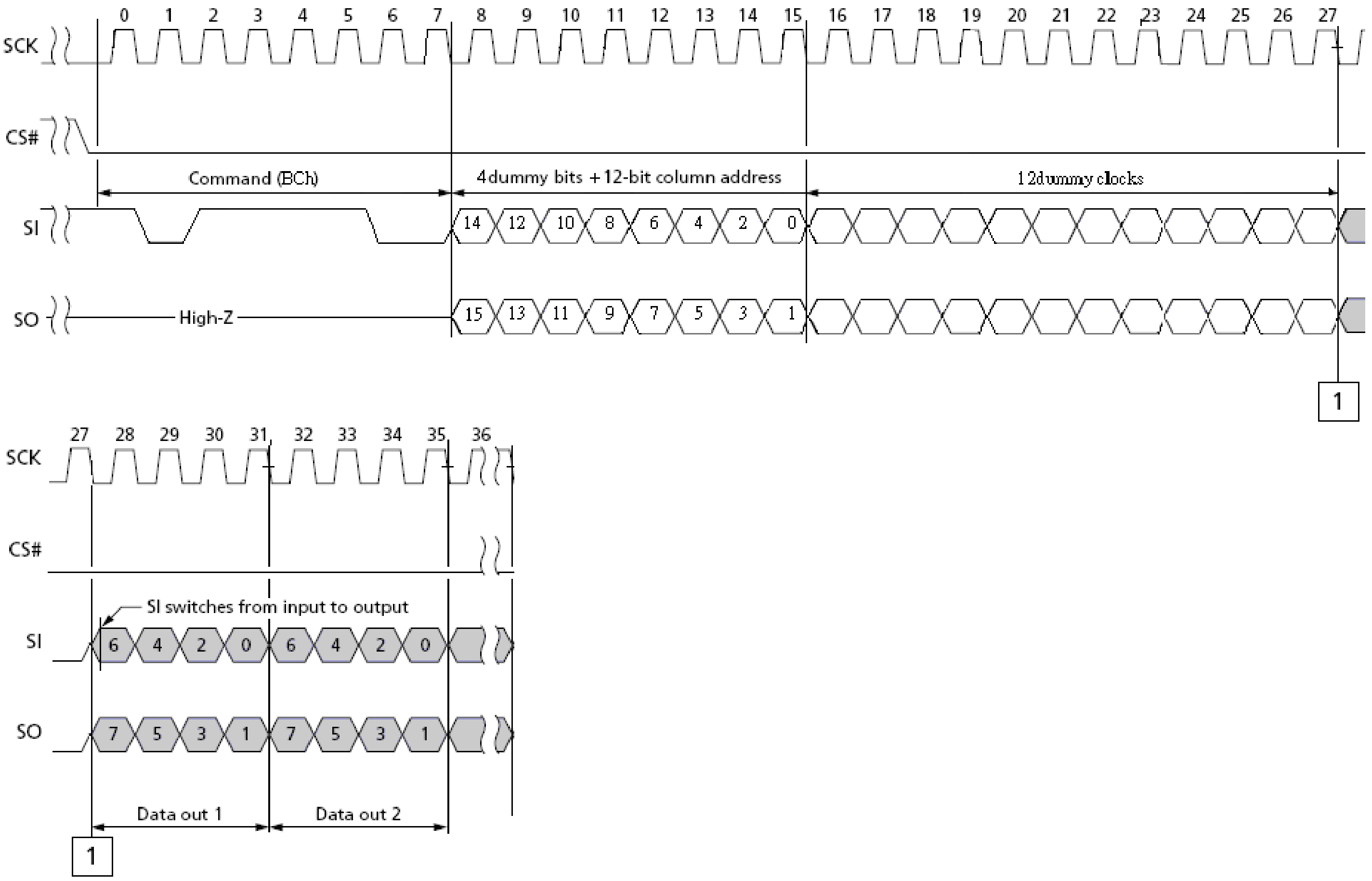




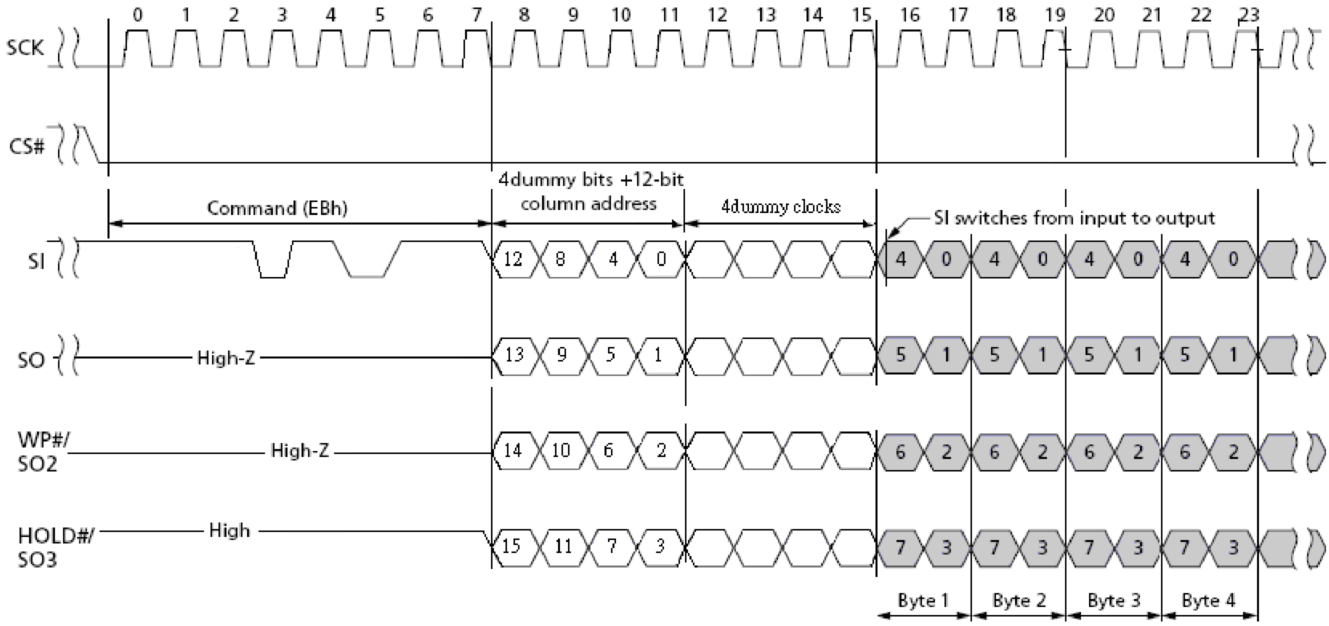
Fast Read X2 IO (BBh) Timing



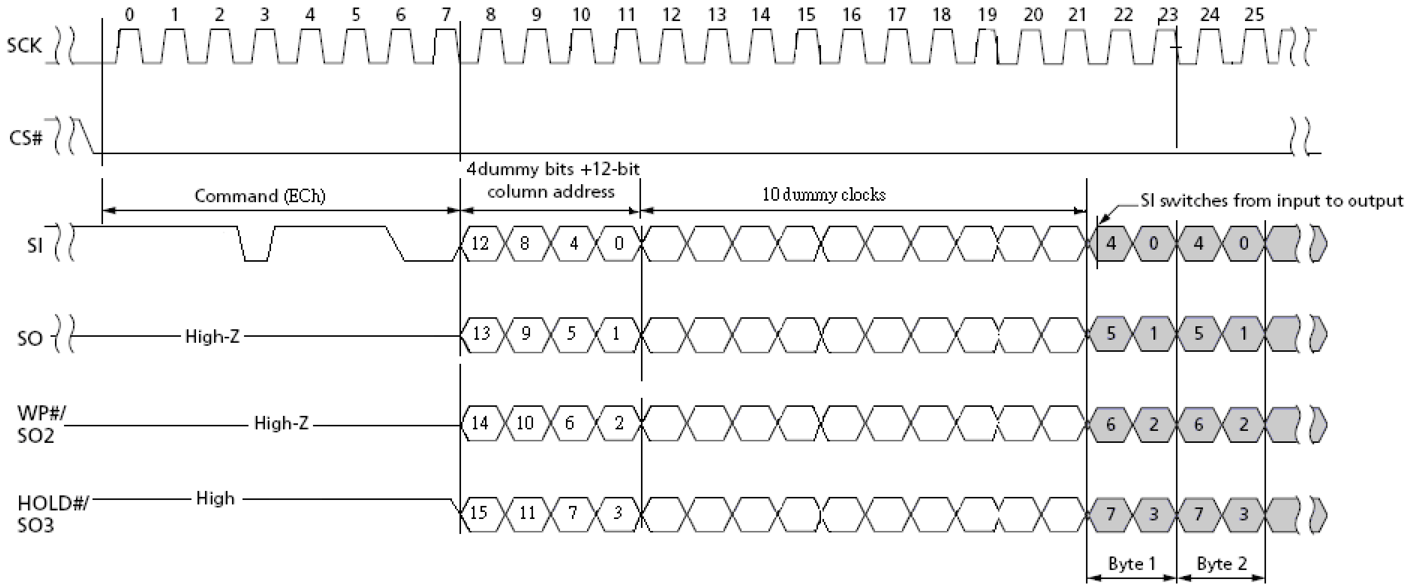
Fast Read X2 IO with 4Byte Address (BCh) Timing



Fast Read X4IO (EBh) Timing



Fast Read X4IO with 4Byte Address (ECh) Timing



Program Operations and Serial Input

Page Program

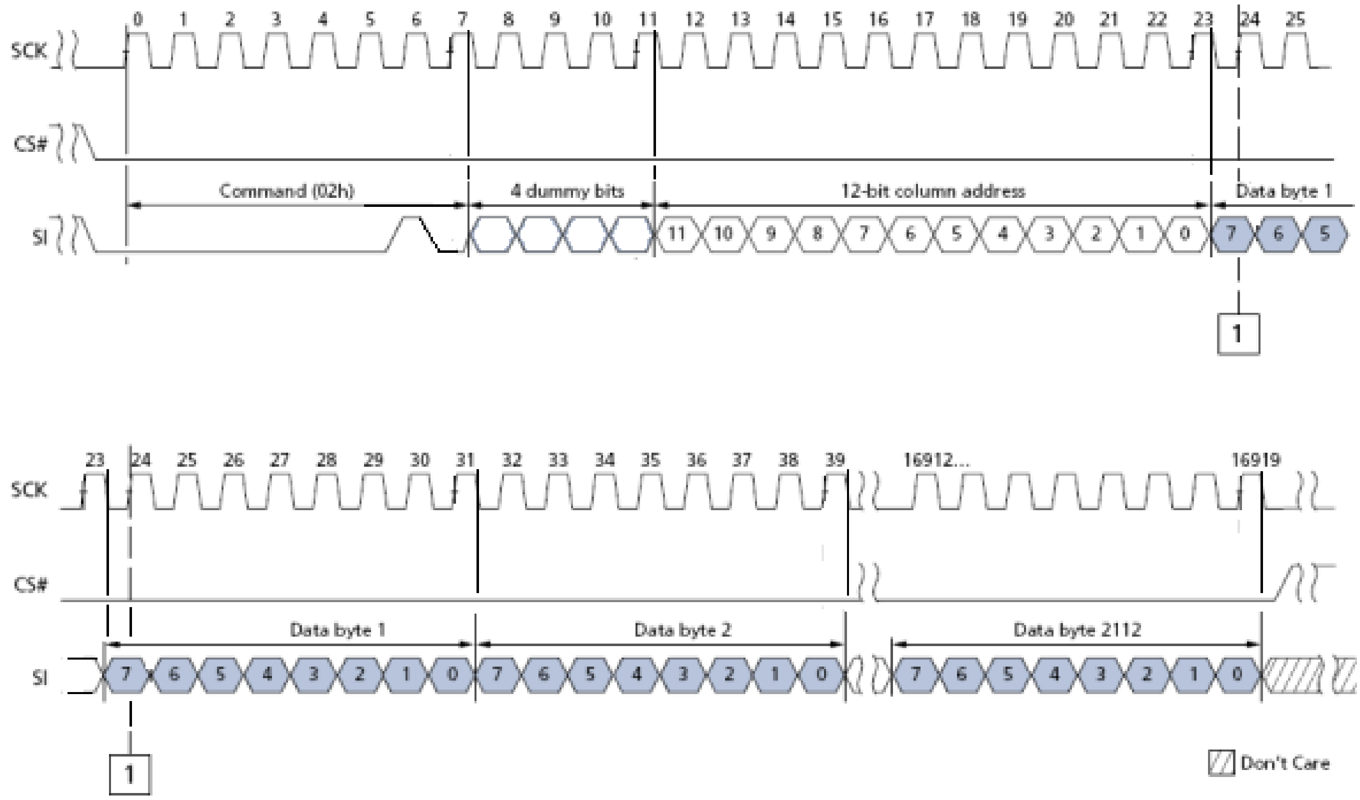
The command sequence is follows:

- 06h (WRITE ENABLE)
- 02h (PROGRAM LOAD x1) / 32h (x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

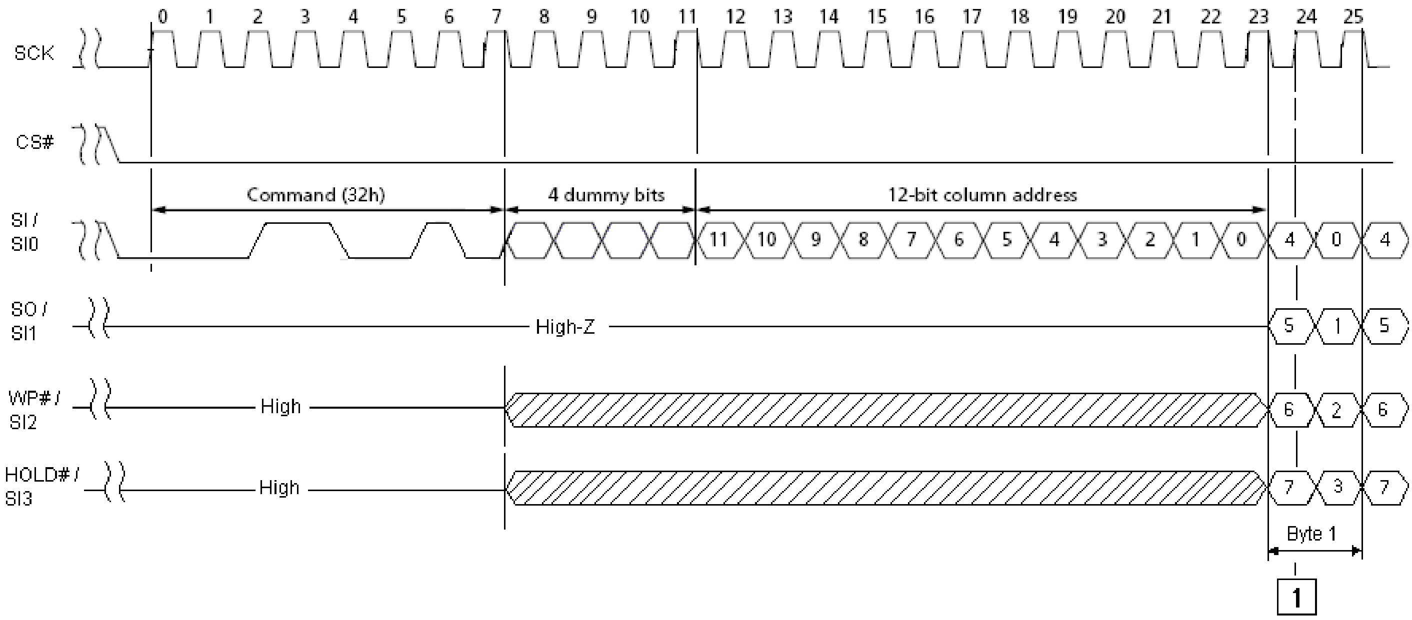
The page program operation sequence programs 1 byte to 2112 bytes of data within a page. If WRITE ENABLE command is not issued (WEL bit is not set), then the rest of the program sequence is ignored. PROGRAM LOAD command requires 16-bit address with 4 dummy and a 12-bit column address, then the data bytes to be loaded into cache register. Only four partial page programs are allowed on a single page. If more than 2112 bytes are loaded, then those additional bytes are ignored by the cache register.

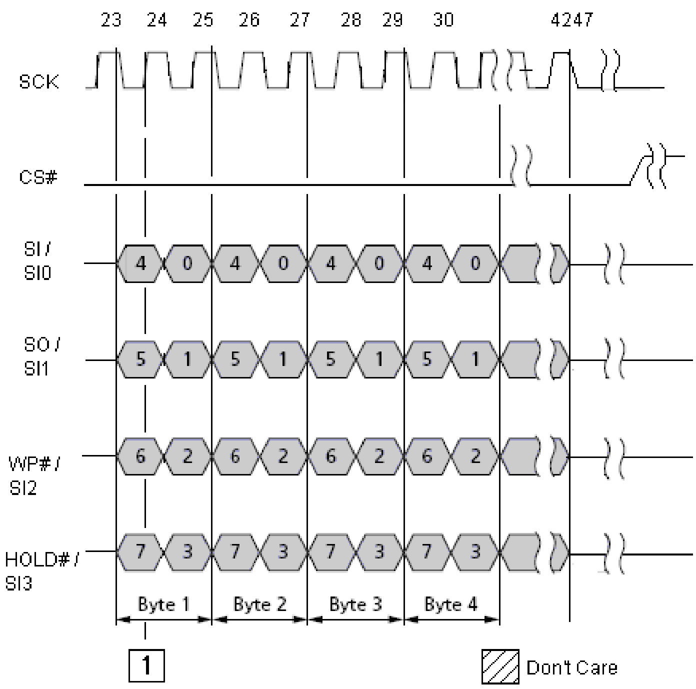
After the data is loaded, PROGRAM EXECUTE command must be issued to transfer the data from cache register to main array, and is busy for t_{PROG} time. PROGRAM EXECUTE command requires 24-bit address with 8 dummy bits and a 16-bit row address.

PROGRAM LOAD (02h) Timing

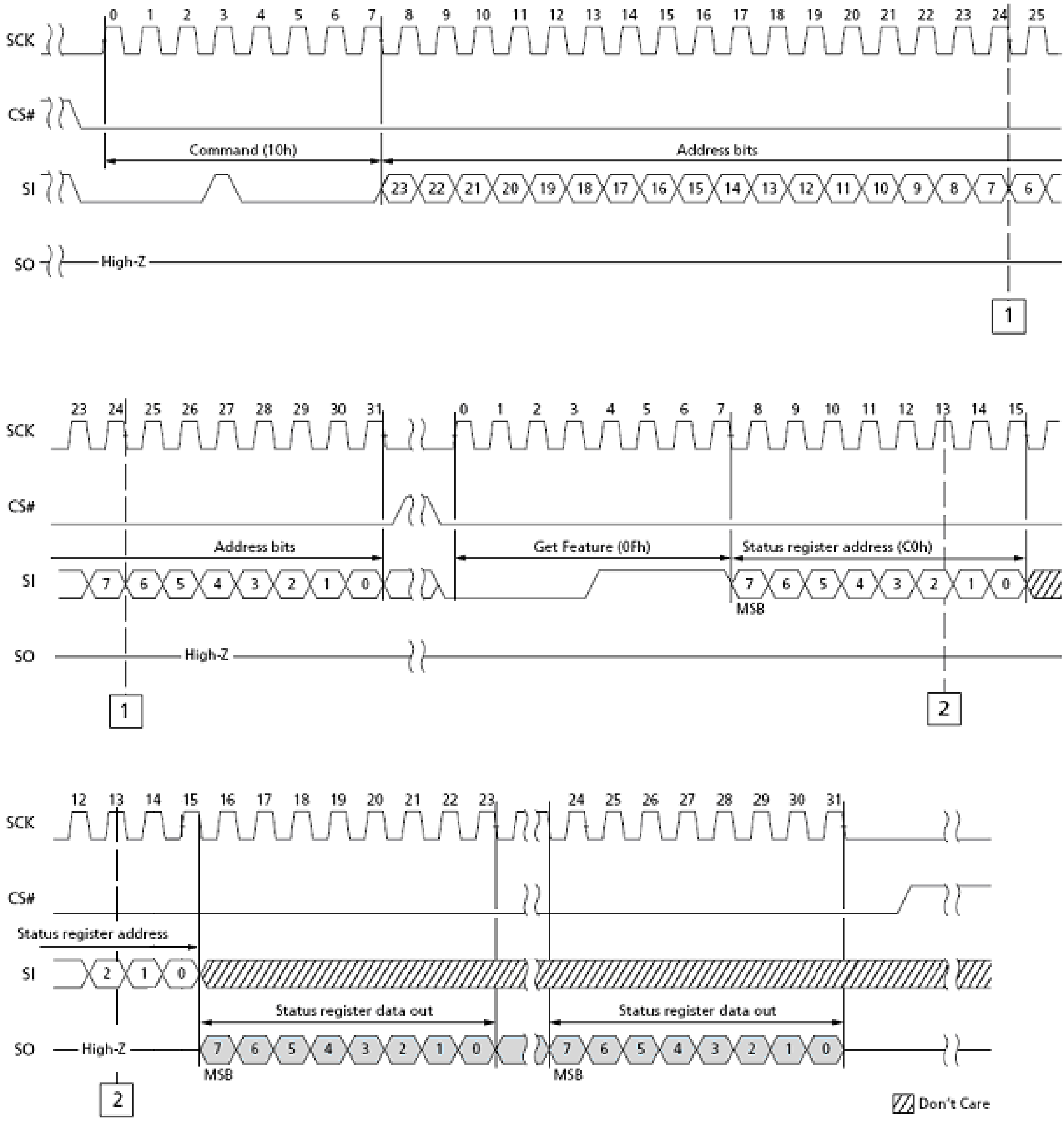


PROGRAM LOAD x4 (32h) Timing





PROGRAM EXECUTE (10h) Timing



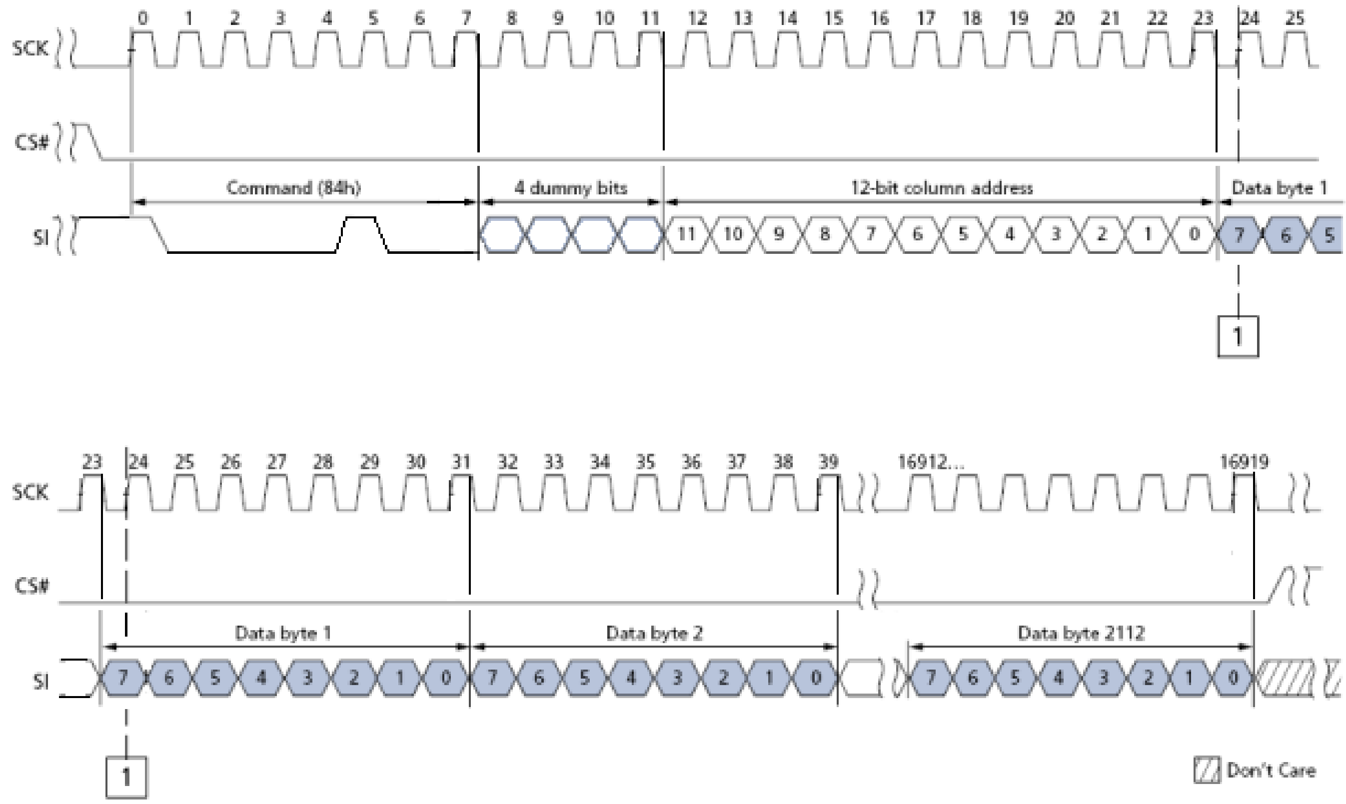
Random Data Program

The command sequence is follows:

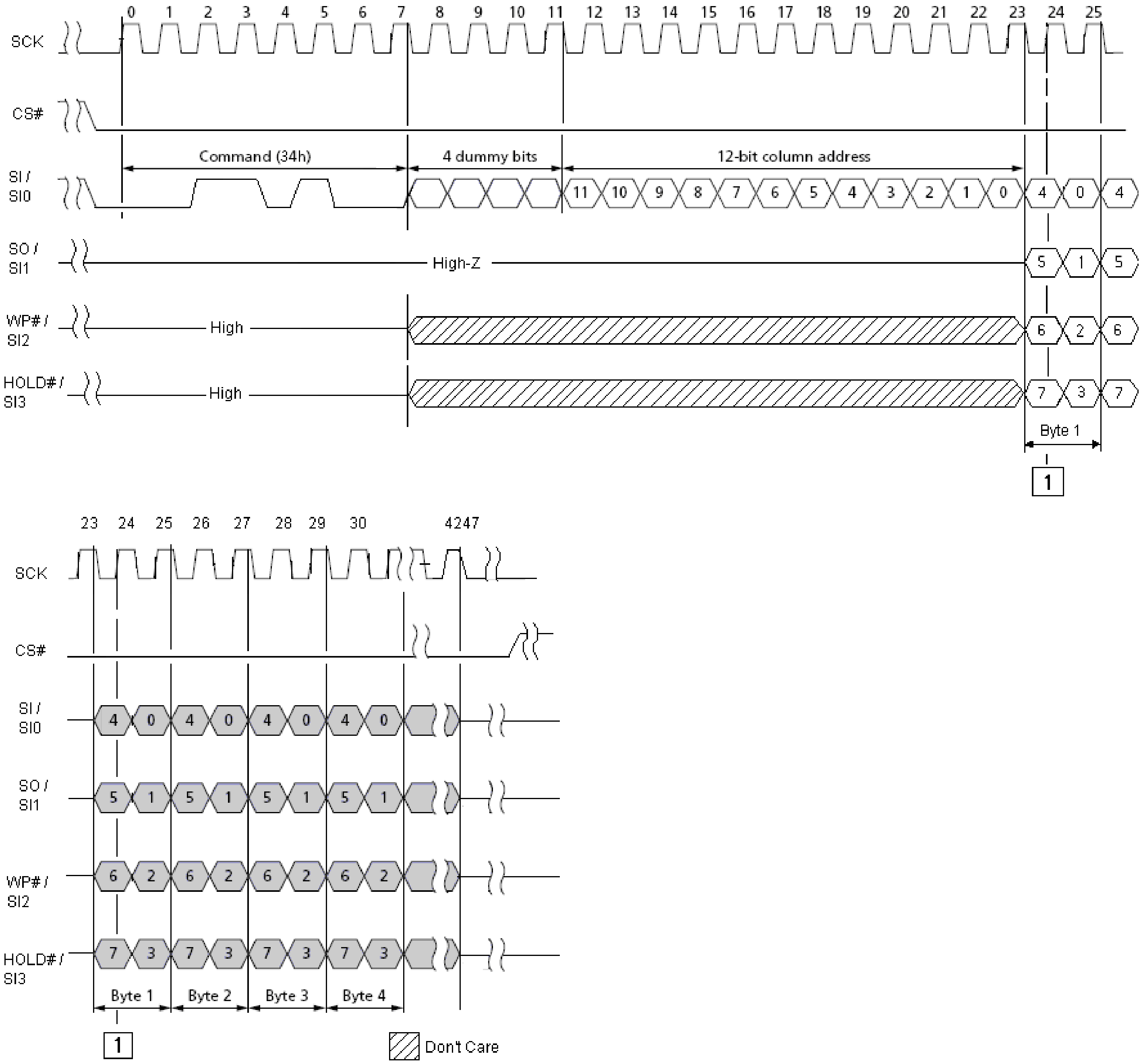
- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA x1) / 34h (x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The random data program operation sequence programs or replaces data in a page with existing data. PROGRAM LOAD RANDOM DATA command requires 16-bit address with 4 dummy bits and a 12-bit column address. New data is loaded in the column address provided. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA command must be issued with a new column address. After the data is loaded, PROGRAM EXECUTE command can be issued to start the programming operation.

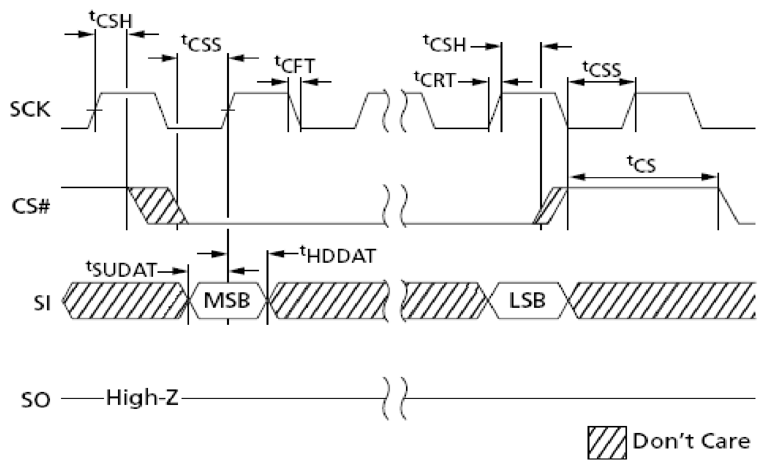
PROGRAM LOAD RANDOM DATA (84h) Timing



PROGRAM LOAD RANDOM DATA x4 (34h) Timing



Serial Input Timing



Internal Data Move

The command sequence is follows:

- 13h (PAGE READ to cache)
- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA x1) / 34h (x4); this is OPTIONAL in sequence.
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The INTERNAL DATA MOVE operation sequence programs or replaces data in a page with existing data. Prior to performing an INTERNAL DATA MOVE operation, the target page content must be read into the cache register. PAGE READ command must be followed with a WRITE ENABLE command to change the contents of memory array.

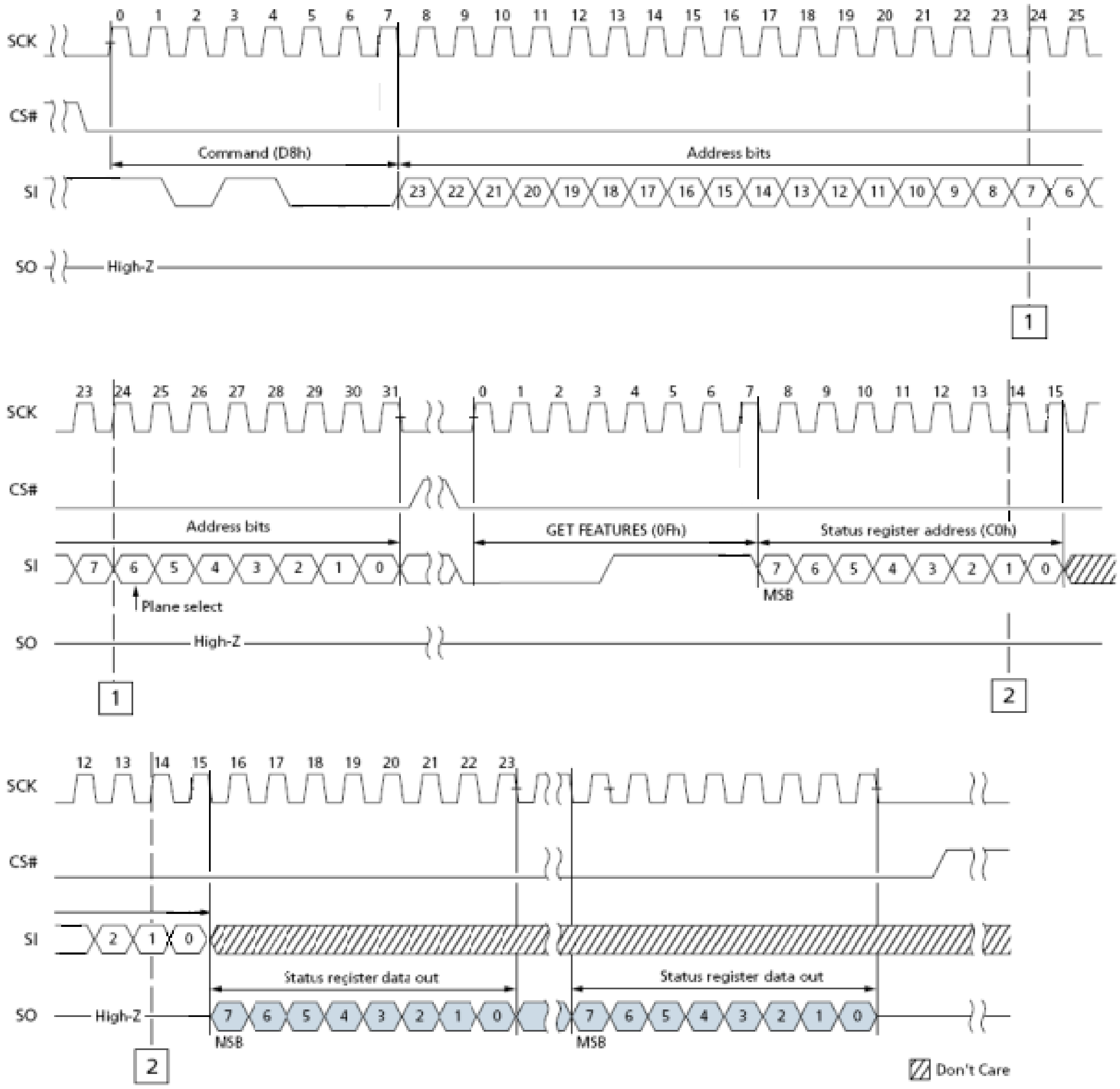
Erase Operation

The command sequence is follows:

- 06h (WRITE ENABLE)
- D8h (BLOCK ERASE)
- 0Fh (GET FEATURE command to read the status)

BLOCK ERASE command requires 24-bit address with 8 dummy bits and a 16-bit row address. If WRITE ENABLE command is not issued (WEL bit is not set), then the rest of the erase sequence is ignored. After the row address is registered, the control logic automatically controls the timing and the erase-verify operations, and the device is busy for t_{BERS} time. BLOCK ERASE command operates on one block at a time.

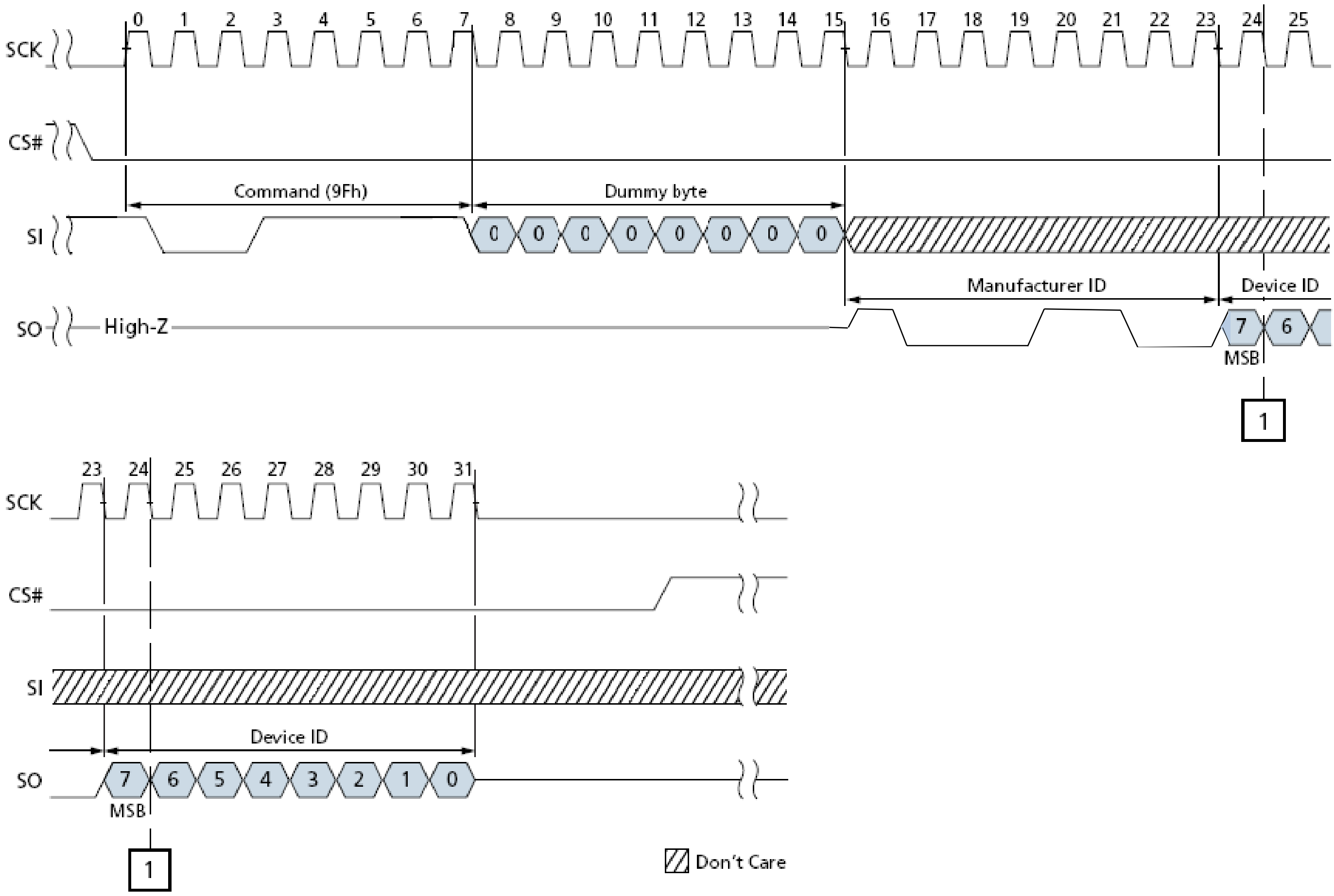
BLOCK ERASE (D8h) Timing



Read ID

READ ID reads the 2-byte identifier code programmed into the device, which includes ID and device configuration data as shown in the table below.

READ ID Timing



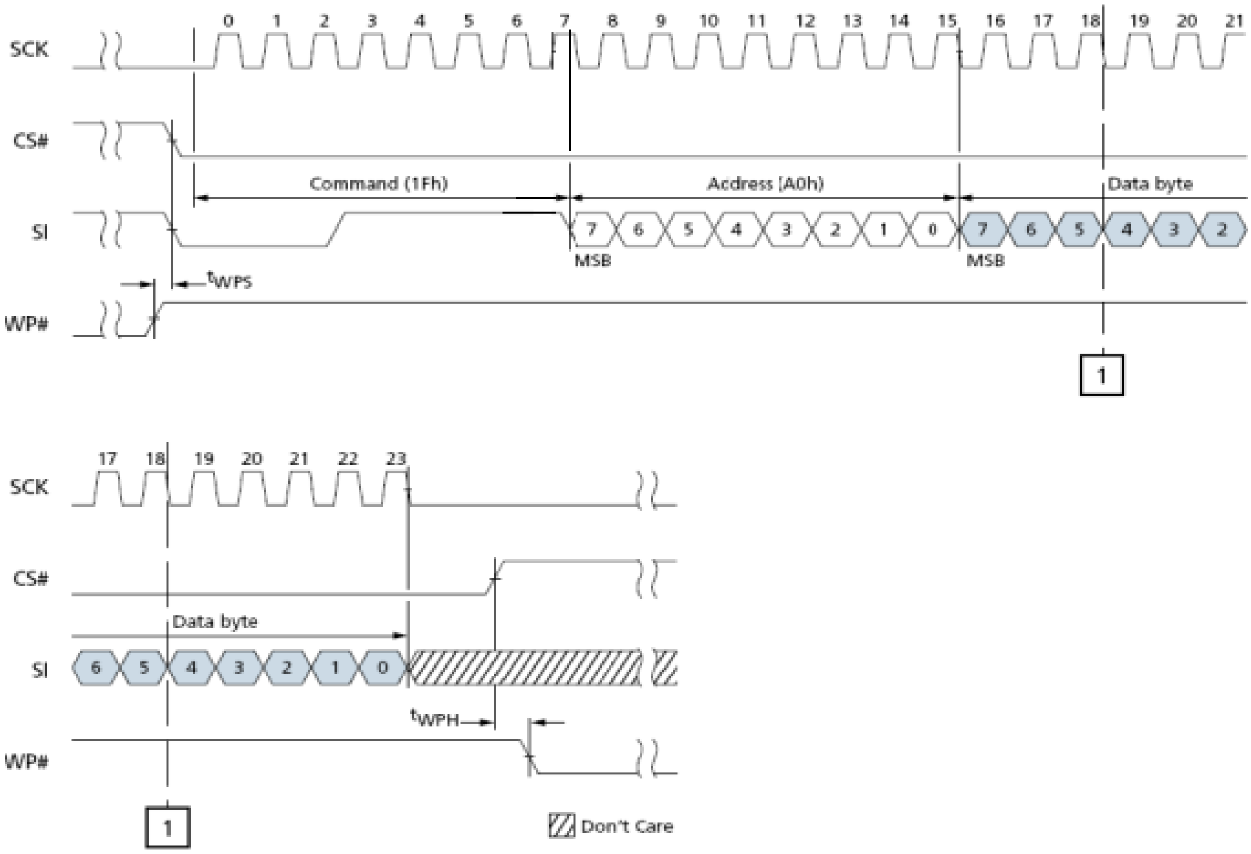
ID Definition Table

Product ID	1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle
F50L1G41LC (2P)	8Ch	2Ch	(repeat 1st Cycle)	(repeat 2nd Cycle)

	Description
1st Byte 2nd Byte	Maker Code Device Code

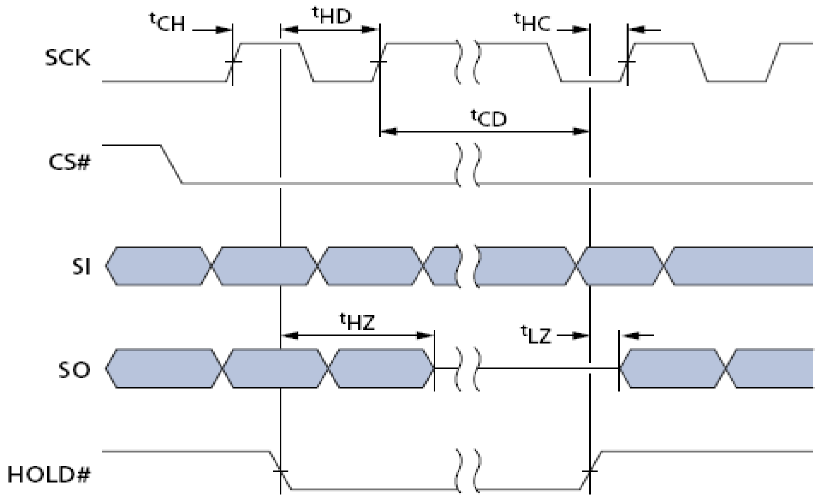
Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Density	1Gb 2Gb 4Gb 8Gb	0 0 0 1	0 1 1 0	1 0 1 0					
Voltage	1.8V 3.3V								1 0
Interface	SPI X8 X16				0 0 1	1 0 0			
Default ECC	Disable Enable						0 1		
Reserved	Reserved							0	

WP# Timing


SCK
CS#
SI
WP#
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
Command (1Fh)
Address (A0h)
Data byte
7 6 5 4 3 2 1 0
7 6 5 4 3 2
MSB
MSB
tWPS
1
17 18 19 20 21 22 23
Data byte
6 5 4 3 2 1 0
tWPH
1
Don't Care

HOLD# Timing

HOLD# input provides a method to pause serial communication with the device but doesn't terminate any READ, PROGRAM, or ERASE operation currently in progress.
Hold mode starts at the falling edge of HOLD# provided SCK is also Low. If SCK is High when HOLD# goes Low, hold mode begins after the next falling edge of SCK. Similarly, hold mode is exited at the rising edge of HOLD# provided SCK is also Low. If SCK is High, hold mode ends after the next falling edge of SCK.
During hold mode, SO is Hi-Z, and SI and SCK inputs are ignored.

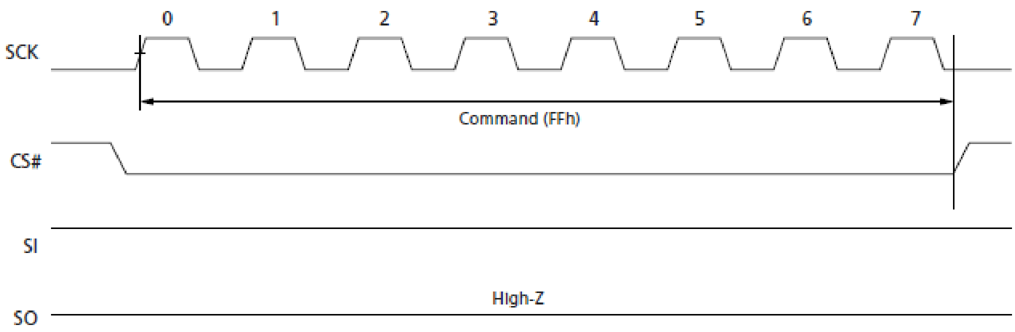


RESET Operation

The RESET command (FFh) is used to put the memory device into a known condition and to abort the command sequence in progress. READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. Once the RESET command is issued to the device, it will take tRST to reset. During this period, the GET FEATURE command could be issued to monitor the status (OIP).

All other status register bits will be cleared. The ECC status register bits will be cleared after a reset. The configuration register bits and the block lock register bits will not be cleared after reset until the device is power cycled or is written to by SET FEATURE command.

RESET (FFh) Timing



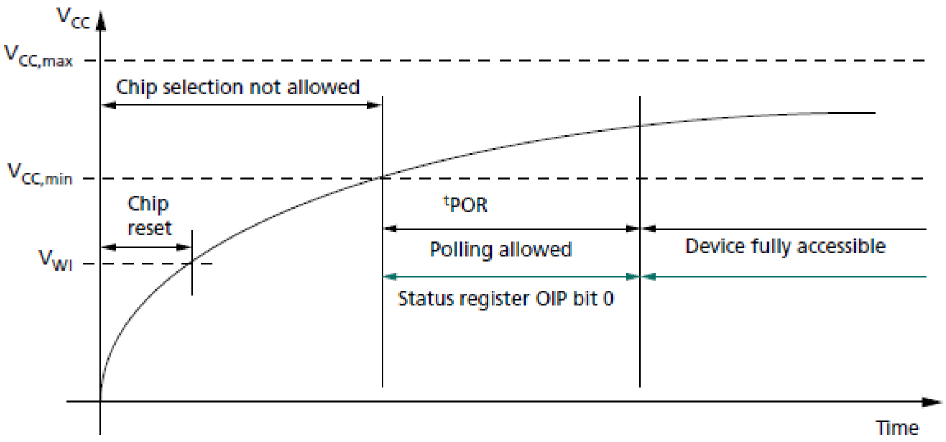
Power-Up and Power-Down

At power-up and power-down, the device must not be selected; that is, CS# must follow the voltage applied on VCC until VCC reaches the correct values: VCC, min at power-up and VSS at power-down. NAND Flash devices are designed to prevent data corruption during power transitions. VCC is internally monitored and when VCC reaches the write inhibit voltage VWI, a minimum of 250μs must elapse before issuing a RESET (FFh) command. After issuing the RESET command, 1ms must elapse before issuing any other command. GET FEATURE command could be issued to poll the status register (OIP) before the first access. Normal precautions must be taken for supply line decoupling to stabilize the VCC supply. Each device in a system should have the VCC line decoupled by a suitable capacitor (typically 100nF) close to the package pins.

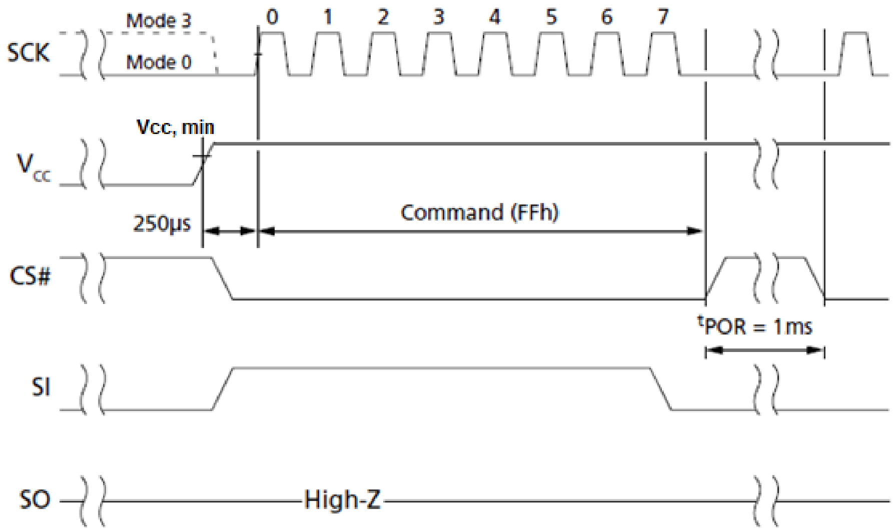
At power-down, the device is designed to offer protection from any involuntary operation during power-transitions. An internal voltage detector disables all functions whenever VCC is below VWI.

Note: For power cycle testing, the system must not initiate the power-up sequence until VCC drops down to 0V.

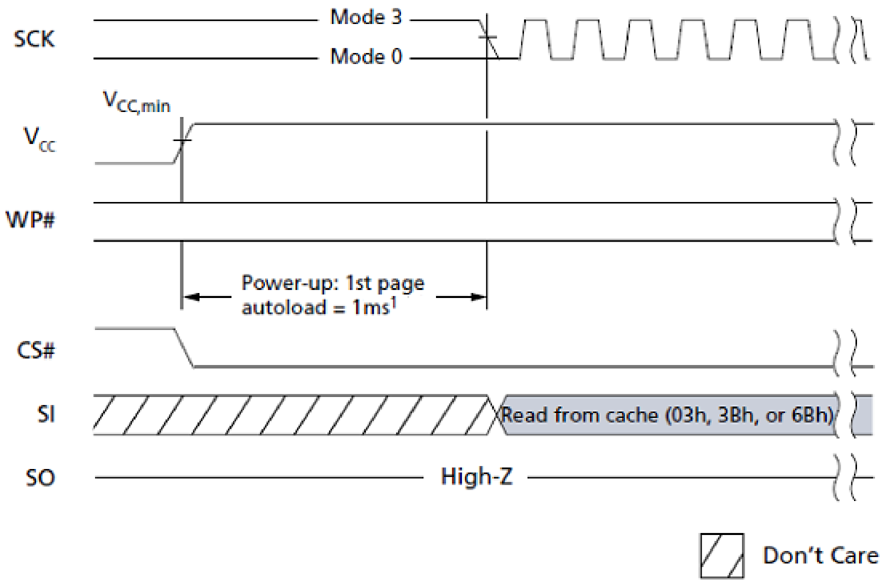
SPI Power-Up



SPI Power-Up Timing



Developed an alternative SPI NAND sequence that does not require issuing an explicit RESET(FFh) command upon power-up. This is default device initialization setting. When device V_{CC} has reached the write inhibit voltage, the device automatically kicks off the initialization. At default setting, first page data would be automatically loaded into cache register. During the initialization, GET FEATURE command could be issued to poll the status register (OIP) before the first access; Or, the first access can occur 1.25ms after V_{CC} reaches $V_{CC,min}$.



Note:

1. Poll status register OIP bit is allowed during device initialization. During initialization, page autoload is independent of the state of CS#.

Read Unique ID Page / Read Parameter Page / Read CASN Page / OTP Operations

In addition to the main memory array, the device is also equipped with one Unique ID Page, and twenty-eight One-Time-Programmable Pages. The Unique ID Page contains 16 identical copies of the 32-Byte data. The Parameter Page contains 3 identical copies of the 256-Byte data. The CASN Page contains 3 identical copies of the 256-Byte data. Both pages are Read only.

This flash device also offers one-time programmable memory area. 28 full pages of OTP data are available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands. Regarding OTP Read, Read Unique ID Page, Read Parameter Page and Read CASN Page, please refers to the specific Page addresses defined in OTP Area Details Table.

The OTP area leaves the factory in an unwritten state. The OTP area cannot be erased, whether it is protected or not. Protecting the OTP area prevents further programming of that area. It means the OTP area becomes read-only after being locked.

The OTP area is only accessible while CFG[2:0]=010b. To set the device to OTP operation mode, issue the Set Feature (1Fh) command. When the device is in OTP operation mode, subsequent Read and/or Page Program (both X1 and X4) are applied to the OTP area. Please refer to relative command sequences defined in datasheet. When you want to come back to normal operation, you need to set CFG[2:0]=000b. Otherwise, device will stay in OTP mode.

OTP/ Read / Read Unique ID / Read Parameter Page / Read CASN Page:

- Issue the Set Feature (1Fh) command.
- Issue the feature address (B0h).
- Set CFG[2:0] =010b.
- Issue the Page Read (13h) command with a specific Page address.

OTP Program:

- Issue the Set Feature (1Fh) command.
- Issue the feature address (A0h).
- Set Protection bit to 0.
- Issue the feature address (B0h).
- Set CFG[2:0] =010b.
- Issue the Write Enable (06h) command.
- Issue the Program Load (02h) and Program Execute (10h) commands.

OTP Lock:

- Issue the Set Feature (1Fh) command.
- Issue the feature address (A0h).
- Set Protection bit to 0.
- Issue the feature address (B0h).
- Set CFG[2:0] =110b.
- Issue the Write Enable (06h) command.
- Issue the Program Execute (10h) command.

OTP Area Details Table

Item	Value	Description	Data Length
Unique ID Page address	00h	Factory programmed, Read only	32-Byte x 16
Parameter Page address / CASN Page address	01h	Factory programmed, Read only	256-Byte x 6
Number of OTP pages	28	One Time Program and OTP lockable	2112-Byte
OTP page address	02h – 1Dh	One Time Program and OTP lockable	2112-Byte
Number of partial page programs for each page in the OTP area	1	One Time Program and OTP lockable	2112-Byte

Parameter Page Data Table

Byte	Description	Value
0-3	Parameter page signature ("O", "N", "F", "I")	4Fh, 4Eh, 46h, 49h
4-5	Revision number	00h, 00h
6-7	Features supported	00h, 00h
8-9	Optional commands supported	06h, 00h
10-31	Reserved	All 00h
32-43	Device manufacturer	45h, 53h, 4Dh, 54h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
44-63	Device model	46h, 35h, 30h, 4Ch, 31h, 47h, 34h, 31h, 4Ch, 43h, 50h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID	8Ch
65-66	Date code	00h, 00h
67-79	Reserved	All 00h
80-83	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	Number of spare bytes per page	40h, 00h
86-89	Number of data bytes per partial page	00h, 02h, 00h, 00h
90-91	Number of spare bytes per partial page	10h, 00h
92-95	Number of pages per block	40h, 00h, 00h, 00h
96-99	Number of blocks per unit	00h, 04h, 00h, 00h
100	Number of logical units	01h
101	Number of address cycles	00h
102	Number of bits per cell	01h
103-104	Number of maximum bad blocks per unit	14h, 00h
105-106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	01h
108-109	Block endurance of guaranteed valid blocks	00h, 00h
110	Number of partial programs per page	04h
111	Reserved	00h
112	Number of bits ECC	00h
113	Number of Interleaved address bits	00h
114	Interleaved operation attributes	00h
115-127	Reserved	All 00h
128	I/O pin capacitance	08h
129-130	Timing mode support (Reserved)	00h, 00h
131-132	Program cache timing mode support (Reserved)	00h, 00h
133-134	tPROG (max)	84h, 03h
135-136	tBERS (max)	10h, 27h
137-138	tR (max)	64h, 00h
139-140	tCCS (min)	00h, 00h
141-163	Reserved	All 00h
164-165	Vendor-specific revision number	00h, 00h
166-253	Reserved	All 00h
254-255	Integrity CRC	Set at test
256-511	Values of bytes 0-255	Values of bytes 0-255
512-767	Values of bytes 0-255	Values of bytes 0-255

CASN Page Data Table

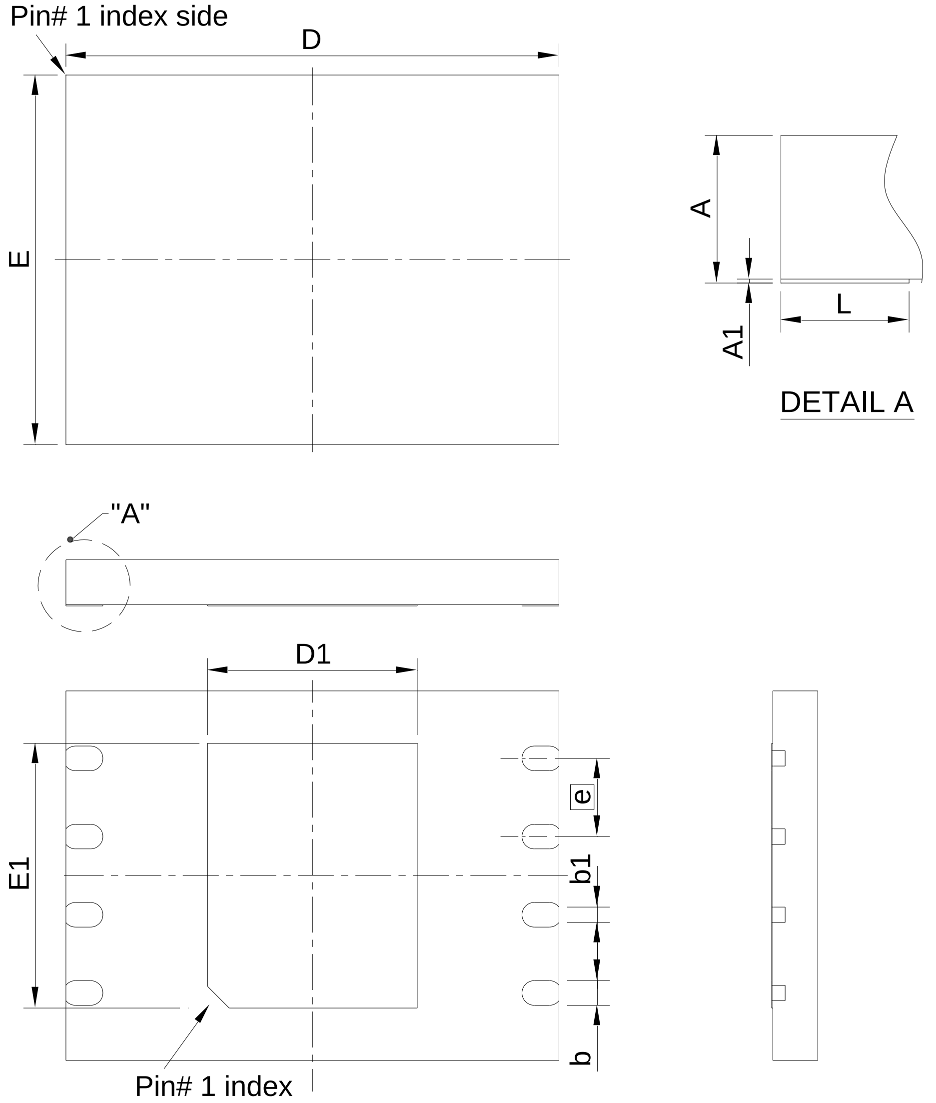
Byte	Description	Value
768~771	Symbol (CASN)	43h, 41h, 53h, 4Eh
772	Version + Subversion	10h
773~785	Manufacturer name	45h, 53h, 4Dh, 54h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
786~801	Model name	
	F50L1G41LC	46h, 35h, 30h, 4Ch, 31h, 47h, 34h, 31h, 4Ch, 43h, 20h, 20h, 20h, 20h, 20h, 20h
802~805	Bits per cell (1: SLC, 2: MLC, 3:TLC)	00h, 00h, 00h, 01h
806~809	Page size (do not include OOB)	00h, 00h, 08h, 00h
810~813	OOB size (physical)	00h, 00h, 00h, 40h
814~817	Pages per block	00h, 00h, 00h, 40h
818~821	Erase block per lun	00h, 00h, 04h, 00h
822~825	Max bad blocks per lun	00h, 00h, 00h, 14h
826~829	Planes per lun (logical)	00h, 00h, 00h, 01h
830~833	Luns per target	00h, 00h, 00h, 01h
834~837	Total targets	00h, 00h, 00h, 01h
838~841	ECC strength (decimal)	00h, 00h, 00h, 01h
842~845	ECC step size (decimal)	00h, 00h, 02h, 00h
846	Flags	18h
847	Reserved	00h
848~849	SDR Read ability	00h, 3Fh
850~851	SDR 1_1_1 read	03h, 21h
852~853	SDR 1_1_1 fast read	0Bh, 21h
854~855	SDR 1_1_2 read (x2)	3Bh, 21h
856~857	SDR 1_2_2 read (dual)	BBh, 21h
858~859	SDR 1_1_4 read (x4)	6Bh, 21h
860~861	SDR 1_4_4 read (Quad)	EBh, 22h

862~863	SDR 1_1_8 read (x8)	00h, 00h
864~865	SDR 1_8_8 read (Octal)	00h, 00h
866~867	(Continuous) SDR 1_1_1 read	00h, 00h
868~869	(Continuous) SDR 1_1_1 fast read	00h, 00h
870~871	(Continuous) SDR 1_1_2 read (x2)	00h, 00h
872~873	(Continuous) SDR 1_2_2 read (dual)	00h, 00h
874~875	(Continuous) SDR 1_1_4 read (x4)	00h, 00h
876~877	(Continuous) SDR 1_4_4 read (Quad)	00h, 00h
878~879	(Continuous) SDR 1_1_8 read (x8)	00h, 00h
880~881	(Continuous) SDR 1_8_8 read (Octal)	00h, 00h
882~883	DDR Read ability	00h, 00h
884~885	DDR 1_1_1 read	00h, 00h
886~887	DDR 1_1_1 fast read	00h, 00h
888~889	DDR 1_1_2 read (x2)	00h, 00h
890~891	DDR 1_2_2 read (dual)	00h, 00h
892~893	DDR 1_1_4 read (x4)	00h, 00h
894~895	DDR 1_4_4 read (Quad)	00h, 00h
896~897	DDR 1_1_8 read (x8)	00h, 00h
898~899	DDR 1_8_8 read (Octal)	00h, 00h
900~901	(Continuous) DDR 1_1_1 read	00h, 00h
902~903	(Continuous) DDR 1_1_1 fast read	00h, 00h
904~905	(Continuous) DDR 1_1_2 read (x2)	00h, 00h
906~907	(Continuous) DDR 1_2_2 read (dual)	00h, 00h
908~909	(Continuous) DDR 1_1_4 read (x4)	00h, 00h
910~911	(Continuous) DDR 1_4_4 read (Quad)	00h, 00h
912~913	(Continuous) DDR 1_1_8 read (x8)	00h, 00h
914~915	(Continuous) DDR 1_8_8 read (Octal)	00h, 00h
916	SDR Program load ability	03h
917~918	SDR 1_1_1 program load	02h, 20h
919~920	SDR 1_1_4 program load (x4)	32h, 20h
921~922	Reserved	00h, 00h
923~924	Reserved	00h, 00h
925~926	Reserved	00h, 00h
927~928	Reserved	00h, 00h
929~930	Reserved	00h, 00h
931~932	Reserved	00h, 00h
933	DDR Program load ability	00h
934~935	Reserved	00h, 00h
936~937	Reserved	00h, 00h
938~939	Reserved	00h, 00h
940~941	Reserved	00h, 00h

942~943	Reserved	00h, 00h
944~945	Reserved	00h, 00h
946~947	Reserved	00h, 00h
948~949	Reserved	00h, 00h
950	SDR Random program load ability	03h
951~952	SDR 1_1_1 random program load	84h, 20h
953~954	SDR 1_1_4 random program load	34h, 20h
955~956	Reserved	00h, 00h
957~958	Reserved	00h, 00h
959~960	Reserved	00h, 00h
961~962	Reserved	00h, 00h
963~964	Reserved	00h, 00h
965~966	Reserved	00h, 00h
967	DDR Random program load ability	00h
968~969	Reserved	00h, 00h
970~971	Reserved	00h, 00h
972~973	Reserved	00h, 00h
974~975	Reserved	00h, 00h
976~977	Reserved	00h, 00h
978~979	Reserved	00h, 00h
980~981	Reserved	00h, 00h
982~983	Reserved	00h, 00h
984	OOB overall layout	00h
985~987	OOB free layout	
	OOB free start	00h
	OOB free length	08h
	BBM (bad block mark) length	02h
988~990	ECC parity layout	
	ECC parity start	08h
	ECC parity space	08h
	ECC parity (real) length	08h
991~1001	Advanced ECC status CMD0 (higher bit)	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
1002~1012	Advanced ECC status CMD1 (lower bit)	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
1013	ECC no error status	00h
1014	ECC uncorrectable status	00h
1015~1016	If correctable bit flips happen (return ECC max if number exceeds ECC max capability)	00h,00h
1017~1021	Reserved	00h, 00h, 00h, 00h, 00h
1022~1023	CRC	Set at Test
1024~1279	Value of bytes 768~1023	Value of bytes 768~1023
1280~1535	Value of bytes 768~1023	Value of bytes 768~1023

PACKING DIMENSIONS

8-Contact WSON (8x6 mm)

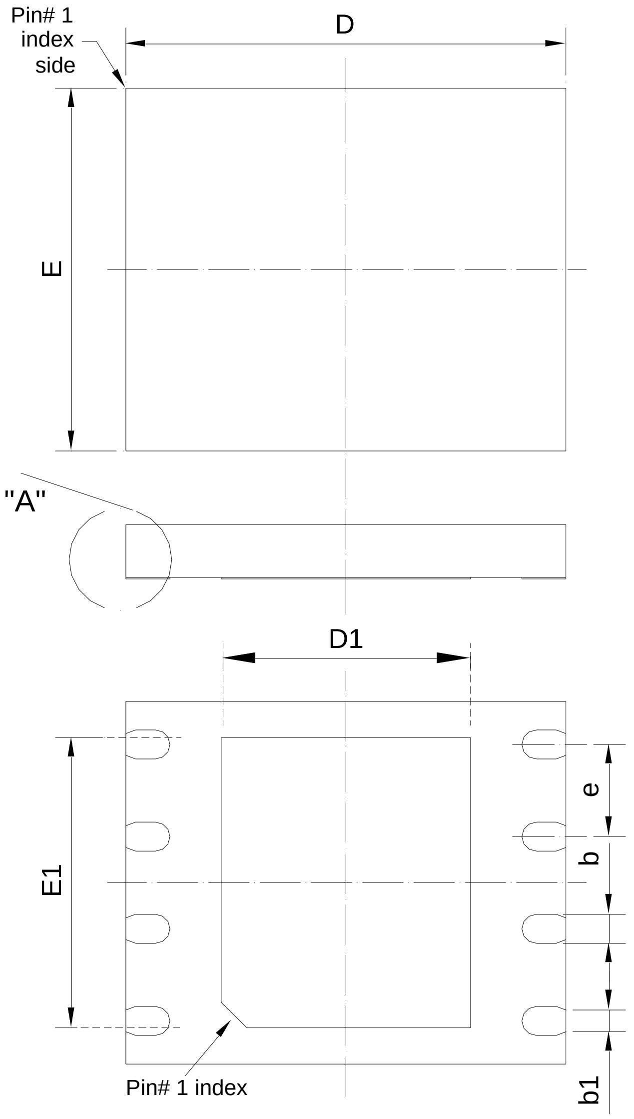


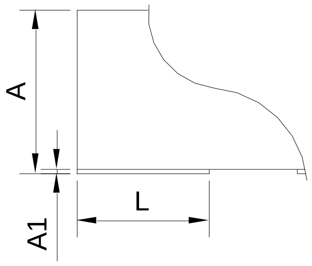
Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.48	0.014	0.016	0.019
b1	0.22	-	0.48	0.009	-	0.019
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	3.30	3.40	3.50	0.130	0.134	0.138
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	4.20	4.30	4.40	0.165	0.169	0.173
e	1.27 BSC			0.050 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024

Controlling dimension : Millimeter.
(Revision date : Sep 09. 2025)

PACKING DIMENSIONS

8-Contact WSON (6x5 mm)





DETAIL : "A"

Symbol	Dimension in mm			Dimension in inch		
	Min	Min	Min	Min	Norm	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
b1	0.30 REF			0.012 REF		
D	5.90	6.00	6.10	0.232	0.236	0.240
D1	3.30	3.40	3.50	0.130	0.134	0.138
E	4.90	5.00	5.10	0.193	0.197	0.201
E1	3.90	--	4.40	0.154	--	0.173
e	1.27 BSC			0.050 BSC		
L	0.50	0.60	0.70	0.020	0.024	0.028

Controlling dimension : Millimeter.
(Revision date : Dec 08 2025)

Revision History

Revision	Date	Description
0.1	2024.08.19	Original
1.0	2025.02.17	Modify: 1. Version upgrade / “Preliminary” deleted 2. General description 3. CASN page related data
1.1	2025.07.10	Modify: Read ID Timing diagram
1.2	2025.09.18	Modify 8-contact WSON PKG dimension
1.3	2026.01.13	Add 8-contact WSON 6x5mm package