



F5N50K-TC

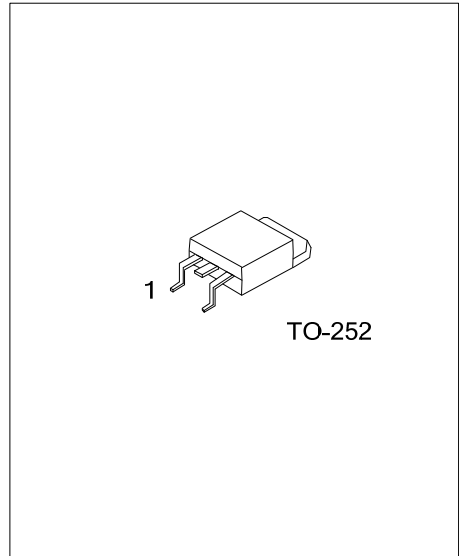
Power MOSFET

**5.0A, 500V N-CHANNEL
POWER MOSFET**

■ DESCRIPTION

The UTC **F5N50K-TC** is a N-channel power MOSFET adopting UTC's advanced technology to provide customers with DMOS, planar stripe technology. This technology is designed to meet the requirements of the minimum on-state resistance and perfect switching performance. It also can withstand high energy pulse in the avalanche and communication mode.

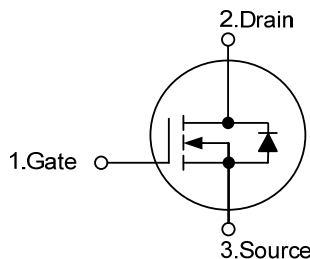
The UTC **F5N50K-TC** can be used in applications, such as active power factor correction, high efficiency switched mode power supplies, electronic lamp ballasts based on half bridge topology.



■ FEATURES

- * $R_{DS(ON)} \leq 1.8\Omega @ V_{GS}=10V, I_D=2.5A$
- * 100% avalanche tested
- * High switching speed

■ SYMBOL



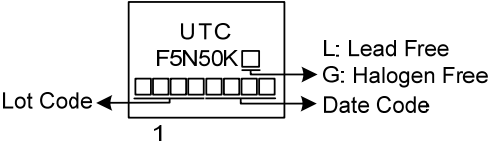
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
F5N50KL-TN3-R	F5N50KG-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>F5N50KG-TN3-R</p> <ul style="list-style-type: none"> (1)Packing Type (2)Package Type (3)Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) TN3: TO-252 (3) G: Halogen Free and Lead Free, L: Lead Free
---	--

MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	5	A
	Pulsed (Note 2)	I_{DM}	20	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	104	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	6.3	V/ns
Power Dissipation		P_D	54	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3. $L = 16\text{mH}$, $I_{AS} = 3.6\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 5.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case		θ_{JC}	2.3	$^\circ\text{C}/\text{W}$

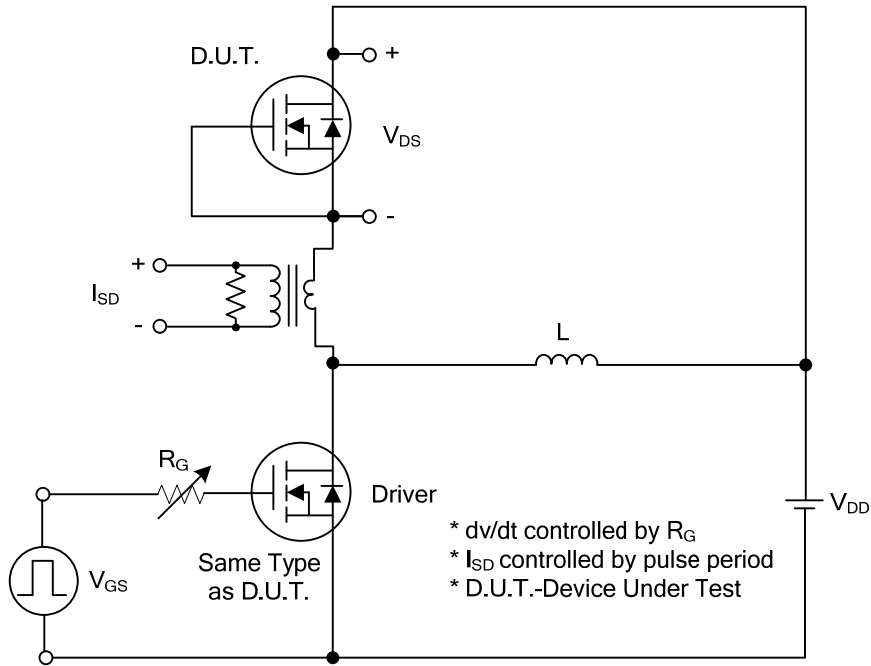
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS								
Drain-Source Breakdown Voltage		BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	500			V	
Drain-Source Leakage Current		I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			1	μA	
Gate- Source Leakage Current	Forward	I_{GSS}	$V_{GS}=30\text{V}$, $V_{DS}=0\text{V}$			100	nA	
	Reverse		$V_{GS}=-30\text{V}$, $V_{DS}=0\text{V}$			-100	nA	
ON CHARACTERISTICS								
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V	
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=2.5\text{A}$			1.8	Ω	
DYNAMIC PARAMETERS								
Input Capacitance		C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		585		pF	
Output Capacitance		C_{OSS}				58		pF
Reverse Transfer Capacitance		C_{RSS}			7.0			pF
SWITCHING PARAMETERS								
Total Gate Charge (Note 1)		Q_G	$V_{DS}=200\text{V}$, $V_{GS}=10\text{V}$, $I_D=5.0\text{A}$ $I_G=1\text{mA}$ (Note 1, 2)		5.2		nC	
Gate to Source Charge		Q_{GS}				2.8		nC
Gate to Drain Charge		Q_{GD}				1.1		nC
Turn-ON Delay Time (Note 1)		$t_{D(ON)}$	$V_{DD}=30\text{V}$, $V_{GS}=10\text{V}$, $D=0.75\text{A}$, $R_G = 25\Omega$ (Note 1, 2)		7.6		ns	
Rise Time		t_R				18.6		ns
Turn-OFF Delay Time		$t_{D(OFF)}$				36		ns
Fall-Time		t_F				18		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS								
Maximum Body-Diode Continuous Current		I_S				5	A	
Maximum Body-Diode Pulsed Current		I_{SM}				20	A	
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	$I_S=5.0\text{A}$, $V_{GS}=0\text{V}$			1.4	V	
Body Diode Reverse Recovery Time (Note 1)		t_{rr}	$I_S=5.0\text{A}$, $V_{GS}=0\text{V}$,			102	ns	
Body Diode Reverse Recovery Charge		Q_{rr}	$di_F/dt=100\text{A}/\mu\text{s}$			0.33	μC	

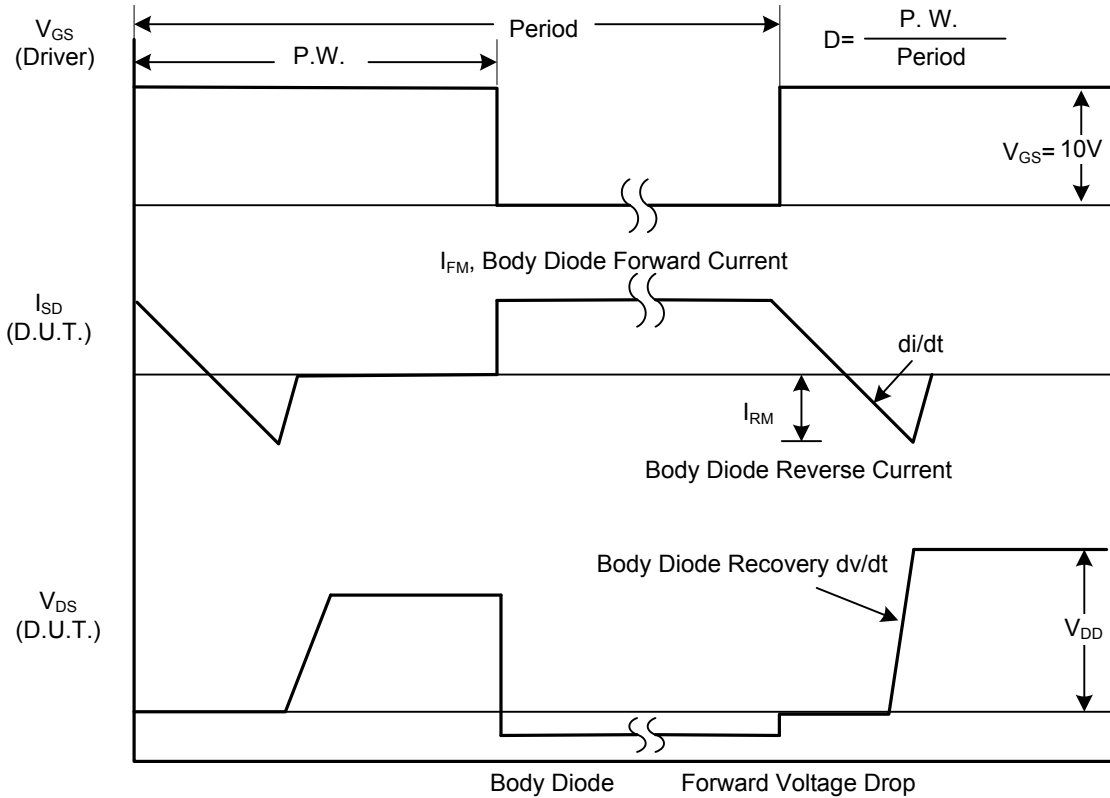
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature.

TEST CIRCUITS AND WAVEFORMS

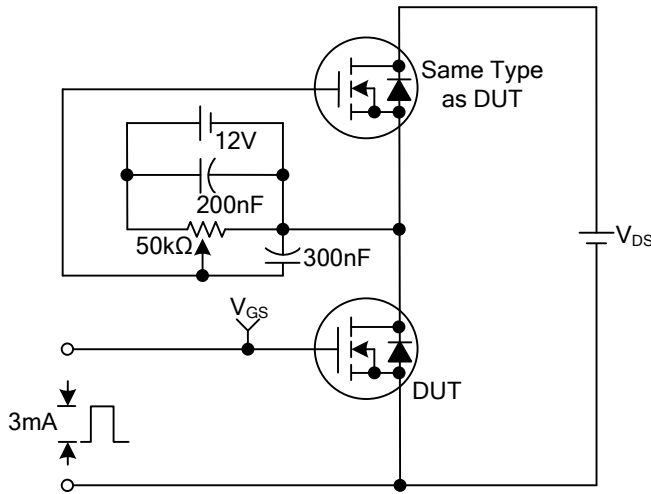


Peak Diode Recovery dv/dt Test Circuit

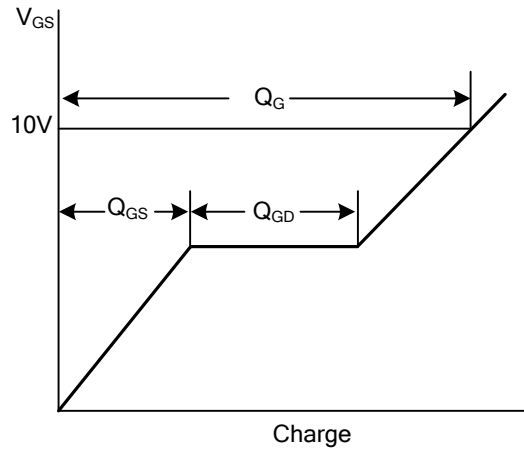


Peak Diode Recovery dv/dt Waveforms

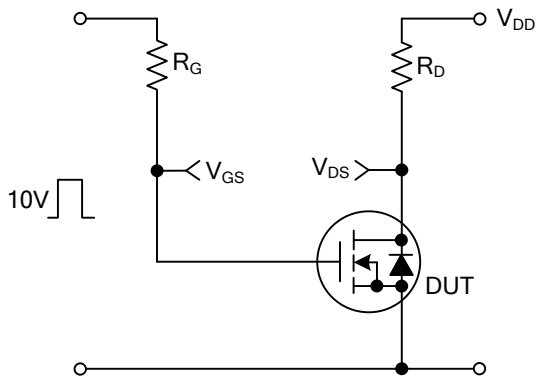
TEST CIRCUITS AND WAVEFORMS



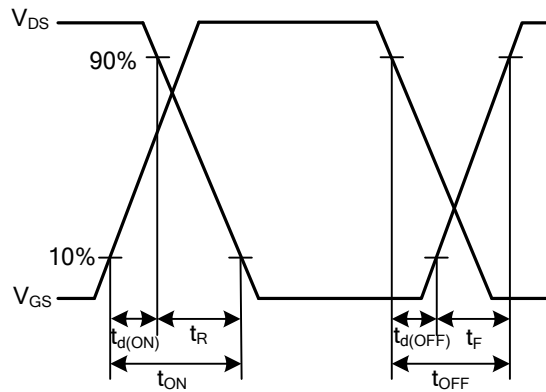
Gate Charge Test Circuit



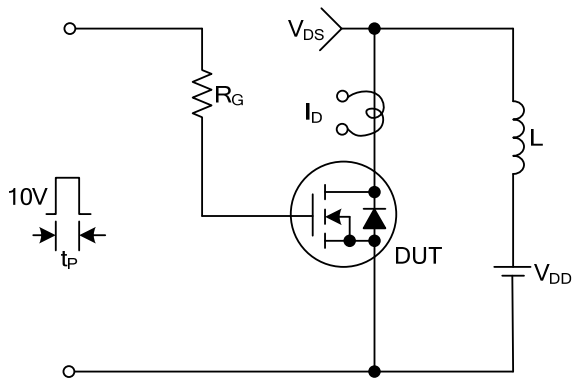
Gate Charge Waveforms



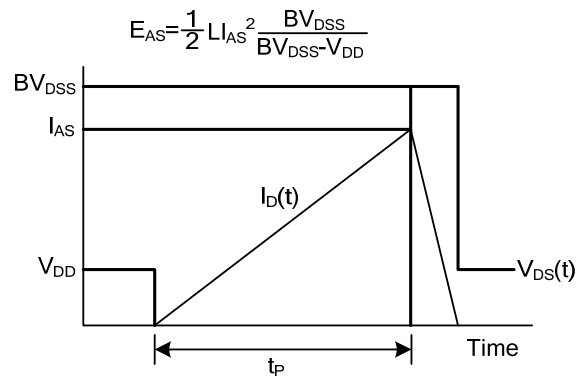
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.