

General Description

This planar stripe MOSFET has better characteristics, such as fast switching time, low on resistance, low gate charge and excellent avalanche characteristics. It is mainly suitable for active power factor correction, electronic lamp ballasts based on half bridge topology, DC/DC Converters and switching mode power supplies.

FEATURES

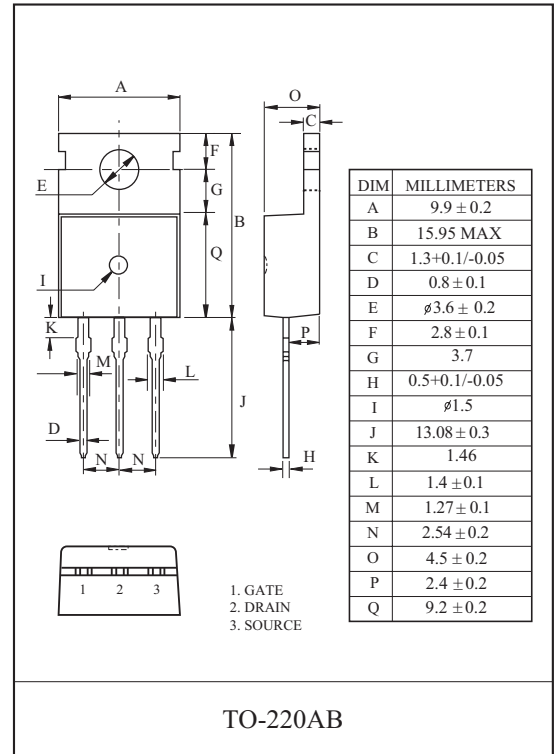
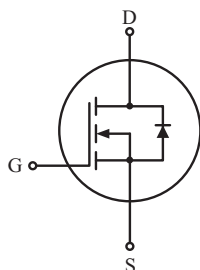
- $V_{DSS} = 60V$, $I_D = 60A$
- Drain-Source ON Resistance :
 $R_{DS(ON)} = 13.2m\ \Omega$ (Max.) @ $V_{GS} = 10V$
- Qg (typ.) = 48nC

MOSFET MAXIMUM RATING (Ta=25 °C Unless otherwise noted)

| CHARACTERISTIC | | SYMBOL | RATING | UNIT |
|---|-----------------|------------|----------|------|
| Drain-Source Voltage | | V_{DSS} | 60 | V |
| Gate-Source Voltage | | V_{GSS} | ± 20 | V |
| Drain Current | @ $T_C=25$ | I_D^* | 60 | A |
| | @ $T_C=100$ | | 37 | |
| | Pulsed (Note1) | I_{DP} | 230 | |
| Single Pulsed Avalanche Energy (Note 2) | | E_{AS} | 430 | mJ |
| Repetitive Avalanche Energy (Note 1) | | E_{AR} | 13.5 | mJ |
| Peak Diode Recovery dv/dt (Note 3) | | dv/dt | 4.5 | V/ns |
| Drain Power Dissipation | $T_C=25$ | P_D | 113 | W |
| | Derate above 25 | | 0.90 | W/ |
| Maximum Junction Temperature | | T_j | 150 | |
| Storage Temperature Range | | T_{stg} | -55 150 | |
| Thermal Characteristics | | | | |
| Thermal Resistance, Junction-to-Case | | R_{thJC} | 1.1 | /W |
| Thermal Resistance, Junction-to-Ambient | | R_{thJA} | 62.5 | /W |

* : Drain current limited by maximum junction temperature.

PIN CONNECTION



KF60N06P

ELECTRICAL CHARACTERISTICS (T_c=25 °C)

| CHARACTERISTIC | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|------------------------------------|---|------|------|-------|------|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | BV _{DSS} | I _D =250 μA, V _{GS} =0V | 60 | - | - | V |
| Breakdown Voltage Temperature Coefficient | BV _{DSS} / T _j | I _D =250 μA, Referenced to 25 | - | 0.08 | - | V/ |
| Drain Cut-off Current | I _{DSS} | V _{DS} =60V, V _{GS} =0V, | - | - | 10 | μA |
| Gate Threshold Voltage | V _{th} | V _{DS} =V _{GS} , I _D =250 μA | 2 | - | 4 | V |
| Gate Leakage Current | I _{GSS} | V _{GS} =± 20V, V _{DS} =0V | - | - | ± 100 | nA |
| Drain-Source ON Resistance | R _{DS(ON)} | V _{GS} =10V, I _D =30A | - | 11.5 | 13.2 | m |
| Dynamic | | | | | | |
| Total Gate Charge | Q _g | V _{DS} =48V, I _D =60A V _{GS} =10V (Note4,5) | - | 48 | - | nC |
| Gate-Source Charge | Q _{gs} | | - | 9.2 | - | |
| Gate-Drain Charge | Q _{gd} | | - | 19 | - | |
| Turn-on Delay time | t _{d(on)} | V _{DD} =30V I _D =60A R _G =25 (Note4,5) | - | 35 | - | ns |
| Turn-on Rise time | t _r | | - | 75 | - | |
| Turn-off Delay time | t _{d(off)} | | - | 100 | - | |
| Turn-off Fall time | t _f | | - | 75 | - | |
| Input Capacitance | C _{iss} | V _{DS} =25V, V _{GS} =0V, f=1.0MHz | - | 1860 | - | pF |
| Output Capacitance | C _{oss} | | - | 490 | - | |
| Reverse Transfer Capacitance | C _{rss} | | - | 92 | - | |
| Source-Drain Diode Ratings | | | | | | |
| Continuous Source Current | I _S | V _{GS} <V _{th} | - | - | 60 | A |
| Pulsed Source Current | I _{SP} | | - | - | 240 | |
| Diode Forward Voltage | V _{SD} | I _S =60A, V _{GS} =0V | - | - | 1.4 | V |
| Reverse Recovery Time | t _{rr} | I _S =60A, V _{GS} =0V, dI _S /dt=100A/μs | - | 70 | - | ns |
| Reverse Recovery Charge | Q _{rr} | | - | 180 | - | nC |

Note 1) Repetivity rating : Pulse width limited by junction temperature.

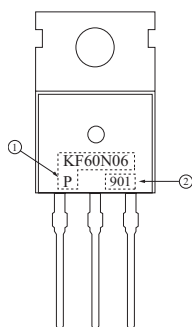
Note 2) L =120 μH, I_S=60A, V_{DD}=30V, R_G=25 Ω, Starting T_j=25 °C.

Note 3) I_S 60A, dI/dt 200A/μs, V_{DD} BV_{DSS}, Starting T_j=25 °C.

Note 4) Pulse Test : Pulse width 300μs, Duty Cycle 2%.

Note 5) Essentially independent of operating temperature.

Marking



① PRODUCT NAME
② LOT NO

KF60N06P

Fig1. $I_D - V_{DS}$

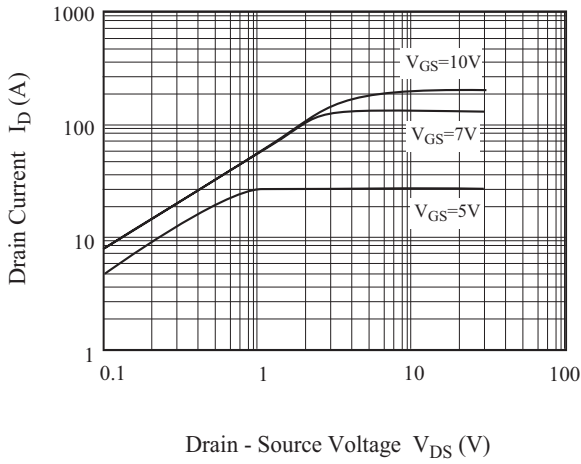


Fig2. $I_D - V_{GS}$

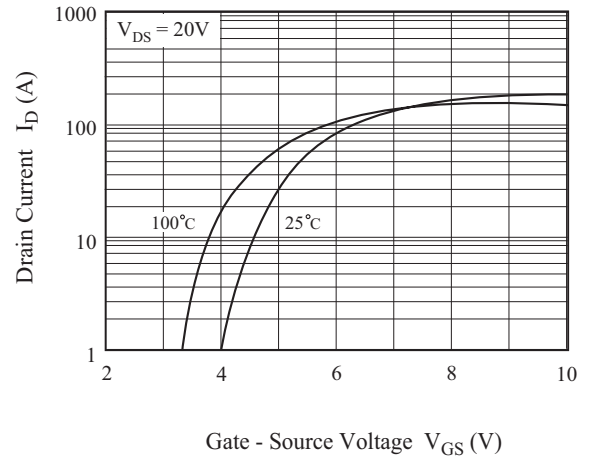


Fig3. $BV_{DSS} - T_j$

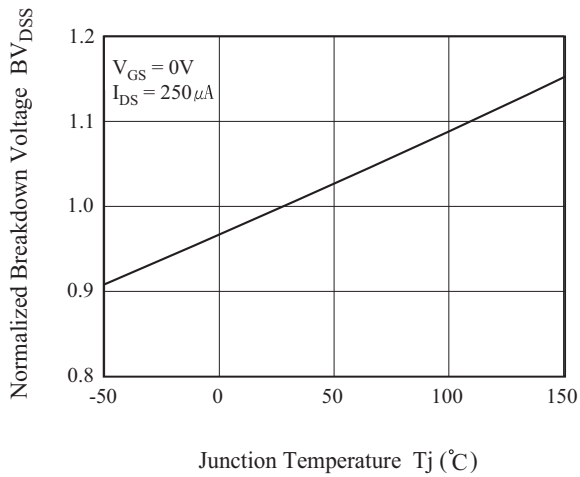


Fig4. $R_{DS(ON)} - I_D$

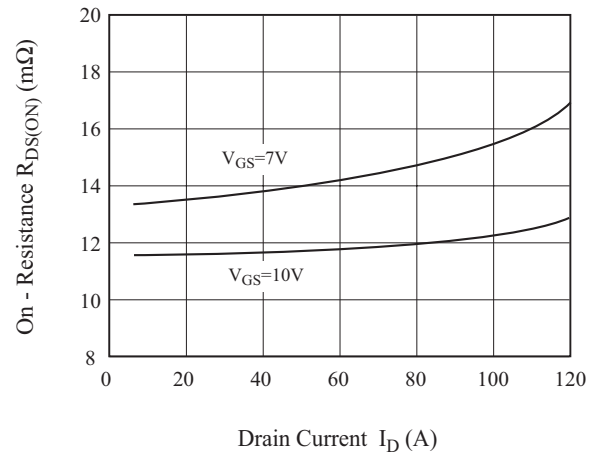


Fig5. $I_S - V_{SD}$

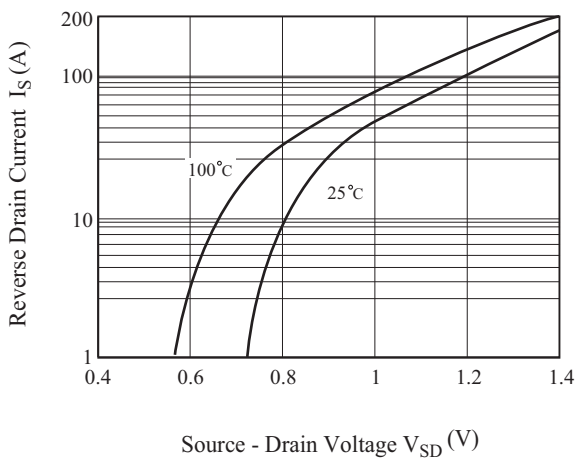
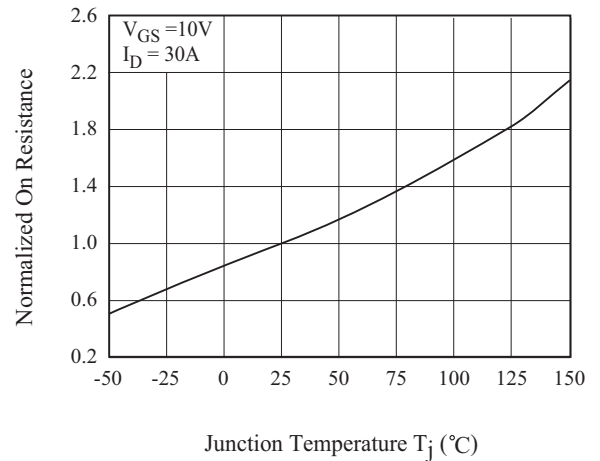


Fig6. $R_{DS(ON)} - T_j$



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Fig 7. C - V_{DS}

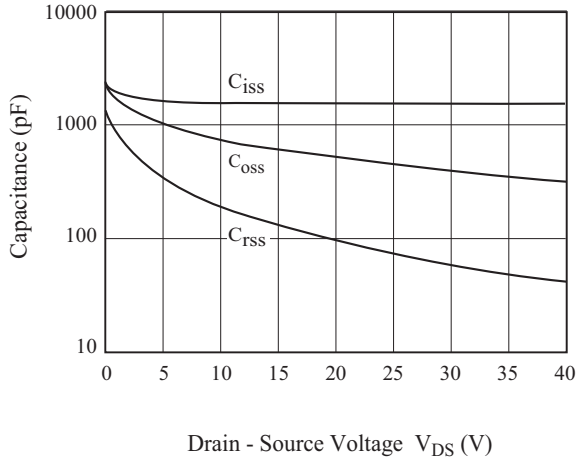


Fig 8. Q_g - V_{DS}

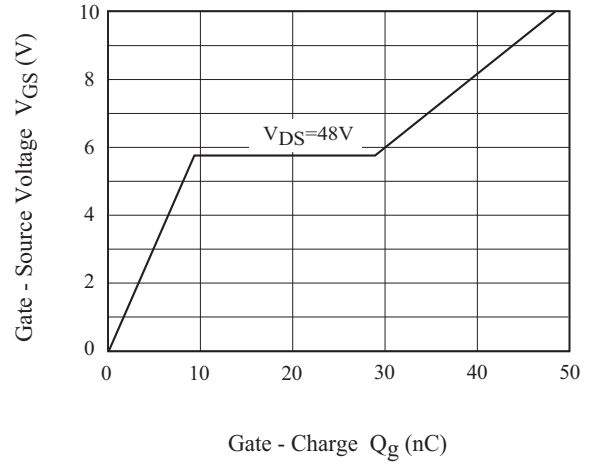


Fig 9. Safe Operation Area

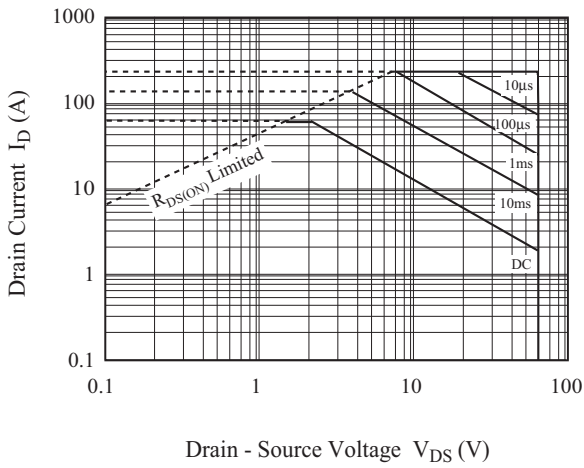


Fig 10. I_D - T_C

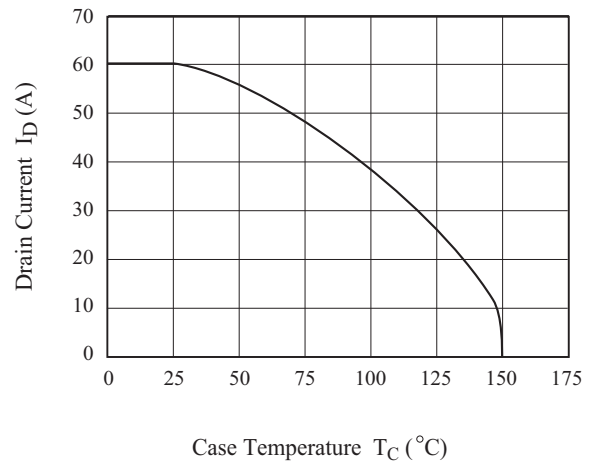
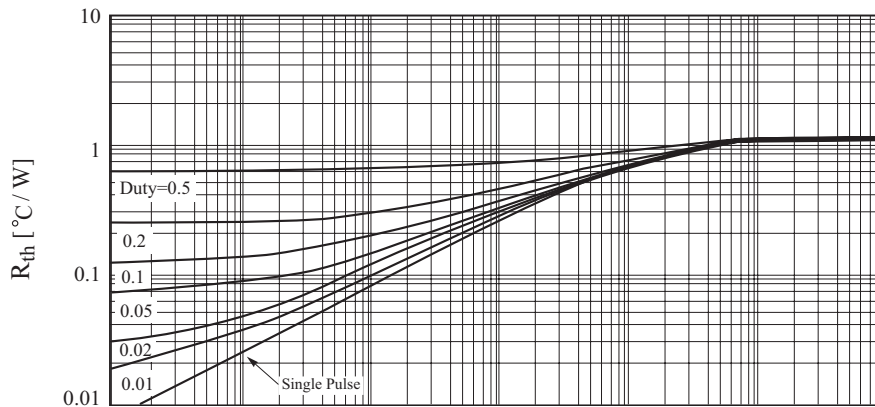


Fig 11. $R_{th}(j-c)$



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Fig12. Gate Charge

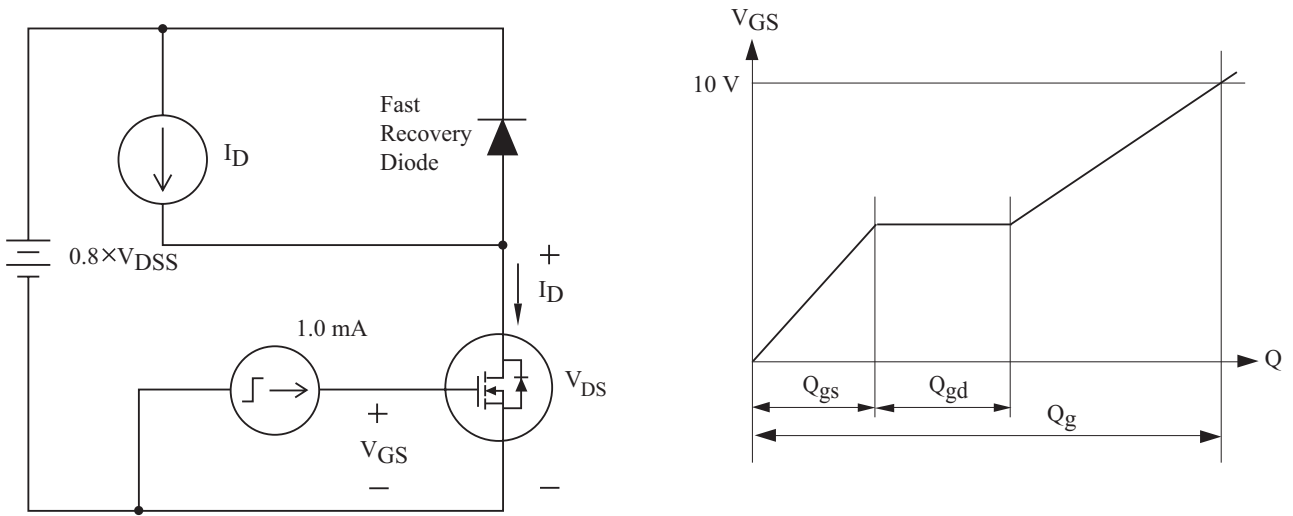


Fig13. Single Pulsed Avalanche Energy

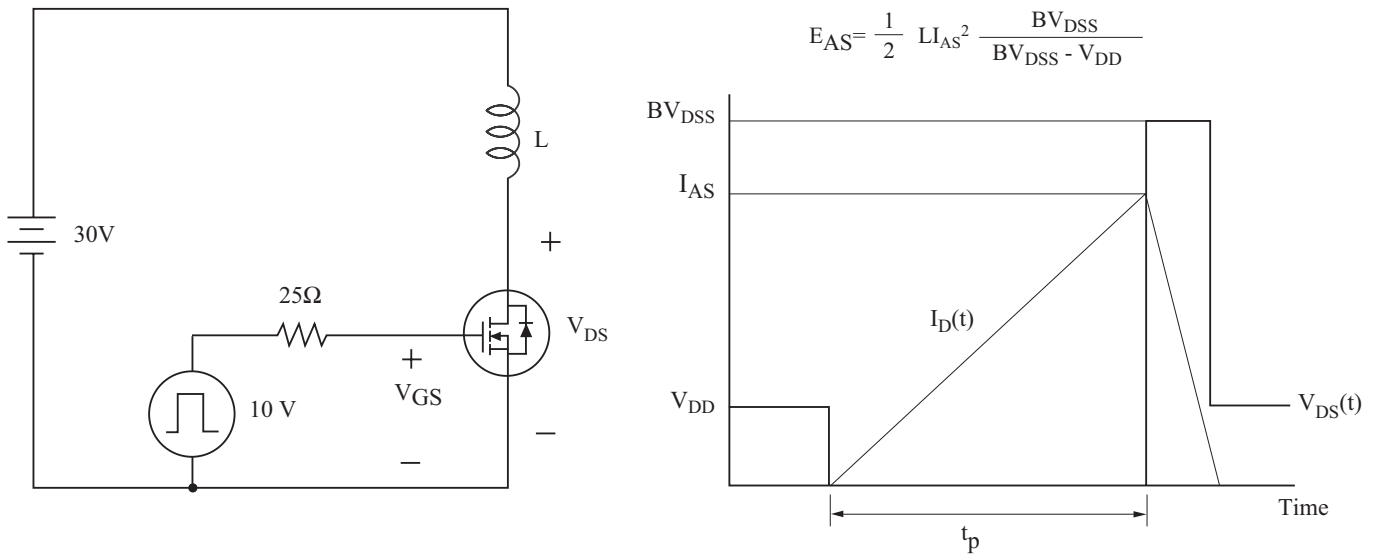


Fig14. Resistive Load Switching

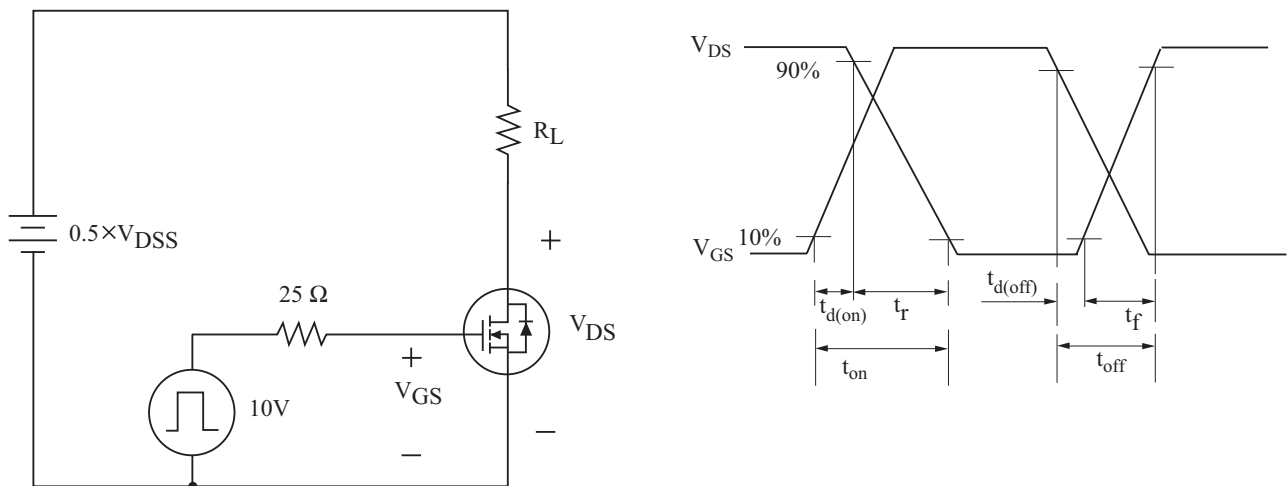


Fig15. Source - Drain Diode Reverse Recovery and dv/dt

