

## 17 ELECTRICAL SPECIFICATIONS

**Table 17-1: 65550 Absolute Maximum Conditions**

Symbol	Parameter	Min	Typical	Max	Units
P <sub>D</sub>	Power Dissipation	—	—	3.0	W
V <sub>CC</sub>	Supply Voltage†	-0.5	—	7.0	V
V <sub>I</sub>	Input Voltage	-0.5	—	V <sub>CC</sub> +0.5	V
V <sub>O</sub>	Output Voltage	-0.5	—	V <sub>CC</sub> +0.5	V
T <sub>OP</sub>	Operating Temp	-25	—	85	°C
T <sub>STG</sub>	Storage Temp	-40	—	125	°C

**Note:** Permanent device damage may occur if Absolute Maximum Rating are exceeded.  
Functional operation must be restricted to the conditions under Normal Operating Conditions.

**Table 17-2: 65550 Normal Operating Conditions**

Symbol	Parameter	Min	Typical	Max	Units
V <sub>CC5</sub>	Supply Voltage†	4.5	5.0	5.5	V
V <sub>CC33</sub>	Supply Voltage†	3.0	3.3	3.6	V
T <sub>A</sub>	Ambient Temperature	0	—	70	°C

**Table 17-3: 65550 DAC Characteristics  
(Under Normal Operating Conditions Unless Noted Otherwise)**

Symbol	Parameter	Notes	Min	Typical	Max	Units
V <sub>O</sub>	Output Voltage	I <sub>O</sub> ≤ 10 mA	1.5	—	—	V
I <sub>O</sub>	Output Current	V <sub>O</sub> ≤ 1V @ 37.5Ω Load	21	—	—	mA
	Full Scale Error		—	—	± 5	%
	DAC to DAC Correlation		—	1.27	—	%
	DAC Linearity		± 2	—	—	LSB
	Glitch Energy		—	—	200	pVsec
	Comparator Sensitivity		—	50	—	mV

**Note:**  
† IVCC and CVCC must ALWAYS be tied to the same voltage supply, and AVCC must NEVER be provided with a voltage supply that is higher than IVCC and CVCC.

**Table 17- 4: 65550 DC Characteristics  
(Under Normal Operating Conditions Unless Noted Otherwise)**

Symbol	Parameter	Notes	Min	Typical	Max	Units
P <sub>D33</sub>	Power Dissipation	All VCCs at 3.3V	–	–	1.5	W
P <sub>D50</sub>	Power Dissipation	All VCCs at 5.0V	–	–	2.5	W
I <sub>CCES</sub>	Power Supply Current	0°C, 5.5V, MCLK=40 MHz, DAC on ††	–	TBD	TBD	mA
I <sub>CCO5</sub>	Power Supply Current	0°C, 5.5V, MCLK=40 MHz, DAC off ††	–	TBD	TBD	mA
I <sub>CCES</sub>	Power Supply Current	0°C, 3.3V, MCLK=40 MHz, DAC on ††	–	TBD	TBD	mA
I <sub>CCO3</sub>	Power Supply Current	0°C, 3.3V, MCLK=40 MHz, DAC off ††	–	TBD	TBD	mA
I <sub>CCSD</sub>	Power Supply Current	0°C, 3.3V, Standby, Self Refresh DRAMs†	–	TBD	TBD	μA
I <sub>CCSS</sub>	Power Supply Current	0°C, 3.3V, Standby, SlowRfsh 32KHz in	–	TBD	TBD	μA
I <sub>CCSR</sub>	Power Supply Current	0°C, 3.3V, Standby, SlowRfsh XTALI in	–	TBD	TBD	μA
I <sub>IL</sub>	Input Leakage Current		–100	–	+100	μA
I <sub>oZ</sub>	Output Leakage Current	High Impedance	–100	–	+100	μA
V <sub>IL</sub>	Input Low Voltage	All input pins	–0.5	–	0.8	V
V <sub>IH</sub>	Input High Voltage	All input pins	2.0	–	VCC+0.5	V
V <sub>THR</sub>	Input Switch Point	All inputs except RESET# & STNDBY#	–	1.4	–	V
V <sub>HYS</sub>	Input Hysteresis	RESET# and STNDBY#	–	± 0.15	–	V
V <sub>OL5</sub>	Output Low Voltage	Under max load per table 17-5 (5V)	–	–	0.5	V
V <sub>OL3</sub>	Output Low Voltage	Under max load per table 17-5 (3.3V)	–	–	0.5	V
V <sub>OH5</sub>	Output High Voltage	Under max load per table 17-5 (5V)	2.4	–	–	V
V <sub>OH3</sub>	Output High Voltage	Under max load per table 17-5 (3.3V)	0.7xV <sub>CC</sub>	–	–	V

**Notes:**

† Measured with all chip inputs driven to inactive levels and outputs not connected (or connected to typical external loads).

†† 640x480x8bpp, TFT panel (for power data regarding other configurations, contact Chips and Technobgies, Inc.).

**Table 17- 5: 65550 DC Drive Characteristics  
(Under Normal Operating Conditions Unless Noted Otherwise)**

Symbol	Parameter	Output Pins	DC Test Conditions	Min	Units
I <sub>OL</sub>	Output Low Drive	AA0-AA9	V <sub>OUT</sub> =V <sub>OL</sub> , see note†	12	mA
		H/VSYNC, P0-P23, SHFCLK, M	V <sub>OUT</sub> =V <sub>OL</sub> , see note†	8	mA
		DEVSEL#, PAR, PERR#, SERR#, STOP#, TRDY#			
		CASAH/L#, CASBH/L#, CASCH/L#, CASDH/L#	V <sub>OUT</sub> =V <sub>OL</sub> , see note†	4	mA
		ACTI, D0-D31, ENABKL, ENAVDD, ENAVEE,FLM, LP			
COE#, RAS0#, RAS1#, WEA#, WEB#, WEC#, WED#					
I <sub>OH</sub>	Output High Drive	All other outputs	V <sub>OUT</sub> =V <sub>OL</sub> , see note†	2	mA
		AA0-AA9	V <sub>OUT</sub> =V <sub>OL</sub> , see note†	12	mA
		H/VSYNC, P0-P23, SHFCLK, M	V <sub>OUT</sub> =V <sub>OL</sub> , see note†	8	mA
		DEVSEL#, PAR, PERR#, SERR#, STOP#, TRDY#			
		CASAH/L#, CASBH/L#, CASCH/L#, CASDH/L#	V <sub>OUT</sub> =V <sub>OL</sub> , see note†	4	mA
		ACTI, D0-D31, ENABKL, ENAVDD, ENAVEE,FLM, LP			
COE#, RAS0#, RAS1#, WEA#, WEB#, WEC#, WED#					
		All other outputs	V <sub>OUT</sub> =V <sub>OL</sub> , see note†	2	mA

**Note:** †I<sub>OL</sub> & I<sub>OH</sub> drive listed above indicates 5V low drive (V<sub>CC</sub>=4.5V) and 3.3V high drive (V<sub>CC</sub>=3V), as programmed.

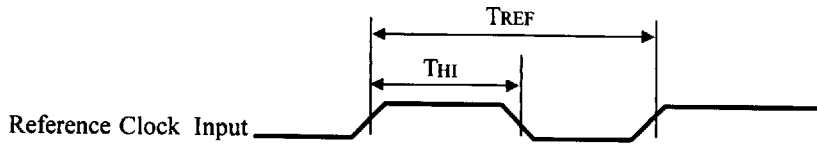
**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation.  
Electrical specifications contained herein are preliminary and subject to change without notice.

**Table 17- 6: 65550 AC Test Conditions  
(Under Normal Operating Conditions Unless Noted Otherwise)**

Output Pins	Output Low Voltage	Output High Voltage	Capacitive Load
All 12mA, 8mA, 4mA outputs plus PAR for PCI	V <sub>OL</sub>	2.4V	85pF
All Other 2mA output pads	V <sub>OL</sub>	2.4V	40pF

**Table 17- 7: 65550 AC Timing Characteristics - Reference Clock**

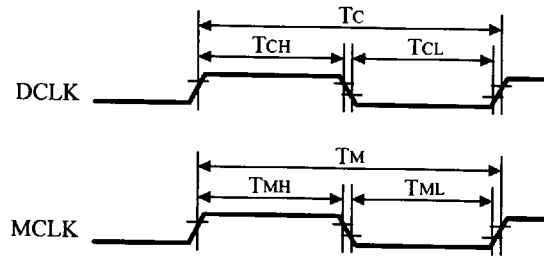
Symbol	Parameter	Notes	Min	Typical	Max	Units
F <sub>REF</sub>	Reference Frequency	(±100 ppm)	1	14.31818	60	MHz
T <sub>REF</sub>	Reference Clock Period	1/F <sub>REF</sub>	16.6	69.84128	1000	nS
T <sub>HI</sub> / T <sub>REF</sub>	Reference Clock Duty Cycle		25	-	75	%



**Figure 17-1: Reference Clock Timing**

**Table 17- 8: 65550 AC Timing Characteristics - Clock Generator**

Symbol	Parameter	Notes	Min	Typical	Max	Units
T <sub>C</sub>	DCLK Frequency (3.3V)-- 550A1		-	-	80	MHz
	DCLK Frequency (5.0V) -- 550A1 and 550A1-5		-	-	100	MHz
T <sub>C</sub>	DCLK Frequency (3.3V)-- 550B		-	-	95	MHz
T <sub>CH</sub>	DCLK High -- 550A1		TBD	-	TBD	
T <sub>CL</sub>	DCLK Low -- 550A1		TBD	-	TBD	
T <sub>CH</sub>	DCLK High -- 550B		TBD	-	TBD	
T <sub>CL</sub>	DCLK Low -- 550B		TBD	-	TBD	
T <sub>M</sub>	MCLK Frequency (3.3V)-- 550A1		-	-	38	MHz
	MCLK Frequency (5.0V) -- 550A1 and 550A1-5		-	-	38	MHz
T <sub>M</sub>	MCLK Frequency (3.3V)-- 550B		-	-	50	MHz
T <sub>MH</sub>	MCLK High -- 550A1 and 550A1-5		TBD	-	TBD	
T <sub>ML</sub>	MCLK Low -- 550A1 and 550A1-5		TBD	-	TBD	
T <sub>MH</sub>	MCLK High -- 550B		TBD	-	TBD	
T <sub>ML</sub>	MCLK Low -- 550B		TBD	-	TBD	



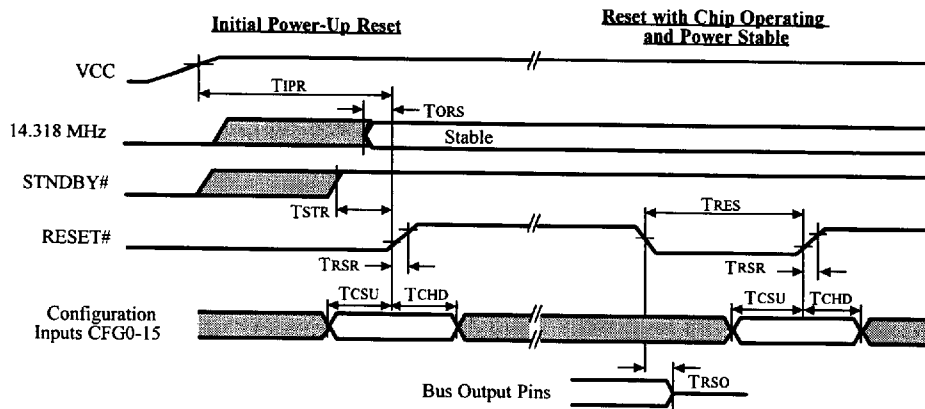
**Figure 17-2: Clock Timing**

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation.  
Electrical specifications contained herein are preliminary and subject to change without notice.

**Table 17-9: 65550 AC Timing Characteristics - Reset**

Symbol	Parameter	Notes	Min	Max	Units
T <sub>IPR</sub>	Reset Active Time from Power Stable	See Note 1	5	–	mS
T <sub>ORS</sub>	Reset Active Time from Ext. Osc. Stable		0	–	mS
T <sub>RES</sub>	Reset Active Time with Power Stable	See Note 2	2	–	mS
T <sub>STR</sub>	Reset Active Time from Standby	RESET# is ignored in Standby Mode	2	–	mS
T <sub>RSR</sub>	Reset Rise Time	Reset fall time is non-critical	–	20	nS
T <sub>RSO</sub>	Reset Active to Output Float Delay		–	40	nS
T <sub>CSU</sub>	Configuration Setup Time	See Note 3	20	–	nS
T <sub>CHD</sub>	Configuration Hold Time		5	–	nS

- Note 1:** This parameter includes time for internal voltage stabilization of all sections of the chip, startup and stabilization of the internal clock synthesizer, and setting of all internal logic to a known state.
- Note 2:** This parameter includes time for the internal clock synthesizer to reset to its default frequency and time to set all internal logic to a known state. It assumes power is stable and the internal clock synthesizer is already operating at some stable frequency.
- Note 3:** This parameter specifies the setup time to latch reliably the state of the configuration bits. Changes in some configuration bits may take longer to stabilize inside the chip (such as internal clock synthesizer-related bits 4 and 5). The recommended configuration bit setup time is T<sub>RES</sub> (2mS) to insure that the chip is in a completely stable state when Reset goes inactive.



**Figure 17-3: Reset Timing**

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation. Electrical specifications contained herein are preliminary and subject to change without notice.

Table 17- 10: 65550 AC Timing Characteristics - PCI Bus Frame(33 MHz)

Symbol	Parameter	Notes	Min	Max	Units
T <sub>FRS</sub>	FRAME# Setup to CLK		7	-	nS
T <sub>CMS</sub>	C/BE#[3:0] (Bus CMD) Setup to CLK		7	-	nS
T <sub>CMH</sub>	C/BE#[31:0] (Bus CMD) Hold from CLK		2	-	nS
T <sub>BES</sub>	C/BE#[3:0] (Byte Enable) Setup to CLK		7	-	nS
T <sub>BEH</sub>	C/BE#[3:0] (Byte Enable) Hold from CLK		2	-	nS
T <sub>ADS</sub>	AD[31:0] (Address) Setup to CLK		7	-	nS
T <sub>ADH</sub>	AD[31:0] (Address) Hold from CLK		2	-	nS
T <sub>DAS</sub>	AD[31:0] (Data) Setup to CLK		7	-	nS
T <sub>DAH</sub>	AD[31:0] (Data) Hold from CLK		2	-	nS
T <sub>DAD</sub>	AD[31:0] (Data) Valid from CLK		2	11	nS
T <sub>TZH</sub>	TRDY# High Z to High from CLK		2	11	nS
T <sub>THL</sub>	TRDY# Active from CLK		2	11	nS
T <sub>TLH</sub>	TRDY# Inactive from CLK		2	11	nS
T <sub>THZ</sub>	TRDY# High before High Z		1	-	CLK
T <sub>DZL</sub>	DEVSEL# Active from CLK		2	11	nS
T <sub>DLH</sub>	DEVSEL# Inactive from CLK		2	11	nS
T <sub>DHZ</sub>	DEVSEL# High before High Z		1	-	CLK
T <sub>ISC</sub>	IRDY# Setup to CLK		7	-	nS
T <sub>IHC</sub>	IRDY# Hold from CLK		2	-	nS

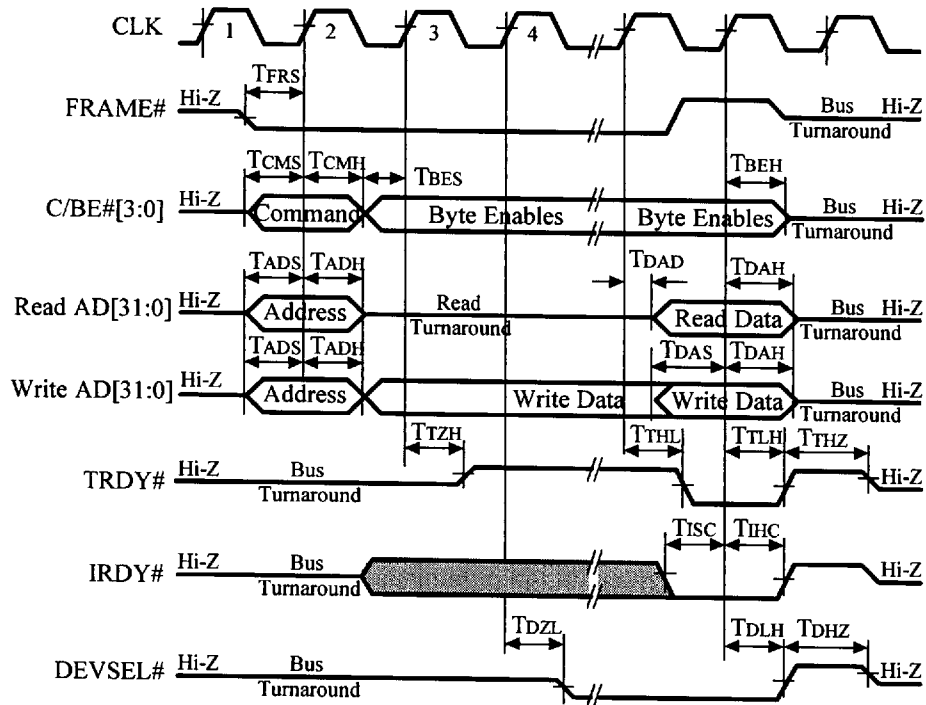
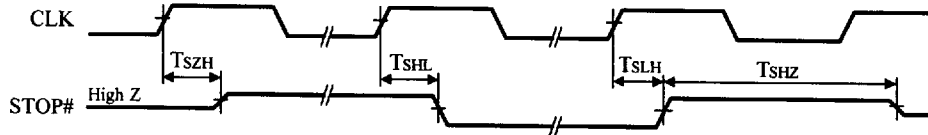


Figure 17-4: PCI Bus Frame Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation. Electrical specifications contained herein are preliminary and subject to change without notice.

**Table 17- 11: 65550 AC Timing Characteristics - PCI Bus Stop(33 MHz)**

Symbol	Parameter	Notes	Min	Max	Units
T <sub>SZH</sub>	STOP# High Z to High from CLK		2	11	nS
T <sub>SHL</sub>	STOP# Active from CLK		2	11	nS
T <sub>SLH</sub>	STOP# Inactive from CLK		2	11	nS
T <sub>SHZ</sub>	STOP# High before High Z		1	—	CLK

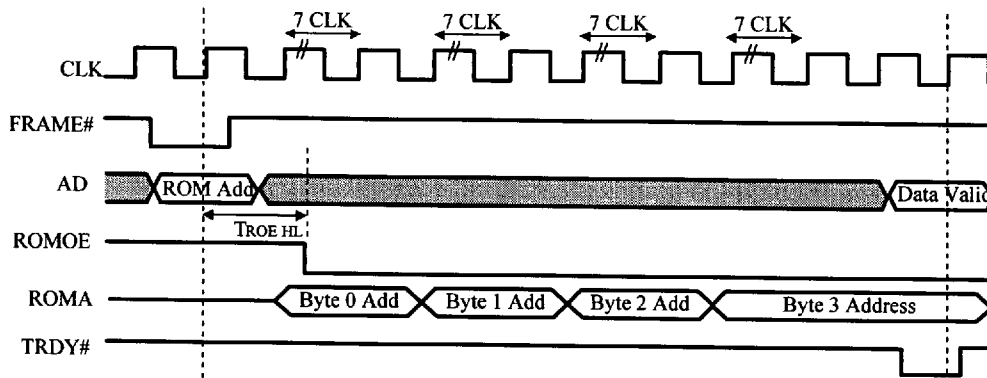


**Figure 17-5: PCI Bus Stop Timing**

**Table 17- 12: 65550 AC Timing Characteristics PC BIOS ROM**

Symbol	Parameter	Notes	Min	Max	Units
T <sub>ROE</sub>	ROMOE# Active from CLK		—	40	nS

**Note:** PCI BIOS ROM timing is derived from the PCI bus clock. Timing sequences are fixed assuming the use of widely-available, low-cost, typical industry-standard EPROMs. Timing specifications and performance of BIOS ROM memory accesses are non-critical since PCI BIOS ROM data is always shadowed into high-speed system memory prior to execution of BIOS code.



**Figure 17-6: PCI BIOS ROM Timing**



Table 17- 13: 65550 AC Timing Characteristics - DRAM Read / Write

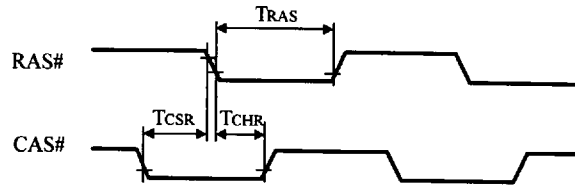
Symbol	Parameter	Notes	Versions ES 2.0 and Earlier		Versions ES 2.1 and Later		Units
			Min	Max	Min	Max	
T <sub>RC</sub>	Read/Write Cycle Time	Std DRAM	4T <sub>m</sub> - 15	-	4T <sub>m</sub> - 15	-	nS
		EDO DRAM	5T <sub>m</sub> - 5	-	6T <sub>m</sub> - 5	-	nS
T <sub>RAS</sub>	RAS# Pulse Width	Std DRAM	2T <sub>m</sub> - 5	-	2T <sub>m</sub> - 5	-	nS
		EDO DRAM	3T <sub>m</sub> - 5	-	4T <sub>m</sub> - 5	-	nS
T <sub>RP</sub>	RAS# Precharge	Std DRAM	2T <sub>m</sub> - 5	-	2T <sub>m</sub> - 5	-	nS
		EDO DRAM	2T <sub>m</sub> - 5	-	2T <sub>m</sub> - 5	-	nS
T <sub>CRP</sub>	CAS# to RAS# Precharge	Std DRAM	2T <sub>m</sub> - 15	-	2T <sub>m</sub> - 15	-	nS
		EDO DRAM	2T <sub>m</sub> - 15	-	2T <sub>m</sub> - 15	-	nS
T <sub>CSH</sub>	CAS# Hold from RAS#	Std DRAM	2T <sub>m</sub>	-	2T <sub>m</sub>	-	nS
		EDO DRAM	2T <sub>m</sub>	-	3T <sub>m</sub> -5	-	nS
T <sub>RCd</sub>	RAS# to CAS# Delay	Std DRAM	1.5T <sub>m</sub> - 10	1.5T <sub>m</sub>	1.5T <sub>m</sub> - 10	1.5T <sub>m</sub>	nS
		EDO DRAM	1.5T <sub>m</sub> - 10	-	2.5T <sub>m</sub> - 5	-	nS
T <sub>RSH</sub>	RAS# Hold from CAS#	Std DRAM	0.5T <sub>m</sub>	-	0.5T <sub>m</sub>	-	nS
		EDO DRAM	1.5T <sub>m</sub> - 15	-	1.5T <sub>m</sub> - 15	-	nS
T <sub>CP</sub>	CAS# Precharge		-	0.5T <sub>m</sub>	0.5T <sub>m</sub>	-	nS
T <sub>CAS</sub>	CAS# Pulse Width		-	0.5T <sub>m</sub>	9.5	-	nS
T <sub>ASR</sub>	Row Address Setup to RAS#		0.5T <sub>m</sub> - 5	-	0.5T <sub>m</sub> - 5	-	nS
T <sub>ASC</sub>	Column Address Setup to CAS#	Std DRAM	0.5T <sub>m</sub>	-	0.5T <sub>m</sub>	-	nS
		EDO DRAM	0.5T <sub>m</sub> - 5	-	0.5T <sub>m</sub> - 5	-	nS
T <sub>RAH</sub>	Row Address Hold from RAS#		T <sub>m</sub> - 5	-	2T <sub>m</sub> - 5	-	nS
T <sub>CAH</sub>	Column Address Hold from CAS#		0.5T <sub>m</sub>	-	0.5T <sub>m</sub>	-	nS
T <sub>CAC</sub>	Data Access Time from CAS#	Std DRAM	-	0.5T <sub>m</sub>	-	0.5T <sub>m</sub>	nS
		EDO DRAM	-	T <sub>m</sub> -8	-	T <sub>m</sub> -8	nS
T <sub>RAC</sub>	Data Access Time from RAS#	Std DRAM	-	2T <sub>m</sub>	-	2T <sub>m</sub>	nS
		EDO DRAM	-	2.5T <sub>m</sub>	-	4T <sub>m</sub> -23	nS
T <sub>DS</sub>	Write Data Setup to CAS#	Std DRAM	0.5T <sub>m</sub> - 5		0.5T <sub>m</sub> - 5		nS
		EDO DRAM	0.5T <sub>m</sub> - 5		0.5T <sub>m</sub> - 5		nS
T <sub>DH</sub>	Write Data Hold from CAS#		0.5T <sub>m</sub>		0.5T <sub>m</sub>		nS
T <sub>COH</sub>	Read data hold from CAS# fall	EDO DRAM	2		5		nS
T <sub>OFF</sub>	Read data hold from CAS# rise	Std DRAM	0		0		nS
T <sub>PC</sub>	CAS Cycle Time		T <sub>m</sub>		T <sub>m</sub>		nS
T <sub>WS</sub>	WE# Setup to CAS#		T <sub>m</sub> - 10		2T <sub>m</sub> - 10		nS
T <sub>WH</sub>	WE# Hold from CAS#		2T <sub>m</sub> - 5		2T <sub>m</sub> - 5		nS

**Note:** The 65550 does not perform mixed read and write (or read modify write) cycles during the same CAS low interval. Unless otherwise specified, specifications above apply to both 5V & 3.3V operation. Electrical specifications contained herein are preliminary and subject to change without notice.



**Table 17-14: 65550 AC Timing Characteristics - CBR Refresh**

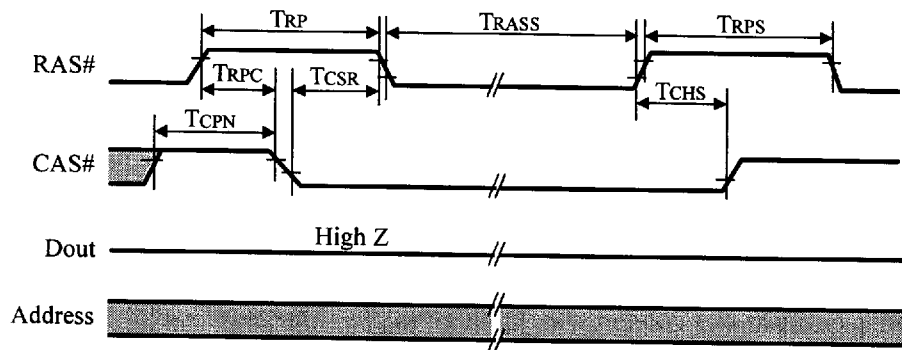
Symbol	Parameter	Notes	Min	Typical	Max	Units
T <sub>CHR</sub>	RAS# to CAS# Delay		5T <sub>m</sub> - 5	-	-	nS
T <sub>CSR</sub>	CAS# to RAS# Delay	Normal Operation Standby Mode	T <sub>m</sub> - 5 2T <sub>m</sub> - 5	-	-	nS
T <sub>RAS</sub>	RAS# Pulse Width		5T <sub>m</sub> - 5	-	-	nS



**Figure 17-9: CAS-Before-RAS (CBR) DRAM Refresh Cycle Timing**

**Table 17-15: 65550 AC Timing Characteristics - Self Refresh**

Symbol	Parameter	Notes	Min	Typical	Max	Units
T <sub>RASS</sub>	RAS# Pulse Width for Self-Refresh		100	-	-	μS
T <sub>RP</sub>	RAS# Precharge		4T <sub>m</sub> - 3	-	-	nS
T <sub>RPS</sub>	RAS# Precharge for Self-Refresh		10T <sub>m</sub>	-	-	nS
T <sub>RPC</sub>	RAS# to CAS# Delay		3T <sub>m</sub> - 5	-	-	nS
T <sub>CSR</sub>	CAS# to RAS# Delay	Normal Operation Standby Mode	T <sub>m</sub> - 5 2T <sub>m</sub> - 5	-	-	nS
T <sub>CHS</sub>	CAS# Hold Time		0	-	-	nS
T <sub>CPN</sub>	CAS# Precharge		T <sub>m</sub> - 5	-	-	nS

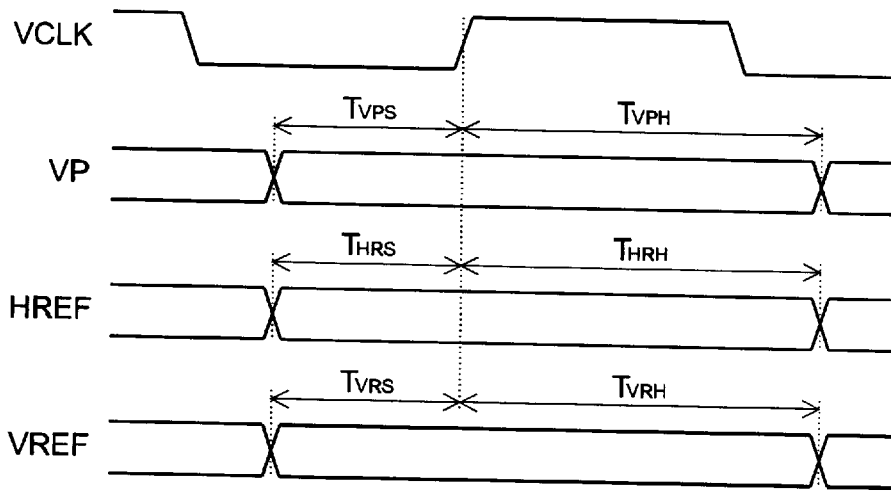


**Figure 17-10: "Self Refresh DRAM" Refresh Cycle Timing**

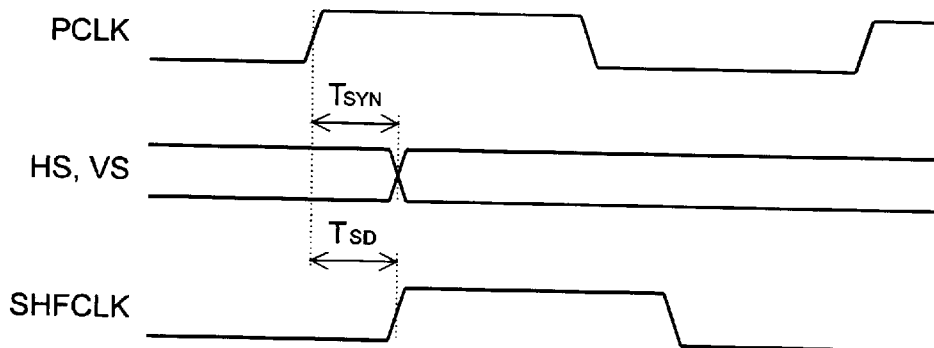
**Table 17-16: 65550 AC Timing Characteristics - Video Data Port**

Symbol	Parameter	Notes	Min	Max	Units
T <sub>VDS</sub>	VP (Incoming Data) Setup	ZV-Port Mode	5*	—	nS
T <sub>VDH</sub>	VP (Incoming Data) Hold		3*	—	nS
T <sub>HRS</sub>	HREF (Incoming HS) Setup		5*	—	nS
T <sub>HRH</sub>	HREF (Incoming HS) Hold		3*	—	nS
T <sub>VRS</sub>	VREF (Incoming VS) Setup		5*	—	nS
T <sub>VRH</sub>	VREF (Incoming VS) Hold		3*	—	nS

\* Note: To be confirmed.



**Figure 17-11: Video Data Port Timing**

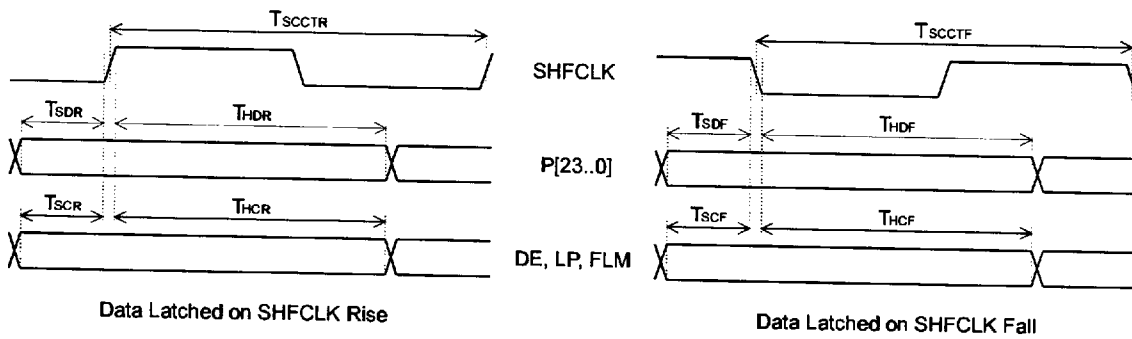


**Figure 17-12: CRT Output Timing**

**Table 17- 17: 65550 AC Timing Characteristics - Panel Output Timing**

Symbol	Parameter	Notes	Min	Max	Units
T <sub>SCCTR</sub>	SHFCLK cycle time	Data latched on SHFCLK rise	15	–	nS
T <sub>SDR</sub>	Panel data setup to SHFCLK rise		T <sub>sc</sub> -5	–	nS
T <sub>HDR</sub>	Panel data hold from SHFCLK rise		0	–	nS
T <sub>SCR</sub>	Panel control setup to SHFCLK rise		T <sub>sc</sub> -3	–	nS
T <sub>HCR</sub>	Panel control hold from SHFCLK rise		-3	–	nS
T <sub>SCCTF</sub>	SHFCLK cycle time	Data latched on SHFCLK fall	25	–	nS
T <sub>SDF</sub>	Panel data setup to SHFCLK fall		0.5 T <sub>sc</sub> -5	–	nS
T <sub>HDF</sub>	Panel data hold from SHFCLK fall		0.5 T <sub>sc</sub>	–	nS
T <sub>SCF</sub>	Panel control setup to SHFCLK fall		0.5 T <sub>sc</sub> -3	–	nS
T <sub>HCF</sub>	Panel control hold from SHFCLK fall		0.5 T <sub>sc</sub> -3	–	nS
T <sub>SCDC</sub>	SHFCLK Duty Cycle (% high)	Color STN-DD or STN-SS	TBD	TBD	
	SHFCLK Duty Cycle (% high)	TFT or Mono STN	TBD	TBD	

**Note:** AC Timing is valid when either:  
 DVCC=5V, max output loading=50pF  
 DVCC=3.3V, max output loading=25pF.



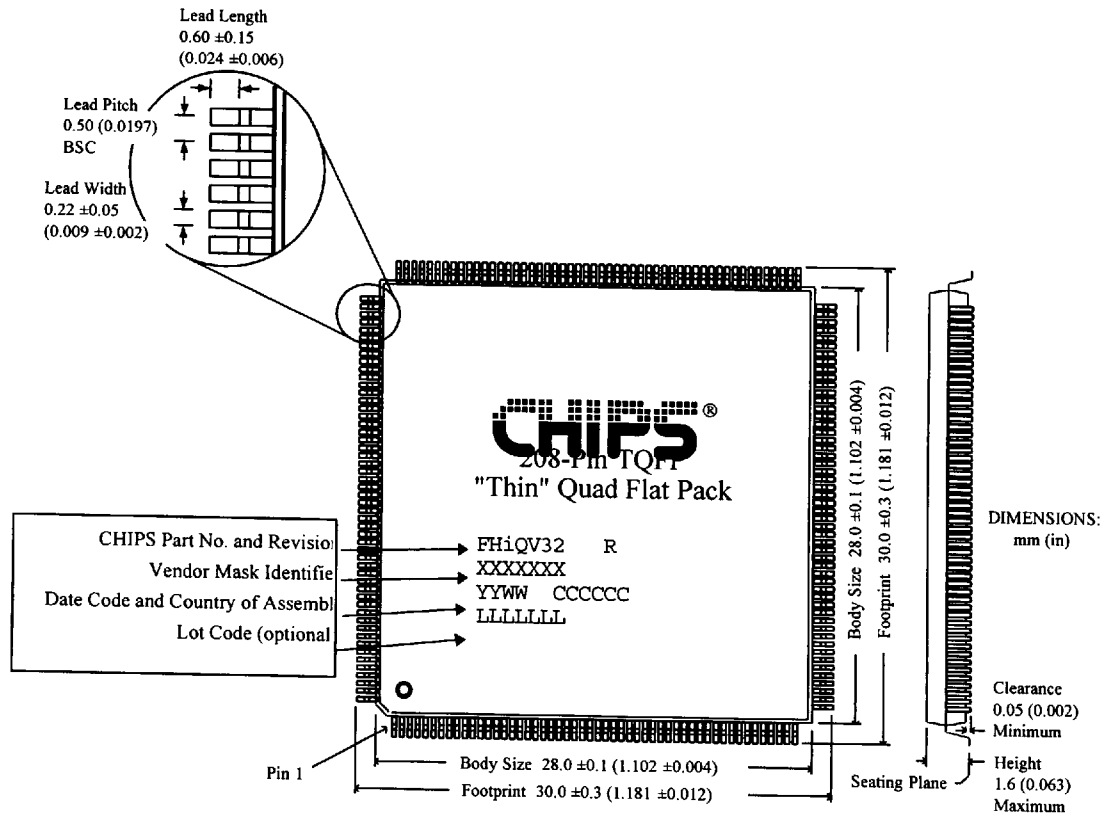
**Figure 17-13: Panel Output Timing**

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation.  
 Electrical specifications contained herein are preliminary and subject to change without notice.

## 18.0 MECHANICAL SPECIFICATIONS

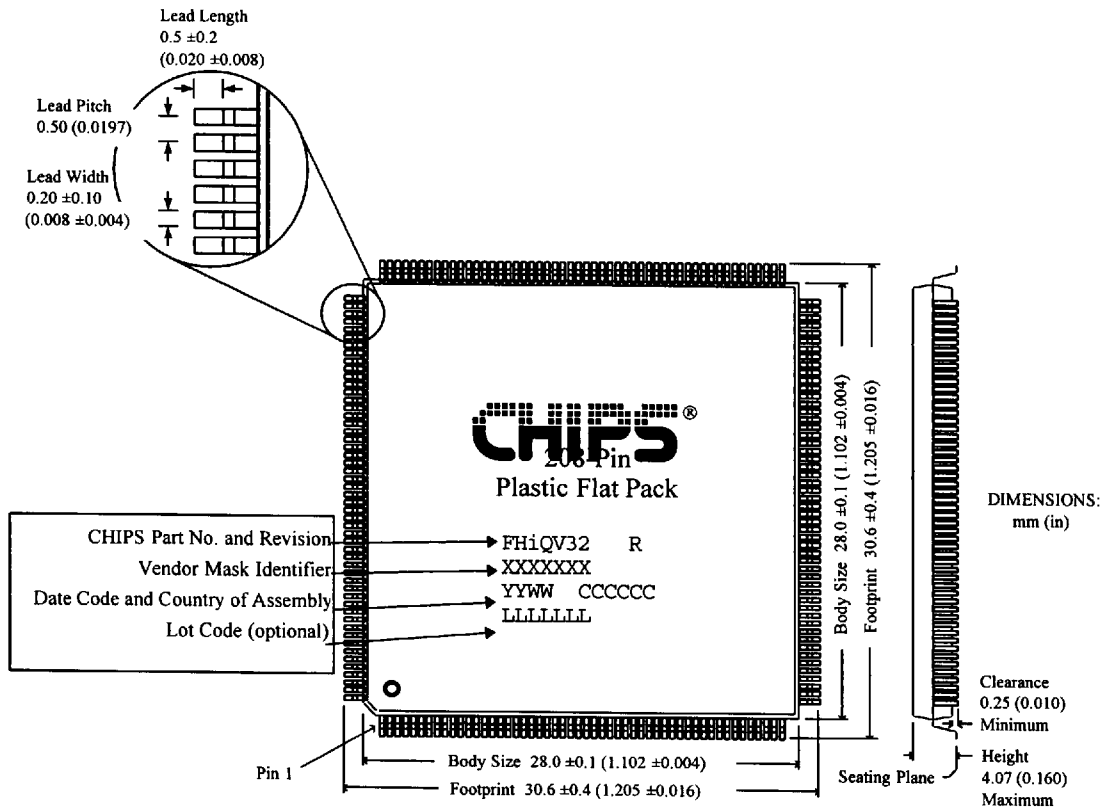
This sections provides the mechanical specifications for the Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), and Ball Grid Array (BGA).

### 18.1 Thin Quad Flat Pack (TQFP)



**Figure 18-1: Thin Quad Flat Pack (TQFP)**

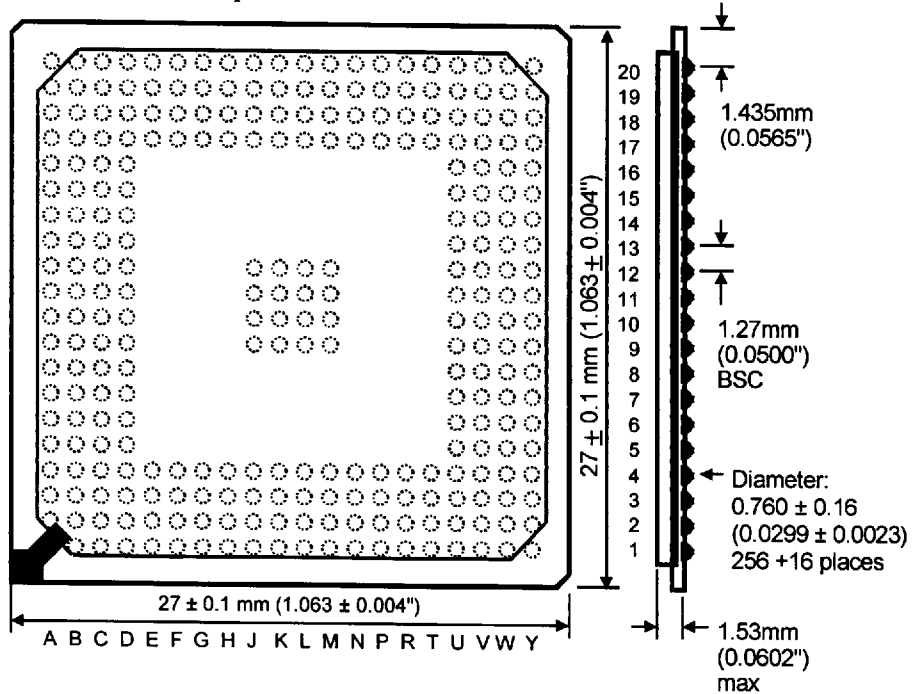
### 18.2 Plastic Quad Flat Pack



**Figure 18-2: Plastic Quad Flat Pack**

### 18.3 256+16-Contact Ball Grid Array

Top View



Bottom View

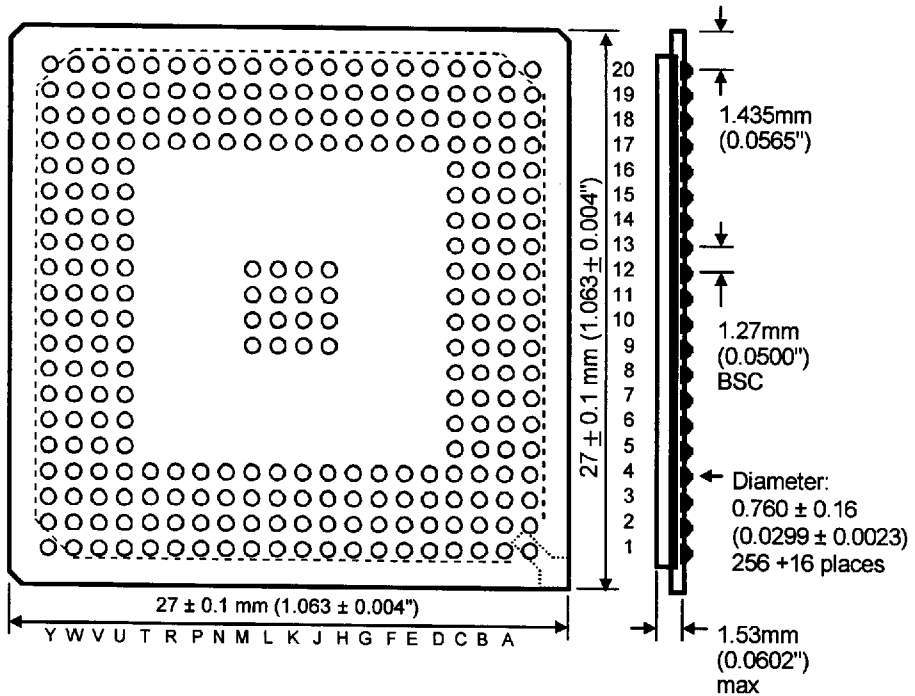


Figure 18-3: 256+16-Contact Ball Grid Array