FORESEE®

Nand-based MCP Datasheet

M-00221

F70ME0101D-R6WA

F70ME0101D-RDWA

Version: 1.1

Revision History

Rev.	Date	Change	Editor
1.0	2020/11/18	Basic spec and architecture	Kelly. Guan
1.1	2021/1/27	Add Note in 1.3	Kelly.Guan

Contents

1. INTRODUCTION

1.1 General Description

FORESEE MCP products combine NAND Flash and Mobile LPDRAM devices in a single MCP. These products target mobile applications with low-power, high-performance, and minimal package-footprint design requirements.

The NAND Flash and Mobile LPDRAM devices are packaged with separate interfaces(no shared address, control, data, or power balls). This bus architecture supports an optimized interface to processors with separate NAND Flash and Mobile LPDRAM buses.

The NAND Flash and Mobile LPDRAM devices have separate core power connections and share a common ground (that is, VSS is tied together on the two devices).

The bus architecture of this device also supports separate NAND Flash and Mobile LPDRAM functionality without concern for device interaction.

1.2 Product List

[Table 1] Product List

Part Number	Density	Package Type	Package Size(mm)
F70ME0101D-R6WA	1Gbits NAND +1Gbits LPDDR2	FBGA162	8.0x10.5x1.0
F70ME0101D-RDWA	1Gbits NAND +1Gbits LPDDR2	FBGA162	8.0x10.5x1.0

Marketing Part Number Chart

F 70 M E 0101 D - X X X X

Brand
F=FORESEE

Product Family
70= Nand-based MCP

Supply voltage
M=NAND VCC 1.8V+LPDDR2 VDD1 1.8V, VDD2 VDDQ 1.2V

Width
E=NAND*8bit+LPDDR2*32bit

Density
0201：2Gb+1Gb
0101：1Gb+1Gb

Wafer Type

Hyphen

Package Type
R=FBGA162(8*10.5*1.0mm)

Dram Rate
6=533MHz
D=400MHz

Temperature
W=-40~85℃

DIE stack number
A=1FLASH+1DRAM

1.3 Device Features

[nMCP]

- **Operation Temperature**
  - (-40)°C ~ 85°C
- **Package**
  - 162-ball FBGA – 8x10.5mm^2

[NAND FLASH]

- **Voltage Supply**
  - V_{CC}: 1.8V (1.7V ~ 1.95V) 1)

- **Organization**
  - Memory Cell Array : (128M + 4M) Byte
  - Page Size : (2K + 64) Byte
  - Data Register : (2K + 64) Byte
  - Block Erase : (128K + 4K) Byte

- **Automatic Program and Erase**
  - Page Program : (2K + 64) Byte

- **Page Read Operation**
  - Random Read: 25μs(Max.)
  - Serial Access : 45ns(Min.)

- **Fast Write Cycle Time**
  - Page Program time : 300μs(Typ.)
  - Block Erase Time : 3ms(Typ.)

- **Command/Address/Data Multiplexed I/O Port**

- **COMMAND SET**
  - ONFI1.0 Compliant command set
  - Read Unique ID

- **Reliability**
  - 100,000 P/E Cycle
  - 10 Year Data retention (Typ.)

[LPDDR2]

- **Functionality**

- VDD2 = 1.14–1.30V
- VDDQ = 1.14–1.30V
- VDD1 = 1.70–1.95V
- Interface : HSUL_12
- Data width : x32
- Clock frequency : 400MHz/533MHz
- Four-bit pre-fetch DDR architecture
- Eight internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
- Bidirectional/differential data strobe per byte of data(DQS/DQS#).
- DM masks write date at the both rising and falling edge of the data strobe
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- Auto refresh and self refresh supported
- All bank auto refresh and per bank auto refresh supported
- Clock stop capability

- **Configuration**

- 32 Meg X 32 (4 Meg X 32 X 8 Banks).

- **Low Power Features**

- Low voltage power supply.
- Auto TCSR (Temperature Compensated Self Refresh).
- PASR (Partial Array Self Refresh) power-saving mode.
- DPD (Deep Power Down) Mode.
- DS (Driver Strength) Control.

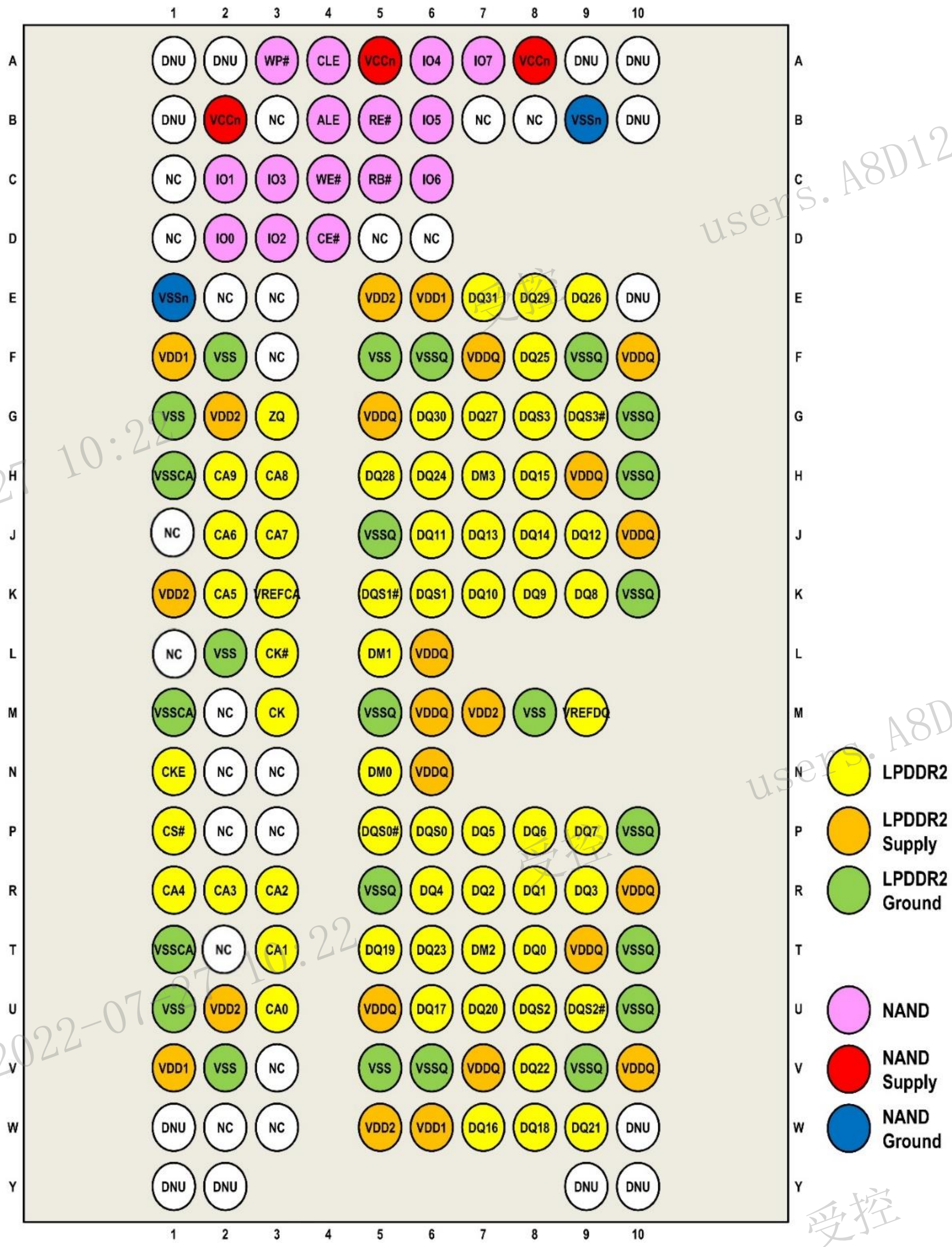
- **Auto refresh duty cycle :**

- 7.8us for -40 to 85 °C
- 1.95us for 85 to 105°C

Notes:

1) While -40℃≤Ta≤-25℃，NAND Voltage supply(Vcc) should be less than or equal to 1.9V.

1.4 Connection Diagram



	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU	WP#	CLE	VCCn	IO4	IO7	VCCn	DNU	DNU
B	DNU	VCCn	NC	ALE	RE#	IO5	NC	NC	VSSn	DNU
C	NC	IO1	IO3	WE#	RB#	IO6				
D	NC	IO0	IO2	CE#	NC	NC				
E	VSSn	NC	NC		VDD2	VDD1	DQ31	DQ29	DQ26	DNU
F	VDD1	VSS	NC		VSS	VSSQ	VDDQ	DQ25	VSSQ	VDDQ
G	VSS	VDD2	ZQ		VDDQ	DQ30	DQ27	DQS3	DQS3#	VSSQ
H	VSSCA	CA9	CA8		DQ28	DQ24	DM3	DQ15	VDDQ	VSSQ
J	NC	CA6	CA7		VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ
K	VDD2	CA5	VREFCA		DQS1#	DQS1	DQ10	DQ9	DQ8	VSSQ
L	NC	VSS	CK#		DM1	VDDQ				
M	VSSCA	NC	CK		VSSQ	VDDQ	VDD2	VSS	VREFDQ	
N	CKE	NC	NC		DM0	VDDQ				
P	CS#	NC	NC		DQS0#	DQS0	DQ5	DQ6	DQ7	VSSQ
R	CA4	CA3	CA2		VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ
T	VSSCA	NC	CA1		DQ19	DQ23	DM2	DQ0	VDDQ	VSSQ
U	VSS	VDD2	CA0		VDDQ	DQ17	DQ20	DQS2	DQS2#	VSSQ
V	VDD1	VSS	NC		VSS	VSSQ	VDDQ	DQ22	VSSQ	VDDQ
W	DNU	NC	NC		VDD2	VDD1	DQ16	DQ18	DQ21	DNU
Y	DNU	DNU							DNU	DNU

Figure 1-1 162-BGA MCP Contact (X8/X32) Top View (Ball Down)

1.5 Pin Description

[Table 2] Pin Description

Symbol	Description	Type
<NAND(x8)>		
I/O0~ I/O7	Data I/O	Input/Output
CLE	Command Latch Enable	Input
ALE	Address Latch Enable	Input
CE#	Chip Enable	Input
RE#	Read Enable	Input
WE#	Write Enable	Input
WP#	Write Protect	Input
R/B#	Ready/Busy	Output
VCC	Power Supply	Power
VSS	Ground	Ground
<LPDDR2(x32)>		
CK, CK#	Clock	Input
CKE	Clock enable	Input
CS#	Chip select	Input
DM0–DM3	Input data mask	Input
DQ0 – DQ31	Data input/output	I/O
DQS0 – DQS3，DQS0# – DQS3#	Data strobe	I/O
CA0 – CA9	Command/address inputs	Input
VDDQ	DQ power supply	Supply
VSSQ	DQ ground	Supply
VSSCA	Command/address ground	Supply
VDD1	Core power supply	Supply
VDD2	Core power supply	Supply
VSS	Common ground.	Supply
VREFCA, VREFDQ	Reference voltage: VREFCA is reference for command/address input buffers, VREFDQ is reference for DQ input buffers.	Supply
ZQ	External reference ball for output drive calibration	Reference
DNU	Do not use: Must be grounded or left floating	–
NC	No connect: Not internally connected	–
RFU	Reserved for future use	–

Notes:

1.Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

1.6 System Block Diagram

DRAM Block Diagram:

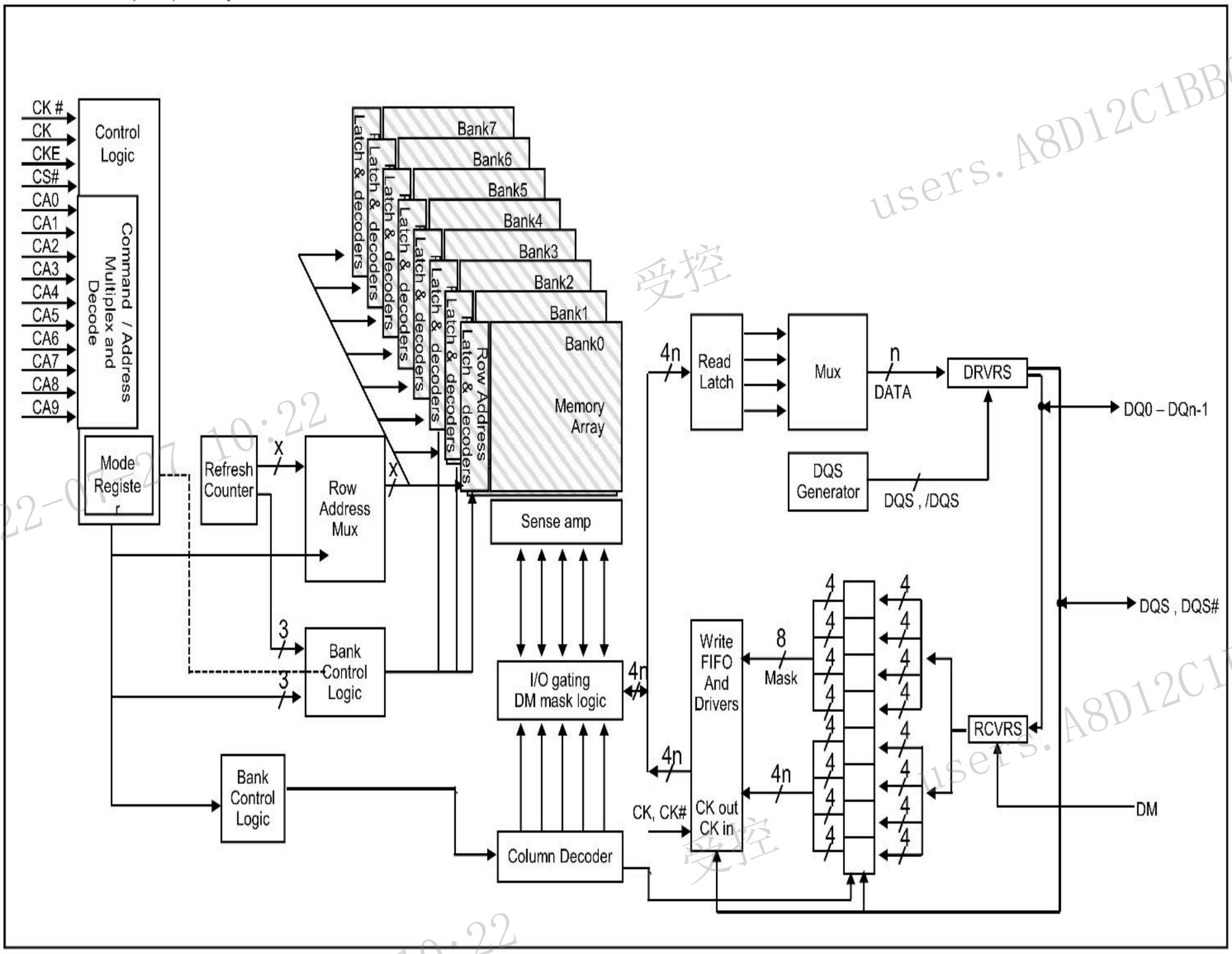


Figure 1-2 DRAM Block Diagram

NAND Block Diagram:

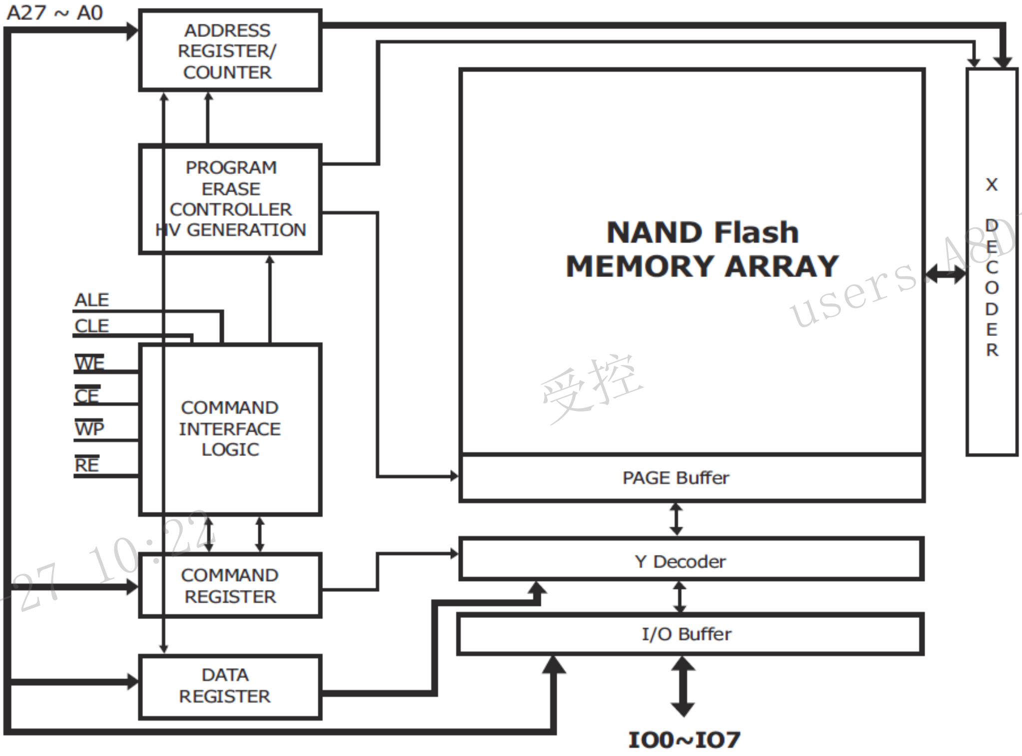
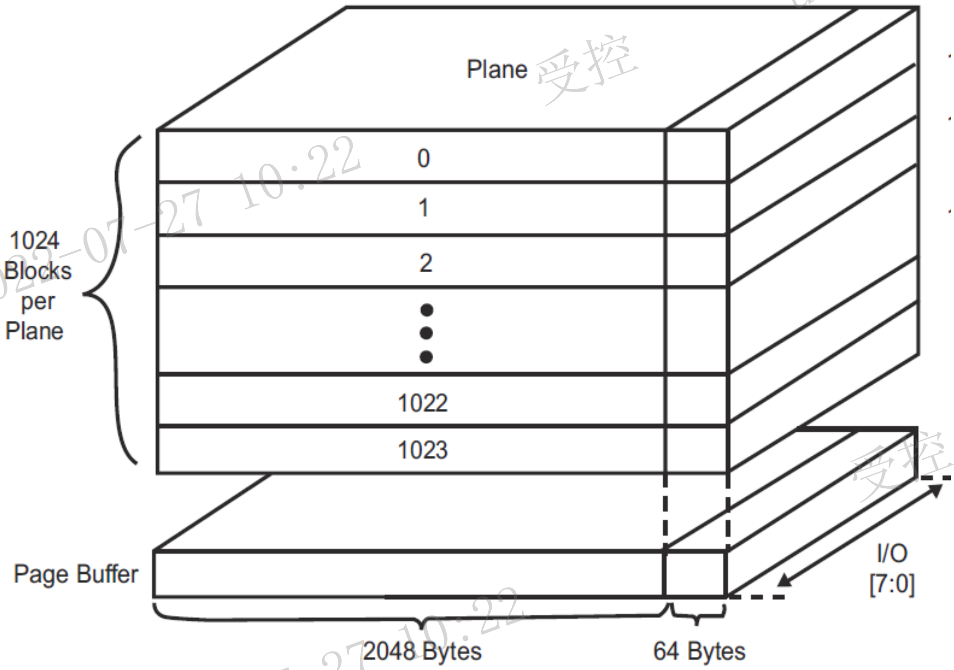


Figure 1-3 NAND Block Diagram

Array Organization:



1 Page = (2K+64) Bytes
1 Block = (2K+64) Bytes x 64 pages = (128K + 4K) Bytes
1 Device = (128+4K) Bytes x 1024 Blocks=(128M+4M)Bytes

Figure 1-4 1Gb NAND Array Organization

LPDDR2
SDRAM

2. LPDDR2

2.1 LPDDR2 SDRAM Addressing

[Table 3] LPDDR2 SDRAM Addressing

Items		1Gb
Number of Banks		8
Bank Addresses		BA0-BA2
t_{REFI}(us)[2]		7.8
t_{REFI}(us)[3]		1.95
×32	Row Addresses [4]	R0-R12
	Column Addresses[1], [4]	C0-C8

Notes:

1.The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

2.tREFI values for all bank refresh is Tc = -40~85°C, Tc means Operating Case Temperature.

3.tREFI values for all bank refresh is Tc = 85~105°C, Tc means Operating Case Temperature.

4.Row and Column Address values on the CA bus that are not used are "don’t care."

2.2 INPUT/OUTPUT FUNCTIONAL DESCRIPTION

[Table 4] Pad Definition and Description

Name	Type	Description
CK, CK#	Input	**Clock**: CK and CK# are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK. Single Data Rate (SDR) inputs, CS# and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK and CK#. The positive Clock edge is defined by the cross point of a rising CK and a falling CK#. The negative Clock edge is defined by the cross point of a falling CK and a rising CK#.
CKE	Input	**Clock Enable**: CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command truth table for command code descriptions. CKE is sampled at the positive Clock edge.
CS#	Input	**Chip Select**: CS# is considered part of the command code. See Command truth table for command code descriptions. CS # is sampled at the positive Clock edge.
CA0 - CA9	Input	**DDR Command/Address Inputs**: Uni-directional command/address bus inputs. CA is considered part of the command code. See Command truth table for command code descriptions.
DQ0 - DQ15 (×16) DQ0 - DQ31 (×32)	I/O	**Data Inputs/Outputs**: Bi-directional data bus
DQS0 - DQS1 DQS0 #- DQS1# (×16) DQS0 - DQS3 DQS0# - DQS3# (×32)	I/O	**Data Strobes (Bi-directional, Differential)**: The data strobe is bi-directional (used for read and write data) and Differential (DQS and DQS#). It is output with read data and input with write data. DQS is edge-aligned to read data and centered with write data. For x16, DQS0 and DQS0# correspond to the data on DQ0 - DQ7, DQS1 and DQS1# to the data on DQ8 - DQ15. For x32, DQS0 and DQS0# correspond to the data on DQ0 - DQ7, DQS1 and DQS1# to the data on DQ8 - DQ15, DQS2 and DQS2# to the data on DQ16 - DQ23, DQS3 and DQS3# to the data on DQ24 - DQ31.
DM0 - DM1 (×16) DM0 - DM3 (×32)	Input	**Input Data Mask**: DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM is for input only, the DM loading shall match the DQ and DQS (or DQS#). DM0 is the input data mask signal for the data on DQ0-7. For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 device, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
VDD1	Supply	**Core Power Supply 1**: Core power supply.
VDD2	Supply	**Core Power Supply 2**: Core power supply.
VDDQ	Supply	**I/O Power Supply**: Power supply for Data input/output buffers.
VREFCA	Supply	**Reference Voltage for CA Command and Control Input Receiver**: Reference voltage for all CA0-9, CKE, CS#, CK, and CK# input buffers.
VREFDQ	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all Data input buffers.
VSS	Supply	**Ground**
VSSCA	Supply	**Ground for Input Receivers**
VSSQ	Supply	**I/O Ground**
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

Notes : Data includes DQ and DM.

2.3 FUNCTIONAL DESCRIPTION

This device contains the following number of bits: 1Gb has 1,073,741,824 bits. All LPDDR2 devices use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock. LPDDR2 uses a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half- clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

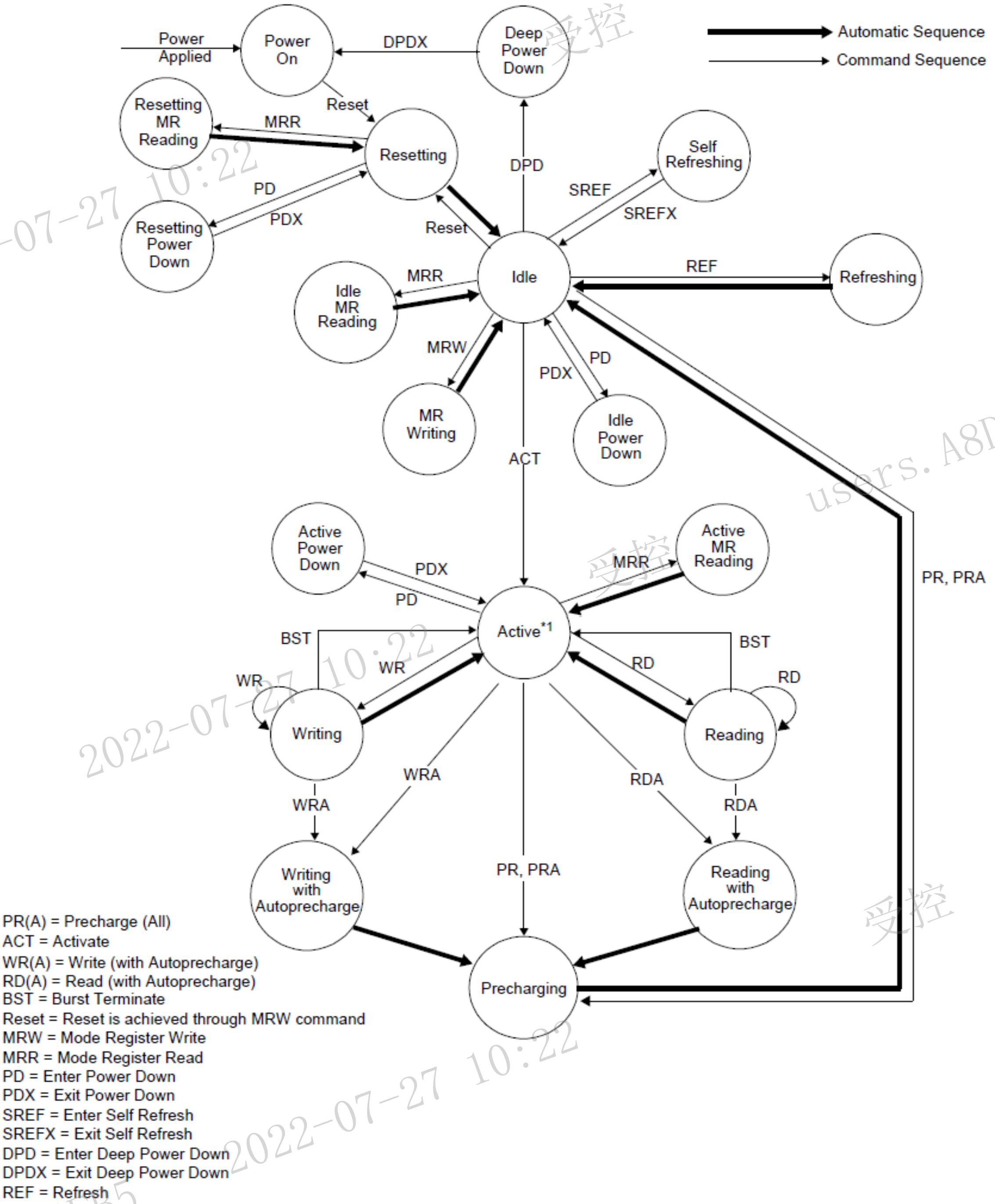
For LPDDR2 devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR2 must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

2.4 Simplified LPDDR2 Bus Interface State Diagram

The simplified LPDDR2 bus interface state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks. For the command definition, see datasheet of [Command Definition & Timing Diagram].



PR(A) = Precharge (All)
ACT = Activate
WR(A) = Write (with Autoprecharge)
RD(A) = Read (with Autoprecharge)
BST = Burst Terminate
Reset = Reset is achieved through MRW command
MRW = Mode Register Write
MRR = Mode Register Read
PD = Enter Power Down
PDX = Exit Power Down
SREF = Enter Self Refresh
SREFX = Exit Self Refresh
DPD = Enter Deep Power Down
DPDX = Exit Deep Power Down
REF = Refresh

Figure 2-1 LPDDR2: Simplified Bus Interface State Diagram

Notes: For LPDDR2-SDRAM in the Idle state, all banks are precharged.

3. Mode Register Definition

3.1 Mode Register Assignment and Definition in LPDDR2 SDRAM

[Table 5] Mode Register Assignment in LPDDR2 SDRAM (Common Part) shows the 16 common mode registers for LPDDR2 SDRAM. [Table 6]Mode Register Assignment in LPDDR2 SDRAM (SDRAM part) shows only LPDDR2 SDRAM mode registers and [Table 7]Mode Register Assignment in LPDDR2 SDRAM (NVM Part) shows only LPDDR2 NVM mode registers. Additionally [Table 8]Mode Register Assignment in LPDDR2 SDRAM (DQ Calibration and Reset Command) shows RFU mode registers and Reset Command. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

[Table 5] Mode Register Assignment in LPDDR2 SDRAM (Common part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	Device Info.	R	(RFU)			RZQI		(RFU)	DI	DAI
1	01_H	Device Feature 1	W	nWR (for AP)			WC	BT	BL		
2	02_H	Device Feature 2	W	(RFU)				RL & WL			
3	03_H	I/O Config-1	W	(RFU)				DS			
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05_H	Basic Config-1	R	LPDDR2 Manufacturer ID							
6	06_H	Basic Config-2	R	Revision ID1							
7	07_H	Basic Config-3	R	Revision ID2							
8	08_H	Basic Config-4	R	I/O width		Density				Type	
9	09_H	Test Mode	W	Vendor-Specific Test Mode							
10	$0A_H$	IO Calibration	W	Calibration Code							
11:15	$0B_H$~$0F_H$	(reserved)		(RFU)							

[Table 6] Mode Register Assignment in LPDDR2 SDRAM (SDRAM part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
16	10_H	PASR_Bank	W	Bank Mask							
17	11_H	PASR_Seg	W	Segment Mask (SDRAM only)							
18-19	12_H-13_H	(Reserved)		(RFU)							

[Table 7] Mode Register Assignment in LPDDR2 SDRAM (NVM Part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
20:31	14_H~$1F_H$	(Do Not Use)									

[Table 8]Mode Register Assignment in LPDDR2 SDRAM (DQ Calibration and Reset Command)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
32	**20H**	DQ Calibration Pattern A	R	See "DQ Calibration" on Operations & Timing Diagram.							
33:39	**21H~27H**	(Do Not Use)									
40	**28H**	DQ Calibration Pattern B	R	See "DQ Calibration" on Operations & Timing Diagram.							
41:47	**29H~2FH**	(Do Not Use)									
48:62	**30H~3EH**	(Reserved)		(RFU)							
63	**3FH**	Reset	W	X							
64:126	**40H~7EH**	(Reserved)		(RFU)							
127	**7FH**	(Do Not Use)									
128:190	**80H~BEH**	(Reserved for Vendor Use)		(RFU)							
191	**BFH**	(Do Not Use)									
192:254	**C0H~FEH**	(Reserved for Vendor Use)		(RFU)							
255	**FFH**	(Do Not Use)									

The following notes apply to Table 5 Mode Register Assignment in LPDDR2 SDRAM (Common part), Table 6 Mode Register Assignment in LPDDR2 SDRAM (SDRAM part), Table 7 Mode Register Assignment in LPDDR2 SDRAM (NVM Part), and Table 8 Mode Register Assignment in LPDDR2 SDRAM (DQ Calibration and Reset Command):

Notes:
1.RFU bits shall be set to '0' during Mode Register writes.
2.RFU bits shall be read as '0' during Mode Register reads.
3.All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS, DQS# shall be toggled.
4.All Mode Registers that are specified as RFU shall not be written.
5.Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Device Information (MA<7:0> = 00H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)			RZQI		(RFU)	DI	DAI

DAI (Device Auto-Initialization Status)	Read-only	OP0	**0_B**: DAI complete **1_B**: DAI still in progress
DI (Device Information)	Read-only	OP1	**0_B**: SDRAM **1_B**: Do Not Use
RZQI (Built in Self Test for RZQ Information) 1)	Read-only	OP4:OP3	**00_B**: RZQ self test not supported **01_B**: ZQ-pin may connect to VDD2 or float **10_B**: ZQ-pin may short to GND **11_B**: ZQ-pin self test completed, no error condition detected (ZQ-pin may not con- nect to VDD2 or float nor short to GND)

NOTE :
1.RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.
2.If ZQ is connected to VDD2 to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDD2, either OP[4:3] = 01 or OP[4:3] =10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3.In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 2), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4.In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e 240-ohm +/- 1%).

MR1_Device Feature 1 (MA<7:0> = 01H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL	Write-only	OP<2:0>	**010_B**: BL4 (default) **011_B**: BL8 **100_B**: BL16 **All others**: Reserved
BT 1)	Write-only	OP<3>	**0_B**: Sequential (default) **1_B**: Interleaved (allowed for SDRAM only)
WC	Write-only	OP<4>	**0_B**: Wrap (default) **1_B**: No wrap (allowed for SDRAM BL4 only)
nWR 2)	Write-only	OP<7:5>	**001_B**: nWR=3 (default) **010_B**: nWR=4 **011_B**: nWR=5 **100_B**: nWR=6 **101_B**: nWR=7 **110_B**: nWR=8 **All others**: Reserved

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Notes :
1.BL 16, interleaved is not an official combination to be supported.

2.Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is deter- mined by RU(tWR/tCK).

[Table 9] Burst Sequence by BL, BT, and WC

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	X	0_B	0_B	wrap	any	4	0	1	2	3												
X	X	1_B	0_B				2	3	0	1												
X	X	X	0_B	nw	any		y	y+1	y+2	y+3												
X	0_B	0_B	0_B	wrap	seq	8	0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	4	5	6	7	0	1								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1_B	0_B				6	7	0	1	2	3	4	5								
X	0_B	0_B	0_B		int		0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	0	1	6	7	4	5								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1_B	0_B				6	7	4	5	2	3	0	1								
X	X	X	0_B	nw	any		illegal (not allowed)															
0_B	0_B	0_B	0_B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0_B	0_B	1_B	0_B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0_B	1_B	0_B	0_B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0_B	1_B	1_B	0_B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1_B	0_B	0_B	0_B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1_B	0_B	1_B	0_B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1_B	1_B	0_B	0_B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1_B	1_B	1_B	0_B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
X	X	X	0_B		int		illegal (not allowed)															
X	X	X	0_B	nw	any		illegal (not allowed)															

Notes :
1.C0 input is not present on CA bus. It is implied zero.
2.For BL=4, the burst address represents C1 - C0.
3.For BL=8, the burst address represents C2 - C0.
4.For BL=16, the burst address represents C3 - C0.
5.For no-wrap (nw), BL4, the burst shall not cross the page boundary and shall not cross sub-page boundary. The variable may start at any address with C0 equal to 0 and may not start at any address in Table 10 below for the respective density and bus width combinations.

[Table 10] LPDDR2 Non Wrap Restrictions

1Gb	
Not across full page boundary	
x16	3FE, 3FF, 000, 001
x32	1FE, 1FF, 000, 001
Not across sub page boundary	
x16	1FE, 1FF, 200, 201
x32	None

Notes:
1. Non-wrap BL=4 data-orders shown above are prohibited.

MR2_Device Feature 2 (MA<7:0> = 02H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

RL & WL	Write-only	OP<3:0>	**0001_B:** RL3 / WL1(default) **0010_B:** RL4 / WL2 **0011_B:** RL5 / WL2 **0100_B:** RL6 / WL3 **0101_B:** RL7 / WL4 **0110_B:** RL8 / WL4 **All others:** Reserved

MR3_I/O Configuration 1 (MA<7:0> = 03H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP<3:0>	**0000_B:** Reserved **0001_B:** 34.3-ohmtypical **0010_B:** 40-ohm typical(default) **0011_B:** 48-ohm typical **0100_B:** 60-ohm typical **0101_B:** Reserved for 68.6-ohm typical **0110_B:** 80-ohm typical **0111_B:** 120-ohm typical **All others:** Reserved

MR4_Device Temperature (MA<7:0> = 04H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		

SDRAM Refresh Rate	Read-only	OP<2:0>	**000_B:** SDRAM Low temperature operating limit exceeded **001_B:** 4× t_{REFI}, 4× t_{REFIpb}, 4× t_{REFW} **010_B:** 2× t_{REFI}, 2× t_{REFIpb}, 2× t_{REFW} **011_B:** 1× t_{REFI}, 1× t_{REFIpb}, 1× t_{REFW} (<=85'C) **100_B:** Reserved **101_B:** 0.25× t_{REFI}, 0.25× t_{REFIpb}, 0.25× t_{REFW}, do not de-rate SDRAM AC timing **110_B:** 0.25× t_{REFI}, 0.25× t_{REFIpb}, 0.25× t_{REFW}, de-rate SDRAM AC timing **111_B:** SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<7>	**0_B:** OP<2:0> value has not changed since last read of MR4. **1_B:** OP<2:0> value has changed since last read of MR4.

Notes:
1.A Mode Register Read from MR4 will reset OP7 to ‘0’.
2.OP7 is reset to ‘0’ at power-up. OP[2:0] bits are undefined after power-up.
3.If OP2 equals ‘1’, the device temperature is greater than 85℃.
4.OP7 is set to ‘1’ if OP2:OP0 has changed at any time since the last read of MR4.
5.LPDDR2 might not operate properly when OP[2:0] = 000_B or 111_B
6.For specified operating temperature range and maximum operating temperature refer to Input Leakage Current Table.
7.LPDDR2 devices shall be de-rated by adding 1.875 ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in Table 34 LPDDR2 AC Timing Table. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
8.See "Temperature Sensor" on [Command Definition & Timing Diagram] for information on the recommended frequency of reading MR4.

MR5_Basic Configuration 1 (MA<7:0> = 05H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							

LPDDR2 Manufacturer ID	Read-only	OP<7:0>	**$0000\ 0000_B$** : Reserved **$0000\ 0001_B$** : Reserved **$0000\ 0010_B$** : Do Not Use **$0000\ 0011_B$** : Do Not Use **$0000\ 0100_B$** : Do Not Use **$0000\ 0101_B$** : Do Not Use **$0000\ 0110_B$** : Do Not Use **$0000\ 0111_B$** : Do Not Use **$0000\ 1000_B$** : Do Not Use **$0000\ 1001_B$** : Do Not Use **$0000\ 1010_B$** : Reserved **$0000\ 1011_B$** : Do Not Use **$0000\ 1100_B$** : Do Not Use **$0000\ 1101_B$** : Do Not Use **$0000\ 1110_B$** : Do Not Use **$1111\ 1110_B$** : Do Not Use **$1111\ 1111_B$** : Do Not Use **All others** : Reserved

MR6_Basic Configuration 2 (MA<7:0> = 06H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP<7:0>	**0000 0011$_B$:** H-version

Notes :MR6 is vendor specific.

MR7_Basic Configuration 3 (MA<7:0> = 07H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP<7:0>	**0000 0000$_B$:** A-version

Notes :MR7 is vendor specific.

MR8_Basic Configuration 4 (MA<7:0> = 08H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP<1:0>	**00$_B$**: SDRAM **01$_B$**: Reserved **10$_B$**: Do Not Use **11$_B$**: Reserved
Density	Read-only	OP<5:2>	**0000$_B$**: 64Mb **0001$_B$**: 128Mb **0010$_B$**: 256Mb **0011$_B$**: 512Mb **0100$_B$**: 1Gb **0101$_B$**: 2Gb **0110$_B$**: 4Gb **0111$_B$**: 8Gb **1000$_B$**: 16Gb **1001$_B$**: 32Gb **all others**: reserved
I/O width	Read-only	OP<7:6>	**00$_B$**: x32 **01$_B$**: x16 **10$_B$**: x8 **11$_B$**: Do Not Use

MR9_Test Mode (MA<7:0> = 09H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

MR10_Calibration (MA<7:0> = 0AH):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write-only	OP<7:0>	**0xFF:** Calibration command after initialization **0xAB:** Long calibration **0x56:** Short calibration **0xC3:** ZQ Reset **others:** Reserved

Notes:
1.Host processor shall not write MR10 with “Reserved” values.
2.LPDDR2 devices shall ignore calibration command when a “Reserved” value is written into MR10.
3.See AC timing table for the calibration latency.
4.If ZQ is connected to V_{SSCA} through R_{ZQ}, either the ZQ calibration function (see "Mode Register Write ZQ Calibration Command" on [Command Definition & Timing Diagram]) or default calibration (through the ZQ reset command) is supported. If ZQ is connected to VDD2, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
5.LPDDR2 devices that do not support calibration shall ignore the ZQ Calibration command.
6.Optionally,the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR_11:15_(Reserved) (MA<7:0> = 0BH-0FH):

MR_16_PASR_Bank Mask (MA<7:0> = 010H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask (4-Bank or 8-Bank)							

SDRAM:

Bank <7:0> Mask [1)]	Write-only	OP<7:0>	0_B: refresh enable to the bank (=unmasked, default) 1_B: refresh blocked (=masked)

Notes :1) For 4 bank SDRAM, only OP<3:0> are used.

OP	Bank Mask	4 Bank	8 Bank
0	XXXXXXX1	Bank 0	Bank 0
1	XXXXXX1X	Bank 1	Bank 1
2	XXXXX1XX	Bank 2	Bank 2
3	XXXX1XXX	Bank 3	Bank 3
4	XXX1XXXX	-	Bank 4
5	XX1XXXXX	-	Bank 5
6	X1XXXXXX	-	Bank 6
7	1XXXXXXX	-	Bank 7

MR17_PASR_Segment Mask (MA<7:0> = 011_H): 1Gb ~ 8Gb S4 SDRAM only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment <7:0> Mask	Write-only	OP<7:0>	0_B: refresh enable to the segment (=unmasked, default) 1_B: refresh blocked (=masked)

			1Gb	2Gb/4Gb	8Gb
Segment	**OP**	**Segment Mask**	**R12:10**	**R13:11**	**R14:12**
0	0	XXXXXXX1	000_B		
1	1	XXXXXX1X	001_B		
2	2	XXXXX1XX	010_B		
3	3	XXXX1XXX	011_B		
4	4	XXX1XXXX	100_B		
5	5	XX1XXXXX	101_B		
6	6	X1XXXXXX	110_B		
7	7	1XXXXXXX	111_B		

Notes :This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment.

MR18-19_(Reserved) (MA<7:0> = 012_H - 013_H):

MR20-31_(Do Not Use) (MA<7:0> = 14_H -$1F_H$):

MR32_DQ Calibration Pattern A (MA<7:0>=20_H)

Reads to MR32 return DQ Calibration Pattern "A". See "DQ Calibration" on Operations & Timing Diagram.

MR33:39_(Do Not Use) (MA<7:0> = 21_H-27_H):

MR40_DQ Calibration Pattern B (MA<7:0>=28_H):

Reads to MR40 return DQ Calibration Pattern "B". See "DQ Calibration" on Operations & Timing Diagram

MR41:47_(Do Not Use) (MA<7:0> = 29_H-$2F_H$):

MR48:62_(Reserved) (MA<7:0> = 30_H-$3E_H$):

MR63_Reset (MA<7:0> = $3F_H$): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

Notes :
1. For additional information on MRW RESET see "Mode Register Write Command" on [Command Definition & Timing Diagram].

MR64:126_(Reserved) (MA<7:0> = 40$_H$-7E$_H$):

MR127_(Do Not Use) (MA<7:0> = 7F$_H$):

MR128:190_(Reserved for Vendor Use) (MA<7:0> = 80$_H$-BE$_H$):

MR191_(Do Not Use) (MA<7:0> = BF$_H$):

MR192:254_(Reserved for Vendor Use) (MA<7:0> = C0$_H$-FE$_H$):

MR255:(Do Not Use) (MA<7:0> = FF$_H$):

4. TRUTH TABLES

4.1 Truth Tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

[Table 11] Command truth table

	SDR Command Pins			DDR CA pins (10)										
SDRAM Command	CKE		CS#	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK EDGE
	CK(n-1)	CK(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
			X	MA6	MA7	X								↓
Refresh (per bank)11)	H	H	L	L	L	H	L	X						↑
			X	X										↓
Refresh (all bank)	H	H	L	L	L	H	H	X						↑
			X	X										↓
Enter Self Refresh	H	L	L	L	L	H	X							↑
	X		X	X										↓
Activate (bank)	H	H	L	L	H	R8/a15	R9/a16	R10/a17	R11/a18	R12/a19	BA0	BA1	BA2	↑
			X	R0/a5	R1/a6	R2/a7	R3/a8	R4/a9	R5/a10	R6/a11	R7/a12	R13/a13	R14/a14	↓
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
			X	AP[3),4)])	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
			X	AP[3),4)]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Precharge (pre bank, all bank)	H	H	L	H	H	L	H	AB/a30	X/a31	/a32	BA0	BA1	BA2	↑
			X	X/a20	X/a21	X/a22	X/a23	X/a24	X/a25	X/a26	X/a27	X/a28	X/a29	↓
BST	H	H	L	H	H	L	L	X						↑
			X	X										↓
Enter Deep Power Down	H	L	L	H	H	L	X							↑
	X		X	X										↓
NOP	H	H	L	H	H	H	X							↑
			X	X										↓
Maintain PD, SREF, DPD (NOP)	L	L	L	H	H	H	X							↑
			X	X										↓
NOP	H	H	H	X										↑
			X	X										↓
Maintain PD, SREF, DPD (NOP)	L	L	H	X										↑
			X	X										↓

SDRAM Command	SDR Command Pins			DDR CA pins (10)										
	CKE		CS#	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK EDGE
	CK(n-1)	CK(n)												
Enter Power Down	H	L	H	X										↑
	X		X	X										↓
Exit PD, SREF, DPD	L	H	H	X										↑
	X		X	X										↓

Notes:
1)All LPDDR2 commands are defined by states of CS#, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2)For LPDDR2 SDRAM, Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
3)AP is significant only to SDRAM.
4)AP “high” during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
5)“X” means “H or L (but a defined logic level)”
6)Self refresh exit and Deep Power Down exit are asynchronous.
7)VRef must be between 0 and VDDQ during Self Refresh and Deep Power Down operation.
8)CAxr refers to command/address bit “x” on the rising edge of clock.
9)CAxf refers to command/address bit “x” on the falling edge of clock.
10)CS #and CKE are sampled at the rising edge of clock.
11)Per Bank Refresh is only allowed in devices with 8 banks.
12)The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
13)AB "high" during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.

4.2 LPDDR2-SDRAM Truth Tables

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the Banks.

[Table 12] LPDDR2 : CKE Table

Device Current State[3]	CKE$_{n-1}$[1]	CKE$_n$[1]	CS#[2]	Command n[4]	Operation n[4]	Device Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6, 9
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6, 9
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6, 9, 12
Deep Power Down	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7, 10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	
	H	L	L	Enter Self-Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Deep Power Down	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
	H	H	Refer to the Command Truth Table				

NOTE :

1)"CKE$_n$" is the logic state of CKE at clock rising edge n; "CKE$_{n-1}$" was the state of CKE at the previous clock edge.
2)"CS#" is the logic state of CS# at the clock rising edge n;
3)"Current state" is the state of the LPDDR2 device immediately prior to clock edge n.
4)"Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".
5)All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
6)Power Down exit time (t$_{XP}$) should elapse before a command other than NOP is issued.
7)Self-Refresh exit time (t$_{XSR}$) should elapse before a command other than NOP is issued.
8)The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9)The clock must toggle at least twice during the t$_{XP}$ period.
10)The clock must toggle at least twice during the t$_{XSR}$ time.

11.'X' means 'Don't care'.
12.Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.

[Table 13] Current State Bank n - Command to Bank n

Current State	Command	Operation	Next State	NOTES
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing(All Bank)	7
	MRW	Load value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	7, 8
	Precharge	Deactivate row in bank or banks	Precharging	9, 15
Row Active	Read	Select column, and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10, 11
	Write	Select column, and start write burst	Writing	10, 11, 12
	BST	Read burst terminate	Active	13
Writing	Write	Select column, and start new write burst	Writing	10, 11
	Read	Select column, and start read burst	Reading	10, 11, 14
	BST	Write burst terminate	Active	13
Power On	Reset	Begin Device Auto-Initialization	Resetting	7, 9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:

1.The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Power Down.

2.All states and sequences not shown are illegal or reserved.

3.Current State Definitions:

-Idle: The bank or banks have been precharged, and tRP has been met.

-Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accesses are in progress.

-Reading: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

-Writing: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

4.The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and [Table 2]PinPad Definition and Description, and according to [Table 1]LPDDR2 SDRAM Addressing.

-Precharging: starts with the registration of a Precharge command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

-Row Activating: starts with registration of an Activate command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'Active' state.

-Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.

-Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

5.The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.

-Refreshing (Per Bank): starts with registration of an Refresh (Per Bank) command and ends when tRFCpb is met. Once tRFCpb is met, the bank will be in an 'idle' state.

-Refreshing (All Bank): starts with registration of an Refresh (All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.

-Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.

-Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.

-Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.

-MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.

-Precharging All: starts with the registration of a Precharge-All command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

6.Bank-specific; requires that the bank is idle and no bursts are in progress.

7.Not bank-specific; requires that all banks are idle and no bursts are in progress.

8.Not bank-specific reset command is achieved through Mode Register Write command.

9.This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.

10.A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.

11.The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.

12.A Write command may be applied after the completion of the Read burst; otherwise, a BST must be used to end the Read prior to asserting a Write command.

13Not bank-specific. Burst Terminate (BST) command affects the most recent read/write burst started by the most recent Read/Write command, regardless of bank.

14.A Read command may be applied after the completion of the Write burst; otherwise, a BST must be used to end the Write prior to asserting a Read command.

15.If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.

[Table 14] Current State Bank n - Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	NOTES
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	18
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	7
	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8
	Precharge	Deactivate row in bank or banks	Precharging	9
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	10, 11, 13
	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	18
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8, 14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8, 16
	Write	Select column, and start write burst to Bank m	Writing	8
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15
	Write	Select column, and start write burst to Bank m	Writing	8, 14, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15, 16
	Write	Select column, and start write burst to Bank m	Writing	8, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Power On	Reset	Begin Device Auto-Initialization	Resetting	12, 17
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes :

1.The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.

2.All states and sequences not shown are illegal or reserved.

3.Current State Definitions:

-Idle: the bank has been precharged, and tRP has been met.

-Active: a row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

-Reading: a Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

-Writing: a Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

4.Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.

5.A Burst Terminate (BST) command cannot be issued to another bank; it applies to the bank represented by the current state only.

6.The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:

-Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.

-Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.

-Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.

-MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.

7.tRRD must be met between Activate command to Bank n and a subsequent Activate command to Bank m.

8.Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.

9.This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.

10.MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when tRCD is met.)

11.MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when tRP is met.

12.Not bank-specific; requires that all banks are idle and no bursts are in progress.

13.The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon tRCD and tRP respec- tively.

14.A Write command may be applied after the completion of the Read burst, otherwise a BST must be issued to end the Read prior to asserting a Write command.

15.Read with Auto Precharge enabled or a Write with Auto Precharge enabled may be followed by any valid command to other banks provided that the timing restrictions in Precharge & Auto Precharge clarification on Timing spec are followed.

16.A Read command may be applied after the completion of the Write burst; otherwise, a BST must be issued to end the Write prior to asserting a Read command.

17.Reset command is achieved through Mode Register Write command.

18.BST is allowed only if a Read or Write burst is ongoing.

4.3 Data mask truth table

Table 15 DM truth table provides the data mask truth table.

[Table 15] DM truth table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

Notes :Used to mask write data, provided coincident with the corresponding data.

5. ABSOLUTE MAXIMUM DC RATINGS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

[Table 16] Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	2
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.6	V	2,4
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	2,3
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.6	V	
Storage Temperature	TSTG	-55	125	℃	5

Notes:
1.Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2.See “Power-Ramp” section in "Power-up, Initialization, and Power-Off" on [Command Definition & Timing Diagram] for relationships between power supplies.
3.VRefDQ ≤ 0.6 × VDDQ; however, VRefDQ may be ≥ VDDQ provided that VRefDQ ≤ 300mV.
4.VRefCA ≤ 0.6 × VDD2; however, VRefCA may be ≥ VDD2 provided that VRefCA ≤ 300mV.
5.Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

6. AC & DC OPERATING CONDITIONS

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

6.1 Recommended DC Operating Conditions

[Table 17] Recommended LPDDR2 DC Operating Conditions

Symbol	LPDDR2			DRAM	Unit
	Min	Typ	Max		
VDD1	1.70	1.80	1.95	Core Power1	V
VDD2	1.14	1.20	1.3	Core Power2	V
VDDQ	1.14	1.20	1.3	I/O Buffer Power	V

Notes :

1. VDD1 uses significantly less power than VDD2.

6.2 Input Leakage Current

[Table 18] Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage current For CA, CKE, CS#, CK, CK# Any input 0V ≤VIN ≤VDD2 (All other pins not under test = 0V)	I_L	-2	2	uA	2
VRef supply leakage current VRefDQ = VDDQ/2 or VRefCA = VDD2/2 (All other pins not under test = 0V)	I_{VREF}	-1	1	uA	1

Notes:

1. The minimum limit requirement is for testing purposes. The leakage current on VRefCA and VRefDQ pins should be minimal.
2. Although DM is for input only, the DM leakage shall match the DQ and DQS/DQS# output leakage specification.

6.3 Operating Temperature Range

[Table 19] Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard	TOPER	-40	85	℃
Extended		85	105	

Notes :

1.Operating Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

2.Either the device case temperature rating or the temperature sensor (See "Temperature Sensor" on [Command Definition & Timing Diagram]) may be used to set an appropriate refresh rate(SDRAM), determine the need for AC timing de-rating(SDRAM) and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Extended Temperature Ranges. For example, TCASE may be above 85℃ when the temperature sensor indicates a temperature of less than 85℃

7.0 AC AND DC INPUT MEASUREMENT LEVELS

7.1 AC and DC Logic Input Levels for Single-Ended Signals

7.1.1 AC and DC Input Levels for Single-Ended CA and CS_n Signals

[Table 20] Single-Ended AC and DC Input Levels for CA and CS# inputs

Symbol	Parameter	LPDDR2-1066 to LPDDR2-533		Unit	Notes
		Min	Max		
V_{IHCA}(AC)	AC input logic high	Vref + 0.220	Note 2	V	1,2
V_{ILCA}(AC)	AC input logic low	Note 2	Vref - 0.220	V	1,2
V_{IHCA}(DC)	DC input logic high	Vref + 0.130	VDD2	V	1
V_{ILCA}(DC)	DC input logic low	VSSCA	Vref - 0.130	V	1
V_{RefCA}(DC)	Reference Voltage for CA and CS# inputs	0.49 × VDD2	0.51 × VDD2	V	3,4

Notes :
1. For CA and CS# input only pins. VRef = VRefCA(DC).
2. See Overshoot and Undershoot Specifications on page37.
3. The ac peak noise on VRefCA may not allow VRefCA to deviate from VRefCA(DC) by more than +/-1% VDD2 (for reference: approx. +/- 12 mV).
4. For reference: approx. VDD2/2 +/- 12 mV.

7.2 AC and DC Input Levels for CKE

[Table 21] Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHCKE}	CKE Input High Level	0.8 × VDD2	Note 1	V	1
V_{ILCKE}	CKE Input Low Level	Note 1	0.2 × VDD2	V	1

Notes :
1. See Overshoot and Undershoot Specifications on page 37.

7.2.1AC and DC Input Levels for Single-Ended Data Signals

[Table 22] Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	LPDDR2-1066 to LPDDR2-533		Unit	Notes
		Min	Max		
V_{IHDQ}(AC)	AC input logic high	Vref + 0.220	Note 2	V	1, 2
V_{ILDQ}(AC)	AC input logic low	Note 2	Vref - 0.220	V	1, 2
V_{IHDQ}(DC)	DC input logic high	Vref + 0.130	VDDQ	V	1
V_{ILDQ}(DC)	DC input logic low	VSSQ	Vref - 0.130	V	1
V_{RefDQ}(DC)	Reference Voltage for DQ, DM inputs	0.49 × VDDQ	0.51 × VDDQ	V	3, 4

Notes :
1.For DQ input only pins. Vref = VRefDQ(DC).
2.See Overshoot and Undershoot Specifications on page 37.
3.The ac peak noise on VRefDQ may not allow VRefDQ to deviate from VRefDQ(DC) by more than +/-1% VDDQ (for reference: approx. +/ - 12 mV).
4.For reference: approx. VDDQ/2 +/- 12 mV.

8.0 AC AND DC OUTPUT MEASUREMENT LEVELS

8.1 Single Ended AC and DC Output Levels

Table 23 shows the output levels used for measurements of single ended signals.

[Table 23] Single-ended AC and DC Output Levels

Symbol	Parameter		LPDDR2-1066 to LPDDR2-533	Unit	Notes
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)		0.9 × V_{DDQ}	V	1
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)		0.1 × V_{DDQ}	V	2
V_{OH}(AC)	AC output high measurement level (for output slew rate)		V_{Ref}DQ+ 0.12	V	
V_{OL}(AC)	AC output low measurement level (for output slew rate)		V_{Ref}DQ- 0.12	V	
I_{OZ}	Output Leakage current (DQ, DM, DQS, DQS#) (DQ, DQS, DQS #are disabled; 0V ≤ VOUT ≤ VDDQ	Min	-5	uA	
		Max	5	uA	
MM_{PUPD}	Delta RON between pull-up and pull-down for DQ/DM	Min	-15	%	
		Max	15	%	

Notes :
1. IOH = -0.1mA.
2. IOL = 0.1mA.

8.2 Differential AC and DC Output Levels

Table 24 shows the output levels used for measurements of differential signals (DQS, DQS#).

[Table 24] Differential AC and DC Output Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-533	Unit	Notes
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	+ 0.20 × VDDQ	V	
V_{OLdiff}(AC)	AC differential output low measurement level (for output SR)	- 0.20 × VDDQ	V	

Notes :
1) IOH = -0.1mA.
2) IOL = 0.1mA.

8.3 Overshoot and Undershoot Specifications

[Table 25] AC Overshoot/Undershoot Specification.

Parameter		1066	800	667	533	Units
Maximum peak amplitude allowed for overshoot area.	Max	0.35				V
Maximum peak amplitude allowed for undershoot area.	Max	0.35				V
Maximum area above VDD.	Max	0.15	0.20	0.24	0.30	V-ns
Maximum area below VSS.	Max	0.15	0.20	0.24	0.30	V-ns

(CA0-9, CS#, CKE, CK, CK#, DQ, DQS, DQS#, DM)

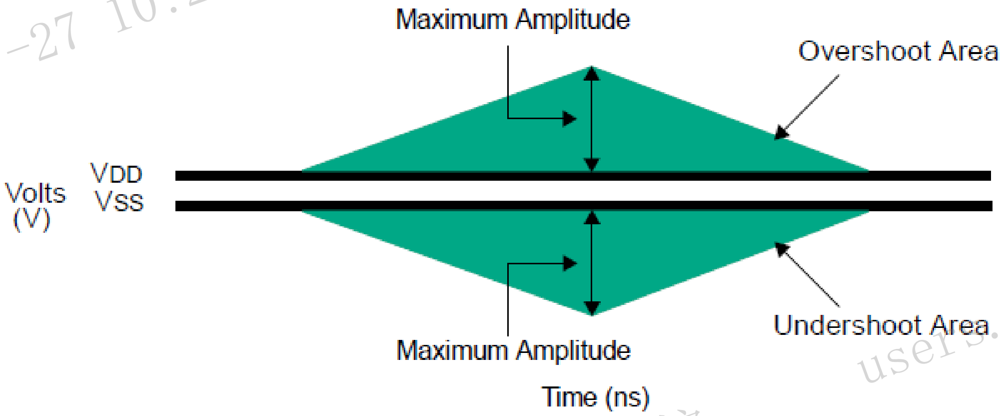


Figure 8-1 Overshoot and Undershoot Definition

Notes：
1.For CA0-9, CK, CK#, CS#, and CKE, VDD stands for VDD2. For DQ, DM, DQS, and DQS#, VDD stands for VDDQ.
2.For CA0-9, CK, CK#, CS#, and CKE, VSS stands for VSSCA. For DQ, DM, DQS, and DQS#, VSS stands for VSSQ.
3.Maximum peak amplitude values are referenced from actual VDD and VSS values.
4.Maximum area values are referenced from maximum operating VDD and VSS values

9.0 INPUT/OUTPUT CAPACITANCE

[Table 26] Input/output capacitance

Parameter	Symbol		LPDDR2 1066-533	Units	Notes
Input capacitance, CK and CK#	CCK	Min	1.0	pF	1,2
		Max	3.0	pF	1,2
Input capacitance delta, CK and CK#	CDCK	Min	0.0	pF	1,2,3
		Max	0.20	pF	1,2,3
Input capacitance, all other input-only pins	CI	Min	1.0	pF	1,2,4
		Max	3.0	pF	1,2,4
Input capacitance delta, all other input-only pins	CDI	Min	-0.5	pF	1,2,5
		Max	0.5	pF	1,2,5
Input/output capacitance, DQ, DM, DQS, DQS#	CIO	Min	1.25	pF	1,2,6,7
		Max	3.5	pF	1,2,6,7
Input/output capacitance delta, DQS, DQS#	CDDQS	Min	0.0	pF	1,2,7,8
		Max	0.25	pF	1,2,7,8
Input/output capacitance delta, DQ, DM	CDIO	Min	-0.5	pF	1,2,7,9
		Max	0.5	pF	1,2,7,9
Input/output capacitance ZQ Pin	CZQ	Min	0.0	pF	1,2
		Max	3.5	pF	1,2

Notes :
1.This parameter applies to both die and package.
2.This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating.
3.Absolute value of CCK – CCK#.
4.CI applies to CS#, CKE, CA0-CA9.
5.CDI = CI - 0.5 × (CCK + CCK#)
6.DM loading matches DQ and DQS.
7.MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ohm typical)
8.Absolute value of CDQS and CDQS#.
9.CDIO = CIO - 0.5 × (CDQS + CDQS#) in byte-lane.

10.0 IDD SPECIFICATION PARAMETERS AND TEST CONDITIONS

10.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:
LOW: $V_{IN} \leq V_{IL}$(DC) MAX
HIGH: $V_{IN} \geq V_{IH}$ (DC) MIN
STABLE: Inputs are stable at a HIGH or LOW level SWITCHING: See Table 27 and Table 28.

[Table 27] Definition of Switching for CA Input Signals

Switching for CA								
	CK (RISING) / CK# (FALLING)	CK (FALLING)/ CK# (RISING)	CK (RISING) / CK# (FALLING)	CK (FALLING) / CK# (RISING)	CK (RISING) / CK# (FALLING)	CK (FALLING) / CK# (RISING)	CK (RISING) / CK#(FALLING)	CK (FALLING) / CK# (RISING)
Cycle	N		N+1		N+2		N+3	
CS#	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Notes :
1.CS# must always be driven HIGH.
2.50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3.The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require SWITCHING on the CA bus.

[Table 28] Definition of Switching for IDD4R

Clock	CKE	CS#	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Read_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Read_Rising	HLH	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Read_Falling	LLL	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

Notes:
1.Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2.The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4R.

[Table 29] Definition of Switching for IDD4W

Clock	CKE	CS#	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Write_Rising	HLL	LHLHLHL	L
Falling	HIGH	LOW	N	Write_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Write_Rising	HLL	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Write_Falling	LLL	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

Notes：
1.Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2.Data masking (DM) must always be driven LOW.
3.The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.

10.2 IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the standard range.

[Table 30] LPDDR2 IDD Specification Parameters and Operating Condition

Parameter/Condition	Symbol	Power Supply	Units	Notes
Operating one bank active-precharge current (SDRAM) : $t_{CK} = t_{CK(avg)min}$; $t_{RC} = t_{RCmin}$; CKE is HIGH; CS# is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD0_{1}$	VDD1	mA	3
	$IDD0_{2}$	VDD2	mA	3
	$IDD0_{IN}$	VDD2 + VDDQ	mA	3,4
Idle power-down standby current: $t_{CK} = t_{CK(avg)min}$; CKE is LOW; CS# is HIGH; All banks/RBs idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2P_{1}$	VDD1	mA	3
	$IDD2P_{2}$	VDD2	mA	3
	$IDD2P_{IN}$	VDD2 + VDDQ	mA	3,4
Idle power-down standby current with clock stop: CK =LOW, CK# =HIGH; CKE is LOW; CS# is HIGH; All banks/RBs idle; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD2PS_{1}$	VDD1	mA	3
	$IDD2PS_{2}$	VDD2	mA	3
	$IDD2PS_{IN}$	VDD2 + VDDQ	mA	3,4
Idle non power-down standby current: $t_{CK} = t_{CK(avg)min}$; CKE is HIGH; CS# is HIGH; All banks/RBs idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2N_{1}$	VDD1	mA	3
	$IDD2N_{2}$	VDD2	mA	3
	$IDD2N_{IN}$	VDD2 + VDDQ	mA	3,4
Idle non power-down standby current with clock stop: CK=LOW, CK#=HIGH; CKE is HIGH; CS# is HIGH; All banks/RBs idle; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD2NS_{1}$	VDD1	mA	3
	$IDD2NS_{2}$	VDD2	mA	3
	$IDD2NS_{IN}$	VDD2 + VDDQ	mA	3,4

Parameter/Condition	Symbol	Power Supply	Units	Notes
Active power-down standby current: t_{CK} = $t_{CK(avg)min}$; CKE is LOW; CS# is HIGH; One bank/RB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD3P$_1$	VDD1	mA	3
	IDD3P$_2$	VDD2	mA	3
	IDD3P$_{IN}$	VDD2 + VDDQ	mA	3,4
Active power-down standby current with clock stop: CK=LOW, CK#=HIGH; CKE is LOW; CS #is HIGH; One bank/RB active; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD3PS$_1$	VDD1	mA	3
	IDD3PS$_2$	VDD2	mA	3
	IDD3PS$_{IN}$	VDD2 + VDDQ	mA	3,4
Active non power-down standby current: t_{CK} = $t_{CK(avg)min}$; CKE is HIGH; CS# is HIGH; One bank/RB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD3N$_1$	VDD1	mA	3
	IDD3N$_2$	VDD2	mA	3
	IDD3N$_{IN}$	VDD2 + VDDQ	mA	3,4
Active non power-down standby current with clock stop: CK=LOW, CK#=HIGH; CKE is HIGH; CS# is HIGH; One bank/RB active; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD3NS$_1$	VDD1	mA	3
	IDD3NS$_2$	VDD2	mA	3
	IDD3NS$_{IN}$	VDD2 + VDDQ	mA	3,4
Operating burst read current: t_{CK} = $t_{CK(avg)min}$; CS# is HIGH between valid commands; One bank/RB active; BL = 4; RL = RLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	IDD4R$_1$	VDD1	mA	3
	IDD4R$_2$	VDD2	mA	3
	IDD4R$_{IN}$	VDD2	mA	3
	IDD4R$_Q$	VDDQ	mA	3,6
Operating burst write current: t_{CK} = $t_{CK(avg)min}$; CS is HIGH between valid commands; One bank/RB active; BL = 4; WL = WLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	IDD4W$_1$	VDD1	mA	3
	IDD4W$_2$	VDD2	mA	3
	IDD4W$_{IN}$	VDD2 + VDDQ	mA	3,4
All Bank Refresh Burst current: t_{CK} = $t_{CK(avg)min}$; CKE is HIGH between valid commands; t_{RC} = $t_{RFCabmin}$; Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	IDD5$_1$	VDD1	mA	3
	IDD5$_2$	VDD2	mA	3
	IDD5$_{IN}$	VDD2 + VDDQ	mA	3,4
All Bank Refresh Average current: t_{CK} = $t_{CK(avg)min}$; CKE is HIGH between valid commands; t_{RC} = t_{REFI}; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	IDD5AB$_1$	VDD1	mA	3
	IDD5AB$_2$	VDD2	mA	3
	IDD5AB$_{IN}$	VDD2 + VDDQ	mA	3,4
Per Bank Refresh Average current: t_{CK} = $t_{CK(avg)min}$; CKE is HIGH between valid commands; t_{RC} = t_{REFI}/8; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	IDD5PB$_1$	VDD1	mA	1,3
	IDD5PB$_2$	VDD2	mA	1,3
	IDD5PB$_{IN}$	VDD2 + VDDQ	mA	1,3,4

Parameter/Condition	Symbol	Power Supply	Units	Notes
Self refresh current (Standard Temperature Range): CK=LOW,CK#=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE; Maximum 1x Self-Refresh Rate;	$IDD6_1$	VDD1	mA	2,3,8,9
	$IDD6_2$	VDD2	mA	2,3,8,9
	$IDD6_{IN}$	VDD2 + VDDQ	mA	2,3,4,8,9
Deep Power-Down current: CK=LOW,CK#=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;	$IDD8_1$	VDD1	uA	3,11,10
	$IDD8_2$	VDD2	uA	3,11,10
	$IDD8_{IN}$	VDD2 + VDDQ	uA	3,4,11,10

Notes:
1.Per Bank Refresh only applicable for LPDDR2 devices of 1Gb or higher densities.
2.This is the general definition that applies to full array Self Refresh. Refer to Table 32, IDD6 Partial Array Self-Refresh Current for details of Partial Array Self Refresh IDD6 specification.
3.IDD values published are the maximum of the distribution of the arithmetic mean.
4.Measured currents are the summation of VDDQ and VDD2.
5.To calculate total current consumption, the currents of all active operations must be considered.
6.Guaranteed by design with output load of 5pF and RON=40Ohm.
7.IDD current specifications are tested after the device is properly initialized.
8.In addition, supplier data sheets may include additional Self Refresh IDD values for temperature subranges within the Standard or Extended Temperature Ranges.
9.1x Self-Refresh Rate is the rate at which the LPDDR2 device is refreshed internally during Self-Refresh before going into the Extended Temperature range.
10.DPD (Deep Power Down) function is an optional feature, and it will be enabled upon request.

10.3 IDD Spec Table

[Table 31] IDD Specification for 1Gb LPDDR2

Symbol			Power Supply	VDD2=1.2V				Units
				1066Mbps	800Mbps	667Mbps	533Mbps	
IDD0	IDD0$_{1}$		VDD1	6	6	6	6	mA
	IDD0$_{2}$		VDD2	43	41	39	38	mA
	IDD0$_{IN}$		VDD2 + VDDQ	0.1	0.1	0.1	0.1	mA
IDD2P	IDD2P$_{1}$	25°C	VDD1	0.12				mA
		85°C		0.2				
		105°C		0.5				
	IDD2P$_{2}$	25°C	VDD2	0.31				mA
		85°C		0.65				
		105°C		1.3				
	IDD2P$_{IN}$	25°C	VDD2 + VDDQ	0.01				mA
		85°C		0.05				
		105°C		0.1				
IDD2PS	IDD2PS$_{1}$	25°C	VDD1	0.12				mA
		85°C		0.2				
		105°C		0.5				
	IDD2PS$_{2}$	25°C	VDD2	0.31				mA
		85°C		0.65				
		105°C		1.3				
	IDD2PS$_{IN}$	25°C	VDD2 + VDDQ	0.01				mA
		85°C		0.05				
		105°C		0.1				
IDD2N	IDD2N$_{1}$		VDD1	1	1	1	1	mA
	IDD2N$_{2}$		VDD2	15	14	13	12	mA
	IDD2N$_{IN}$		VDD2 + VDDQ	0.1	0.1	0.1	0.1	mA
IDD2NS	IDD2NS$_{1}$		VDD1	1	1	1	1	mA
	IDD2NS$_{2}$		VDD2	9	9	9	9	mA
	IDD2NS$_{IN}$		VDD2 + VDDQ	0.1.	0.1	0.1	0.1	mA
IDD3P	IDD3P$_{1}$		VDD1	2	2	2	2	mA
	IDD3P$_{2}$		VDD2	6	6	6	6	mA
	IDD3P$_{IN}$		VDD2 + VDDQ	0.1	0.1	0.1	0.1	mA
IDD3PS	IDD3PS$_{1}$		VDD1	2	2	2	2	mA
	IDD3PS$_{2}$		VDD2	6	6	6	6	mA
	IDD3PS$_{IN}$		VDD2 + VDDQ	0.1	0.1	0.1	0.1	mA
IDD3N	IDD3N$_{1}$		VDD1	2	2	2	2	mA
	IDD3N$_{2}$		VDD2	17	16	15	14	mA
	IDD3N$_{IN}$		VDD2 + VDDQ	0.1	0.1	0.1	0.1	mA
IDD3NS	IDD3NS$_{1}$		VDD1	2	2	2	2	mA
	IDD3NS$_{2}$		VDD2	11	11	11	11	mA
	IDD3NS$_{IN}$		VDD2 + VDDQ	0.1	0.1	0.1	0.1	mA

Symbol			Power Supply	VDD2=1.2V				Units
				1066Mbps	800Mbps	667Mbps	533Mbps	
IDD4R	IDD4R1		VDD1	2	2	2	2	mA
	IDD4R2		VDD2	146	121	106	96	mA
	IDD4RQ		VDDQ	170	130	110	100	mA
IDD4W	$IDD4W_1$		VDD1	2	2	2	2	mA
	$IDD4W_2$		VDD2	145	120	105	95	mA
	$IDD4W_{IN}$		VDD2 + VDDQ	15	15	15	15	mA
IDD5	$IDD5_1$		VDD1	30	30	30	30	mA
	$IDD5_2$		VDD2	110	110	110	110	mA
	$IDD5_{IN}$		VDD2 + VDDQ	0.1	0.1	0.1	0.1	mA
IDD5AB	$IDD5AB_1$		VDD1	3	3	3	3	mA
	$IDD5AB_2$		VDD2	22	22	22	22	mA
	$IDD5AB_{IN}$		VDD2 + VDDQ	0.1	0.1	0.1	0.1	mA
IDD5PB	$IDD5PB_1$		VDD1	3	3	3	3	mA
	$IDD5PB_2$		VDD2	30	30	30	30	mA
	$IDD5PB_{IN}$		VDD2 + VDDQ	0.1	0.1	0.1	0.1	mA
IDD6	$IDD6_1$	25°C	VDD1	0.15				mA
		85°C		0.4				
		105°C		2.0				
	$IDD6_2$	25°C	VDD2	0.26				mA
		85°C		1.4				
		105°C		6.6				
	$IDD6_{IN}$	25°C	VDD2 + VDDQ	0.01				mA
		85°C		0.05				
		105°C		0.1				
IDD8	$IDD8_1$	45°C	VDD1	100				uA
		85°C		200				
		105°C		400				
	$IDD8_2$	45°C	VDD2	100				uA
		85°C		200				
		105°C		400				
	$IDD8_{IN}$	45°C	VDD2 + VDDQ	100				uA
		85°C		200				
		105°C		400				

[Table 32] IDD6 Partial Array Self-Refresh Current

Parameter			1Gb LPDDR2			Unit
			25℃	**85℃**	**105℃**	
IDD6 Partial Array Self-Refresh Current (max)	Full Array	VDD1	150	400	2000	uA
		VDD2	260	1400	6600	
		VDD2 + VDDQ	10	50	100	
	1/2 Array	VDD1	148	380	1900	uA
		VDD2	235	1180	5650	
		VDD2 + VDDQ	10	50	100	
	1/4 Array	VDD1	147	375	1850	uA
		VDD2	220	1050	5100	
		VDD2 + VDDQ	10	50	100	
	1/8 Array	VDD1	147	370	1830	uA
		VDD2	210	990	4800	
		VDD2 + VDDQ	10	50	100	

11.0 ELECTRICAL CHARACTERISTICS AND AC TIMING

11.1 LPDDR2 Refresh Requirements by Device Density

[Table 33] LPDDR2 Refresh Requirement Parameters (per density)

Parameter		Symbol	1 Gb	Unit
Number of Banks			8	
Refresh Window Tcase ≤ 85°C		tREFW	32	ms
Refresh Window 85°C ≤ Tcase ≤ 105°C		tREFW	8	ms
Required number of REFRESH commands (min)		R	4,096	
average time between REFRESH commands (for reference only) Tcase ≤ 85°C	REFab	tREFI	7.8	us
	REFpb	tREFIpb	0.975	us
average time between REFRESH commands (for reference only) 85°C ≤ Tcase ≤ 105°C	REFab	tREFI	1.95	us
	REFpb	tREFIpb	0.244	us
Refresh Cycle time		tRFCab	130	ns
Per Bank Refresh Cycle time		tRFCpb	60	ns
Burst Refresh Window $= 4 \times 8 \times t_{RFCab}$		tREFBW	4.16	us

Notes :

1.Please refer to the addressing table “LPDDR2 SDRAM Addressing”

11.2 AC Timings

[Table 34] LPDDR2 AC Timing Table

Parameter	Symbol	min max	min tCK	LPDDR2				Unit
				1066	800	667	533	
Max. Frequency$^{4)}$		~		533	400	333	266	MHz
Clock Timing								
Average Clock Period	t_{CK}(avg)	min		1.875	2.5	3.0	3.75	ns
		max		100				
Average high pulse width	t_{CH}(avg)	min		0.45				tCK(avg)
		max		0.55				
Average low pulse width	t_{CL}(avg)	min		0.45				tCK(avg)
		max		0.55				
Absolute Clock Period	t_{CK}(abs)	min		tCK(avg)min + tJIT(per),min				ps
Absolute clock HIGH pulse width (with allowed jitter)	t_{CH}(abs), allowed	min		0.43				tCK(avg)
		max		0.57				
Absolute clock LOW pulse width (with allowed jitter)	t_{CL}(abs), allowed	min		0.43				tCK(avg)
		max		0.57				
Clock Period Jitter (with allowed jitter)	t_{JIT}(per), allowed	min		-90	-100	-110	-120	ps
		max		90	100	110	120	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	t_{JIT}(cc), allowed	max		180	200	220	240	ps
Duty cycle Jitter (with allowed jitter)	t_{JIT}(duty), allowed	min		min((t_{CH}(abs),min - t_{CH}(avg),min), (t_{CL}(abs),min - t_{CL}(avg),min)) × t_{CK}(avg)				ps
		max		max((t_{CH}(abs),max - t_{CH}(avg),max), (t_{CL}(abs),max - t_{CL}(avg),max)) × t_{CK}(avg)				ps
Cumulative error across 2 cycles	t_{ERR}(2per), allowed	min		-132	-147	-162	-177	ps
		max		132	147	162	177	
Cumulative error across 3 cycles	t_{ERR}(3per), allowed	min		-157	-175	-192	-210	ps
		max		157	175	192	210	
Cumulative error across 4 cycles	t_{ERR}(4per), allowed	min		-175	-194	-214	-233	ps
		max		175	194	214	233	
Cumulative error across 5 cycles	t_{ERR}(5per), allowed	min		-188	-209	-230	-251	ps
		max		188	209	230	251	
Cumulative error across 6 cycles	t_{ERR}(6per), allowed	min		-200	-222	-244	-266	ps
		max		200	222	244	266	
Cumulative error across 7 cycles	t_{ERR}(7per), allowed	min		-209	-232	-256	-279	ps
		max		209	232	256	279	
Cumulative error across 8 cycles	t_{ERR}(8per), allowed	min		-217	-241	-266	-290	ps
		max		217	241	266	290	
Cumulative error across 9 cycles	t_{ERR}(9per), allowed	min		-224	-249	-274	-299	ps
		max		224	249	274	299	
Cumulative error across 10 cycles	t_{ERR}(10per), allowed	min		-231	-257	-282	-308	ps
		max		231	257	282	308	
Cumulative error across 11 cycles	t_{ERR}(11per), allowed	min		-237	-263	-289	-316	ps
		max		237	263	289	316	
Cumulative error across 12 cycles	t_{ERR}(12per), allowed	min		-242	-269	-296	-323	ps
		max		242	269	296	323	

Parameter	Symbol	min max	min tCK	LPDDR2 1066	800	667	533	Unit
Cumulative error across n = 13, 14 . . . 49, 50 cycles	$t_{ERR(nper)}$, allowed	min		$t_{ERR(nper),allowed, min} = (1 + 0.68ln(n)) \times t_{JIT(per), allowed, min}$				ps
		max		$t_{ERR(nper),allowed, max} = (1 + 0.68ln(n)) \times t_{JIT(per), allowed, max}$				
ZQ Calibration Parameters								
Initialization Calibration Time	t_{ZQINIT}	min		1				us
Full Calibration Time	t_{ZQCL}	min	6	360				ns
Short Calibration Time	t_{ZQCS}	min	6	90				ns
Calibration Reset Time	$t_{ZQRESET}$	min	3	50				ns
Read Parameters[11]								
DQS output access time from CK/CK#	t_{DQSCK}	min		2500				ps
		max		5500				
DQSCK Delta Short [15]	$t_{DQSCKDS}$	max		330	450	540	670	ps
DQSCK Delta Medium [16]	$t_{DQSCKDM}$	max		680	900	1050	1350	ps
DQSCK Delta Long [17]	$t_{DQSCKDL}$	max		920	1200	1400	1800	ps
DQS - DQ skew	t_{DQSQ}	max		200	240	280	340	ps
Data hold skew factor	t_{QHS}	max		230	280	340	400	ps
DQS Output High Pulse Width	t_{QSH}	min		$t_{CH}(abs) - 0.05$				$t_{CK}(avg)$
DQS Output Low Pulse Width	t_{QSL}	min		$t_{CL}(abs) - 0.05$				$t_{CK}(avg)$
Data Half Period	t_{QHP}	min		$min(t_{QSH}, t_{QSL})$				$t_{CK}(avg)$
DQ / DQS output hold time from DQS	t_{QH}	min		$t_{QHP} - t_{QHS}$				ps
Read preamble[12, 13]	t_{RPRE}	min		0.9				$t_{CK}(avg)$
Read postamble[12, 14]	t_{RPST}	min		$t_{CL}(abs) - 0.05$				$t_{CK}(avg)$
DQS low-Z from clock[12]	$t_{LZ(DQS)}$	min		$t_{DQSCK(MIN)} - 300$				ps
DQ low-Z from clock[12]	$t_{LZ(DQ)}$	min		$t_{DQSCK(MIN)} - (1.4 \times t_{QHS(MAX)})$				ps
DQS high-Z from clock[12]	$t_{HZ(DQS)}$	max		$t_{DQSCK(MAX)} - 100$				ps
DQ high-Z from clock[12]	$t_{HZ(DQ)}$	max		$t_{DQSCK(MAX)} + (1.4 \times t_{DQSQ(MAX)})$				ps
Write Parameters[11]								
DQ and DM input hold time (Vref based)	t_{DH}	min		210	270	350	430	ps
DQ and DM input setup time (Vref based)	t_{DS}	min		210	270	350	430	ps
DQ and DM input pulse width	t_{DIPW}	min		0.35				tCK(avg)
Write command to 1st DQS latching transition	t_{DQSS}	min		0.75				tCK(avg)
		max		1.25				
DQS input high-level width	t_{DQSH}	min		0.4				tCK(avg)
DQS input low-level width	t_{DQSL}	min		0.4				tCK(avg)
DQS falling edge to CK setup time	t_{DSS}	min		0.2				tCK(avg)
DQS falling edge hold time from CK	t_{DSH}	min		0.2				tCK(avg)
Write postamble	t_{WPST}	min		0.4				tCK(avg)
Write preamble	t_{WPRE}	min		0.35				tCK(avg)
CKE Input Parameters								
CKE min. pulse width (high and low pulse width)	t_{CKE}	min	3	3				tCK(avg)
CKE input setup time	t_{ISCKE}[2]	min		0.25				tCK(avg)
CKE input hold time	t_{IHCKE}[3]	min		0.25				tCK(avg)

Parameter	Symbol	min max	min tCK	LPDDR2				Unit
				1066	800	667	533	
Command Address Input Parameters 11)								
Address and control input setup time (Vref based)	t_{IS} 1)	min		220	290	370	460	ps
Address and control input hold time (Vref based)	t_{IH} 1)	min		220	290	370	460	ps
Address and control input pulse width	t_{IPW}	min		0.40				t_{CK}(avg)
Boot Parameters (10 MHz - 55 MHz) 5),7),8)								
Clock Cycle Time	t_{CKb}	max		100				ns
		min	-	18				
CKE Input Setup Time	t_{ISCKEb}	min	-	2.5				ns
CKE Input Hold Time	t_{IHCKEb}	min	-	2.5				ns
Address & Control Input Setup Time	t_{ISb}	min	-	1150				ps
Address & Control Input Hold Time	t_{IHb}	min	-	1150				ps
DQS Output Data Access Time from CK/CK#	t_{DQSCKb}	min	-	2.0				ns
		max		10.0				
Data Strobe Edge to Output Data Edge tDQSQb - 1.2	t_{DQSQb}	max	-	1.2				ns
Data Hold Skew Factor	t_{QHSb}	max	-	1.2				ns
Mode Register Parameters								
MODE REGISTER Write command period	t_{MRW}	min	5	5				t_{CK}(avg)
Mode Register Read command period	t_{MRR}	min	2	2				t_{CK}(avg)
LPDDR2 SDRAM Core Parameters 9)								
Read Latency	RL	min	3	8	6	5	4	t_{CK}(avg)
Write Latency	WL	min	1	4	3	2	2	t_{CK}(avg)
ACTIVE to ACTIVE command period	t_{RC}	min		t_{RAS} + t_{RPab} (with all-bank Precharge) t_{RAS} + t_{RPpb} (with per-bank Precharge)				ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	t_{CKESR}	min	3	15				ns
Self refresh exit to next valid command delay	t_{XSR}	min	2	tRFCab + 10				ns
Exit power down to next valid command delay	t_{XP}	min	2	7.5				ns
LPDDR2 CAS to CAS delay	t_{CCD}	min	2	2				tCK(avg)
Internal Read to Precharge command delay	t_{RTP}	min	2	7.5				ns
RAS to CAS Delay	t_{RCD}	min	3	18				ns
Row Precharge Time (single bank)	t_{RPpb}	min	3	18				ns
Row Precharge Time (all banks)	t_{RPab} 4-bank	min	3	18				ns
Row Precharge Time (all banks)	t_{RPab} 8-bank	min	3	21				ns
Row Active Time	t_{RAS}	min	3	42				ns
		max	-	70				us
Write Recovery Time	t_{WR}	min	3	15				ns
Internal Write to Read Command Delay	t_{WTR}	min	2	7.5				ns
Active bank A to Active bank B	t_{RRD}	min	2	10				ns
Four Bank Activate Window	t_{FAW}	min	8	50				ns
Minimum Deep Power Down Time	t_{DPD}	min		500				us

Parameter	Symbol	min max	min tCK	LPDDR2				Unit
				1066	800	667	533	
LPDDR2 Temperature De-Rating								
tDQSCK De-Rating	tDQSCK (Derated)	max		5620	6000			ps
Core Timings Temperature De-Rating for SDRAM	tRCD (Derated)	min		tRCD + 1.875				ns
	tRC (Derated)	min		tRAS(derated) + tRP(derated)				ns
	tRAS (Derated)	min		tRAS + 1.875				ns
	tRP (Derated)	min		tRP + 1.875				ns
	tRRD (Derated)	min		tRRD + 1.875				ns

Notes :
1)Input set-up/hold time for signal(CA0 ~ 9, CS#)
2)CKE input setup time is measured from CKE reaching high/low voltage level to CK/CK# crossing.
3)CKE input hold time is measured from CK/CK# crossing to CKE reaching high/low voltage level.
4)Frequency values are for reference only. Clock cycle time (tCK) shall be used to determine device capabilities.
5)To guarantee device operation before the LPDDR2 device is configured a number of AC boot timing parameters are defined in the Table 34, LPDDR2 AC Timing Table. Boot parameter symbols have the letter b appended, e.g. tCK during boot is tCKb.
6)Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.
7)The SDRAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in 3.1Mode Register Definition.
8)The output skew parameters are measured with Ron default settings into the reference load.
9)The min tCK column applies only when tCK is greater than 6ns for LPDDR2 devices. In this case, both min tCK values and analog timing (ns) shall be satisfied.
10)All AC timings assume an input slew rate of 1V/ns.
11)Read, Write, and Input Setup and Hold values are referenced to Vref.
12)For low-to-high and high-to-low transitions, the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure 11-1 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calcula- tion is consistent.

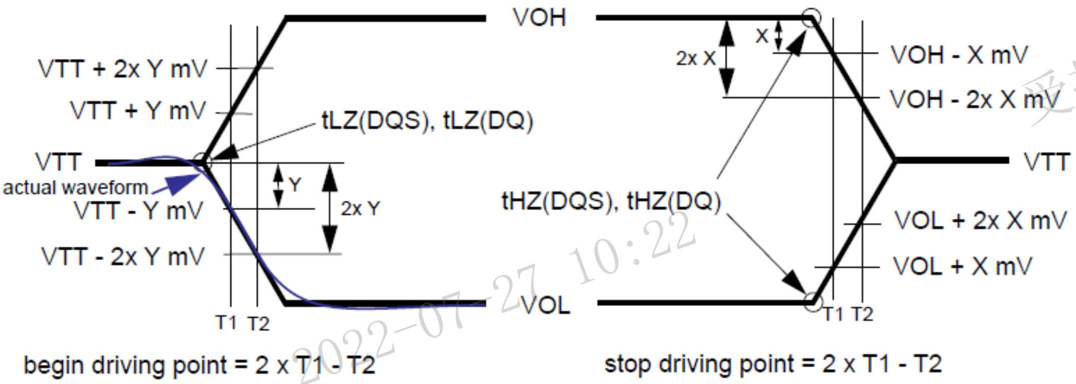


Figure 11-1. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS-DQS#.

13)Measured from the start driving of DQS – DQS# to the start driving the first rising strobe edge.

14)Measured from the start driving the last falling strobe edge to the stop driving DQS – DQS#.

15)tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a contiguous sequence of bursts within a 160ns roll- ing window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.

16)tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 1.6us rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.

17)tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.

18)Min tCK of 5 clocks is valid when the Overlay Window is disabled. Refer to Vendor datasheets for min tCK when the Overlay Window is enabled.

NAND Flash

12. Addressing

[Table 35] Address Cycle Map

Bus cycle	I/O_0	I/O_1	I/O_2	I/O_3	I/O_4	I/O_5	I/O_6	I/O_7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	L	L	L	L	
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	Row Address
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	

Notes:

Column Address : Starting Address of the Register.

A0 - A11 : column address in the page

A12 - A17 : page address in the block

A18 – A27 : block address

L must be set to "Low".

13. Command Sets

[Table 36] Command Sets

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
READ	00h	30h			
READ FOR COPY-BACK	00h	35h			
READ ID	90h	-			
RESET	FFh	-			Yes
READ CACHE (START)	31h				
READ CACHE (END)	3Fh	-			
PAGE PGM (start) / CACHE PGM (end)	80h	10h			
CACHE PGM (Start/continue)	80h	15h			
PAGE RE-PROGRAM	8Bh	10h			
COPY BACK PGM	85h	10h			
BLOCK ERASE	60h	D0h			
READ STATUS REGISTER	70h	-			Yes
RANDOM DATA INPUT	85h	-			
RANDOM DATA OUTPUT	05h	E0h			
READ CACHE ENHANCED (RANDOM)	00h	31h			

13.1 Page Read

This operation is initiated by writing 00h and 30h to the command register along with five address cycles. Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 45nsec (1.8V version) cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command.

Random data output can be operated multiple times regardless of how many times it is done in a page.

After power up device is in read mode, so 00h command cycle is not necessary to start a read operation. Any operation other than read or random data output causes device to exit read mode.

13.2 Page Program

A page program cycle consists of a serial data loading period in which up to 2112 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the four cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command (10h) initiates the programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the sys- tem controller for other tasks. Once the program process starts, the Read Status Register commands (70h) may be issu ed to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h) or Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. The device is programmed basically by page, but it also allows multiple partial page programming.

The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. for example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/16byte).

13.3 Page Re-program

This command allows the re-programming of the same pattern of the last (failed) page into another memory location. The command sequence initiates with re-program setup (8Bh), followed by the four cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the last page, the program confirm can be issued (10h) without any data input cycle. On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm “10h”

The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The “program confirm” command (10h) initiates the re- programming process.

The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be issued to read the status register. The system controller can detect the completion of a pro- gram cycle by monitoring the R/B output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

13.4 Block Erase

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command (60h). Only address A18 to A29 is valid while A12 to A17 are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase verify. Once the erase process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the R/B output, or the Status bit (I/O6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

13.5 Reset

The device offers a reset feature, executed by writing FFh to the command register. If the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations.
The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high. If the device is already in reset state a new reset command will not be accepted by the command register. The RB# pin transitions to low for tRST after the Reset command is written.

13.6 Copy-back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112 bytes(x8 Device) data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or Copy Back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in "Copy Back Program with Random Data Input". "When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, four bit error correction is recommended for the use of Copy-Back operation. shows the command sequence for the copy-back operation. Please note that there are two things to do during copy-back program. First, Random Data Input (with/without data) is entered before Program Confirm command(10h) after Random Data output. Second, WP# value is don't care during Read for copy back, while it must be set to Vcc When performing the program.

13.7 Read Status Register

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs . This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to be toggled for updated status. Refer to “Table 8-2 Status Register Coding" for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

[Table 37] Status Register Coding

I/O	Page Program	Block Erase	Read	Cache Read	Cache Program/ Cache reprogram	Definition
I/O$_0$	Pass/Fail	Pass/Fail	Not use	Not use	Pass/Fail(N)	N Page Pass : "0" Fail : "1"
I/O$_1$	Not use	Not use	Not use	Not use	Pass/Fail(N-1)	N-1 Page Pass : "0" Fail : "1"
I/O$_2$	Not use	Not use	Not use	Not use	Not use	Don't -cared
I/O$_3$	Not use	Not use	Not use	Not use	Not use	Don't -cared
I/O$_4$	Not use	Not use	Not use	Not use	Not use	Don't -cared
I/O$_5$	Ready/Busy	Ready/Busy	Ready/Busy	P/E/R Controller Bit	Ready/Busy	Busy : "0" Ready : "1"
I/O$_6$	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O$_7$	Write Protect	Write Protect	Write Protect	N/A	Write Protect	Protected : "0" Not Protected : "1"

Notes:

1. I/O0: This bit is only valid for Program and Erase operations. During Cache Program operations, this bit is only valid when I/O5 is set to one.
2. I/O1: This bit is only valid for cache program operations. This bit is not valid until after the second 15h command or the 10h command has been transferred in a Cache program sequence. When Cache program is not supported, this bit is not used.
3. I/O5: If set to one, then there is no array operation in progress. If cleared to zero, then there is a command being processed (I/O6 is cleared to zero) or an array operation in progress. When overlapped interleaved operations or cache commands are not supported, this bit is not used.
4. I/O6: If set to one, then the device or interleaved address is ready for another command and all other bits in the status value are valid. If cleared to zero, then the command issued is not yet complete and Status Register bits<5:0> are invalid value. When cache operations are in use, then this bit indicates whether another command can be accepted, and I/O5 indicates whether the operation is complete.

13.8 Cache Read (available only within a block)

The Cache read function permits a page to be read from the page register while another page is simultaneously read from the Flash array. A Read Page command, shall be issued prior to the initial sequential or random Read Cache command in a read cache sequence. The Cache read function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Read Cache function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Cache read function. Issuing an additional Cache read function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command.

The host may begin to read data from the page register when SR[6]is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array.

The host shall not issue a sequential Cache read (31h) command after the page of the device is read.

13.9 Cache Program (available only within a block)

Cache Program is used to improve the program throughput by programing data using the cache register. The cache program operation can only be used within one block. The cache register allows new data to be input while the previous data that was transferred to the page buffer is programmed into the memory array. Cache program is available only within a block. After the serial data input command (80h) is loaded to the command register, followed by 4 cycles of address, a full or partial page of data is latched into the cache register. Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state For a short time (tCBSYW). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence (80h-15h). The Busy time following the first sequence 80h - 15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is consequently processed through a pipeline model. In case of any subsequent sequence 80h - 15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete: till this moment the device will stay in a busy state (tCB-SYW). Read Status commands (70h) may be issued to check the status of the different registers, and the pass/ fail status of the cached program operations. More in detail: a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data. b) the status bit I/O<5> can be used to determine when the cell programming of the current data register contents is complete. c) the cache program error bit I/O<1> can be used to identify if the previous page (page N-1) has been successfully programmed or not in cache program operation. The latter can be polled upon I/O<6> status bit changing to "1". d) the error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while programming page N. The latter can be polled upon I/O<5> status bit changing to "1". I/O<1> may be read together with I/O<0>. If the system monitors the progress of the operation only with R/B#, the page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the programming is finished before starting any other operation.

More in detail:

a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data.
b) the status bit I/O<5> can be used to determine when the cell programming of the current data register contents is complete.
c) the Cache Program error bit I/O<1> can be used to identify if the previous page(page N-1) has been successfully programmed or not in Cache Program operation. The latter can be polled upon I/O<6> status bit changing to "1" .
d) the error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while programming page N. The latter can be polled upon I/O<5> status bit changing to "1". I/O<1> may be read together with I/O<0>. If the system monitors the progress of the operation only with R/B#, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation. See “table5. Status Register Coding".

13.10 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.

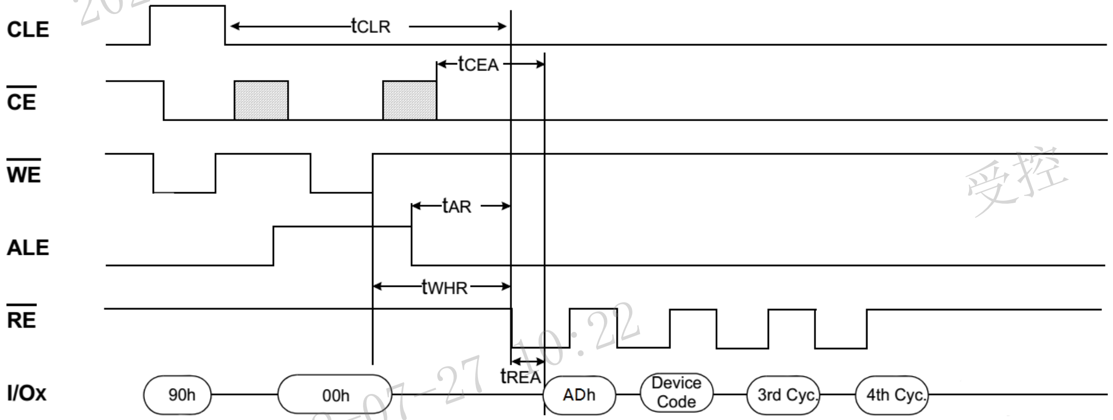


Figure 13-1 Read ID Sequence

[Table 38] 00h Address ID cycle

Part Number	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle
F70ME0101D-R6WA	ADh	A1h	80h	15h
F70ME0101D-RDWA	ADh	A1h	80h	15h

[Table 39] 3rd ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell					0 0 1 1	0 1 0 1		
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 1 1	0 1 0 1				
Interleave Program Between multiple chips	Not Support Support		0 1						
Cache Program	Not Support Support	0 1							

[Table 40] **4th ID Data**

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area)	1KB 2KB 4KB 8KB							0 0 1 1	0 1 0 1
Block Size (w/o redundant area)	64KB 128KB 256KB 512KB			0 0 1 1	0 1 0 1				
Redundant Area Size (byte/512byte)	8 16						0 1		
Organization	x8 x16		0 1						
Serial Access Minimum	45ns 25ns Reserved Reserved	0 0 1 1				0 1 0 1			

13.11 Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values.

13.12 Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timings and other behavioral parameters. This data structure enables the host processor to automatically recognize the Nand Flash configuration of a device. The whole data structure is repeated at least three times.

The Random Data Read command can be issued during execution of the read parameter page to read specific portions of the parameter page.

The Read Status command may be used to check the status of read parameter page during execution. After completion of the Read Status command, 00h is issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.

Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

[Table 41] Parameter Page Data Structure Definition

Byte	O/M	Description
	Revision information and features block	
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache command 0 1 = supports Page Cache Program command
10-31		Reserved (0)
	Manufacturer information block	
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64	M	JEDEC manufacturer ID
65-66	O	Date code
67-79		Reserved (0)
	Memory organization block	

80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89	M	Number of data bytes per partial page
90-91	M	Number of spare bytes per partial page
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	M	Number of logical units (LUNs)
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles
102	M	Number of bits per cell
103-104	M	Bad blocks maximum per LUN
105-106	M	Block endurance
107	M	Guaranteed valid blocks at beginning of target
108-109	M	Block endurance for guaranteed valid blocks
110	M	Number of programs per page
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints
112	M	Number of bits ECC correctability
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support
115-127		Reserved (0)
	Electrical parameters block	
128	M	I/O pin capacitance
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1
131-132	O	Program cache timing mode support

		6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0
133-134	M	tPROG Maximum page program time (µs)
135-136	M	tBERS Maximum block erase time (µs)
137-138	M	tR Maximum page read time (µs)
139-163		Reserved (0)
	Vendor block	
164-165	M	Vendor specific Revision number
166-253		Vendor specific
254-255	M	Integrity CRC
	Redundant Parameter Pages	
256-511	M	Value of bytes 0-255
512-767	M	Value of bytes 0-255
768+	O	Additional redundant parameter pages

Notes:

“O” Stands for Optional, “M” for Mandatory

14. Electrical Characteristic

14.1 Valid Block

[Table 42] The Number of Valid Block

Part Number	Symbol	Min	Typ.	Max	Unit
F70ME0101D-R6WA	NVB	1,004	-	1,024	Blocks
F70ME0101D-RDWA	NVB	1,004	-	1,024	Blocks

Notes:

1. The 1st block is guaranteed to be a valid block at the time of shipment.
2. Invalid blocks are one that contains one or more bad bits. The device may contain bad blocks upon shipment.

14.2 Recommended Operating Conditions

[Table 43] Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Power Supply Voltage	VCC	1.7	1.8	1.95	V
Ground Supply Voltage	VSS	0	0	0	V

14.3 Absolute Maximum DC Ratings

[Table 44] Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to VSS	VCC	-0.6 to + 2.6	V
	VIN	-0.6 to + 2.6	
	VI/O	-0.6 to +2.6	
Ambient Operating Temperature	TA	-40 to +85	℃

Notes:

1.Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -1.0V for periods <30ns.

2.Maximum DC voltage on input/output pins is VCC+0.3V which, during transitions, may overshoot to VCC+1.0V for periods <20ns.

3.tablePermanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this datasheet.

4.Exposure to absolute maximum rating conditions for extended periods may affect reliability.

14.4 DC Operating Characteristics

[Table 45] DC & Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power on reset current	ICC0	FFh command input after power on			50 per device	mA
Page Read Access Operation Current	ICC1	tRC=45ns CE#=VIL, IOUT=0mA	-	15	30	mA
Program Operation Current	ICC2	Normal	-	15	30	
		Cache		15	30	
Erase Operation Current	ICC3	-		15	30	
Stand-by Current (TTL)	ICC4	CE#=VIH, WP#=0V/VCC	-	-	1	
Stand-by Current (CMOS)	ICC5	CE#=VCC-0.2, WP#=0V/VCC	-	10	50	µA
Input Leakage Current	ILI	VIN=0 to VCC(max)	-	-	±10	
Output Leakage Current	ILO	VOUT=0 to VCC(max)	-	-	±10	
Input High Voltage	VIH	-	0.8xVCC	-	VCC+0.3	V
Input Low Voltage, All inputs	VIL	-	-0.3	-	0.2xVCC	
Output High Voltage Level	VOH	IOH=-100µA	VCC-0.1	-	-	
Output Low Voltage Level	VOL	IOL=100µA	-	-	0.1	
Output Low Current (R/B#)	IOL(R/B#)	VOL=0.1V	3	4	-	mA

14.5 Input / Output Capacitance (TA=25℃, VCC=1.8V, f=1.0Mhz)

[Table 46] Input / Output Capacitance

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

Notes:

Capacitance is periodically sampled and not 100% tested.

14.6 Read / Program / Erase Characteristics

[Table 47] NAND Read / Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data Transfer from Cell to Register	tR	-		25	μs
Read Cache busy time	tCBSYR	-	3	tR	μs
Program Time	tPROG	-	300	700	μs
Cache Program short busy time	tCBSYW	-	5	tPROG	μs
Number of Partial Program Cycles	Nop	-	-	4	cycles
Block Erase Time	tBERS	-	3	10	ms

Notes :

1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

2.Typical value is measured at Vcc=1.8 V, TA=25℃ (1.8V Device).Not 100% tested.

14.7 AC Timing Parameters Table

[Table 48] AC Timing Characteristics

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS1)	25	-	ns
CLE Hold Time	tCLH	10	-	ns
CE# Setup Time	tCS1)	35	-	ns
CE# Hold Time	tCH	10	-	ns
WE# Pulse Width	tWP	25	-	ns
ALE Setup Time	tALS1)	25	-	ns
ALE Hold Time	tALH	10	-	ns
Data Setup Time	tDS1)	20	-	ns
Data Hold Time	tDH	10	-	ns
Write Cycle Time	tWC	45	-	ns
WE# High Hold Time	tWH	15	-	ns
Address to Data Loading Time	tADL2)	100	-	ns
ALE toRE# Delay	tAR	10	-	ns
CLE to RE# Delay	tCLR	10	-	ns
Ready to RE# Low	tRR	20	-	ns
RE# Pulse Width	tRP	25	-	ns
WE# High to Busy	tWB	-	100	ns
Read Cycle Time	tRC	45	-	ns
RE# Access Time	tREA	-	30	ns
RE# High to Output Hi-Z	tRHZ	-	100	ns
CE# High to Output Hi-Z	tCHZ	-	50	ns
CE# High to ALE or CLE Don't Care	tCSD	10	-	ns
RE# High to Output Hold	tRHOH	15	-	ns
RE# Low to Output Hold	tRLOH	0		ns
Data Hold Time after CE# Disable	tCOH	15	-	ns
RE# High Hold Time	tREH	15	-	ns
Output Hi-Z to RE# Low	tIR	0	-	ns
RE# High to WE# Low	tRHW	100	-	ns
WE# High to RE# Low	tWHR	60	-	ns
WE# high to RE# low for Random data out	tWHR2	200		ns
CE# low to RE# low	tCR	10		
Device Resetting Time (Read/Program/Erase)	tRST	-	5/10/500 1)	μs
Write protection time	tWW	100		

NOTE :

1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

2. In case of first reset after initial powering up, it takes max 5ms.

15. NAND FLASH TECHNICAL NOTES

15.1 Initial Invalid Block(s)

The initial invalid blocks are included in the device while it gets shipped called. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. During the time of using the device, the additional invalid blocks might be increasing; therefore, it is recommended to check the invalid block marks and avoid using the invalid blocks. Furthermore, please read out the initial invalid block and the increased invalid block information before any erase operation since it may be cleared by any erase operation.

15.2 Identifying Initial Invalid Block(s)

While the device is shipped, the value of all data bytes of the good blocks are FFh. The initial invalid block(s) status is defined by the 1st byte in the spare area. Longsys makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048. Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the following suggested flow chart. The erase operation at the invalid block is not recommended.

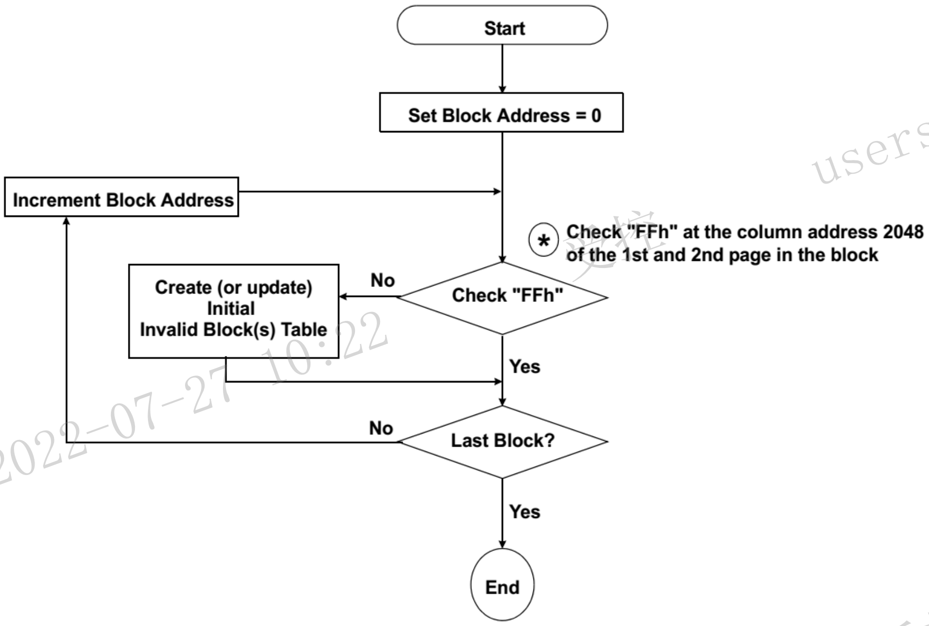


Figure 15-1 Flow Chart to Create Initial Invalid Block Table

Notes:

1. Do not try to erase the detected blocks, because the bock information will be lost.
2. Do not perform program and erase operation in invalid block, it is impossible to guarantee the Input data and to ensure that the function is normal.

15.3 Error in Write or Read Operation

The device may fail during a Read, Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system.Block replacement should be done while status read failure after erase or program. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

[Table 49]Failure Cases

	Failure Mode	Detection and Countermeasure Sequence
Write	Erase Failure	Read Status after Erase --> Block Replacement
	Program Failure	Read Status after Program --> Block Replacement
Read	Single bit Failure	Verify ECC -> ECC Correction

ECC:

Error Correcting Code --> Hamming Code etc.

Example) 1bit correction & 2bit detection

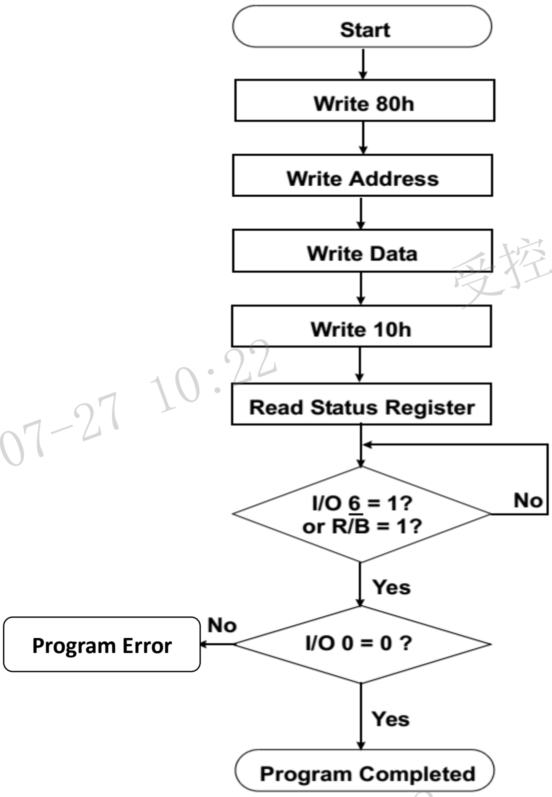
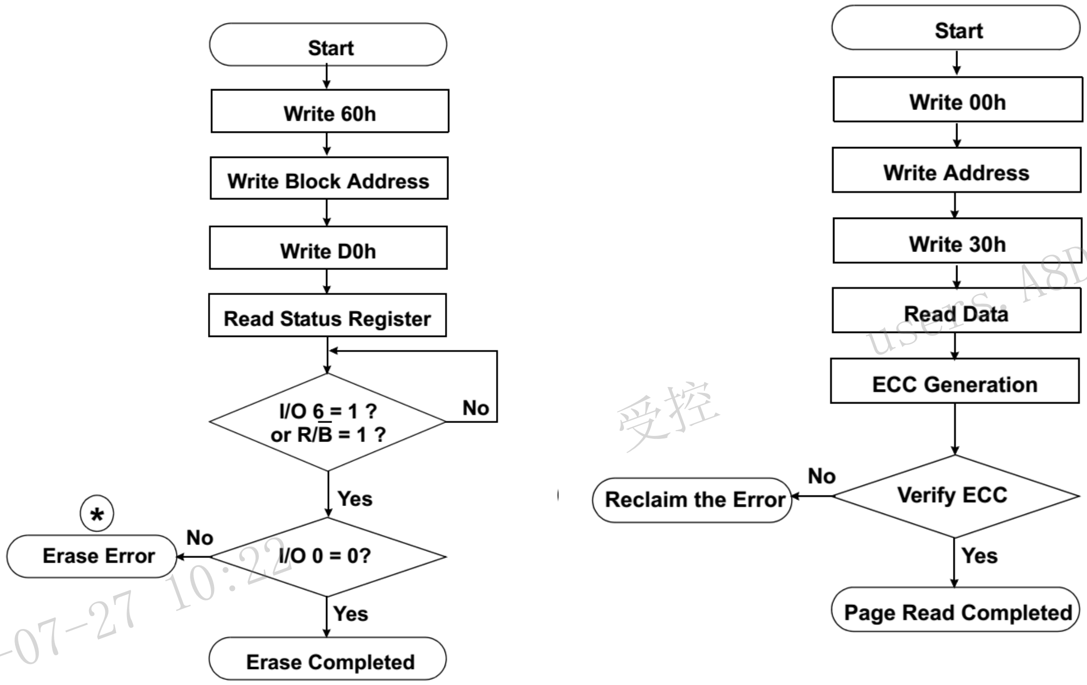


Figure 15-2 Program Flow Chart

If program operation results in an error, map out the block including the page in error and copy the target data to another block.



*If erase operation results in an error, map out the failing block and replace it with another block.

Figure 15-3 Erase Flow Chart& Read Flow Chart

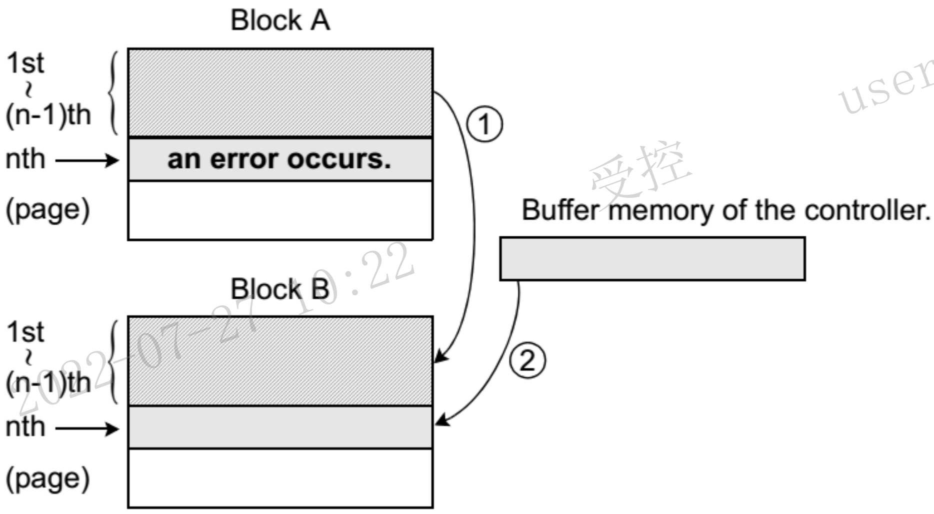


Figure 15-4 Block Replacement

Notes:

1.When an error happens in the nth page of the Block ‘A’ during erase or program operation.

2.Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block’B’)

3. Then, copy the nth page data of the Block ’A’ in the buffer memory to the nth page of the Block’B’.

4. Do not erase or program to Block ‘A’ by creating an ‘invalid block’ table or other appropriate scheme.

16. Nand Flash Timing

16.1 Data Protection & Power Up Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 1.1V(1.8V device). WP# pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 1ms is required before internal circuit gets ready for any command sequences. The two step command sequence for program/erase provides additional software protection.

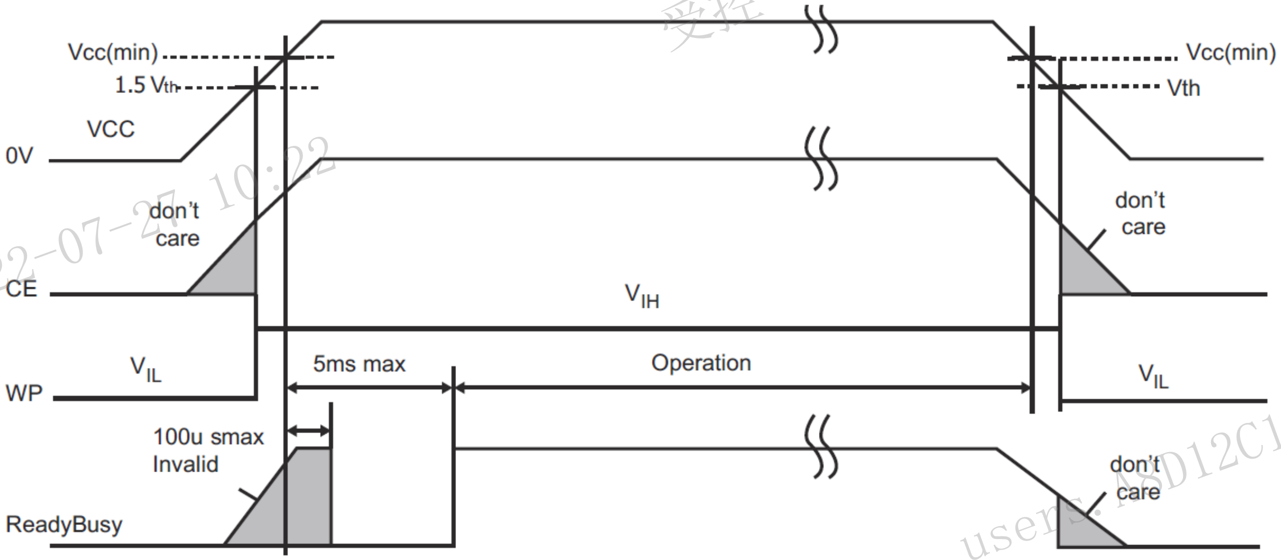


Figure 16-1 AC Waveforms for Power Transition

NOTE :

1. During the initialization, the device consumes a maximum current of 30mA (ICC1).
2. Once Vcc drops under 1.5V, Vcc is recommended that it should be driven down to 0.5V and stay low under 0.5V for at least 1ms before Vcc power up.

16.2 Mode Selection

[Table 50]Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input(4cycles)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input(4cycles)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X$^{1)}$	X	X	X	L	Write Protect	
X	X	H	X	X	0V/VCC$^{2)}$	Stand-by	

Notes:

1. X can be VIL or VIH.
2. WP should be biased to CMOS high or CMOS low for standby.

16.3 Command Latch Cycle

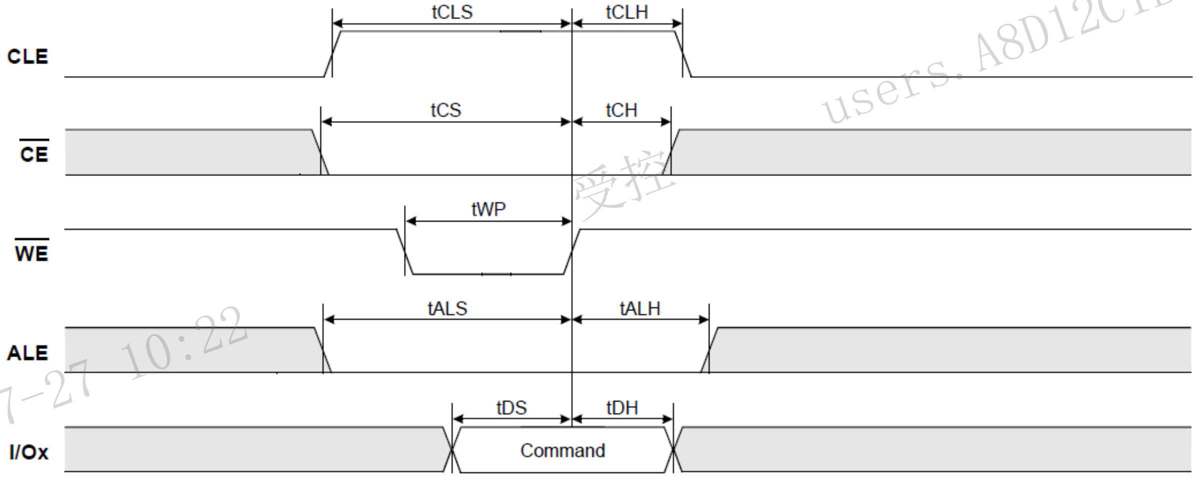


Figure 16-2 Command Latch Cycle

16.4 Address Latch Cycle

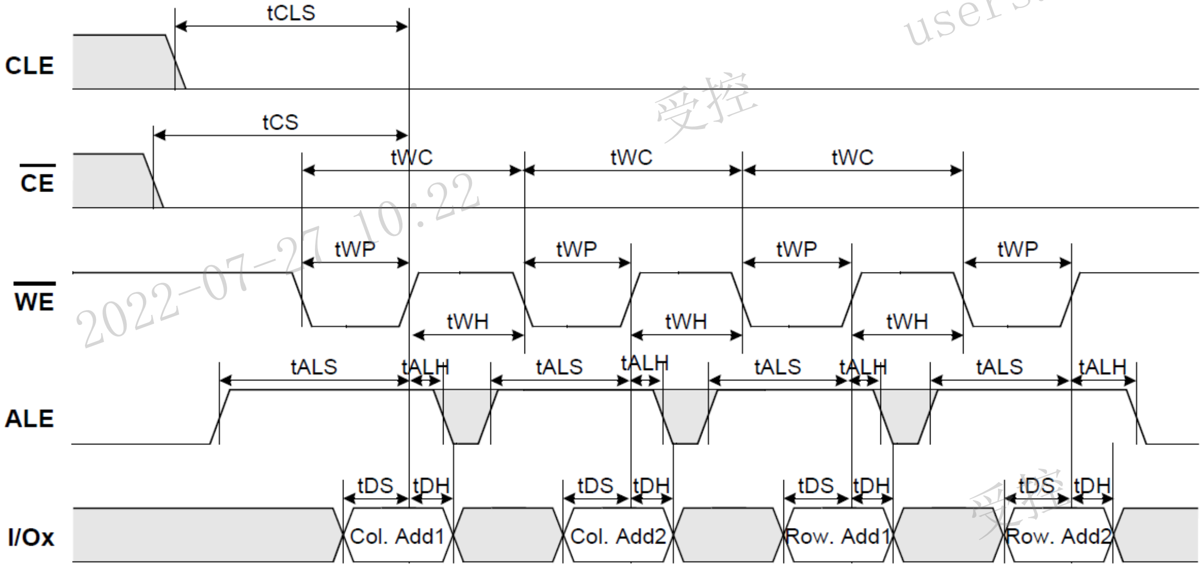


Figure 16-3 Address Latch Cycle

Notes:

All command except Reset, Read Status is issued to command register on the rising edge of /WE, when CLE is high,CE# and ALE is low, and device is not busy state.

16.5 Input Data Latch Cycle

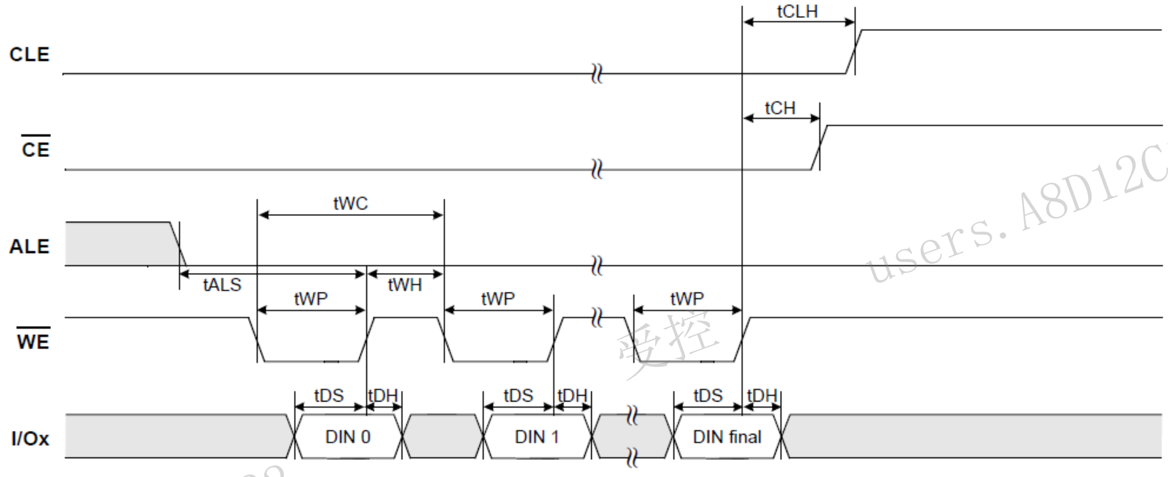


Figure 16-4 Input Data Latch Cycle

Notes:

Data Input cycle is accepted to data register on the rising edge of WE#, when CLE and CE# and ALE are low, and device is not Busy state.

16.6 Data Output Cycle Timings (CLE=L, WE#=H, ALE=L)

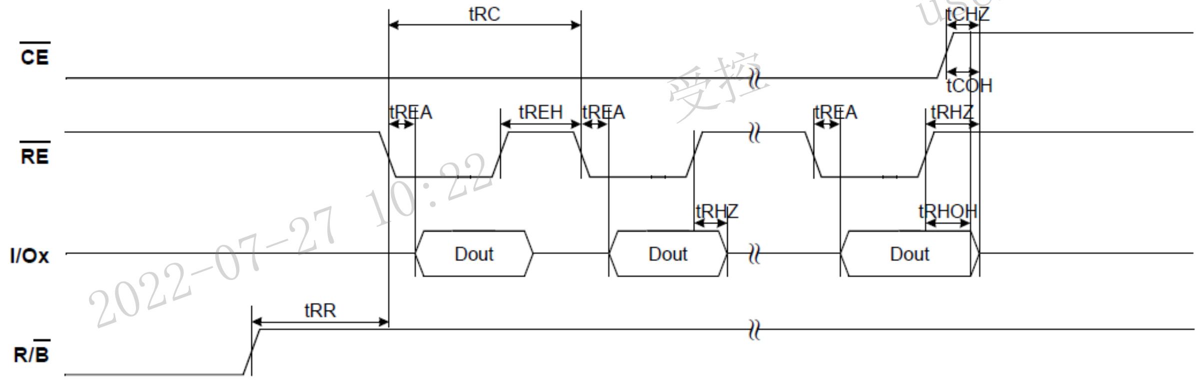


Figure 16-5 Serial Access Cycle after Read (CLE=L, WE#=H, ALE=L)

Notes :

1. Transition is measured at 200mV from steady state voltage with load. This parameter is sampled and not 100% tested.
2. tRHOH starts to be valid when frequency is lower than 33Mhz.

17. Package Information

Unit :mm

162 Ball FBGA, 8mm x 10.5mmx1.0mm

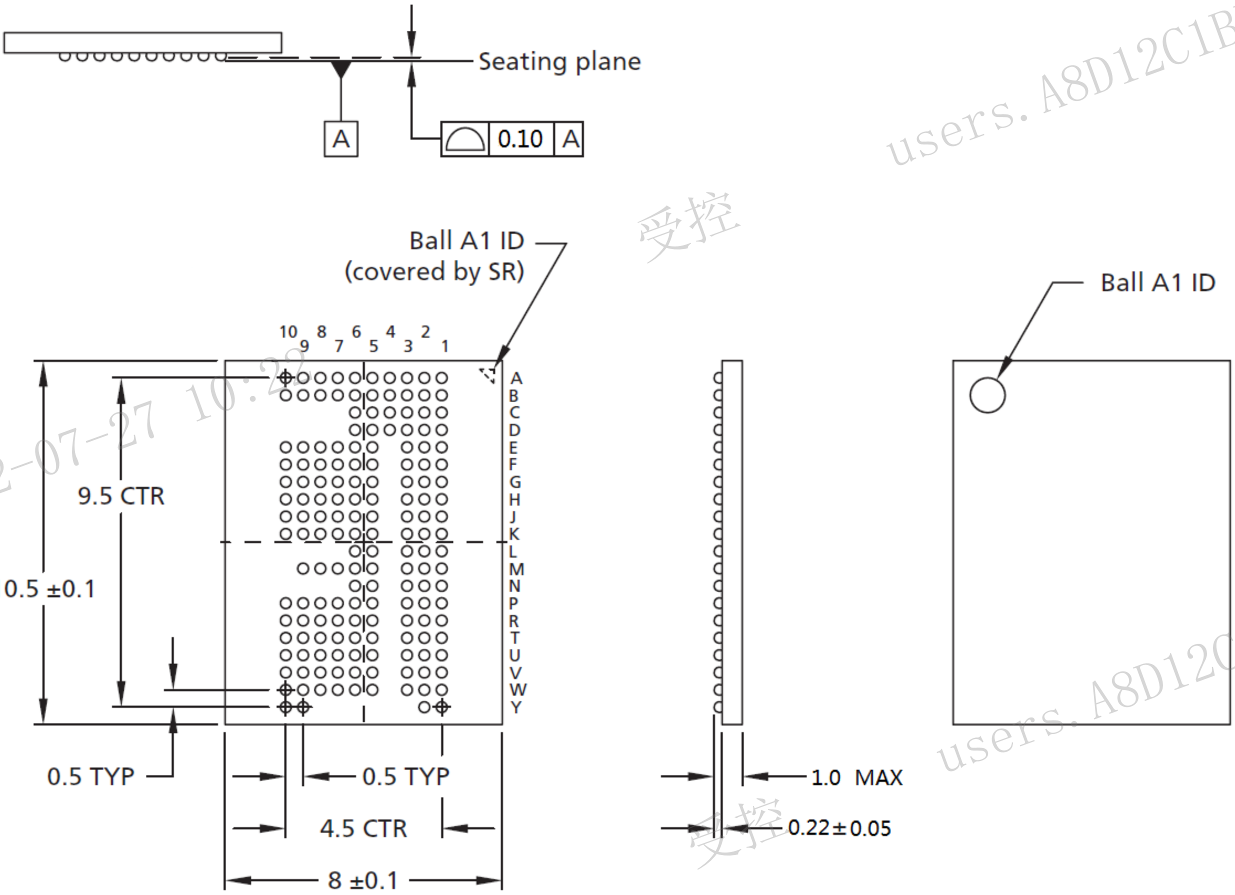


Figure 17-1 162 Ball Grid Array (BGA)