

HEXFET® Power MOSFET for DC-DC Converters

- N-Channel Application-Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- Low Switching Losses

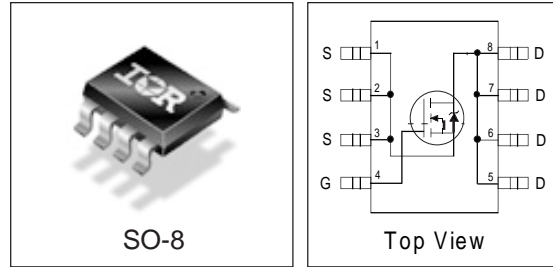
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Description

This new device employs advanced HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make it ideal for high efficiency DC-DC converters that power the latest generation of microprocessors.

The IRF7811W has been optimized for all parameters that are critical in synchronous buck converters including $R_{DS(on)}$, gate charge and Cdv/dt -induced turn-on immunity. The IRF7811W offers particularly low $R_{DS(on)}$ and high Cdv/dt immunity for synchronous FET applications.

The package is designed for vapor phase, infra-red, convection, or wave soldering techniques. Power dissipation of greater than 3W is possible in a typical PCB mount application.



DEVICE CHARACTERISTICS

IRF7811W	
$R_{DS(on)}$	9.0mΩ
Q_G	18nC
Q_{sw}	5.5nC
Q_{oss}	12nC

Absolute Maximum Ratings

Parameter	Symbol	IRF7811W	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±12	
Continuous Drain or Source Current ($V_{GS} \geq 4.5V$)	$T_A = 25^\circ C$	14	A
	$T_L = 90^\circ C$	13	
Pulsed Drain Current①	I_{DM}	109	
Power Dissipation	$T_A = 25^\circ C$	3.1	W
	$T_L = 90^\circ C$	3.0	
Junction & Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C
Continuous Source Current (Body Diode)	I_S	3.8	A
Pulsed Source Current①	I_{SM}	109	

Thermal Resistance

Parameter		Max.	Units
Maximum Junction-to-Ambient③	$R_{\theta JA}$	40	°C/W
Maximum Junction-to-Lead	$R_{\theta JL}$	20	°C/W

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Electrical Characteristics

Parameter		Min	Typ	Max	Units	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	$V_{GS} = 0V, I_D = 250\mu A$
Static Drain-Source on Resistance	$R_{DS(on)}$		9.0	12	$m\Omega$	$V_{GS} = 4.5V, I_D = 15A$ ②
Gate Threshold Voltage	$V_{GS(th)}$	1.0			V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Drain-Source Leakage Current	I_{DSS}			30	μA	$V_{DS} = 24V, V_{GS} = 0$
				150		$V_{DS} = 24V, V_{GS} = 0,$ $T_j = 100^\circ C$
Gate-Source Leakage Current	I_{GSS}			± 100	nA	$V_{GS} = \pm 12V$
Total Gate Chg Cont FET	Q_G		18	24	nC	$V_{GS}=5.0V, I_D=15A, V_{DS}=16V$
Total Gate Chg Sync FET	Q_G		15.6			$V_{GS} = 5V, V_{DS} < 100mV$
Pre-Vth Gate-Source Charge	Q_{GS1}		6.0			$V_{DS} = 16V, I_D = 15A$
Post-Vth Gate-Source Charge	Q_{GS2}		1.4			
Gate to Drain Charge	Q_{GD}		4.1			
Switch Chg($Q_{GS2} + Q_{gd}$)	Q_{sw}		5.5			
Output Charge	Q_{OSS}		12			$V_{DS} = 16V, V_{GS} = 0$
Gate Resistance	R_G		2.0		Ω	
Turn-on Delay Time	$t_{d(on)}$		11		ns	$V_{DD} = 16V, I_D = 15A$ $V_{GS} = 5.0V$ Clamped Inductive Load
Rise Time	t_r		11			
Turn-off Delay Time	$t_{d(off)}$		29			
Fall Time	t_f		9.9			
Input Capacitance	C_{iss}	-	2335	-	pF	$V_{DS} = 16V, V_{GS} = 0$
Output Capacitance	C_{oss}	-	400	-		
Reverse Transfer Capacitance	C_{rss}	-	119	-		

Source-Drain Rating & Characteristics

Parameter		Min	Typ	Max	Units	Conditions
Diode Forward Voltage*	V_{SD}			1.25	V	$I_S = 15A$ ②, $V_{GS} = 0V$
Reverse Recovery Charge④	Q_{rr}		45		nC	$di/dt \sim 700A/\mu s$ $V_{DS} = 16V, V_{GS} = 0V, I_S = 15A$
Reverse Recovery Charge (with Parallel Schottky)④	$Q_{rr(s)}$		41		nC	$di/dt = 700A/\mu s$ (with 10BQ040) $V_{DS} = 16V, V_{GS} = 0V, I_S = 15A$

- Notes:**
- ① Repetitive rating; pulse width limited by max. junction temperature.
 - ② Pulse width $\leq 400 \mu s$; duty cycle $\leq 2\%$.
 - ③ When mounted on 1 inch square copper board
 - ④ Typ = measured - Q_{oss}
 - ⑤ Typical values of $R_{DS(on)}$ measured at $V_{GS} = 4.5V, Q_G, Q_{sw}$ and Q_{OSS} measured at $V_{GS} = 5.0V, I_F = 15A$.

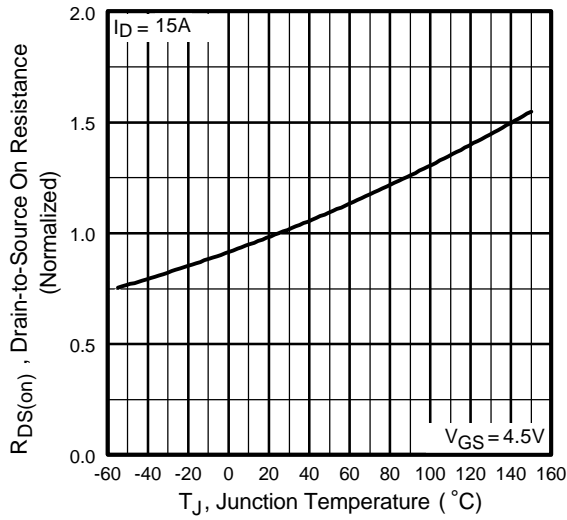


Fig 1. Normalized On-Resistance Vs. Temperature

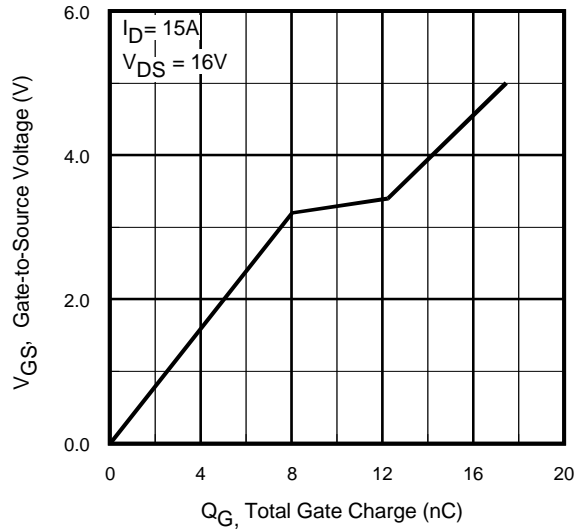


Fig 2. Typical Gate Charge Vs. Gate-to-Source Voltage

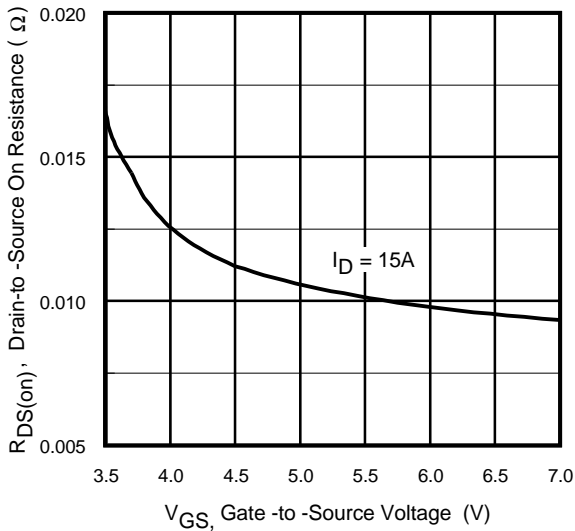


Fig 3. On-Resistance Vs. Gate Voltage

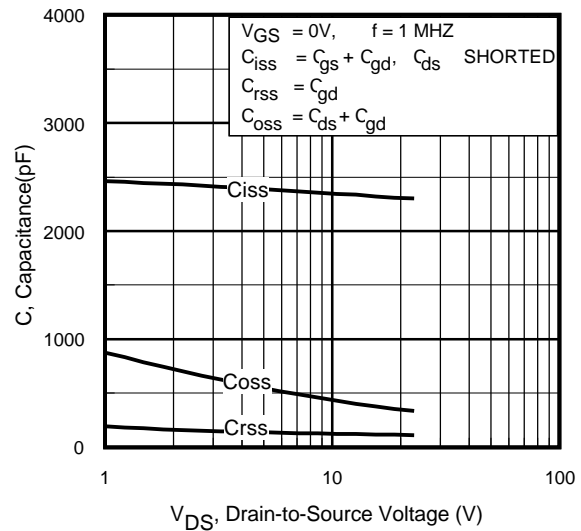


Fig 4. Typical Capacitance Vs. Drain-to-Source Voltage

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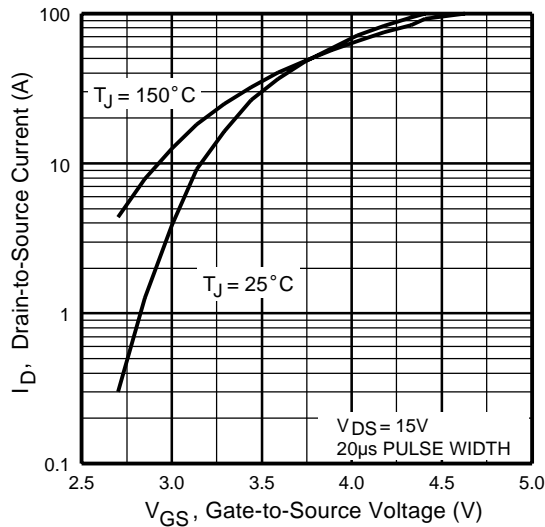


Fig 5. Typical Transfer Characteristics

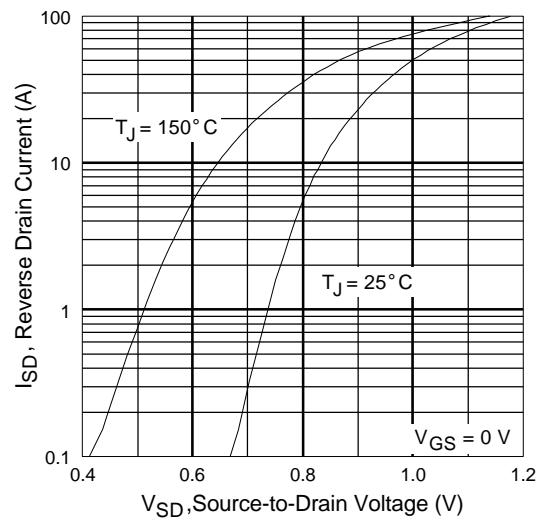


Fig 6. Typical Source-Drain Diode Forward Voltage

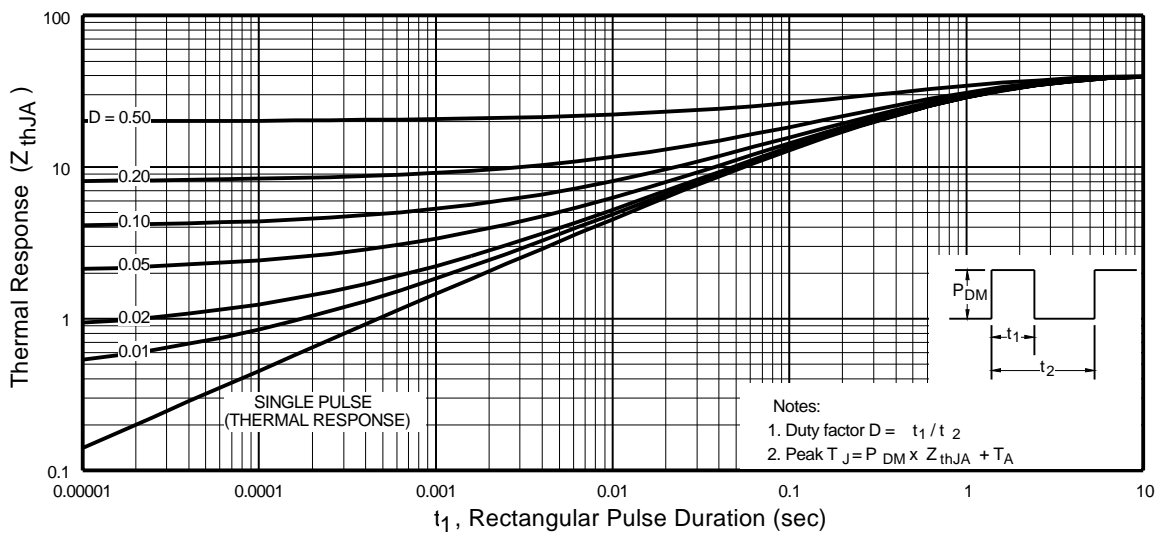
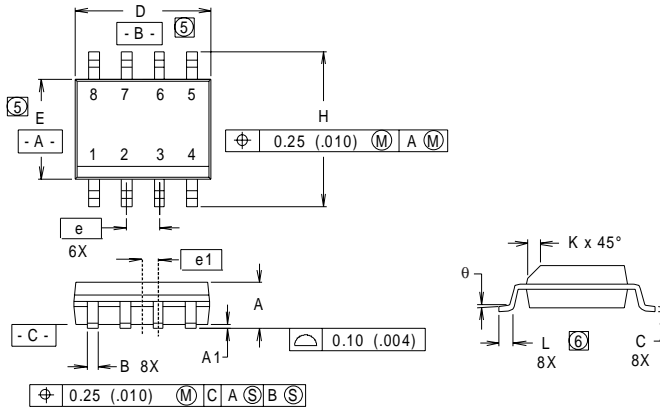


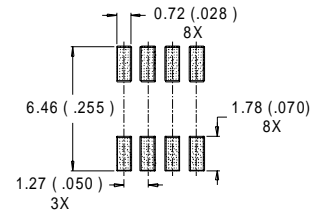
Figure 7. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

SO-8 Package Details



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	0.16	.050	0.41	1.27
θ	0°	8°	0°	8°

RECOMMENDED FOOTPRINT

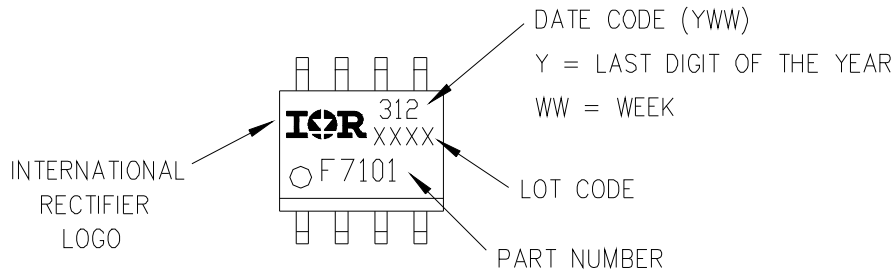


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- 5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS
MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.006).
- 6 DIMENSIONS IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE..

SO-8 Part Marking

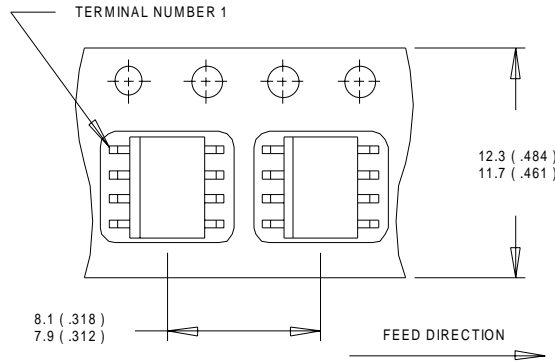
EXAMPLE: THIS IS AN IRF7101



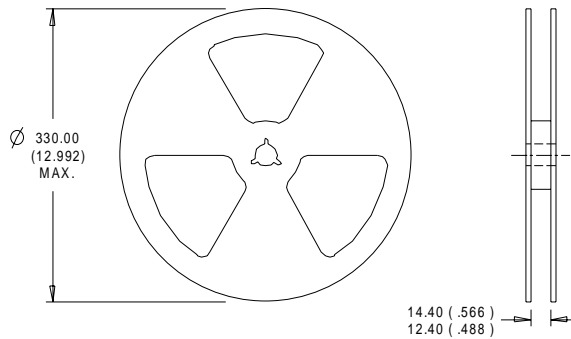
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SO-8 Tape and Reel



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
This product has been designed and qualified for the consumer market.
Qualification Standards can be found on IR's Web site.

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