FAIRCHILD SEMICONDUCTOR®

FAN104W
High-Frequency Primary-Side-Regulation PWM Controller

Features

- Achieves <30 mW; Energy Star's 5-Star Level
- Proprietary 500 V High-Voltage JFET Startup Reduces Startup Resistor Loss
- Low Operation Current in Burst Mode: 600 µA
- Constant-Voltage (CV) and Constant-Current (CC) Control without Secondary-Feedback Circuitry
- Green Mode: PWM Frequency Linearly-Decreasing
- PWM Frequency at 85 kHz with Frequency Hopping to Solve EMI Problem
- Boundary-Conduction-Mode (BCM) Operation at Lower AC Input Voltage
- Cable Compensation in CV Mode
- Cycle-by-Cycle Current Limiting
- Gate Output Maximum Voltage Clamped at 14 V
- V_{DD} Under-Voltage Lockout (UVLO) Available
- Built-in Protections:
  - Output Short-Circuit Protection
  - Output Over-Voltage-Protection (VSOVP) with Latch Mode
  - V_{DD} Over-Voltage-Protection (V_{DD} OVP)
  - CS Pin Single-Fault Protection
  - VS Pin single-Fault Protection
  - Over-Temperature-Protection (OTP) with Latch Mode
- SOIC Package

Description

This highly integrated PWM controller, FAN104W, provides several features to enhance the performance of low-power flyback converters. The proprietary topology of FAN104W enables simplified circuit design for battery charger applications. The result is a lower-cost, smaller, and lighter charger compared to a conventional design or a linear transformer.

To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to linearly decrease PWM frequency under light-load conditions. Green Mode assists the power supply in meeting power conservation requirements.

By using FAN104W, a charger can be implemented with few external components and minimized cost. An output CV/CC characteristic envelope is shown in Figure 1.

Applications

- Battery chargers for smart phones, Pad, PDA, digital cameras.
- Best choice to replace linear transformer and RCC SMPS

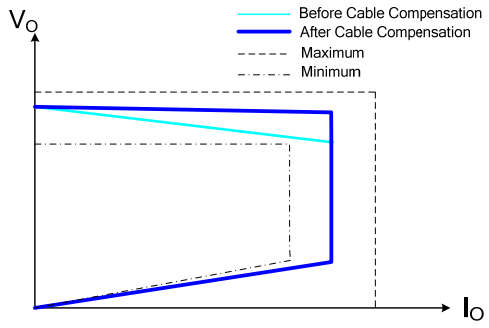


Figure 1. Typical Output V-I Characteristic

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN104WMX	-40°C to +105°C	8-Lead, Small Outline Integrated Circuit (SOIC), JEDEC MS-012, .150-Inch Narrow Body	Tape & Reel

Application Diagram

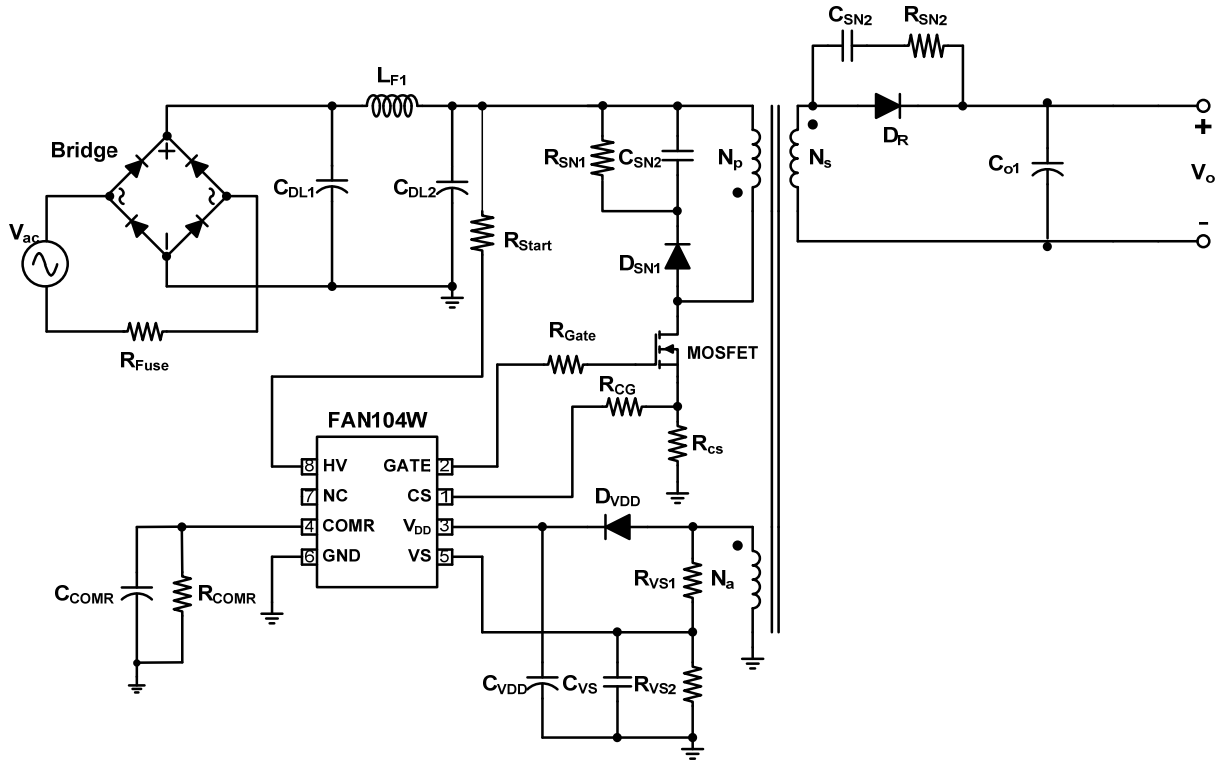


Figure 2. Typical Application

Internal Block Diagram

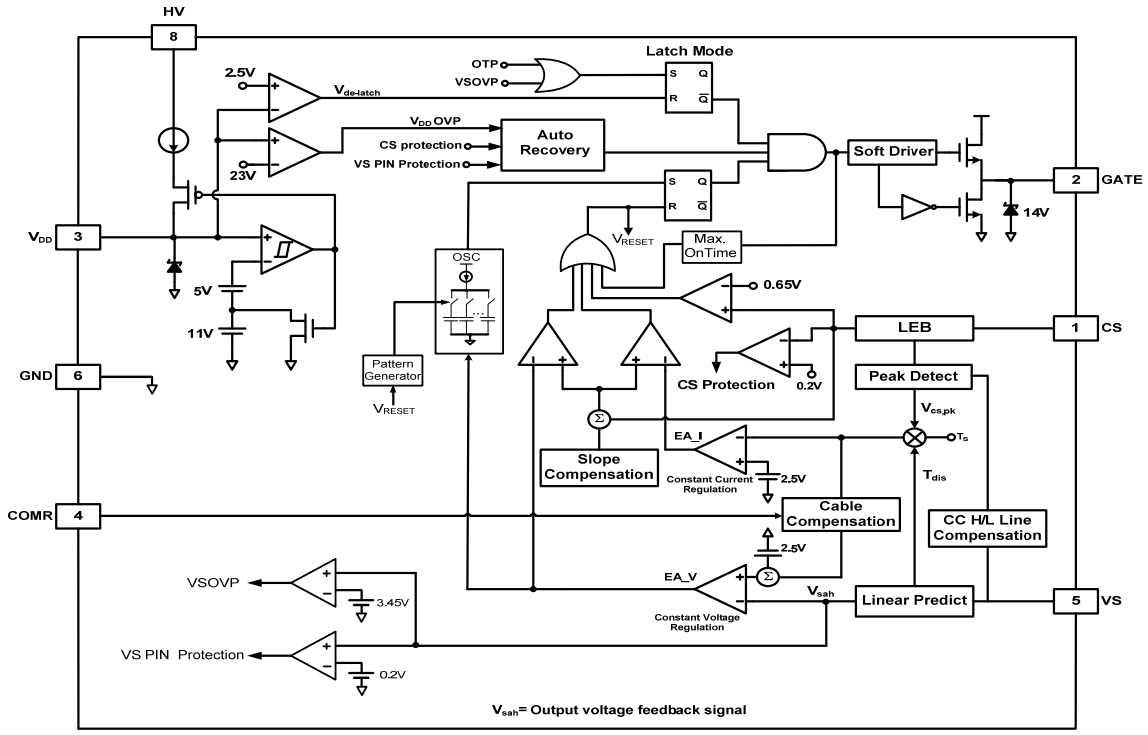
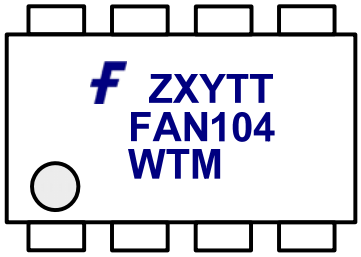


Figure 3. Functional Block Diagram

Marking Information



F: Fairchild Logo
Z: Plant Code
X: 1-Digit Year Code
Y: 1-Digit Week Code
TT: 2-Digit Die Run Code
T: Package Type (M=SOP)
M: Manufacture Flow Code

Figure 4. Top Mark

Pin Configuration

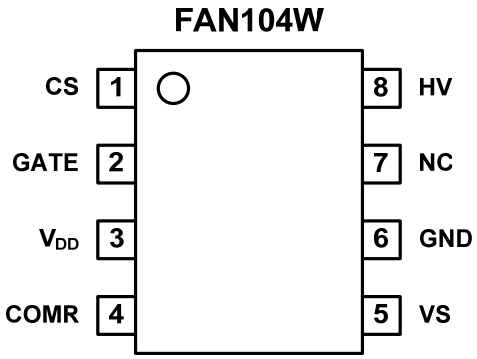


Figure 5. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	CS	**Current Sense**. This pin connects a current sense resistor to detect the MOSFET current for peak-current-mode control in Constant Voltage (CV) regulation and provides the output-current regulation in constant current regulation.
2	GATE	**PWM Signal Output**. This pin uses the internal totem-pole output driver to drive the power MOSFET.
3	V_{DD}	**Power Supply**. IC operating current and MOSFET driving current are supplied using this pin. This pin is connected to an external V_{DD} capacitor. The threshold voltages for startup and turn-off are 16 V and 5 V, respectively. The operating current is lower than 3.5 mA.
4	COMR	**Cable Compensation**. Connect a capacitance and resistor between this pin and the GND pin for compensation voltage drop due to output cable loss in CV regulation.
5	VS	**Voltage Sense**. This pin detects the output voltage information and discharge time for Constant Voltage (CV) and Constant Current (CC) regulation. This pin connects a divider resistor from the transformer of auxiliary winding.
6	GND	Ground
7	NC	No Connect
8	HV	**High Voltage**. This pin connects to bulk capacitor for high-voltage startup.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{HV}	HV Pin Input Voltage			500	V
V_{VDD}	DC Supply Voltage[1,2]			30	V
V_{VS}	VS Pin Input Voltage		-0.3	7.0	V
V_{CS}	CS Pin Input Voltage		-0.3	7.0	V
V_{COMR}	Voltage Error Amplifier Output Voltage		-0.3	7.0	V
V_{HV}	HV Pin Input Voltage			500	V
P_D	Power Dissipation ($T_A < 50°C$)			660	mW
$R_{\Theta JA}$	Thermal Resistance (Junction-to-Air)			127	°C/W
$R_{\Theta JC}$	Thermal Resistance (Junction-to-Case)			27	°C/W
T_J	Operating Junction Temperature			150	°C
T_{STG}	Storage Temperature Range		-55	150	°C
T_L	Lead Temperature (Soldering 10 Seconds)			260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JEDEC:JESD22_A114 (Except HV Pin)[3]		6	kV
		Charged Device Model, JEDEC:JESD22_C101 (Except HV Pin)[3]		2	

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to GND pin.
3. ESD ratings including HV pin: HBM=1 kV, CDM=1.25 kV.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	105	°C

Electrical Characteristics

V_{DD}=15V, T_A=25°C, unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
V_{DD}							
V_{OP}	Continuously Operating Voltage[4]				21		V
V_{DD-ON}	Turn-On Threshold Voltage			15	16	17	V
V_{DD-OFF}	Turn-Off Threshold Voltage			4.5	5.0	5.5	V
$V_{DD-HV-ON}$	HV JFET Turn-On Threshold Voltage[4]				4.2		V
$V_{DD-DELATCH}$	De-latch Threshold Voltage[4]				2.5		V
I_{DD-OP}	Operating Current		V_{DD}=15 V, V_{CS}=4 V, V_{VS}=2.6 V, V_{COMR}=4 V	2.5	3.5	4.5	mA
I_{DD-ST}	Startup Current		V_{DD}=V_{DD-ON} – 0.16 V			100	µA
$I_{DD-GREEN}$	Green-Mode Operating Current		V_{DD}=8.5 V, V_{CS}=4 V, V_{VS}=2.5 V, V_{COMR}=0V	500	600	700	µA
V_{DD-OVP}	V_{DD} Over-Voltage-Protection Level		V_{DD}=0 V→V_{DD-OVP}, V_{CS}=0.25 V, V_{VS}=0.4 V, V_{COMR}=0 V	21.5	23.0	24.5	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage-Protection Debounce Time[4]		V_{DD} = 20 V→30 V, V_{CS}=0 V	50	100	150	µs
HV Section							
V_{HV-MIN}	Minimum Startup Voltage on HV Pin[4]					50	V
I_{HV}	Supply Current Drawn from HV Pin		V_{AC}=90 V (V_{DC}=100 V)	1	3	5	mA
I_{HV-LC}	Leakage Current after Startup		HV=500 V, V_{DD}→V_{DD-ON}→V_{DD-OFF} +1V		1.25	3.00	µA
Oscillator Section							
f_{OSC}	Frequency	Center Frequency	V_{DD}=15 V, V_{CS}=4 V, V_{VS}=2.5 V, V_{COMR}=3.5 V	80	85	90	kHz
		Hopping Range		±2	±3	±4	
t_{FHR}	Frequency Hopping Period[4]			2	3	4	ms
$f_{OSC-N-MIN}$	Minimum Frequency at No-Load in Constant Voltage (CV) Mode		V_{DD}=15 V, V_{CS}=4 V, V_{VS}=2.5 V, V_{COMR}=0 V	1.1	1.2	1.3	kHz
$f_{OSC-CC-MIN}$	Minimum Frequency in Constant Current (CC) Mode[5]		V_{DD}=15 V, V_{CS}=4 V, V_{VS}=0 V, V_{COMR}=3.5 V	39	44	49	kHz
$f_{OSC-BCM}$	Minimum Frequency for Boundary Conduction Mode (BCM) Operation		V_{DD}=15 V, V_{CS}=0 V, V_{VS}=0 V, V_{COMR}=4 V	6	10	14	kHz
f_{DV}	Frequency Variation vs.V_{DD} Deviation[4]		V_{DD}=10 V or 25 V, V_{CS}=4 V, V_{VS}=2.5 V, V_{COMR}=3.5 V			2	%
f_{OSC-T}	Frequency Variation vs. Temperature Deviation[4]		V_{DD}=15 V, T_A=-40°C~125°C	-12		12	%

Continued on the following page…

Electrical Characteristics (Continued)

V_{DD}=15V, T_A=25°C, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Voltage-Sense						
I_{TC}	Bias Current	V_{CS}=4 V, V_{VS}=0 V, Measure I_{VS}	9	10	11	µA
I_{VS-UVP}	Brownout Protection Current(4)			250		µA
$V_{VS-CM-MIN}$	VS Threshold Voltage of ZCD Undetectable Protection(4)			0.55		V
$V_{VS-CM-MAX}$	VS Threshold Voltage of ZCD Undetectable Protection(4)			0.75		V
$t_{VS-BLANK}$	ZCD Blanking Time		1.10	1.45	1.80	µs
$V_{VS-OFFSET}$	ZCD Turn Off Threshold(4)			0.2		V
V_{VSOVP}	V_S Over-Voltage Protection		3.30	3.45	3.60	V
T_{VSOVP}	V_S Over-Voltage Protection Debounce Time(4)			3		Cycle
Current-Sense						
V_{STH}	Threshold Voltage for Current Limit	V_{COMR}=4 V, V_{VS}=0.9 V, CS Pin Input Ramp until Gate OFF	0.60	0.65	0.70	V
V_{STH-VA}	Threshold Voltage for Current Limit when ZCD Undetectable	V_{COMR}=4 V, V_{VS}=0 V, CS Pin Input Ramp Until Gate OFF	0.25	0.30	0.35	V
t_{LEB}	CS Leading Edge Blanking Time	V_{COMR}=4V		150		ns
Voltage-Error-Amplifier						
V_{VR}	Reference Voltage	V_{CS}=4 V, V_{DD}=16 V→26 V Measure V_{COMR}	2.475	2.500	2.525	V
V_{CCR}	Variation Test Voltage for CC Mode Regulation	V_{CS}=0.463 V, V_{VS}=4 V, V_{DD}=26 V→10 V, Measure V_{COMR}	2.380	2.430	2.480	V
V_{SN-CC}	VS Sampling Voltage to Start Frequency Decreasing in CC Mode	V_{CS}=4 V, f_{S1}=f_{OSC}-2 kHz, V_{COMR}=3.5 V, Adjust V_{VS}	2.2	2.3	2.4	V
V_{SG-CC}	VS Sampling Voltage to End Frequency Decreasing in CC Mode	V_{CS}=4 V, f_{S2}=f_{OSC}+2 kHz V_{COMR}=3.5 V, Adjust V_{VS}	0.4	0.8	1.1	V
S_{G-CC}	Frequency Decreasing Slope of CC Mode	S_{G-CC}=(f_{S1}-f_{S2}) / (V_{SN-CC}-V_{SG-CC})	16	28	46	KHz/V
V_{SN-CV}	Starting Voltage of Frequency Decreasing in CV Mode	V_{CS}=4 V, V_{VS}=2.5 V, Adjust V_{COMR}	2.5	2.9	3.3	V
V_{SG-CV}	Ending Voltage of Frequency Decreasing in CV Mode	V_{CS}=4 V, V_{VS}=2.5 V, Adjust V_{COMR}	0.3	0.5	0.7	V
S_{G-CV}	Frequency Decreasing Slope of CV Mode		25	36	47	kHz/V
$t_{ON-MIN-H}$	Minimum On-Time at High Line in CV Mode	V_{VS}=0.9 V, V_{CS}=0.25 V	370	400	430	ns
$t_{ON-MIN-L}$	Minimum On-Time at Low Line in CV Mode		0.75	0.90	1.05	µs
$t_{ON-MIN-SAT}$	Minimum On-Time at Low Line in CV Mode		1.05	1.20	1.35	µs

Continued on the following page…

Electrical Characteristics (Continued)

V_{DD}=15 V, T_A=25°C, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Cable Compensation						
V_{COMR}	Variation Test Voltage on COMR Pin for Cable Compensation	V_{CS}=4 V, V_{VS}=4 V, Measure V_{COMR}	1.00	1.15	1.30	V
Gate						
t_{ON-MAX}	Maximum On-Time	V_{DD}=15 V, V_{CS}=0 V, V_{VS}=0 V, V_{COMR}=4 V	13	15	18	µs
V_{OL}	Output Voltage Low(4)	V_{DD}=20 V			1.5	V
V_{OH}	Output Voltage High(4)	V_{DD}=0 V→18 V→8 V	5			V
V_{OH-MIN}	Output Voltage High(4)	V_{DD}=5.5 V	4			V
t_{PD}	Propagation Delay to GATE Output	V_{DD}=7.5 V	100	150	200	ns
t_r	Gate Output Rising Time	V_D=15 V, C_{Load}=1 nF	100	150	200	ns
t_f	Gate Output Falling Time	V_{DD}=15 V, C_{Load}=1 nF	50	75	100	ns
V_{CLAMP}	Output Clamp Voltage	V_{DD}=2V	12.5	14.0	15.5	V
Over-Temperature Protection (OTP)						
T_{OTP}	Threshold Temperature for OTP(4)(6)				150	°C
$T_{OTP-HYS}$	Restart Junction Temperature(4)(6)			120		°C

Notes:

4. Not tested; guaranteed by design.
5. $f_{OSC-CC-MIN}$ occurs when the power unit enters BCM operation.
6. OTP and VSOVP protection are Latch Mode.

Typical Performance Characteristics

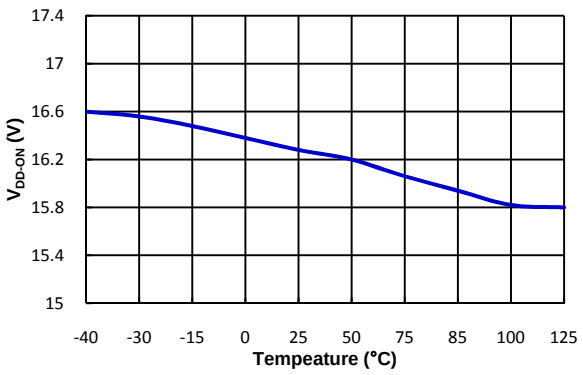


Figure 6. V_{DD} Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

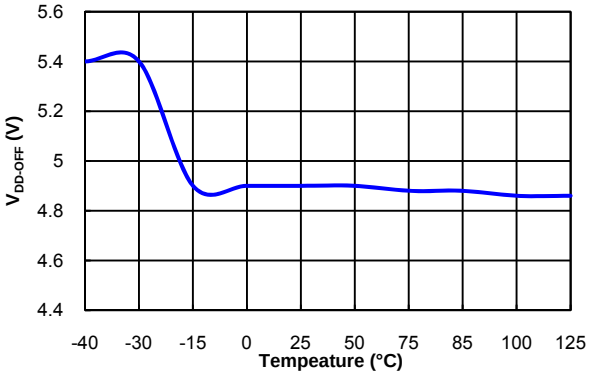


Figure 7. V_{DD} Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

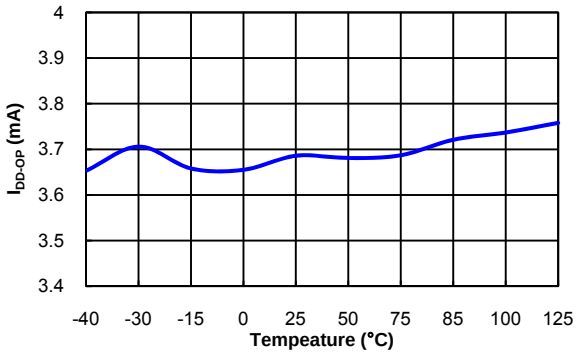


Figure 8. Operating Current (I_{DD-OP}) vs. Temperature

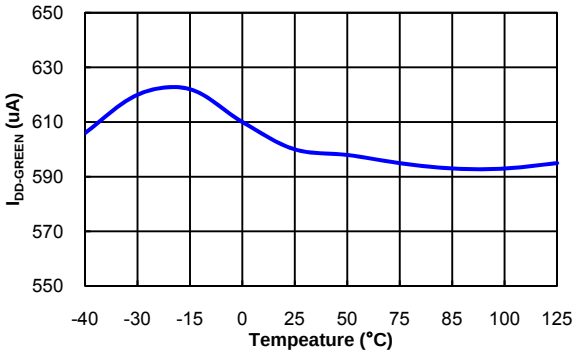


Figure 9. Burst Mode Operating Current ($I_{DD-GREEN}$) vs. Temperature

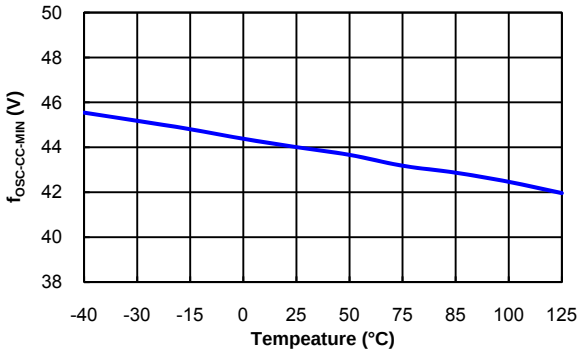


Figure 10. CC Regulation Minimum Frequency ($f_{OSC-CC-MIN}$) vs. Temperature

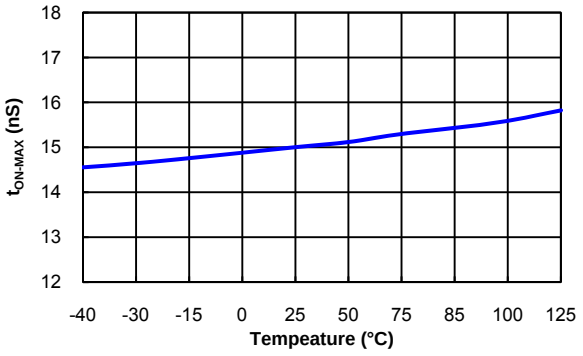


Figure 11. Maximum Gate On Time (t_{ON-MAX}) vs. Temperature

Typical Performance Characteristics (Continued)

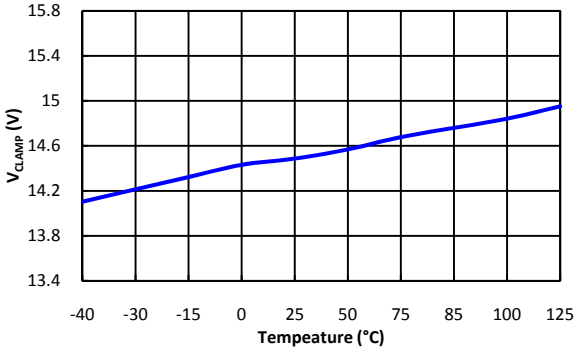


Figure 12. Gate Output Clamp Voltage (V_{CLAMP}) vs. Temperature

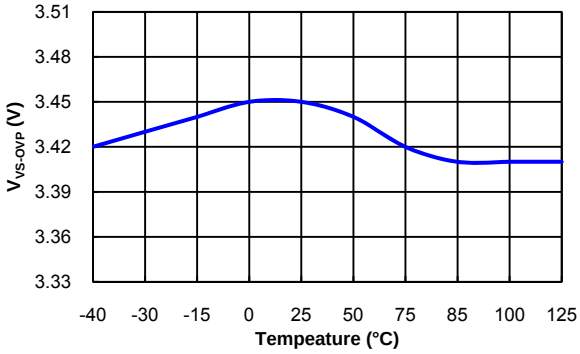


Figure 13. VS Over-Voltage Protection (V_{VS-OVP}) vs. Temperature

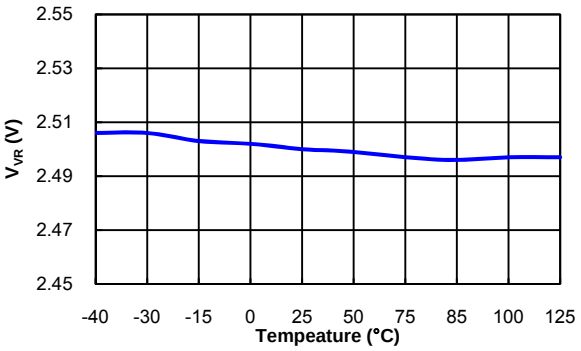


Figure 14. Reference Voltage of CS (V_{VR}) vs. Temperature

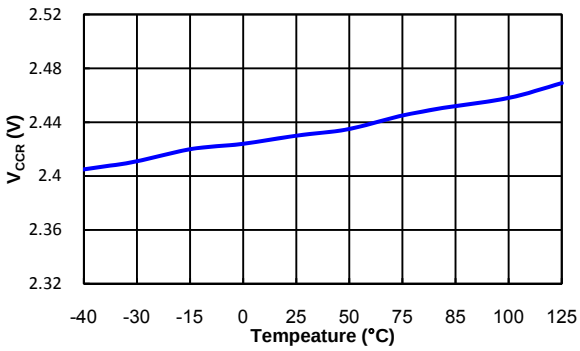


Figure 15. Variation Voltage on CS Pin for Constant-Current Regulation (V_{CCR}) vs. Temperature

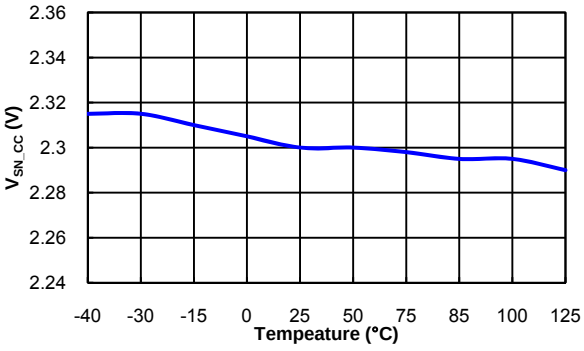


Figure 16. Starting Voltage of Frequency Decreasing of CC Regulation (V_{SN-CC}) vs. Temperature

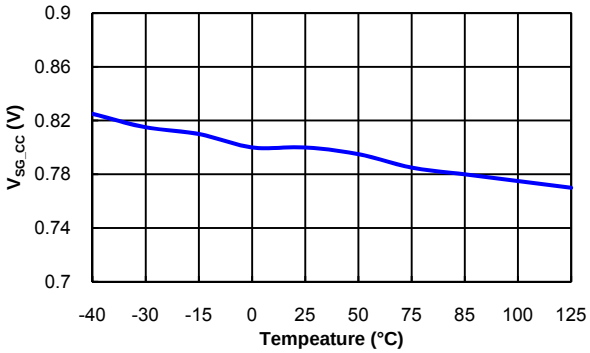


Figure 17. Ending Voltage of Frequency Decreasing of CC Regulation (V_{SG-CC}) vs. Temperature

Typical Performance Characteristics (Continued)

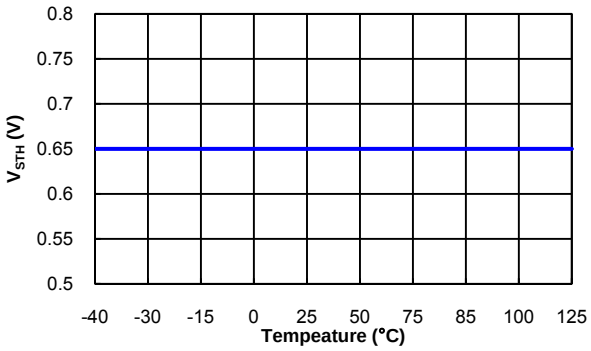


Figure 18. Threshold Voltage for Current Limit (V_{STH}) vs. Temperature

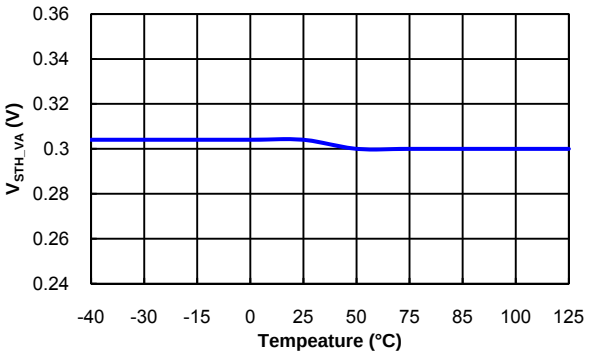


Figure 19. Threshold Voltage for Current Limit at Power Mode (V_{STH-VA}) vs. Temperature

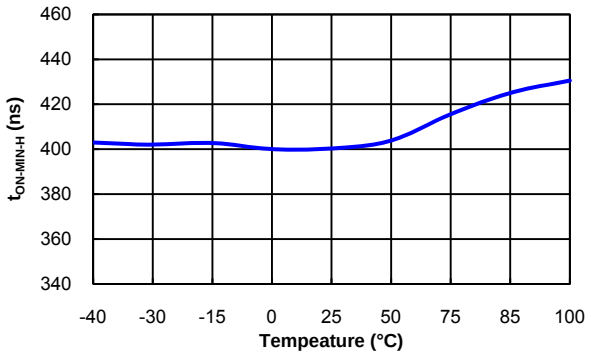


Figure 20. Minimum On Time ($t_{ON-MIN-H}$) vs. Temperature

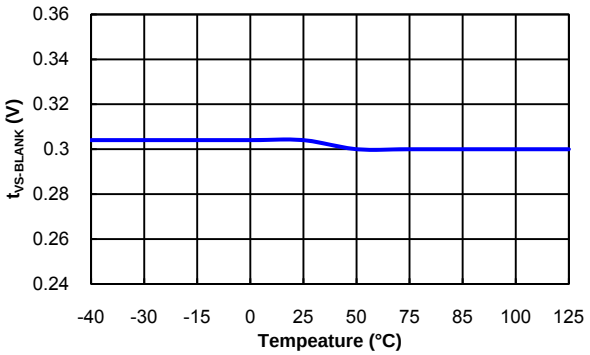


Figure 21. V_S Leading-Edge Blanking Time ($t_{VS-BLANK}$) vs. Temperature

Functional Description

Basic CV/CC Control Principle

Figure 22 shows the basic circuit diagram of a Primary-Side Regulated (PSR) flyback converter with typical waveforms shown in Figure 23. Generally, Discontinuous Conduction Mode (DCM) or Boundary Conduction Mode (BCM) operation is preferred for PSR since it allows better output regulation. The operation principles of DCM/BCM flyback converter are as follows:

During the MOSFET on time (t_{ON}), input voltage (V_{DL}) is applied across the primary-side inductor (L_m). Then MOSFET current (I_{DS}) increases linearly from zero to the peak value (I_{pk}). During this time, the energy is drawn from the input and stored in the inductor.

When the MOSFET is turned off, the energy stored in the inductor forces the secondary diode (D_{sec}) to turn on. While the diode is conducting, the output voltage (V_o), together with diode forward voltage drop (V_F), are applied across the secondary-side inductor ($L_m \times N_s^2 / N_p^2$) and the diode current (I_D) decreases linearly from the peak value ($I_{pk} \times N_p / N_s$) to zero. At the end of inductor current discharge time (t_{DIS}), all the energy stored in the inductor has been delivered to the output.

When the diode current reaches zero, the transformer auxiliary winding voltage (V_{Aux}) begins to oscillate by the resonance between the primary-side inductor (L_m) and the effective capacitor loaded across MOSFET. For BCM operation, this period does not exist.

During the inductor current discharge time, the sum of output voltage and diode forward-voltage drop is reflected to the auxiliary winding side as $(V_o+V_F) \times N_{Aux}/N_s$. Since the diode forward-voltage drop decreases as current decreases, the auxiliary winding voltage reflects the output voltage best at the end of diode conduction time, where the diode current diminishes to zero. By sampling the winding voltage at the end of the diode conduction time, the output voltage information can be obtained. The internal error amplifier for output voltage regulation (EAV) compares the sampled voltage with internal precise reference to generate error voltage (COMV), which determines the duty cycle of the MOSFET in CV Mode.

Meanwhile, the output current is obtained by averaging the triangular output diode current area over a switching cycle as:

$$I_O = < I_D >_{AVG} = \frac{1}{2} \cdot I_{PK} \cdot \frac{N_P}{N_S} \cdot \frac{T_{DIS}}{T_S} \quad (1)$$

The internal FAN104W circuits identify the peak value of the drain current with a peak detection circuit and calculate the output current using the inductor discharge time (t_{DIS}) and switching period (t_S). This output information (EAI) is compared with internal precise reference to generate error voltage (COMI), which determines the duty cycle of the MOSFET in CC Mode. With Fairchild's TRUECURRENT® technique, constant current output can be precisely controlled.

With a given current sensing resistor, the output current can be programmed as:

$$I_o = \frac{1.25}{K} \cdot \frac{N_P}{N_S} \cdot \frac{1}{R_{CS}} \quad (2)$$

where K is the design parameter of IC, which is 10.5.

Of the two error voltages, COMV and COMI, the smaller one determines the duty cycle. During Constant Voltage regulation, COMV determines the duty cycle while COMI is saturated to HIGH. During Constant Current regulation, COMI determines the duty cycle while COMV is saturated to HIGH.

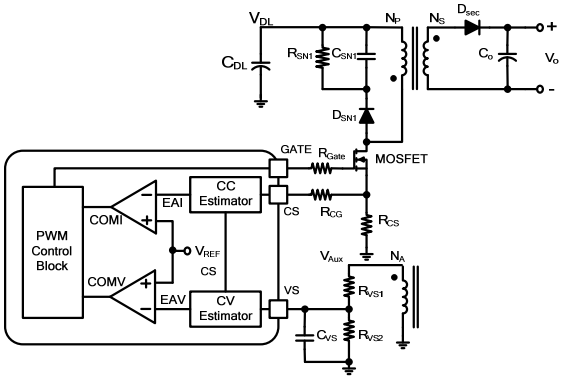


Figure 22. Simplified PSR Flyback Converter Circuit

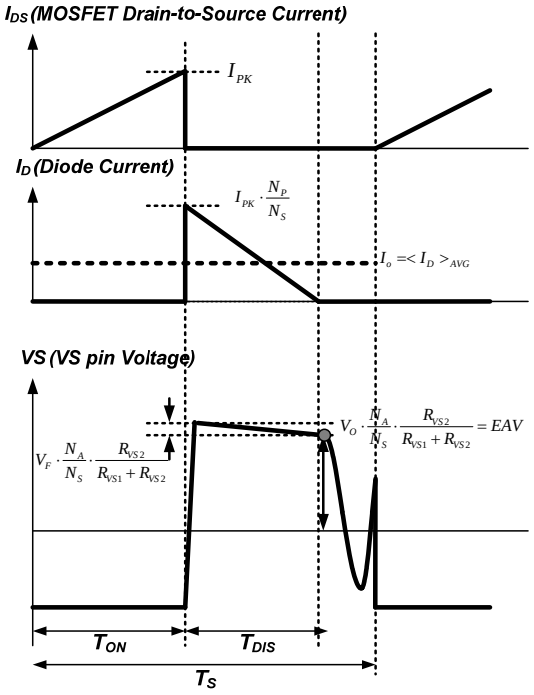


Figure 23. DCM Flyback Converter Waveforms

BCM Operation Function

FAN104W allows BCM operation for better conversion efficiency and low standby power design margin. BCM delays the next cycle turn-on of MOSFET until the discharge time (t_{DIS}) on the VS pin is obtained, as shown in Figure 24. To utilize BCM, FAN104W prohibits the turn-on of next switching cycle for 10% of its switching period after discharge time (t_{DIS}) is obtained. In Figure 24, the first switching cycle has a discharge time (t_{DIS}) before 90% of its original switching period and therefore the turn-on instant of the next cycle is determined its original switching period without being affected by the discharge time (t_{DIS}) point. The second switching cycle does not have discharge time (t_{DIS}) points by the end of its original switching period. Thus, the turn-on of the third switching cycle occurs after discharge time (t_{DIS}) points is obtained, with a delay of 10% of its original switching period. The minimum switching frequency that BCM allows is 10 kHz ($f_{OSC-BCM}$). If the discharge time point is not given until the end of maximum switching period of 100 μs (10 kHz), the converter can go into CCM operation losing output regulation.

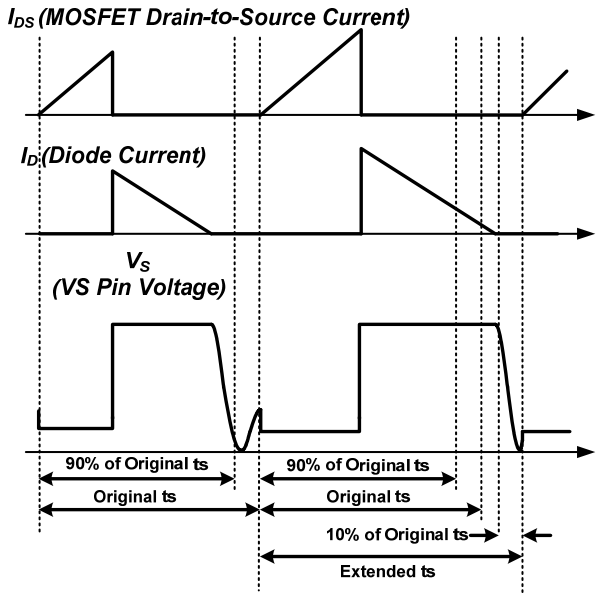


Figure 24. BCM Operation Function Waveform

Green-Mode Operation in CV Mode

The FAN104W uses a voltage regulation error amplifier output (COMV) as an indicator of the output load and modulates the PWM frequency. The switching frequency decreases as load decreases. In heavy load conditions, the switching frequency is fixed at 85 kHz. Once COMV decreases below 2.9 V, PWM frequency linearly decreases from 85 kHz. When FAN104W enters "deep" Green Mode, the PWM frequency is reduced to a minimum frequency ($f_{OSC-N-MIN}$) of 1.2 kHz, saving power to meet international power conservation requirements.

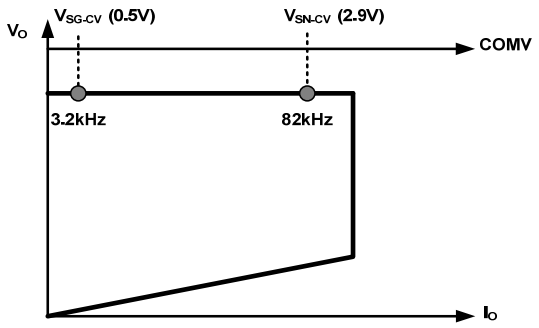


Figure 25. Frequency Reduction with COMV

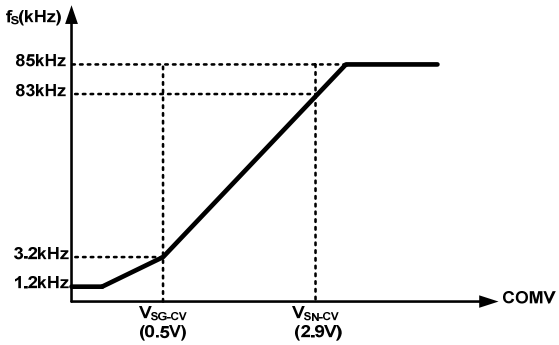


Figure 26. Frequency Reduction Curve in CV Mode

Frequency Reduction in CC Mode

The discharge time (t_{DIS}) of diode current increases as the output voltage decreases in CC Mode.FAN104W decreases switching frequency as output voltage drops, as shown in Figure 27. FAN104W indirectly monitors the output voltage by the sample-and-hold voltage (EAV) of V_S, which is taken at 70% of diode current discharge time of the previous switching cycle. Figure 28 shows how the frequency reduces as the sample-and-hold voltage (EAV) of V_O decreases.

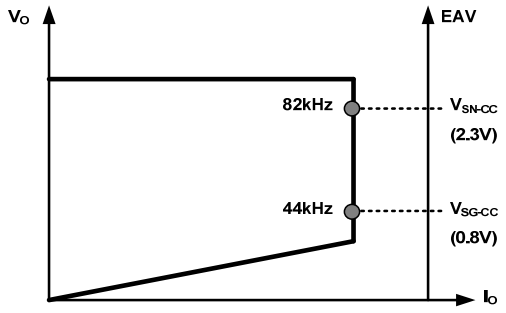


Figure 27. Frequency Reduction with EAV

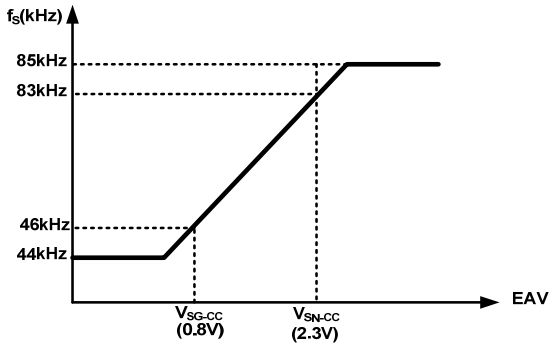


Figure 28. Frequency Reduction Curve in CC Mode

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth of the EMI test equipment, allowing conformation to EMI limitations. The FAN104W internal frequency-hopping circuit changes the switching frequency progressively between 82 kHz and 88 kHz with a period t_{FHR} of 3 ms.

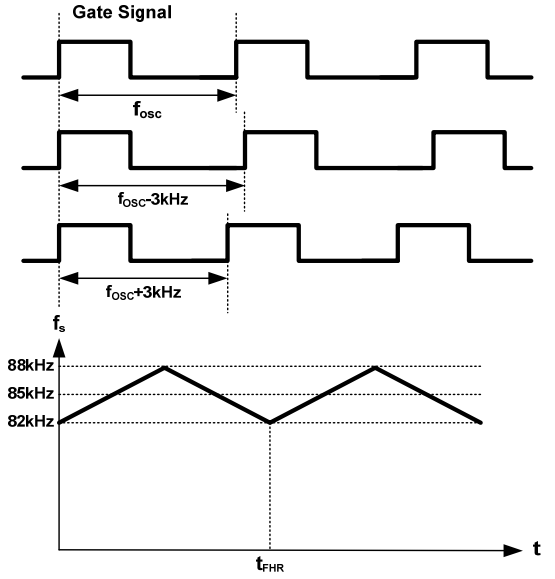


Figure 29. Frequency Hopping

Slope Compensation

The sensed voltage across the current-sense resistor is used for Current-Mode control and pulse-by-pulse current limiting. A synchronized ramp signal with positive slope is added to the current sense information at each switching cycle, improving noise immunity of Current-Mode control.

Cable Voltage Drop Compensation

When it comes to cellular phone charger applications, the battery is located at the end of cable, which typically causes several percentage of voltage drop on the actual battery voltage. FAN104W has a built-in cable voltage drop compensation, which provides a constant output voltage at the end of the cable over the entire load range in CV Mode. As load increases, the voltage drop across the cable is compensated by increasing the reference voltage of voltage regulation error amplifier.

Operating Current

The operating current in FAN104W is as small as 3.5 mA. The small operating current results in higher efficiency and reduces the V_{DD} hold-up capacitance requirement. Once FAN104W enters deep Green Mode, the operating current is reduced to 600 μA, assisting the power supply meet power conservation requirements.

High-Voltage Startup

Figure 30 shows the HV-startup circuit for FAN104W applications. The HV pin is connected to the line input or bulk capacitor through a resistor, R_{Start} (100 kΩ is recommended). During startup, the internal startup circuit is enabled. Meanwhile, line input supplies the current I_{HV}, to charge the hold-up capacitor, C_{VDD} through R_{Start}. When the V_{DD} voltage reaches V_{DD-ON}, the internal startup circuit is disabled, blocking I_{HV} from flowing into the HV pin. Once the IC turns on, C_{VDD} is the only energy source to supply the IC consumption current before the PWM starts to switch. Thus, C_{VDD} must be large enough to prevent V_{DD} from dropping to V_{DD-OFF} before the power can be delivered from the auxiliary winding. The V_{DD} capacitance tolerance is an important factor to consider for C_{DD} selection. Connecting a 22 μF capacitor between the V_{DD} and GND pins is recommended to ensure the system stability across a wide operating temperature range.

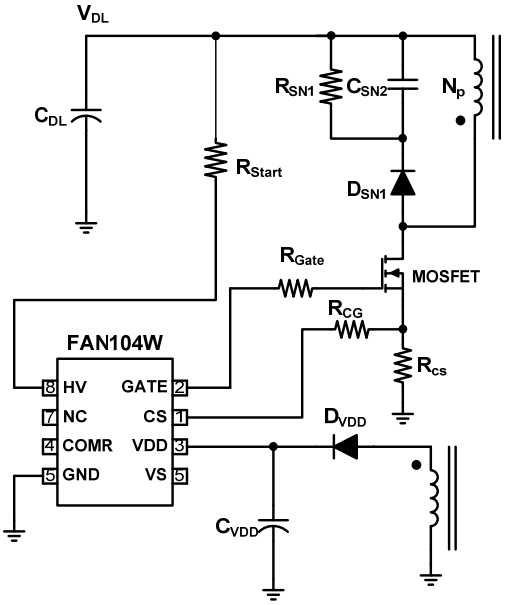


Figure 30. HV Startup Circuit

Protections

The FAN104W self-protection functions include V_{DD} Over-Voltage-Protection (V_{DD} OVP), Over-Temperature-Protection (OTP), VS Over-Voltage Protection (VSOVP), CS pin short-circuit protection, brownout protection, and VS pin low-side resistor open/short protection, and high-side resistor-open protection. The V_{DD} OVP, brownout protection, VS pin low-side resistor short protection, VS pin high-side open protection, and CS pin short-circuit protection are implemented as Auto-Restart Mode. The VSOVP, VS pin low-side resistor open protection and internal OTP are implemented as Latch Mode.

When an Auto-Restart Mode protection is triggered, switching is terminated and the MOSFET remains off, causing V_{DD} to drop. When V_{DD} reaches the V_{DD} turn-off voltage of 5 V; the protection is reset, the internal startup circuit is enabled, and the supply current drawn from the HV pin charges the hold-up capacitor. When V_{DD} reaches the turn-on voltage of 16 V, normal operation resumes. In this manner, Auto-Restart alternately enables and disables the switching of the MOSFET until the abnormal condition is eliminated, as shown in Figure 31.

When a Latch Mode protection is triggered, PWM switching is terminated and the MOSFET remains off, causing V_{DD} to drop. When V_{DD} drops to the V_{DD} turn-off voltage of 5 V, the internal startup circuit is enabled without resetting the protection and the supply current drawn from HV pin charges the hold-up capacitor. Since the protection is not reset, the IC does not resume PWM switching even when V_{DD} reaches the turn-on voltage of 16 V, disabling HV startup circuit. Then, V_{DD} drops again down to 5 V. In this manner, a Latch Mode protection alternately charges and discharges V_{DD} until there is no more energy in DC link capacitor. The protection is reset when V_{DD} drops to 2.5 V, which is allowed only after power supply is unplugged from the AC line, as shown in Figure 32.

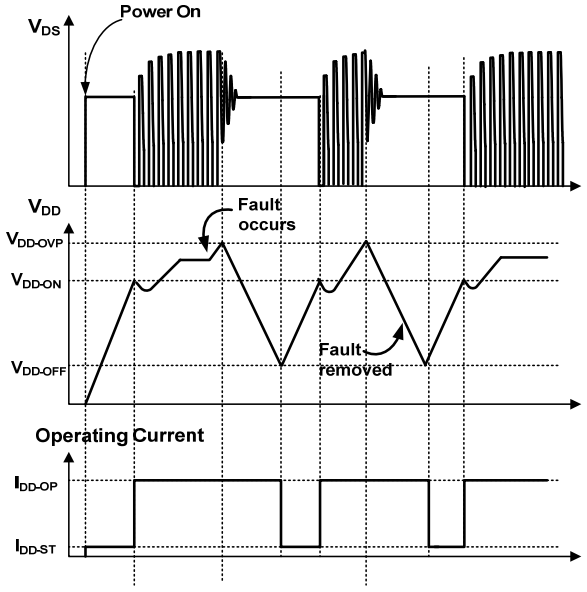


Figure 31. Auto-Restart Mode Operation

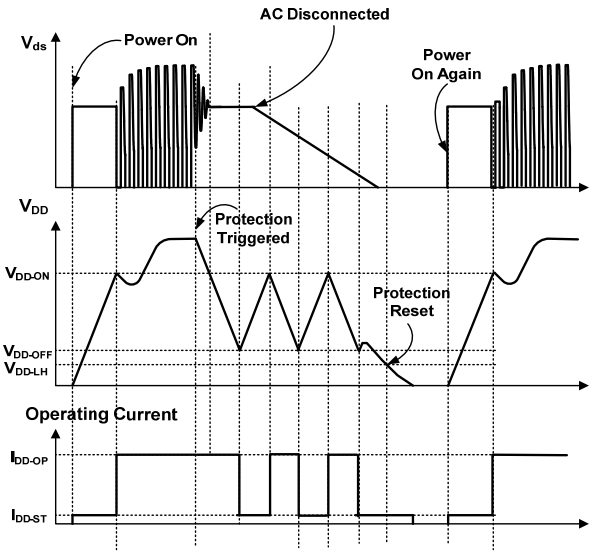


Figure 32. Latch-Mode Operation

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs at the sense resistor. To avoid premature termination of the switching pulse, a 150 ns leading-edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

Noise Immunity

Noise from the current sense or the control signal can cause significant pulse width jitter, particularly in Continuous-Conduction Mode. While slope compensation helps alleviate these problems, further precautions should still be taken. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FAN104W, and increasing the power MOS gate resistance is advised.

Physical Dimensions

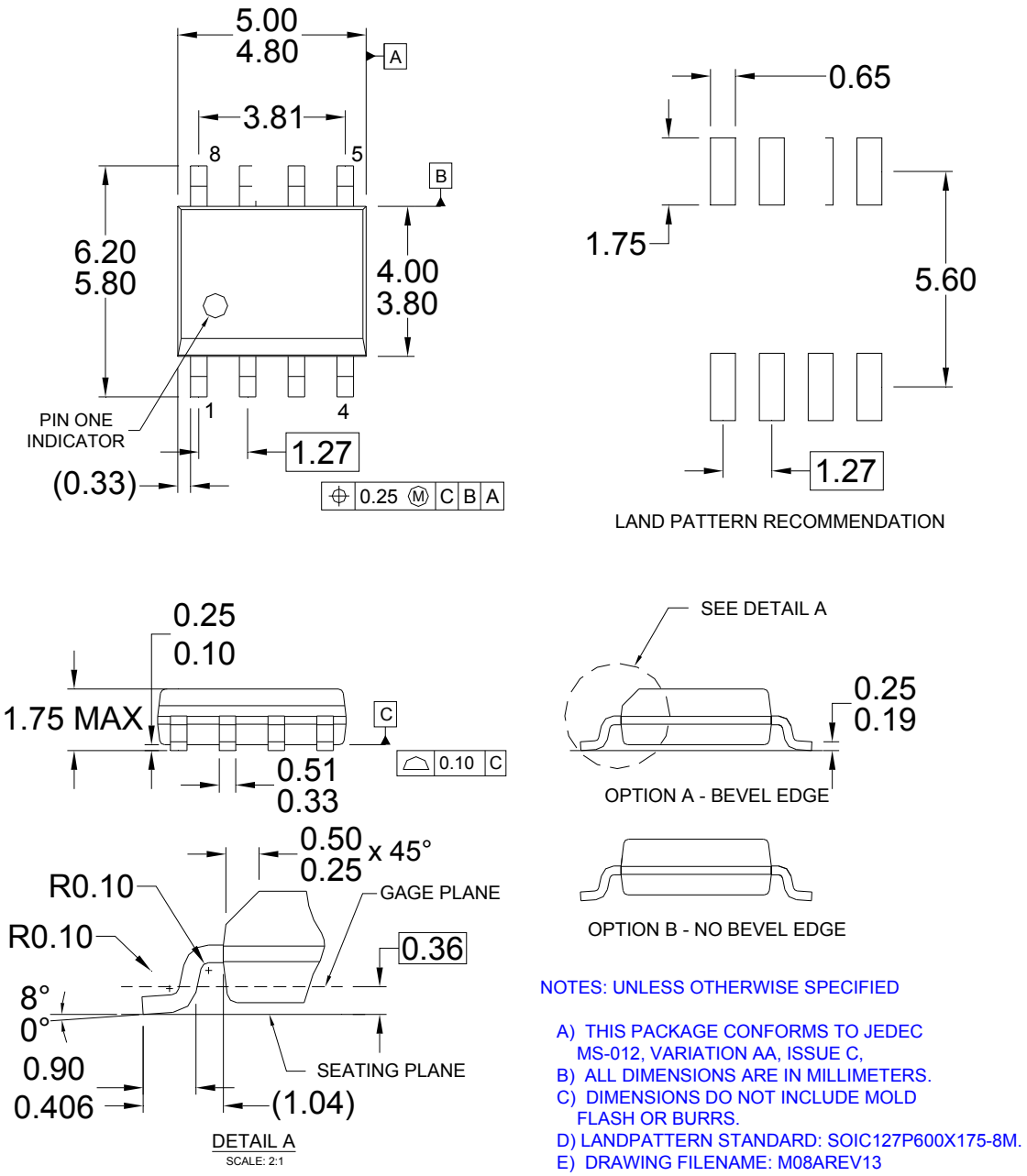


Figure 33. 8-Lead, SOIC, JEDEC MS-012, .150" Narrow Body

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊