FAN3181

Single 2A High-Speed, Low-Side IGBT Driver

The FAN3181 is suitable for designed to stand-alone IGBT driver in low-side switching applications by providing high peak current pulses during the switching intervals. The protection functions include Under-Voltage Lockout (UVLO) and Over-Current Protection (OCP), and Desaturation Protection (DESAT) with fault-out function and active miller clamp function. An open-drain fault-out signal is provided to indicate that an over-current, under-voltage, and Desaturation detect has occurred. Soft turn-off feature is used to increase the reliability of an application during short-circuit or over-current periods. This feature works after the desaturation or over-current protection is activated, which provides protection for IGBT against short-circuit and over-current events. With the "Soft" turn-off feature, the gate voltage will be reduced slowly in order to reduce IGBT current.

Features

- Operating Supply Voltage 25 V
- Typically 1.5 A/2.0 A Sourcing/Sinking Current-Driving Capability at V_{CC} = 15 V
- Output In- Phase with Input Signal
- Active Miller Clamp
- Desaturation Protection
- Cycle-by-Cycle Edge-Triggered Shutdown Function
- Fault-Out and Shutdown Function
- Built-in V_{CC} UVLO Function
- Built-in Soft Turn-Off Function
- Built-in Over-Current Protection (OCP)
- Operating Junction Temperature Range of -40°C to 125°C

Typical Applications

- Switch-Mode Power Supplies
- DC – DC Converters
- Motor Control for PFC in Air-conditioner Application

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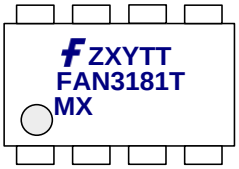
PACKAGE PICTURE

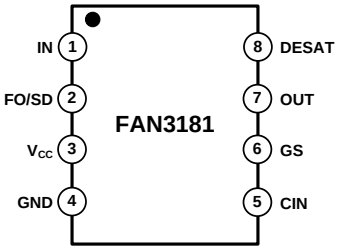
8 Lead SOP
(Small Outline Package)

MARKETING DIAGRAM



F: Fairchild Logo
Z: Plant Code
X: 1-Digit Year Code
Y: 1-Digit Week Code
TT: 2-Digit Die Run Code
M: Package Type (SOP)
X: Packing Type (Tape & Reel)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Packing Method
FAN3181TMX (1)	SOIC-8	Tape & Reel

Note:
1. This device passed wave-soldering test by JESD22A-111

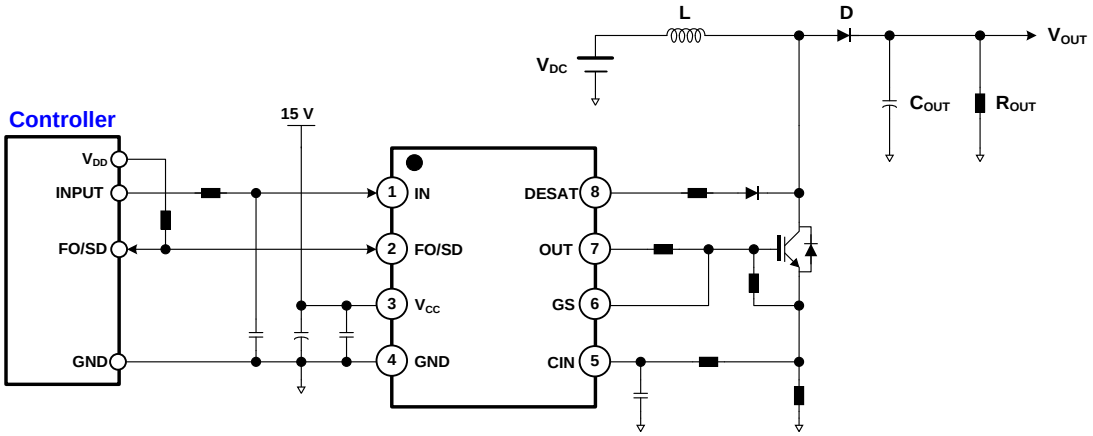


Figure 1 Simplified Application Schematics

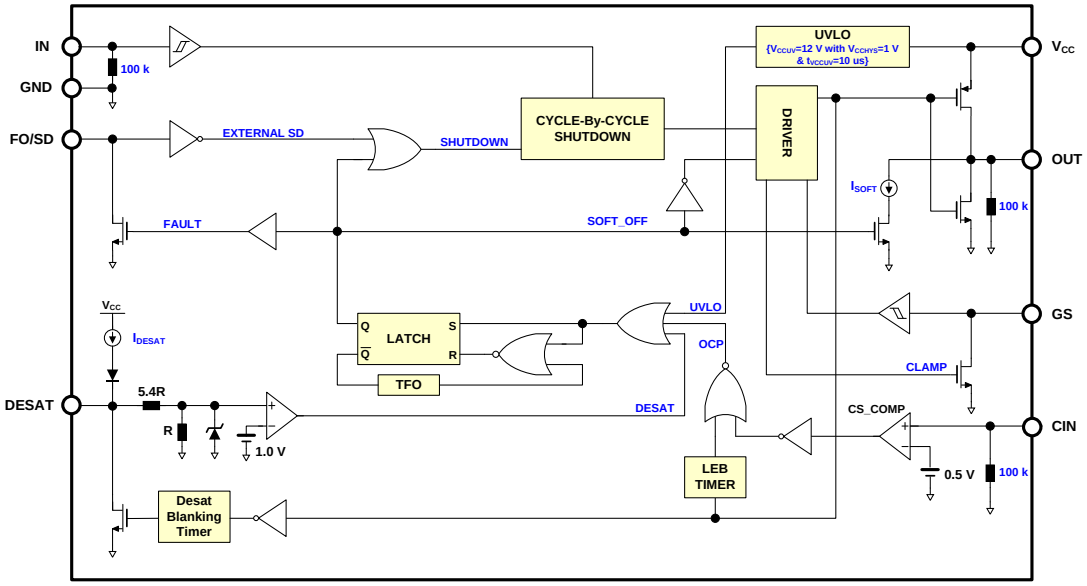


Figure 2. Detailed Block Diagram

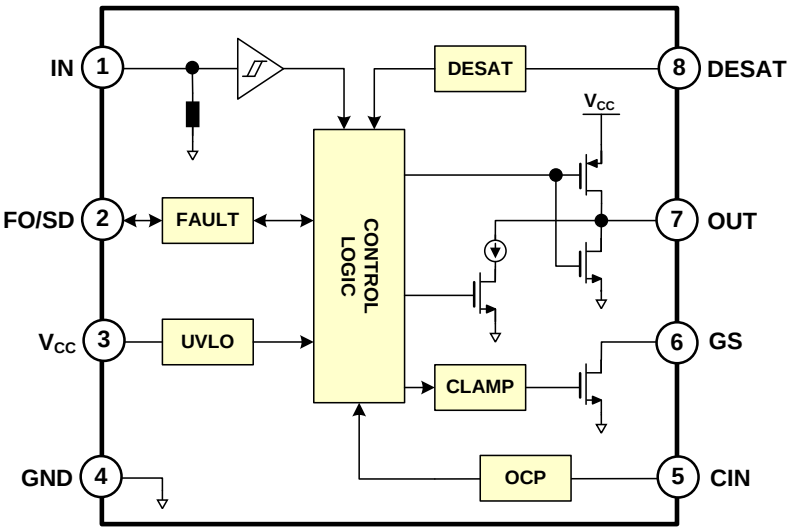


Figure 3. Simplified Block Diagram

PIN CONNECTIONS

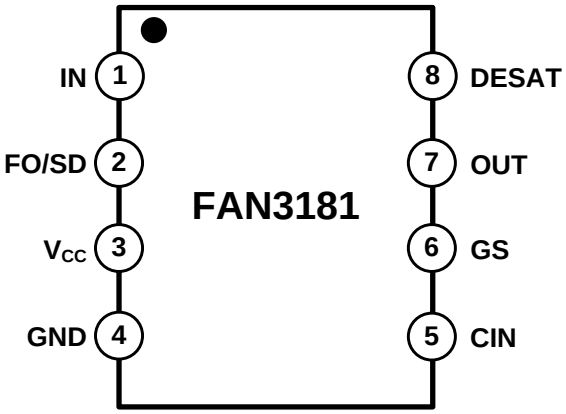


Figure 4. Pin Assignments – 8 Lead SOIC (Top View)

PIN FUNCTION DESCRIPTION

Pin Name	Pin No.	I/O/x	Description
IN	1	I	Input signal to control the output. IN has a pull-down resistor of 100 kΩ. Output In-Phase with Input Signal (Non-Inverting).
FO/SD	2	O	Fault output and shutdown that allows communication to main controller that the drivers has encountered a fault condition and deactivated the output.
V_{CC}	3	x	Power Supply. The bypass capacitor is required this pin to GND and should be placed as close as possible to the V_{CC} pin.
GND	4	x	This pin should connect to the IGBT Emitter or shunt resistor with short trace.
CIN	5	I	Analog Input for Over-Current detect
GS	6	O	Provides clamping for the IGBT gate during the off period to protect it from parasitic turn-on due to high collector-to emitter dv/dt induced.
OUT	7	O	Driver Output.
DESAT	8	I	Input for detecting the desaturation of IGBT due to fault condition.

MAXIMUM RATINGS (Note 2)

Rating		Symbol	Min.	Max.	Unit
Fixed Supply Voltage[3]		V_{CC}	-0.3	30.0	V
Output 1 Voltage		V_{OUT}	-0.3	V_{CC}+0.3	V
Output 2 Voltage		V_{GS}	-0.3	V_{CC}+0.3	V
IN, FO/SD, DESAT, V_{CIN}, and V_{FO} Voltage		V_{IN}	-0.3	V_{CC}+0.3	V
Operating Junction Temperature		T_J	-55	150	°C
Storage Temperature Range		T_{STG}	-55	150	°C
Electrostatic Discharge Capability	Human Body Model[4]	ESD_{HBM}		2	kV
	Charged Device Model[4]	ESD_{CDM}		500	V

2. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
3. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JESD22-A114
   ESD Charged Device Model tested per JESD22-C101
5. All voltage values are given with respect to GND pin.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, 8-SOP[6] Thermal Resistance Junction-Air[7]	θ_{JA}	200	°C/W
Power Dissipation[7]	P_D	0.625	W

6. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
7. JEDEC standard: JESD51-2, JESD51-3. Mounted on 76.2×114.3×1.6mm PCB (FR-4 glass epoxy material).

RECOMMENDED OPERATING CONDITIONS (Note 8)

Rating	Symbol	Min.	Max.	Unit
Fixed Supply Voltage	V_{CC}	UVLO	25	V
Input Voltage	V_{IN}	0	V_{CC}	V
Operating Ambient Temperature Range	T_A	-40	125	°C

8. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{CC}=15 V, for typical values T_A=25 °C, for min/max values T_A=-40°C to +125°C, unless otherwise specified. (Notes 10, 11)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
POWER SUPPLY SECTION						
Quiescent Current for V_{CC}	V_{IN}= 0 V	I_{QCC}	600	850	1050	µA
Operating Current for V_{CC}	f_{IN}= 20 kHz	I_{CC}		1.5	2.0	mA
V_{CC} Supply UV Trip Voltage		V_{CCUV}	11.0	12.0	13.0	V
V_{CC} Supply UV Hysteresis		V_{CCHYS}	0.5	1.0	1.5	V
V_{CC} Supply UV Filter Time[9]		t_{VCCUV}	5	10	15	µs
INPUT LOGIC SECTION						
High Level Input Voltage for IN		V_{IHT}		1.6	2.0	V
Low Level Input Voltage for IN		V_{ILT}	0.8	1.2		V
Input Logic Hysteresis		V_{INHYST}		0.4		V
High Level Logic Input Bias Current	V_{IN}= V_{CC}	I_{IN+}	125	150	200	µA
Low Level Logic Input Bias Current	V_{IN}= 0 V	I_{IN-}			1.0	µA
Logic Input Pull-Down Resistance		R_{IN}	75	100	120	kΩ
GATE DRIVER OUTPUT SECTION						
High Level Output Voltage (V_{CC}- V_{OUT})	I_{OUT}=100 mA	V_{OH}			0.8	V
Low Level Output Voltage	I_{OUT}=100 mA	V_{OL}			0.35	V
Output HIGH Short-Circuit Pulse Current[9]	V_O=0 V, V_{IN}=5 V with PW=10 µs	I_{O+}	1.0	1.5		A
Output LOW Short-Circuit Pulse Current[9]	V_O=15 V, V_{IN}=0 V with PW=10 µs	I_{O-}	1.5	2.0		A
Soft Turn-Off Sink Current	V_{CIN}=1 V, V_O=V_{CC}	I_{SOFT}	20	30	40	mA
OVER-CURRENT PROTECTION SECTION						
Over-Current Detect Threshold		V_{CINTH}	450	500	550	mV
Short-Circuit Input Current	V_{CIN}=1 V	I_{CIN}	5	10	15	µA
DESATURATION PROTECTION SECTION						
Desaturation Threshold Voltage		V_{DESAT}	6.0	6.4	6.8	V
Current Source	IN=HIGH	I_{DESAT}	215	250	285	µA
Switch On Resistance		R_{ONSAT}		2.5	5.0	Ω
ACTIVE MILLER CLAMP SECTION						
GS Pin Threshold Voltage		V_{GSTH}	1.2	1.5	1.8	V
GS Pin Low Level Clamp Voltage	I_{GS}=50 mA	V_{CLAMP}		110	250	mV
GS Pin Clamp Current[9]	V_{GS}=GND + 2.5 V	$I_{GSCLAMP}$	0.5	1.0		A
Clamp Switch Resistance		$R_{ONCLAMP}$		2.2	4.5	Ω
FAULT-OUTPUT SECTION						
FO/SD High Threshold Voltage		V_{FOSDH}		1.6	2.0	V
FO/SD Low Threshold Voltage		V_{FOSDL}	0.8	1.2		V
Fault Output Leakage Current	V_{FOSD}=V_{CC}	I_{FOSDLK}			1.0	µA
Fault Output Low Level Voltage	V_{MCU}=5 V, R_{PULLUP}=20 kΩ	V_{FOL}			0.1	V
Fault Output On Resistance	I_{FO}=5 mA	R_{DSFO}		250	400	Ω

9. This parameter, although guaranteed by design, is not tested in production.
10. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
11. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C.

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{CC}=15 V, and C_{LOAD} = 1000 pF, for typical values T_A=25 °C, for min/max values T_A=-40°C to +125°C, unless otherwise specified. (13, 14)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Turn-On Propagation Delay	V_{IN} From 0 V to 5 V	t_{ON}	10	15	20	ns
Turn-Off Propagation Delay	V_{IN} From 5 V to 0 V	t_{OFF}	12	17	22	ns
Propagation Delay Mismatching I t_{ON}-t_{OFF} I		MT			12	ns
Turn-On Rise Time		t_R		15	20	ns
Turn-Off Fall Time		t_F		10	17	ns
Fault Output Duration		t_{FAULT}	75	110	145	μs
Desat Blanking Time	V_{DESAT} = 6.5 V	$t_{DESABLK}$	1.8	2.8	3.8	μs
FO/SD to Output LOW Propagation Delay		t_{FOSD}		17	22	ns
CIN Pin Leading-Edge Blanking Time(12)		t_{CINBLT}		300	400	ns
Time from CIN Triggering to FO	From V_{CIN}=1 V to FO Turn-Off	t_{CINFO}	250	350	450	ns
Time from CIN Triggering to Output Turn-Off	From V_{CIN}=1 V to Gate Turn-Off	t_{CINOFF}	330	430	530	ns
Time from Clamp Triggering to Output Turn-Off(12)		t_{CLAMP}		6	10	ns
Time from DESAT Triggering to Output Turn-Off		t_{DESAT}	330	430	530	ns
Minimum Input Pulse Width Response at the Output(12)		t_{ONMIN}	40			ns

12. This parameter, although guaranteed by design, is not tested in production.
13. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
14. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C.

TYPICAL CHARACTERISTICS

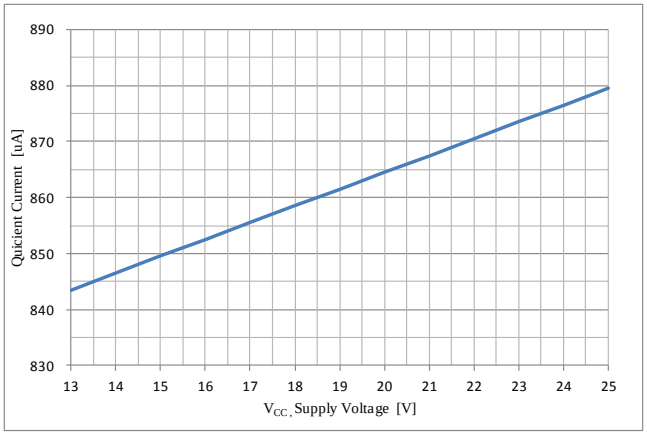


Figure 5.Quiescent Supply Current vs. V_{CC} Supply Voltage

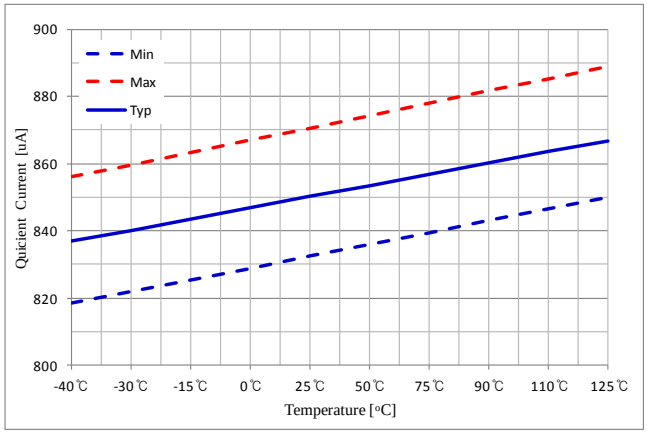


Figure 6.Quiescent Supply Current vs. Temperature

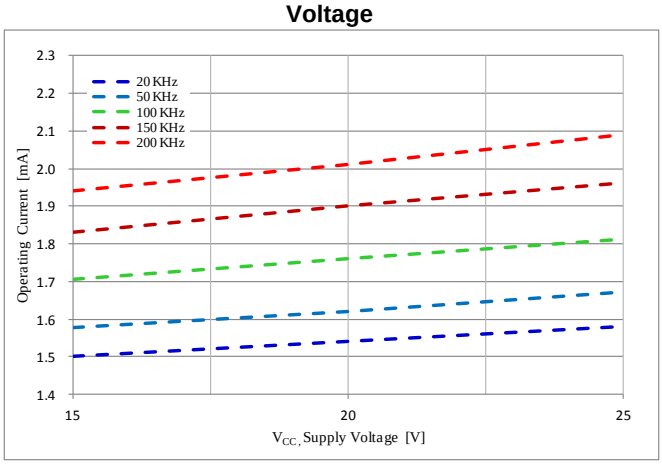


Figure 7. Operating Supply Current vs. V_{CC} Supply Voltage

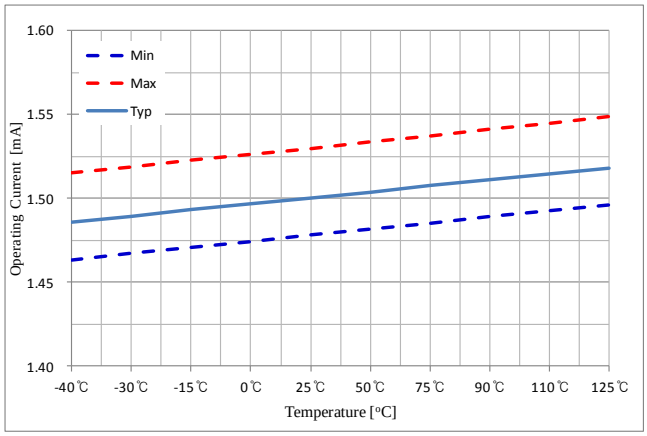


Figure 8. Operating Supply Current vs. Temperature

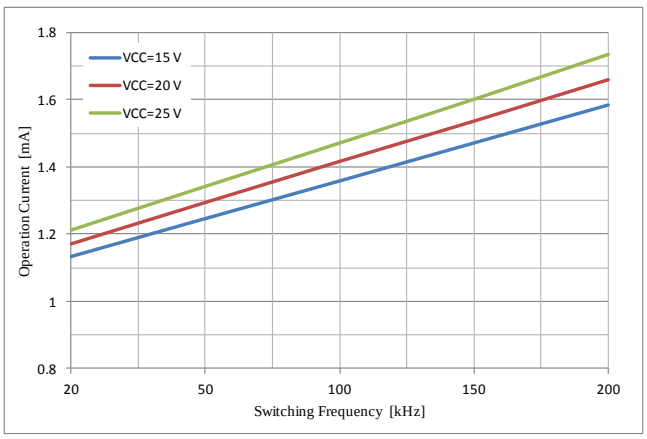


Figure 9.Operating Supply Current vs. Switching Frequency (No Load)

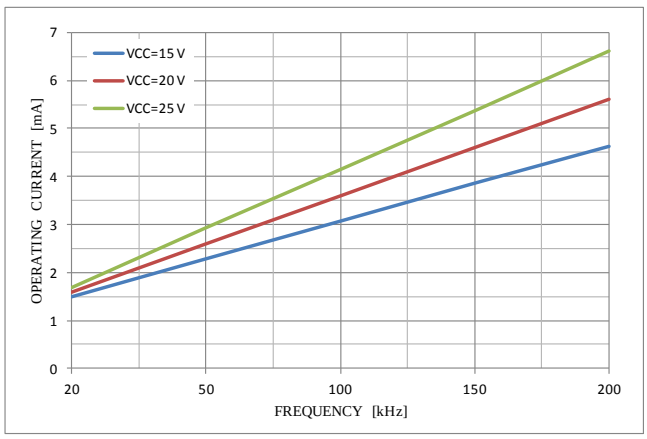


Figure 10.Operating Supply Current vs. Switching Frequency (C_{LOAD} = 1 nF)

TYPICAL CHARACTERISTICS

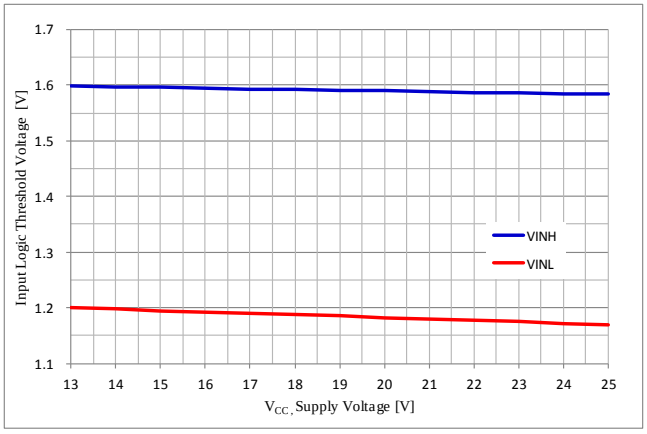


Figure 11. Input Threshold Voltage vs. V_{CC} Supply Voltage

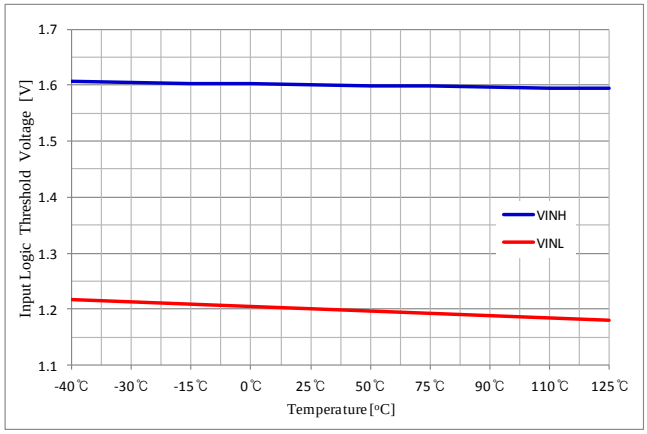


Figure 12. Input Threshold Voltage vs. Temperature

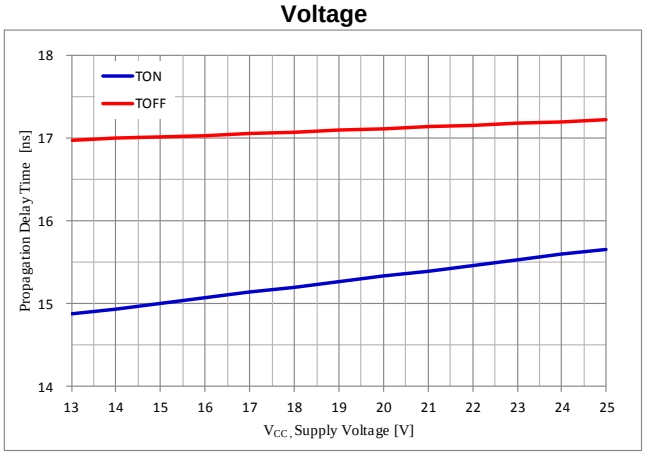


Figure 13.Propagation Delay Time vs. V_{CC} Supply Voltage

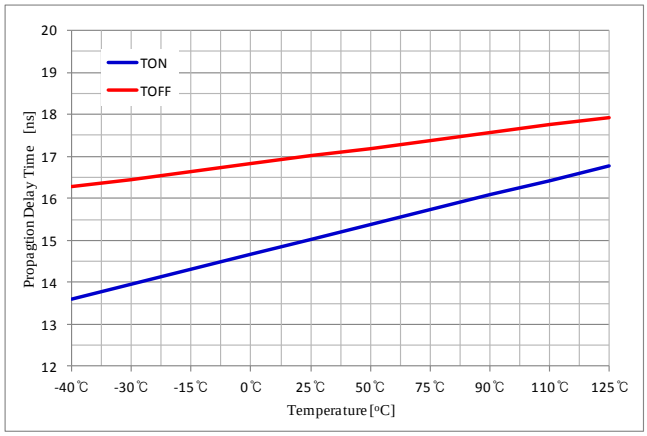


Figure 14.Propagation Delay Time vs. Temperature

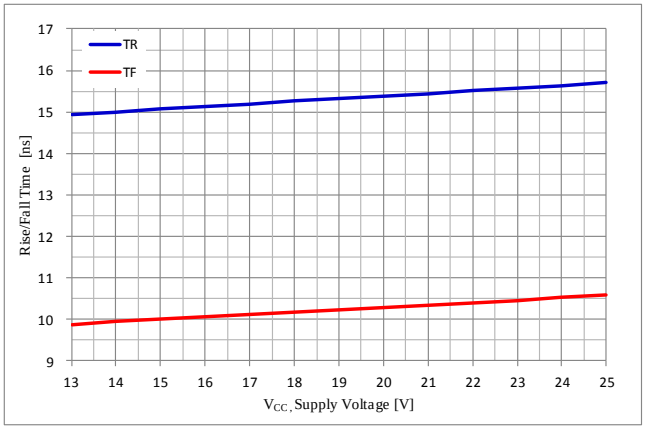


Figure 15.Output Rise/Fall Time vs. V_{CC} Supply Voltage

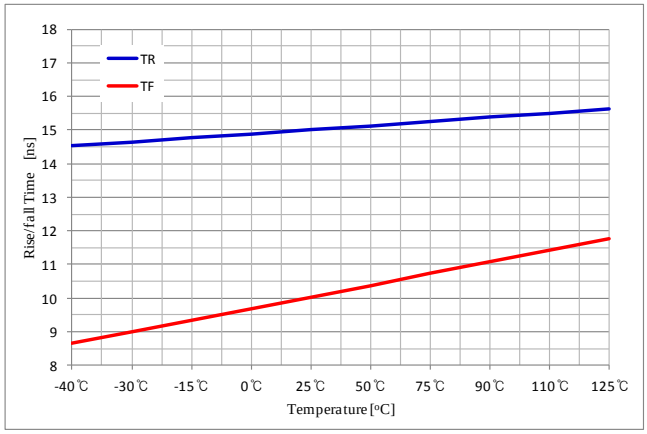


Figure 16.Output Rise/Fall Time vs. Temperature

TYPICAL CHARACTERISTICS1

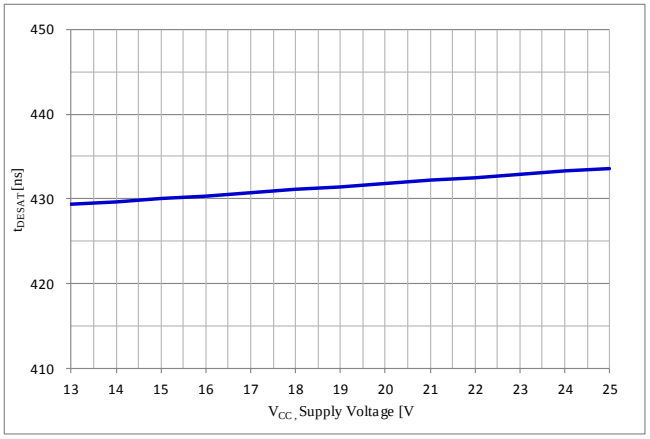


Figure 17. DESAT Triggering to Output OFF Delay Time vs. V_{CC} Supply Voltage

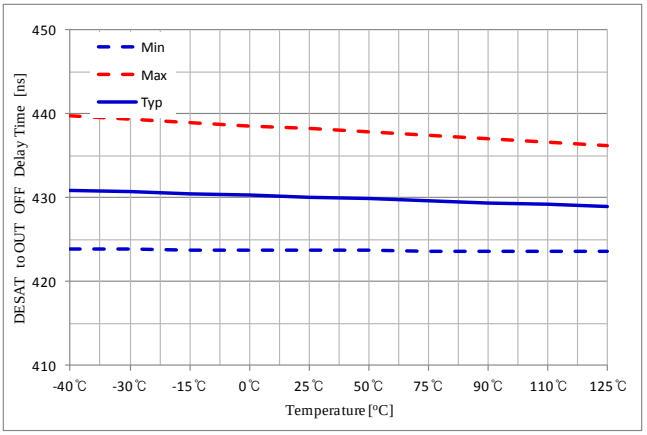


Figure 18. DESAT Triggering to Output OFF Delay Time vs. Temperature

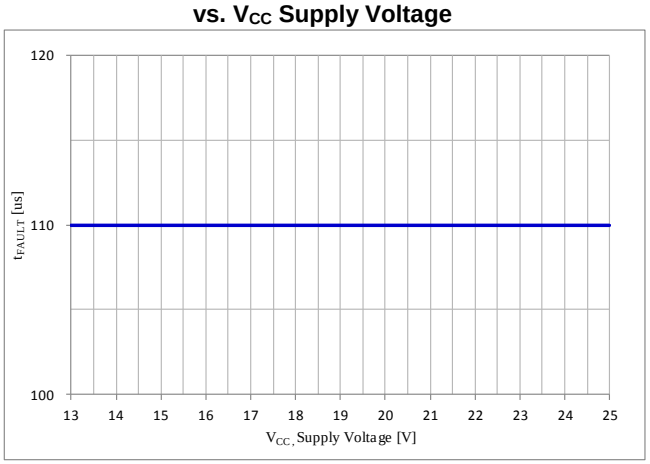


Figure 19. Fault Output Duration vs. V_{CC} Supply Voltage

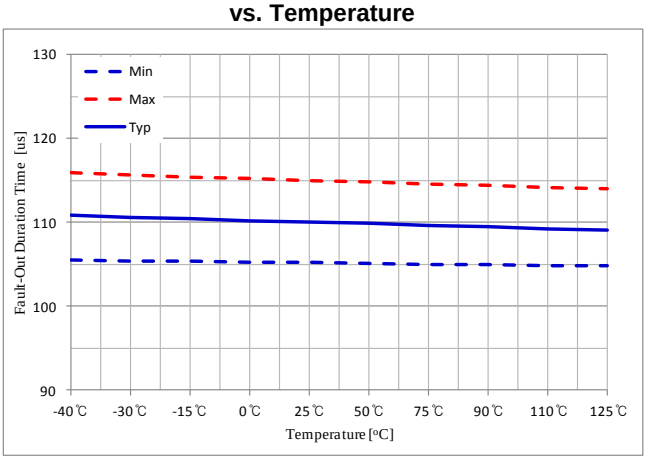


Figure 20. Fault Output Duration vs. Temperature

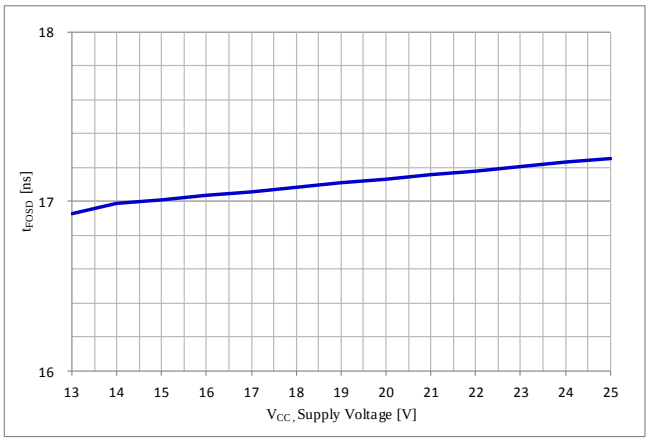


Figure 21. FO/SD to Output LOW Propagation Delay vs. V_{CC} Supply Voltage

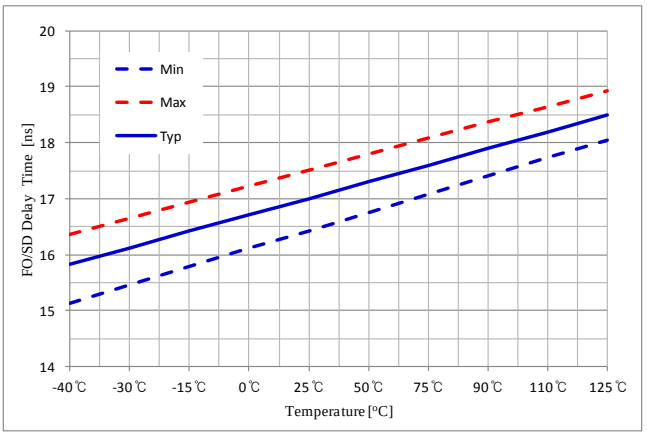


Figure 22. FO/SD to Output LOW Propagation Delay vs. Temperature

TYPICAL CHARACTERISTICS

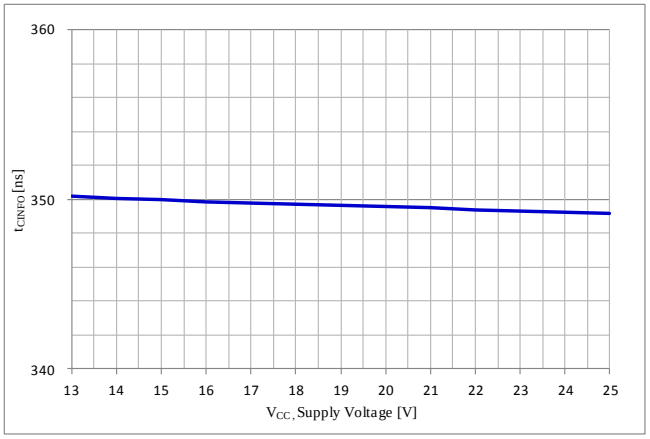


Figure 23. CIN Triggering to FO Delay Time vs. V_{CC} Supply Voltage

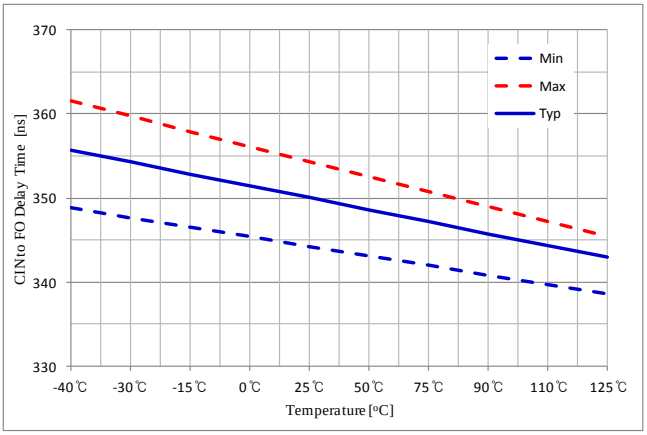


Figure 24. CIN Triggering to FO Delay vs. Temperature

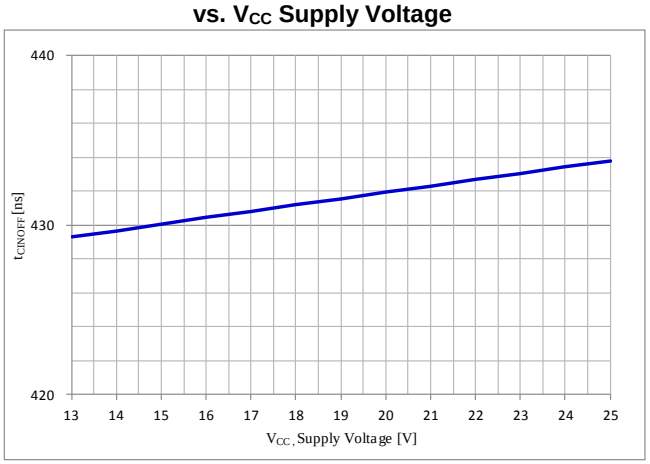


Figure 25. CIN Triggering to Output Low Delay vs. V_{CC} Supply Voltage

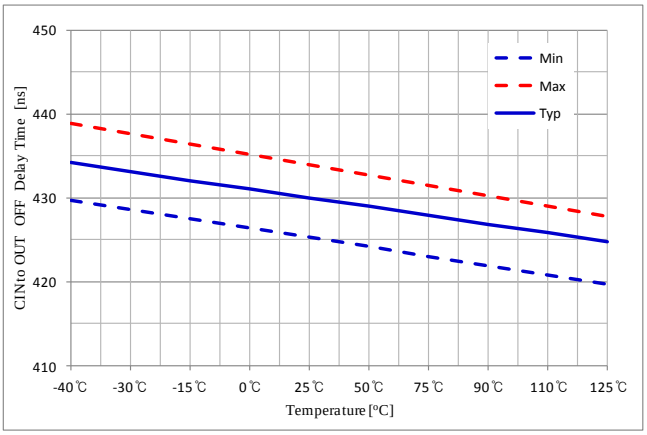


Figure 26. CIN Triggering to Output Low Delay vs. Temperature

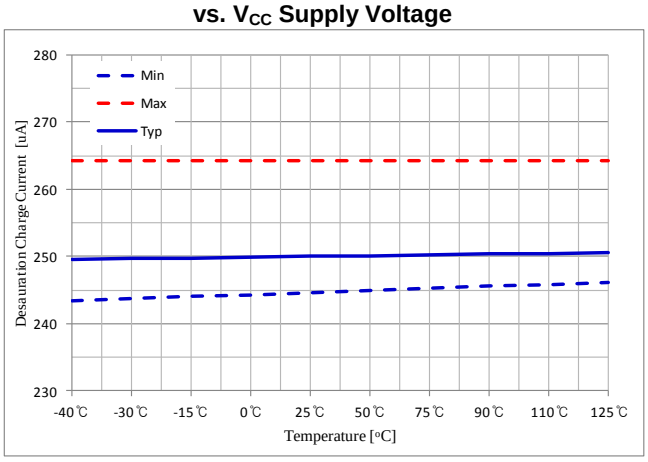


Figure 27. Desaturation Charge Current vs. Temperature

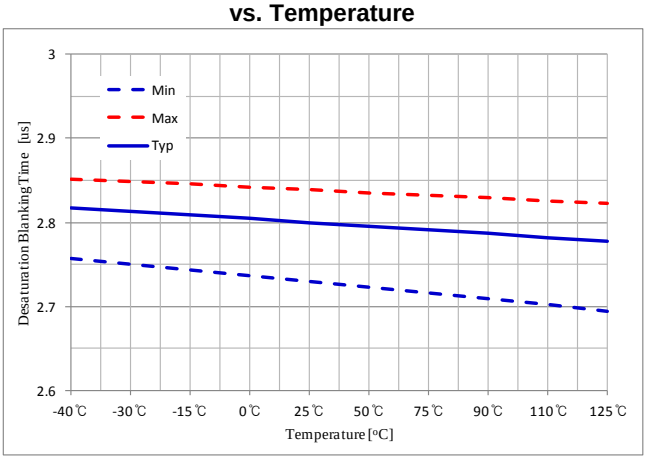


Figure 28. Desaturation Blanking Time vs. Temperature

TYPICAL CHARACTERISTICS

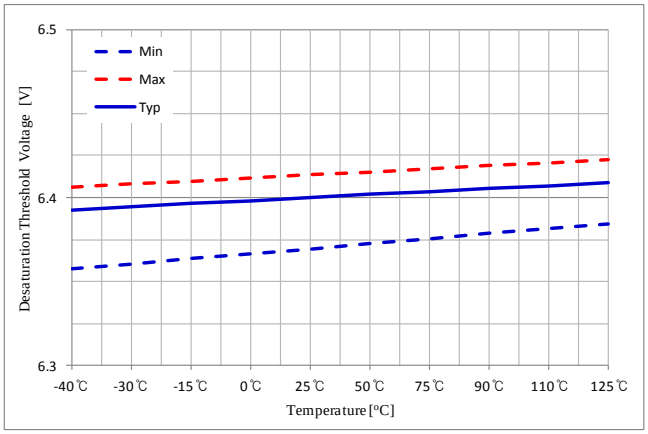


Figure 29. Desaturation Threshold Voltage vs. Temperature

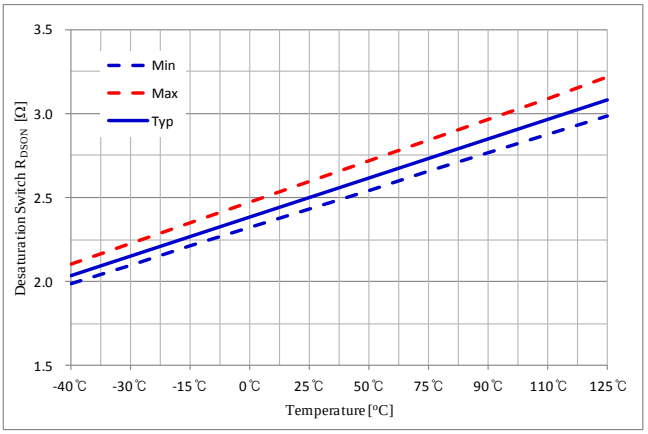


Figure 30. Desaturation Blanking Switch R_{DSON} vs. Temperature

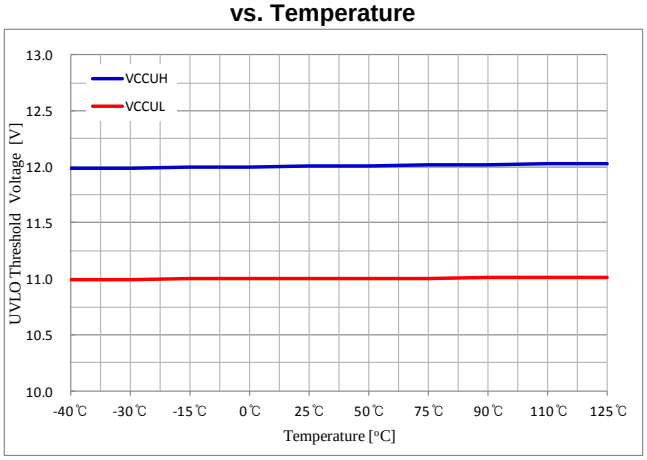


Figure 31. V_{CC} UVLO Threshold Voltage vs. Temperature

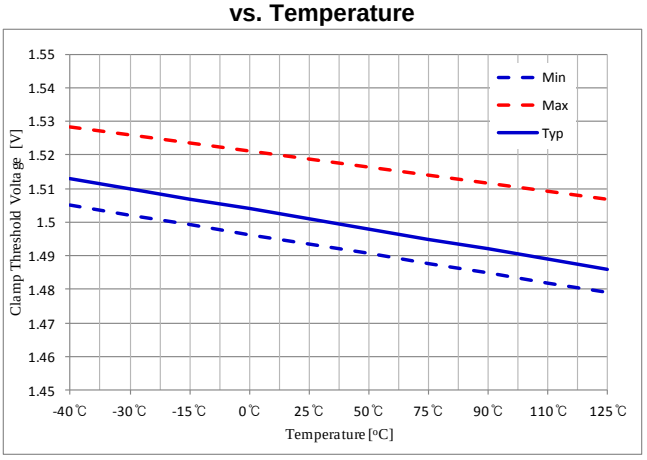


Figure 32. Clamp Threshold Voltage vs. Temperature

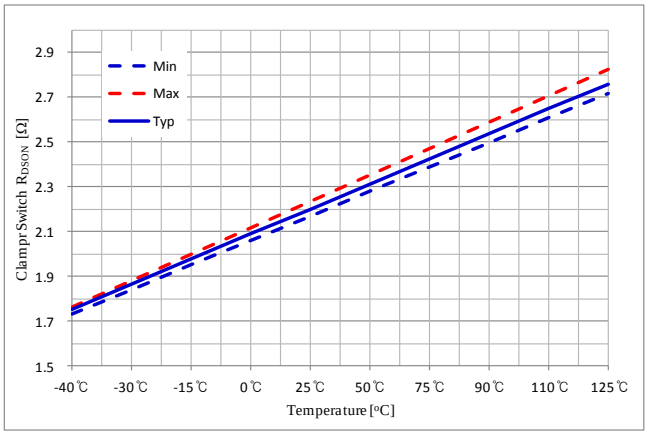


Figure 33. Clamp Switch R_{DSON} vs. Temperature

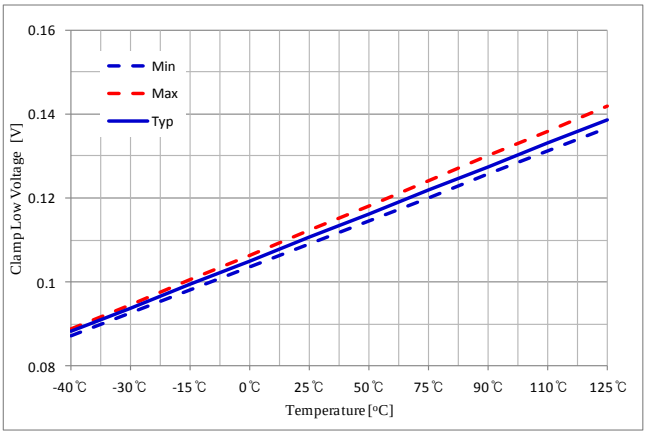


Figure 34. GS Pin Clamp Low Level Voltage at I_{GS}=50 mA vs. Temperature

TYPICAL CHARACTERISTICS

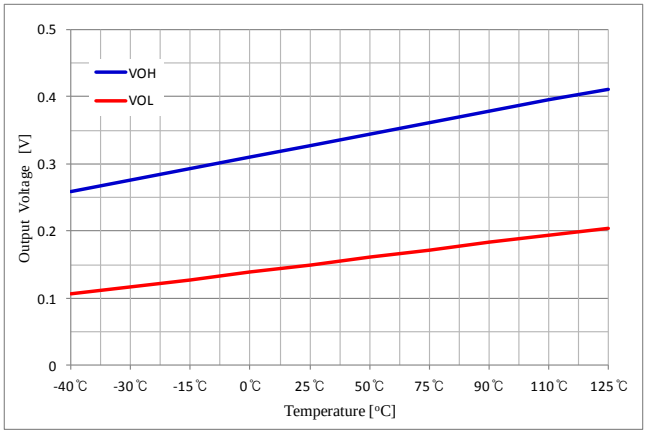


Figure 35. Output Voltage at I_O=100 mA vs. Temperature

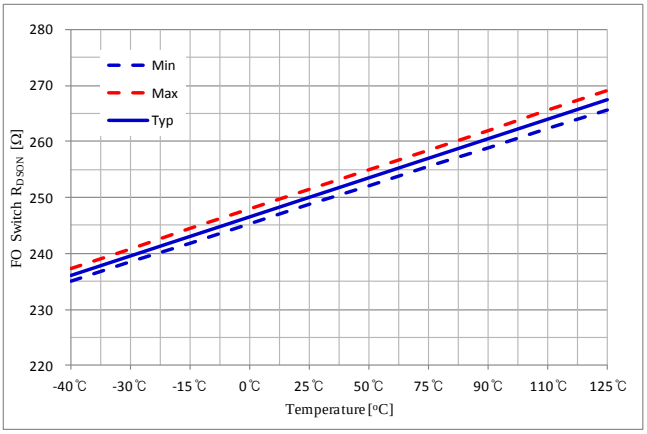


Figure 36. Fault-Out Switch R_{DSON} vs. Temperature

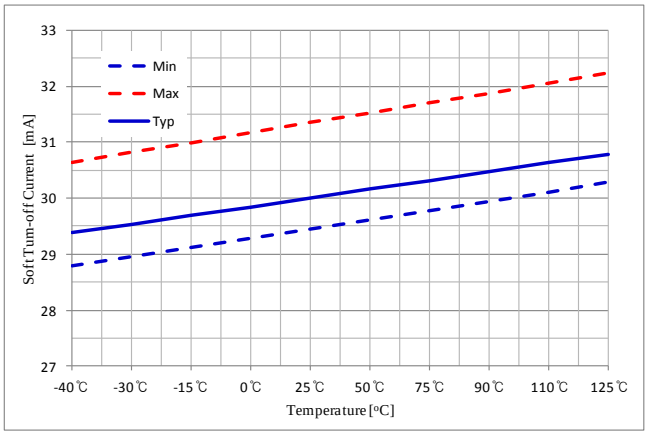


Figure 37. Soft-Off Sink Current vs. Temperature

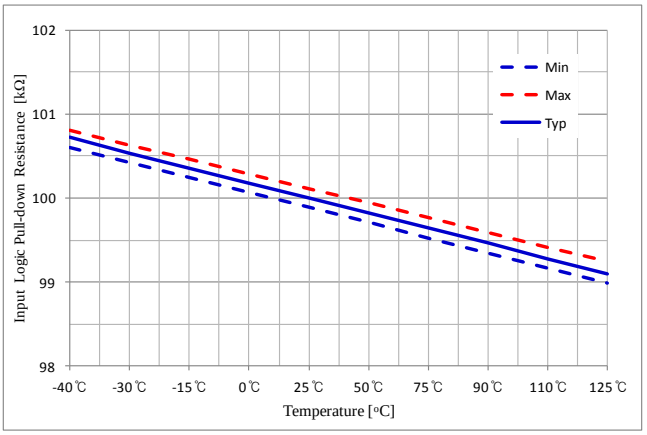


Figure 38. Input Logic Pull-down Resistance vs. Temperature

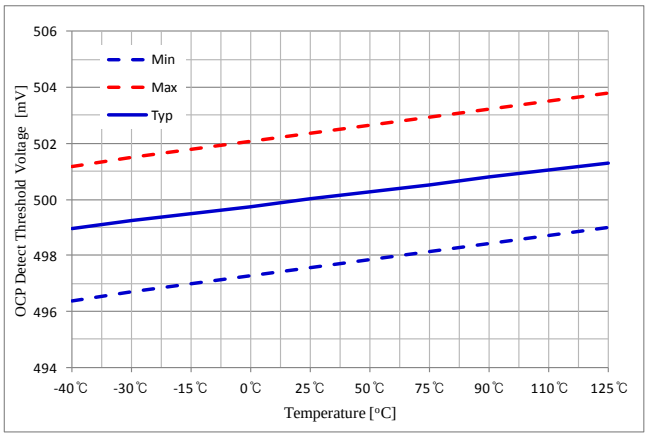


Figure 39. CIN Threshold Voltage vs. Temperature

DEFINITIONS

Input to Output Switching Time Definitions

Figure 40 shows an input to output timing diagram when external shutdown (Case-A), Under-voltage lockout (Case-B), and Over-current (Case-C) and Desaturation Protection (Case-D) events.

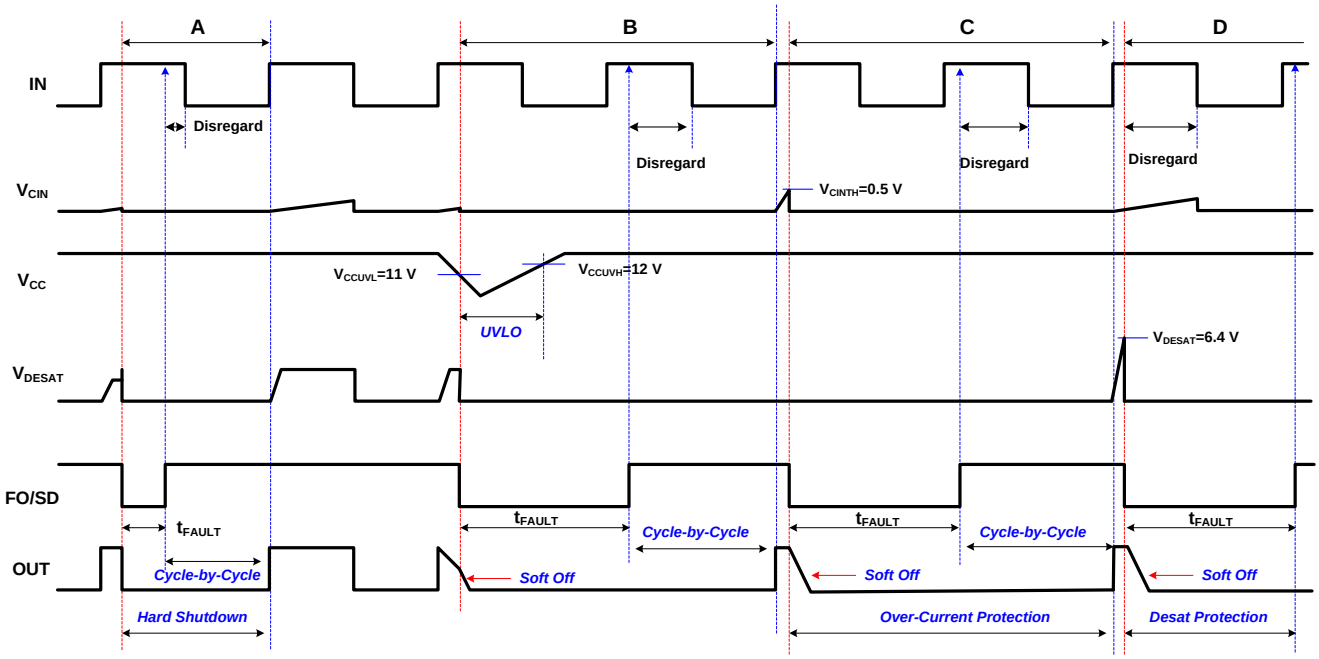


Figure 40. Overall Operating Waveforms Definitions

Switching Time Definitions

Figure 41 shows an input to output switching timing diagram. The output signal is HIGH when input signal is HIGH (Output In-phase with input signal).

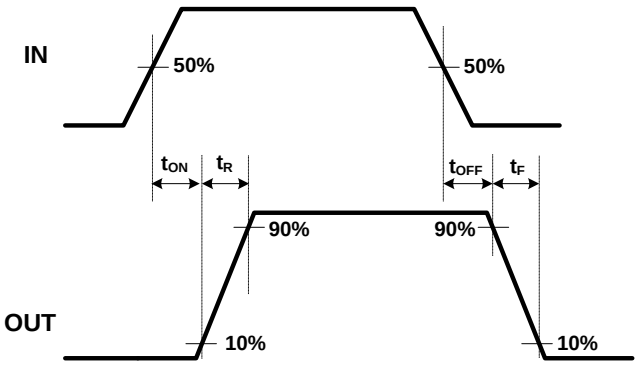


Figure 41. Switching Time Waveforms Definitions

APPLICATIONS INFORMATION

This section lists the detail about key features and operating for the FAN3181.

Input Stage

The input pins of FAN3181 gate-driver devices are based on a TTL compatible input-threshold logic that is independent of the V_{CC} supply voltage. The logic level compatible input provides a typically high threshold of 1.6 V and a typically low threshold of 1.2 V. The input impedance of the FAN3181 is 100 kΩ typically, as shown in the block diagrams. We recommends an RC filter to be added on the input pin for reducing the impact of system noise and ground bounce, the time constant of the RC filter, for example, 100 Ω with 1 nF is an acceptable choice.

Shutdown Function

The FAN3181 provide an external shutdown function when FO/SD pin voltage is below typically 1.2 V. The fault-out signal is report to the FO/SD pin and an external RC network is connected to this FO/SD pin in order to provide an adjustable gate driver disable time, which is consist the internal default fault-clear time (typically 110 µs) and shutdown time that follows the fault condition. The FAN3181 shutdown architecture allows immediate turn-off of the outputs of the gate driver in the case of fault, by minimizing the propagation delay between the fault detection event and the actual output switch-off. In fact, the time delay between the fault detection and the output turn-off is no longer dependent on the value of the external RC network connected to the FO/SD pin. In the shutdown circuitry the fault signal has a preferential path which directly switches off the outputs after the shutdown logic triggering. At the same time the internal logic turns on the open drain fault-out switch and holds it during default fault-clear time (typically 110 µs) and until the FO/SD voltage goes above the shutdown (FO/SD) logic input threshold (typically 1.6 V). When such threshold is reached, the open drain output is turned off, allowing the external pull-up to recharge the capacitor. The driver outputs restart following the input pins as soon as the voltage at the FO/SD pin reaches the higher threshold of the shutdown logic input.

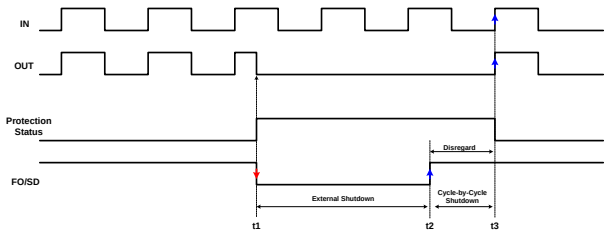


Figure 42. Timing chart of fault and shutdown

The shutdown system provides the possibility to increase the time constant of the external RC network (that determines the disable time after the fault event) up to very large values without increasing the delay time of the protection as shown in Figure 43.

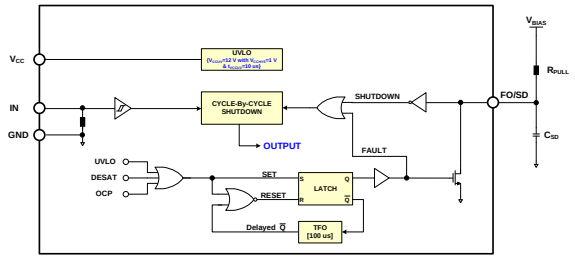


Figure 43. Application Circuit of Fault-Out

An approximation of the disable time is calculated by equation (1):

$$T_{DISABLE} = T_{FAULT} + T_{SD}$$
$$T_{SD} \cong \tau \times \ln\left(\frac{(-V_{BIAS})}{(V_{FOSDH} - V_{BIAS})}\right) \quad (1)$$

Where, T_{FAULT} = 110 µs, V_{FOSDH} = 1.6 V, $\tau = R_{PULL} \times C_{SD}$. We recommended pull-up resistance (R_{PULL}) value is 20 kΩ. The Fault Output (FO) stays in the low state until the fault condition has been removed or the fault clear time (T_{FAULT}) expires; once the fault clear timer expires, allowing the external pull-up resistor to recharge the capacitor. When FO/SD pin voltage is reached threshold, the driver outputs restart following the input signal.

Output Stage

The output stage is able to sink/source about 2.0 A/1.5 A typical at 25°C and the minimum sink/source currents over the full temperature range (-40°C / +125°C) are 1.5 A sink and 1.0 A source. Soft turn-off switch in the output drive stage will turn on to softly turn off the IGBT and prevents large di/dt induced voltages when fault conditions are occurred. This device slowly discharges the IGBT gate to prevent fast changes in collector current that could cause damaging voltage spikes due to stray inductances. During the slow turn off, the output stage device remains off.

Protection Function

FAN3181 provide the protection features include V_{CC} Under-voltage lockout (UVLO), external shutdown (Externally FO/SD pin is LOW), Over-Current Protection (OCP) or Desaturation protection and the FO/SD pin is internally pulled to GND when above mentioned fault events happened.

Fault-Out (FO) Function

FAN3181 provide the fault-out signal when V_{CC} Under-voltage lockout (UVLO), Desaturation protection or Over-current (OCP) events happened as shown in Figure 44. The fault output (FO/SD) pin stays in the low state until the fault condition has been removed and the fault clear timer ($T_{FAULT,}$ typically 110 µs) expires; once the fault clear timer expires, the voltage on the FO/SD pin will return to pull-up voltage.

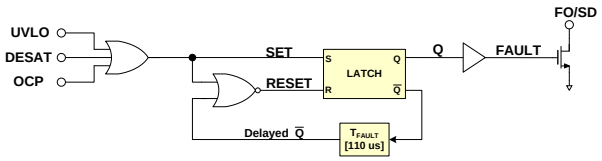
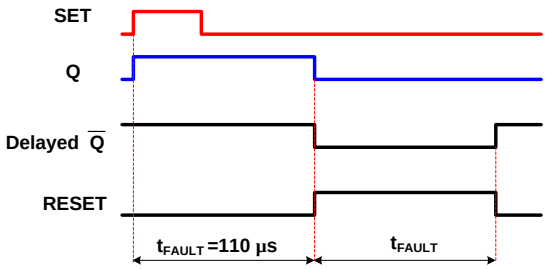
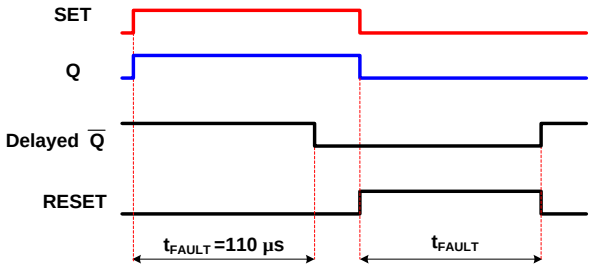


Figure 44. Functional Block of Fault-Out

If fault condition time is less than fault clear time (Case-a), the pulse width of fault-out (FO) is 110 µs. If longer (case-b), pulse width of fault-out same with fault condition time as shown in Figure 45.



(a) In case of fault condition less than t_{FAULT}



(b) In case of fault condition longer than t_{FAULT}

Figure 45. Timing Definition of Fault-Out

Under- Voltage Lockout Protection

FAN3181 provides an Under-voltage lockout (UVLO) protection circuitry that monitors the supply voltage for V_{CC}. It can be designed to prevent malfunction when V_{CC} is lower than the specified threshold voltage and supply voltage (V_{CC}) maintains an under-voltage condition over under-voltage filtering times (t_{VCCUV}, typically 10 µs).

Table 1. UVLO Conditions

Case	Condition	FO	FO	OUT
Case 1	$t_{UVLO} > t_{FAULT}$	t_{UVLO}	LOW	LOW
Case 2	$t_{UVLO} < t_{FAULT}$	t_{FAULT}	LOW	LOW
Case 3	$t_{UVLO} < t_{VCCUV}$		HIGH	HIGH
Case 4	$V_{CC} < 5$ V		X	X
Note	-. t_{FAULT}= 110 µs, t_{VCCUV} =10 µs			

If a fault condition occurs, the FO/SD Pin is internally pulled to GND and output (OUT) of the gate driver is soft turned off. The output decline linearly by the internal sink current source (I_{SOFT}=30 mA) for soft turn-off.

In case of $t_{UVLO} > t_{FAULT}$

Gate drive output is softly turn-off and Fault-Out (FO) stays in low state until fault condition has been removed when the duration of under-voltage condition (t_{UVLO}) longer than fault output (FO) time (typical 110 µs) as shown in Figure 46 The fault output (FO/SD) and gate driver output goes to low state after under-voltage filtering time (t_{VCCUV}, typically10 µs) when the V_{CC} is below the under-voltage lockout low threshold voltage.

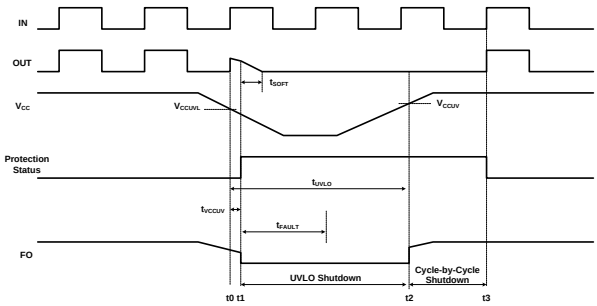


Figure 46. Timing chart of $t_{UVLO} > t_{FAULT}$ condition

In case of $t_{UVLO} < t_{FAULT}$

Gate drive output is softly turn-off and Fault-Out (FO) stays in the low state during fault-out time (typical 110 µs) when the duration of under-voltage condition (t_{UVLO}) less than fault-out time (t_{FAULT}) as shown in Figure 47.

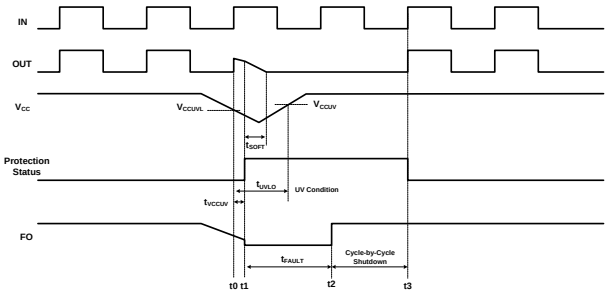


Figure 47. Timing chart of $t_{UVLO} < t_{FAULT}$ condition

Gate drive output and fault output (FO) does not change when an under-voltage duration (t_{UVLO}) less than under voltage filter time (t_{VCCUV}) as shown in Figure 48.

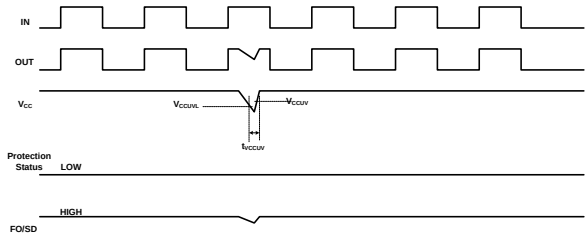


Figure 48. Timing chart of t_{UVLO} < t_{VCCUV} condition

In case of very low V_{CC} (V_{CC} < 5 V)

If V_{CC} is lower than 5 V (UVLO 1 case: t_0 ~ t_1, and t_4 ~ t_5), the fault signal cannot be driven to LOW state because V_{CC} is not enough to drive internal circuit as shown in Figure 49.

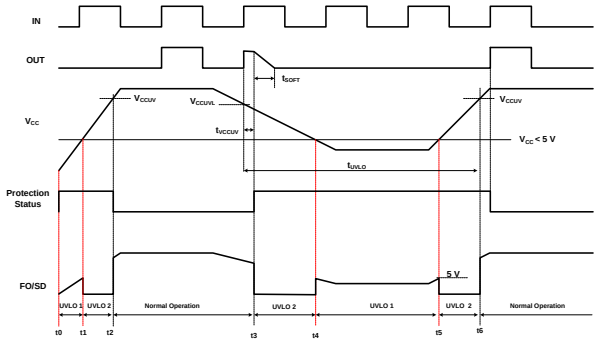


Figure 49. Timing chart of V_{CC} less than 5 V

Over-Current Protection

The CIN pin is used for sensing the current. The current sensing circuit includes a Leading Edge Blanking (LEB) time to ensure there is no nuisance tripping during device switch on (t_{CINBLT}, typically 300 ns). When the input is turned off the fault signal is cleared and the IC is reset. On the next active input signal the IC will repeat the operation described above if the over-current condition remains. Hence the over current control is on a cycle-by-cycle basis. Figure 50 shows the waveform definitions of FO, and an output of low-side driver; which uses a soft turn-off method when the current-sense pin (CIN) recognizes a fault.

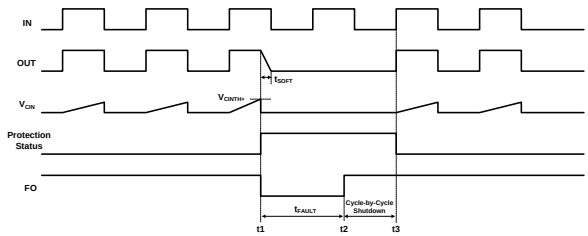


Figure 50. Timing chart of OCP Condition

Desaturation Protection

The desaturation detection technique for identifying a short circuit and fault condition in an IGBT is well known. Generally, a desaturation condition is said to exist if the voltage across the IGBT collector to emitter terminals rises above 5~8 volts while the gate to emitter voltage is high. This condition indicates that the current through the IGBT has exceeded the normal operating level. The gate drive circuit should be designed so that it reacts promptly to the short circuit and safely turns off the IGBT within Short-Circuit Withstand Time (SCWT) rating of the IGBT. However, in recent years, IGBTs have been designed with lower conduction and switching losses but this generally reduces SCWT. A desaturation fault detection circuit provides protection for power semiconductor switches (IGBT or MOSFETs) against short-circuit current events which may lead to destruction of these power switches. The IGBT collector-emitter voltage, V_{CESAT}, is monitored by the DESAT pin of the gate driver. When there is short circuit in an application and a very high current flow through the IGBT, it will go into the desaturation mode; hence its V_{CESAT} voltage will rise. A fault is detected by the gate driver (while the IGBT is on) once this V_{CESAT} voltage goes above the internal desaturation fault detection threshold voltage, which has typically 6.4 V. This fault detection triggers two events:

- Output of the gate driver is slowly brought low in order to “softly” turn off the IGBT and prevent large di/dt induced voltage spikes.
- Fault output (FO/SD) goes to low for the purpose of notifying the microcontroller of the fault condition. At this point, the microcontroller must take the appropriate action to shutdown.

Figure 51 show the desaturation protection circuit, which has 2.8 µs internal desaturation blacking timer. So that, external blank capacitor, $C_{DESAT,}$ is not needed for blanking time less than 2.8 µs.

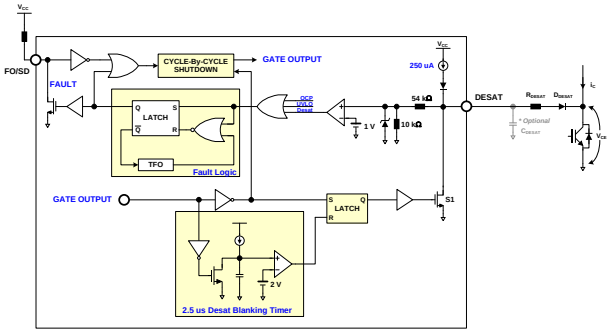


Figure 51. Desaturation Detection Circuit

Consider of Blanking Time

The DESAT fault detection circuitry should remain disabled for a short time period following the turn-on of the IGBT to allow the collector voltage to fall below the DESAT threshold. The time period, called the DESAT blanking time, ensures that there is no nuisance tripping during IGBT turn-on. This time also represents the time it takes for the driver to detect a fault condition. For typical applications, the two external components required to build the DESAT circuit are the DESAT diode, D_{DESAT}, and DESAT resistor, R_{DESAT} and default blanking time has typically 2.8 µs. Also, it is possibile to increase the blanking time by adding an external blank capacitor, C_{DESAT}. During operation, blank capacitor is discharged when the driver output is low (IGBT off). That is, the DESAT detection features becomes active only when the output of the gate driver is in the high state, driving the IGBT into saturation. When the IGBT is turned on, the DESAT capacitor starts charging and protection becomes effective only if the DESAT threshold is exceeded after the blanking time.

Consider of DESAT Resistor (R_{DESAT})

Switching inductive loads causes large instantaneous forward voltage transients across the freewheeling diodes of IGBTs. These transients result in large negative voltage spikes on the DESAT pin which draw substantial current out of the device. To limit the current level drawn from the gate driver, a DESAT resistor (R_{DESAT}) can be added in series with the DESAT diode (D_{DESAT}). The added resistor will not appreciably alter the DESAT threshold or the blanking time. The DESAT resistance value is chosen considering the V_{CESAT} of IGBT, forward voltage drop of DESAT diode, and threshold voltage of DESAT comparator. The sum of V_{CESAT} of IGBT and total voltage drop of DESAT diode and resistor must be less than threshold voltage of DESAT comparator.

$$(V_{DESAT} - 1.5) \geq (V_{CESAT} + (R_{DESAT} \times I_{DESAT}) + V_D) \quad (2)$$

Where, V_{CESAT} is saturation voltage of IGBT at maximum operating temperature and V_D is voltage forward drop of DESAT diode. The output voltage is soft turned off and FO/SD goes to LOW state when the V_{DESAT} voltage goes higher than specified threshold voltage (typically 6.4 V) as shown in Figure 52.

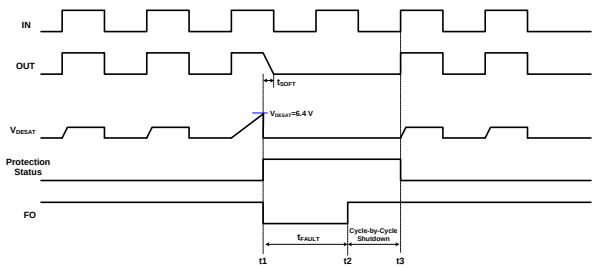


Figure 52. Waveform Definition of Desaturation

Active Miller Clamp

Any change in the collector-emitter voltage (V_{CE}) causes a displacement current (Miller current) through the Miller capacitance (C_{GC}). The value of the current is calculated approximately from the product of the magnitude of the Miller capacitance and the rate of change of the collector-emitter voltage.

$$i_{GC} = C_{GC} \frac{dv_{CE}}{dt} \quad (3)$$

The displacement current i_{GC} increases the voltage at the gate-emitter capacitance (C_{GE}) and thus the gate-emitter voltage V_{GE}' of the IGBT. The amplitude of the voltage depends on the capacitive voltage divider of the internal semiconductor capacitances C_{GC} and C_{GE}, the internal gate resistance RGint, and the gate's external circuitry. Once the gate-emitter voltage V_{GE}' reaches the threshold voltage, the IGBT begins to change into the conductive state. A cross-current begins to flow in the phase leg, causing additional losses in both the IGBTs of the bridge leg concerned. (This phenomenon is also known as Miller-induced shoot-through). Neglecting the parasitic inductances in the gate circuit it reduces the equivalent circuit diagram of the feedback circuit to the RC-network shown in Figure 53. Once the IGBT is in steady state and the change of the collector-emitter voltage is constant, the gate-emitter voltage V_{GEint} caused by the displacement current depends on the sum of the gate resistor values and the internal driver resistance ($R_{GES} = R_{Gext} + R_{Gint} + R_D$). The larger the summed resistance, the larger the gate-emitter voltage ($V_{GEint} = R_{GES} \cdot i_{GC}$). The gate-emitter voltage time function is determined by the time constant of the RC-network connected. The larger the capacitances of the network, the longer it takes for the steady state to arrive.

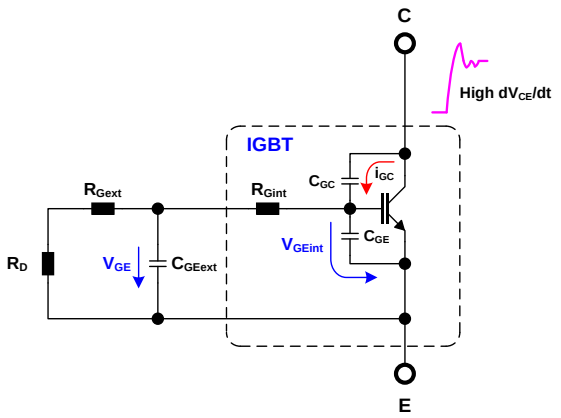


Figure 53. Equivalent circuit of the gate drive

The FAN3181 has an active Miller clamp function to prevent IGBT to turn on due to high collector-to-emitter dv/dt induced during the switching sequence, the GS pin is connected to IGBT gate and Miller current is sinking through a low impedance CLAMP switch. The CLAMP switch is opened when the input is high state and is

closed when the actual gate voltage goes to below Clamp threshold voltage (Typically 1.5 V) during turn-off. In this way, the CLAMP function doesn't affect the turn-off characteristic, but only keeps the gate output low during the off time as shown in Figure 54.

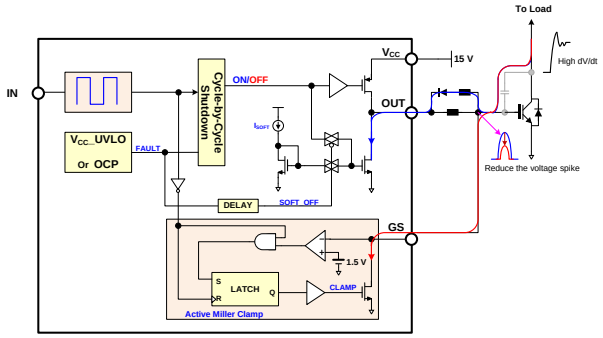


Figure 54. Schematic of Active Miller Clamp

The waveform shown in Figure 55 proves how using the Active Miller Clamp provides a consistent reduction of the voltage spike on MOSFET/IGBT gate cause by dV/dt when gate turn-off.

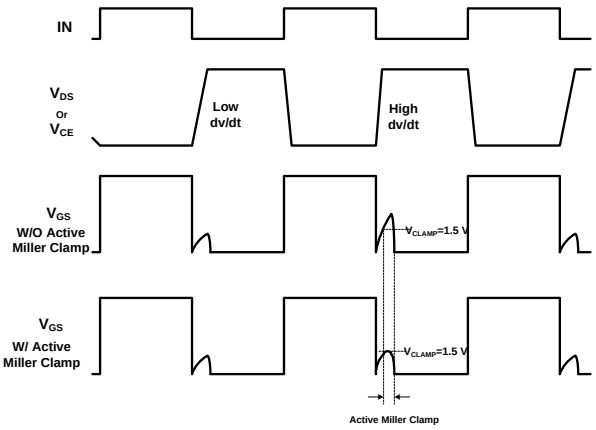


Figure 55. Waveform Definition of Active Miller Clamp

The Miller CLAMP circuit is designed for Miller current typically 1.0 A. When the IGBT is turned-off and the gate driving voltage below 1.5 V the CLAMP current output is activated as shown in Figure 56.

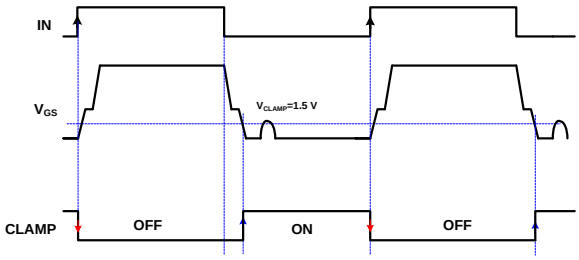


Figure 56. Waveform of Active Miller Clamp

PCB Layout Guideline

To improve the switching characteristics and efficiency of design, the following should be considered before beginning a PCB layout.

- Should be minimize influence of the parasitic inductance and capacitance on the layout.
- The bypass capacitor for V_{CC} should be placed as close as possible to the V_{CC} pin.
- The gate driver should be located switching device as close as possible to gate driver.
- A RC filter with 51 Ω to 100 Ω and 1 nF for IN pin is recommended.

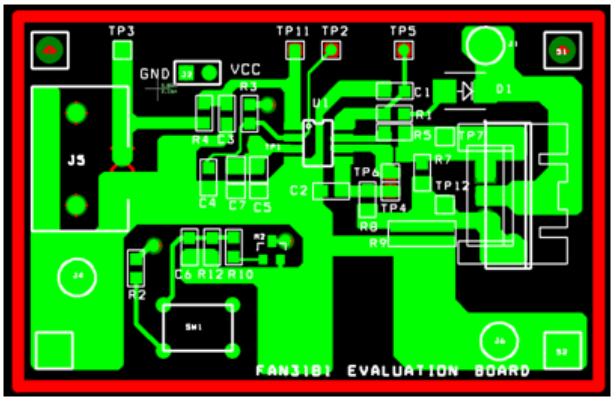


Figure 57. Top View

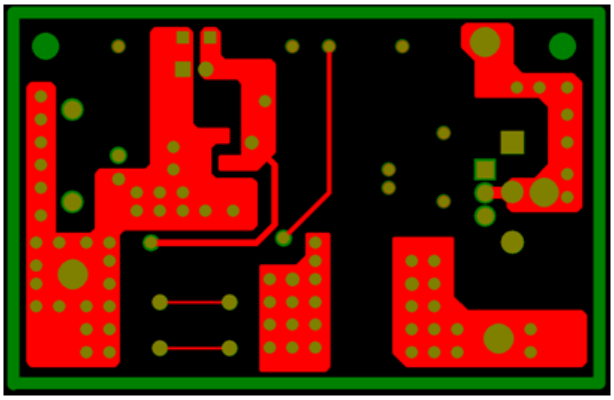
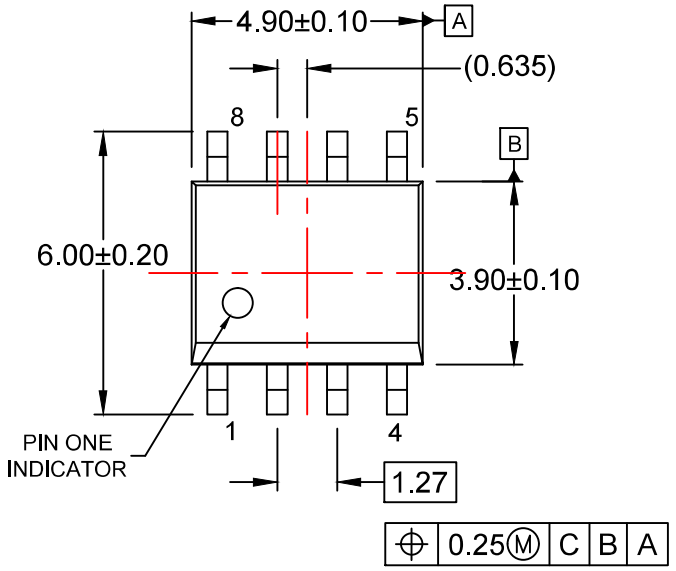
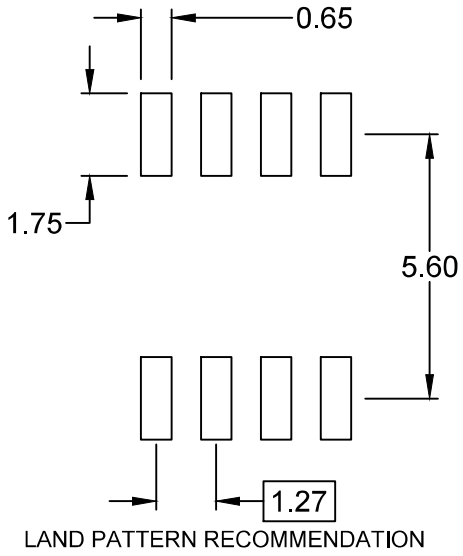
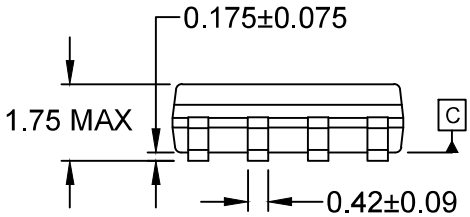


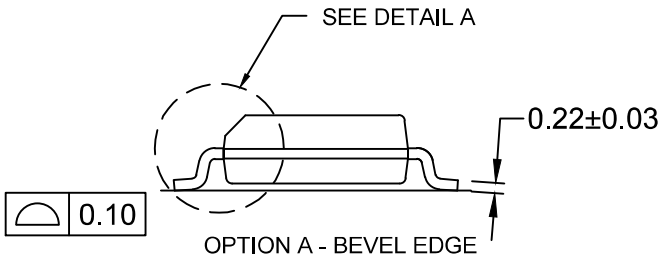
Figure 58. Bottom View



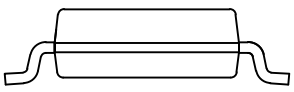


LAND PATTERN RECOMMENDATION

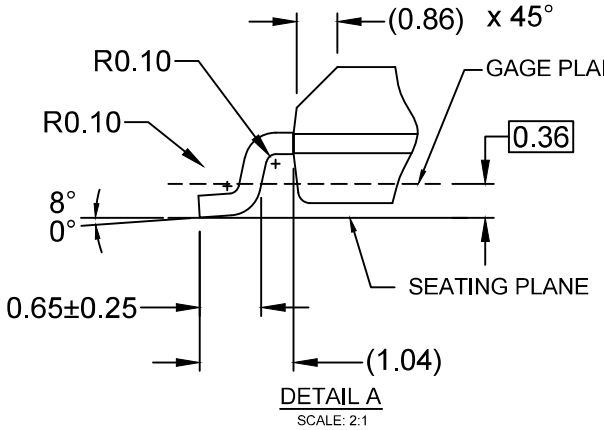




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M
E) DRAWING FILENAME: M08Arev16

FAIRCHILD.

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