FAN5240

Multi-Phase PWM Controller for AMD Mobile Athlon™ and Duron™

Features

- CPU Core power: 0.925V to 2.0V output range
- ±1% reference precision over temperature
- Dynamic voltage setting with 5-bit DAC
- 5V to 24V input voltage range
- 2 phase interleaved switching
- Active droop to reduce output capacitor size
- Differential remote voltage sense
- High efficiency:
  >90% efficiency over wide load range
  >80% efficiency at light load
- Excellent dynamic response with Voltage Feed-Forward and Average Current Mode control
- Dynamic duty cycle clamp minimizes inductor current build up
- Lossless current sensing on low-side MOSFET or Precision current sensing using sense resistor
- Fault protections: Over-voltage, Over-current, and Thermal Shut-down
- Controls: Enable, Forced PWM, Power Good, Power Good Delay
- QSOP28, TSSOP28

Applications

- AMD Mobile Athlon™ CPU V_{CORE} Regulator
- AMD Mobile Duron™ CPU V_{CORE} Regulator

General Description

The FAN5240 is a single output 2-Phase synchronous buck controller to power AMD's mobile CPU core. The FAN5240 includes a 5-bit digital-to-analog converter (DAC) that adjusts the core PWM output voltage from 0.925VDC to 2.0VDC, which may be changed during operation. Special measures are taken to allow the output to transition with controlled slew rate to comply with AMD's Power Now™ technology. The FAN5240 includes a precision reference, and a proprietary architecture with integrated compensation providing excellent static and dynamic core voltage regulation. The regulator includes special circuitry which balances the 2 phase currents for maximum efficiency.

At light loads, when the filter inductor current becomes discontinuous, the controller operates in a hysteretic mode, dramatically improving system efficiency. The hysteretic mode of operation can be inhibited by the FPWM control pin.

The FAN5240 monitors the output voltage and issues a PGOOD (Power-Good) when soft start is completed and the output is in regulation. A pin is provided to add delay to PGOOD with an external capacitor.

A built-in over-voltage protection (OVP) forces the lower MOSFET on to prevent the output from exceeding a set voltage. The PWM controller's overcurrent circuitry monitors the converter load by sensing the voltage drop across the lower MOSFET. The overcurrent threshold is set by an external resistor. If precision overcurrent protection is required, an optional external current-sense resistor may be used.

Typical Application

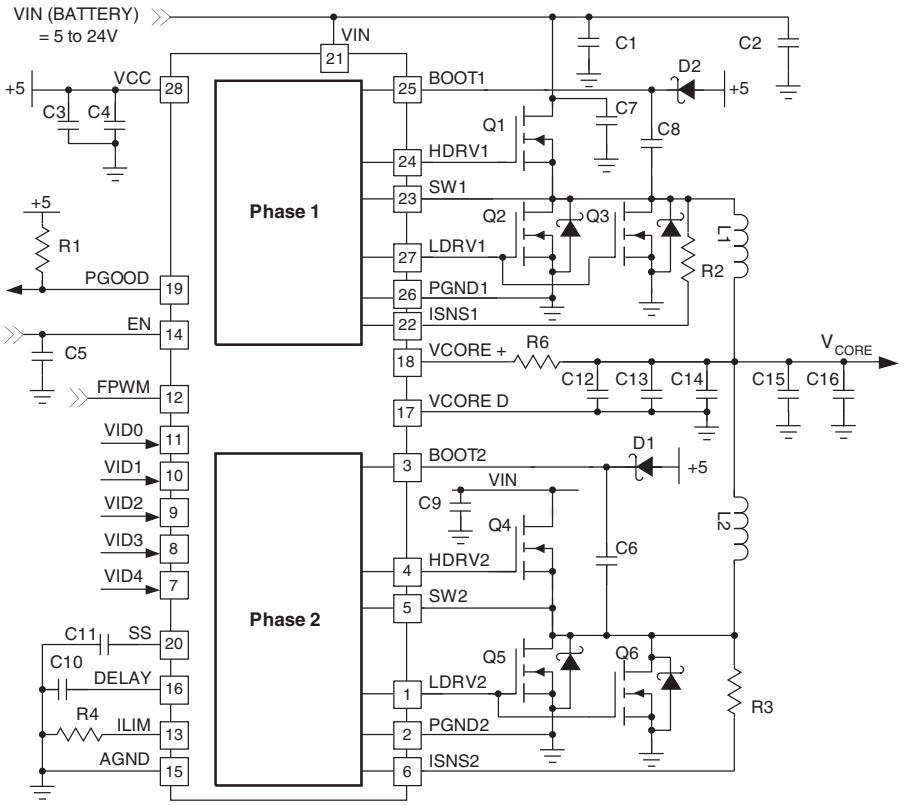
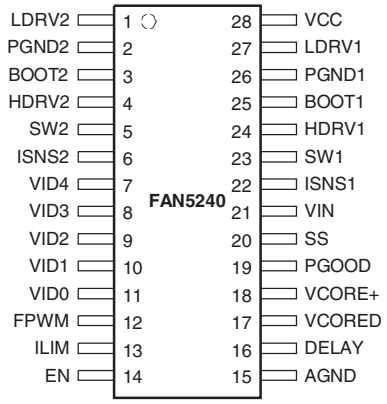


Figure 1. AMD Mobile Athlon/Duron CPU Core Supply

Table 1. BOM for Figure 1

Description	Qty	Ref.	Vendor	Part Number
Capacitor 22µF, Ceramic X7R 25V	2	C1, C2	TDK	
Capacitor 1µF, Ceramic	3	C3,C7,C9	Any	
Capacitor 0.1µF, Ceramic	6	C4–C6, C8, C11, C12	Any	
Capacitor 0.22µF, Ceramic	1	C10	Any	
Capacitor 270µF, 2V, ESR 15mΩ	4	C13–C16	Panasonic	EEFUE0D271R
10KΩ, 5% Resistor	2	R1	Any	
1KΩ, 1% Resistor	1	R2, R3, R6	Any	
56.2KΩ, 1% Resistor	2	R4	Any	
Schottky Diode 40V	2	D1, D2	Fairchild	MBR0540
Inductor 1.6µH, 20A, 2.4mΩ	1	L1, L2	Panasonic	ETQP6F0R8LFA
N-Channel SO-8 MOSFET, 11mΩ	1	Q1, Q4	Fairchild	FDS6694
N-Channel SO-8 SyncFET™ MOSFET, 6mΩ	1	Q2, Q3, Q5, Q6	Fairchild	FDS6676S

Pin Configuration



QSOP-28 or TSSOP-28

θ_{JA} = 90°C/W

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1 27	LDRV2 LDRV1	**Low-Side Drive.** The low-side (lower) MOSFET driver output.
2 26	PGND2 PGND1	**Power Ground.** The return for the low-side MOSFET driver.
3 25	BOOT2 BOOT1	**BOOT.** The positive supply for the upper MOSFET driver. Connect as shown in Figure 1.
4 24	HDRV2 HDRV1	**High-Side Drive.** The high-side (upper) MOSFET driver output.
5 23	SW2 SW1	**Switching node.** The return for the high-side MOSFET driver.
6 22	ISNS2 ISNS1	**Current Sense input.** Monitors the voltage drop across the lower MOSFET or external sense resistor for current feedback.
7 - 11	VID4 - VID0	**Voltage Identification Code.** Input to VID DAC. Sets the output voltage according to the codes set as defined in Table 2. These inputs have 1µA internal pull-up.
12	FPWM	**Forced PWM mode.** When logic high, inhibits the chip from entering hysteretic operating mode. If tied low, hysteretic mode will be allowed.
13	ILIM	**Current Limit.** A resistor from this pin to GND sets the current limit.
14	EN	**ENABLE.** This pin enables IC operation when either left open, or pulled up to VCC. Toggling EN will also reset the chip after a latched fault condition.
15	AGND	**Analog Ground.** This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin.
16	DELAY	**Power Good / Over-Current Delay.** A capacitor to GND on this pin delays the PGOOD from going high as well delaying the over-current shutdown.
18 17	VCORE+ VCORE–	**VCORE Output Sense.** Differential sensing of the output voltage. Used for regulation as well as PGOOD, under-voltage and over-voltage protection and monitoring. A resistor in series with this VCORE+ sets the output voltage droop.
19	PGOOD	**Power Good Flag.** An open-drain output that will pull LOW when the core output below 825mV. PGOOD delays its low to high transition for a time determined by CDELAY when VCORE rises above 875mV.

Pin Definitions (continued)

Pin Number	Pin Name	Pin Function Description
20	SS	**Soft Start.** A capacitor from this pin to GND programs the slew rate of the converter during initialization as well as in operation. This pin is used as the reference against which the output is compared. During initialization, this pin is charged with a 25µA current source. Once this pin reaches 0.5V, its function changes, and it assumes the value of the voltage as set by the VID programming. The current driving this pin is then limited to ±500µA, that together with C_{SS} sets a controlled slew rate for VID code changes.
21	VIN	**Input voltage from battery.** This voltage is used by the oscillator for feed-forward compensation of input voltage variation.
28	VCC	**VCC.** This pin powers the chip. The IC starts to operate when voltage on this pin exceeds 4.6V (UVLO rising) and shuts down when it drops below 4.3V (UVLO falling).

Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Parameter	Min.	Typ.	Max.	Units
VCC Supply Voltage:			6.5	V
VIN			27	V
BOOT, SW, HDRV Pins			33	V
BOOT to SW			6.5	V
All Other Pins	–0.3		VCC+0.3	V
Junction Temperature (T_J)	–10		150	°C
Storage Temperature	–65		150	°C
Lead Soldering Temperature, 10 seconds			300	°C

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCC		4.75	5	5.25	V
Supply Voltage VIN		6		24	V
Ambient Temperature (T_A)		–20		85	°C

Electrical Specifications

(VCC = 5V, VIN = 6V–24V, and T_A = recommended operating ambient temperature range using circuit of Figure 1, unless otherwise noted.)

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supplies					
VCC Current	Operating, C_L = 10pF			2	mA
	Shut-down (EN=0)		1	10	µA
VIN Current	Operating			25	µA
	Shut-down (EN=0)			1	µA
UVLO Threshold	Rising VCC	4.3	4.45	4.6	V
	Falling VCC	3.8	3.95	4.10	V
Regulator / Control Functions					
Output voltage	per Table 2	0.925		2.00	V
Error Amplifier Gain			86		dB
Error Amplifier GBW			2.7		MHz
Error Amplifier Slew Rate			1		V/µS
VCORE+ Input Current		25	30	35	µA
ILIM Voltage	R_{ILIM} = 30KΩ	0.89		0.91	V
ILIM $T_{HOLDOFF}$	C_{DELAY} = 22nF		1.16		mS
Over-voltage Threshold		2.2	2.35	2.5	V
Over-voltage Protection delay			2		µS
EN, input threshold	Logic LOW			0.8	V
	Logic HIGH	2			V
Phase to Phase current mismatch	IC contribution only Guaranteed by design			±5	%
Over-Temperature Shut-down			150		°C
Over-Temperature Hysteresis			25		°C
Output Drivers (note 1)					
HDRV Output Resistance	Sourcing		3.8	5	Ω
	Sinking		1.6	3	Ω
LDRV Output Resistance	Sourcing		3.8	5	Ω
	Sinking		0.8	1.5	Ω
Oscillator					
Frequency		255	300	345	KHz
Ramp Amplitude, pk–pk	VIN = 16V		2		V
Ramp Offset			0.5		V
Ramp Gain	$\frac{RampAmplitude}{V_{IN}}$		125		mV/V
Reference, DAC and Soft-Start					
VID input threshold	Logic LOW			0.8	V
	Logic HIGH	2.0			V
VID pull-up current	to VCC		1		µA
DAC output accuracy		–1		1	%
Soft Start Charging current (I_{SS})	V_{SS} < 90% of Programmed output	20	27	34	µA
	V_{SS} > 90% of Programmed output	350	500	650	µA

Note 1: Guaranteed by slew rate testing.

Electrical Specifications (continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
PGOOD					
VCORE Lower Threshold	Falling Edge	800	825	850	mV
	Rising Edge	850	875	900	mV
PGOOD Output Delay	Low to High, C_{DELAY} = 22nF		12		mS
PGOOD Output Low	I_{PGOOD} = 4mA			0.5	V
Leakage Current	V_{PULLUP} = 5V			1	µA

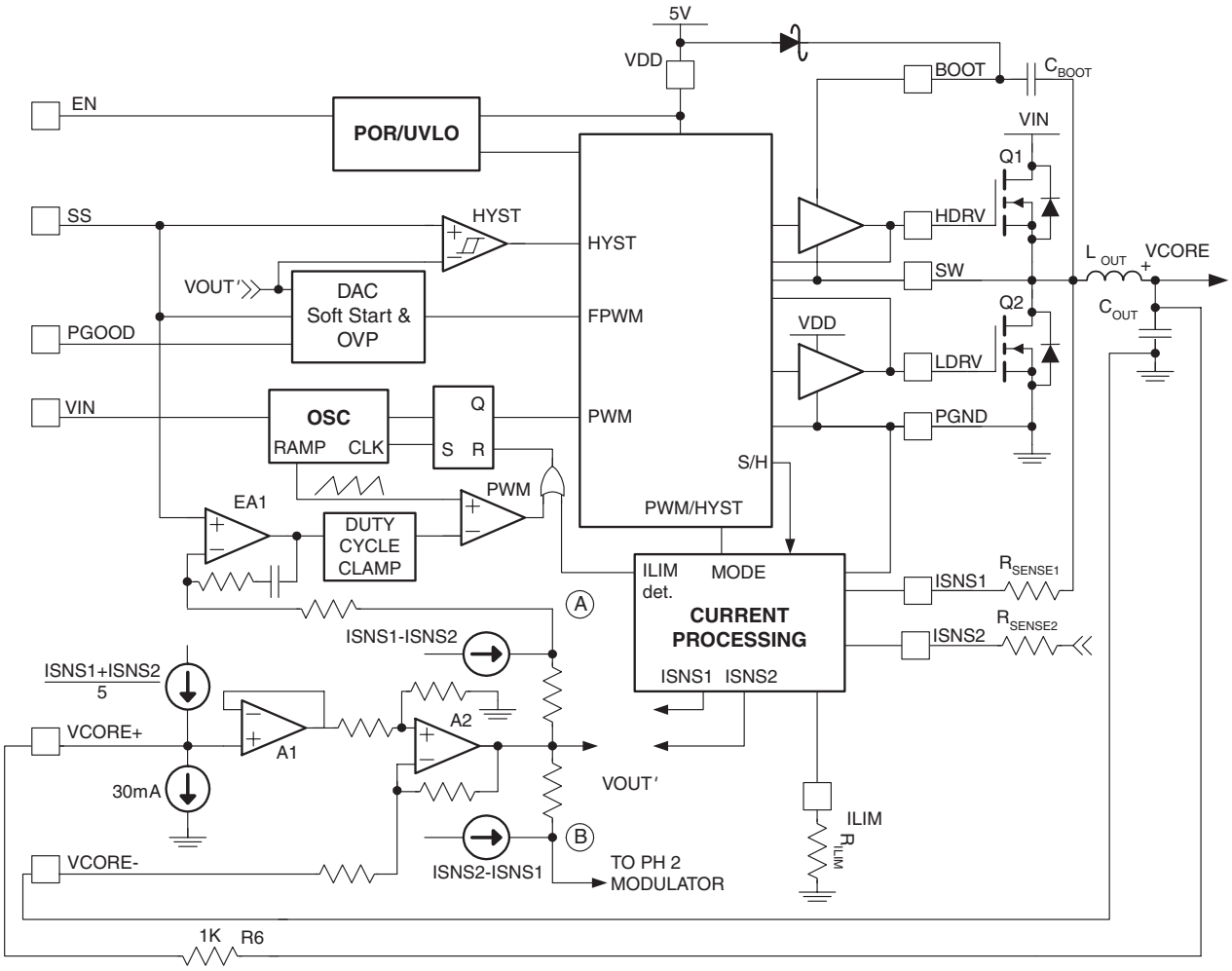


Figure 2. IC Block Diagram

Circuit Description

Overview

The FAN5240 is a 2-phase, single output power management IC, which supplies the low-voltage, high-current power to modern processors for notebook PCs. Using very few external components, the IC controls a precision programmable synchronous buck converter driving external N-Channel power MOSFETs. The output voltage is adjustable from 0.925V to 2.0V by changing the DAC (VID) code settings (see Table 2). The output voltage of the core converter can be changed on-the-fly with programmable slew rate, which meets a key requirement of AMD's Mobile Athlon/Duron™ processors.

The converter can operate in two modes: fixed frequency PWM, and variable frequency hysteretic depending on the load. At loads lower than the point where filter inductor current becomes discontinuous, hysteretic mode of operation is activated. Switchover from PWM to hysteretic operation at light loads improves the converter's efficiency and prolongs battery run time. As the filter inductor resumes continuous current, the PWM mode of operation is restored.

Output Voltage Programming

The output voltage of the converter is programmed by an internal DAC in discrete steps of 25mV from 0.925V to 1.300V and then in 50mV steps from 1.300V to 2.00V:

Table 2. Output voltage VID

VID4	VID3	VID2	VID1	VID0	VOUT to CPU
1	1	1	1	1	0.000
1	1	1	1	0	0.925
1	1	1	0	1	0.950
1	1	1	0	0	0.975
1	1	0	1	1	1.000
1	1	0	1	0	1.025
1	1	0	0	1	1.050
1	1	0	0	0	1.075
1	0	1	1	1	1.100
1	0	1	1	0	1.125
1	0	1	0	1	1.150
1	0	1	0	0	1.175
1	0	0	1	1	1.200
1	0	0	1	0	1.225
1	0	0	0	1	1.250
1	0	0	0	0	1.275
0	1	1	1	1	0.000
0	1	1	1	0	1.300
0	1	1	0	1	1.350
0	1	1	0	0	1.400
0	1	0	1	1	1.450
0	1	0	1	0	1.500
0	1	0	0	1	1.550
0	1	0	0	0	1.600
0	0	1	1	1	1.650
0	0	1	1	0	1.700
0	0	1	0	1	1.750
0	0	1	0	0	1.800
0	0	0	1	1	1.850
0	0	0	1	0	1.900
0	0	0	0	1	1.950
0	0	0	0	0	2.000

1 - Logic High or open, 0 = Logic Low

VID0–4 pins will assume a logic 1 level if left open as each input is pulled up with a 1µA internal current source.

Initialization, Soft Start and PGOOD

Assuming EN is high, FAN5240 is initialized when power is applied on VCC. Should VCC drop below the UVLO threshold, an internal Power-On Reset function disables the chip.

The IC attempts to regulate the VCORE output according to the voltage that appears on the SS pin (V_{SS}). During start-up of the converter, this voltage is initially 0, and rises linearly to 90% of the VID programmed voltage via the current supplied to C_{SS} by the 25µA internal current source. The time it takes to reach this threshold is:

$$T_{90\%} = \frac{0.9 \times V_{VID} \times C_{SS}}{25} \quad (1)$$

where $T_{90\%}$ is in seconds if C_{SS} is in µF.

At that point, the current source changes to 500µA, which establishes the slew rate of voltage changes at the output in response to changes in VID.

This dual slope approach helps to provide safe rise of voltages and currents in the converters during initial start-up and at the same time sets a controlled speed of the core voltage change when the processor commands to do so.

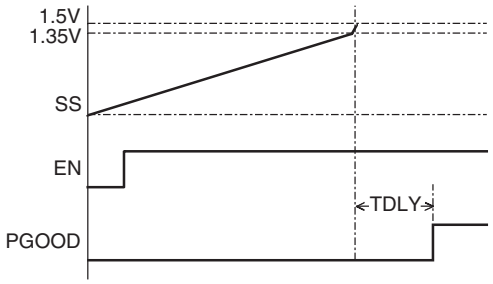


Figure 3. Soft-Start function

C_{SS} typically is chosen based on the slew rate desired in response to a VID change. For example, if the spec requires a 500mV step to occur in 100µS:

$$C_{SS} = \frac{I_{SS}}{\Delta V_{DAC}} \Delta t = \left(\frac{500\mu A}{500mV}\right) 100\mu S = 0.1\mu F \quad (2)$$

Assuming VID is set to 1.5V, with this value of C_{SS} , the time for the output voltage to rise to 0.9 of V_{VID} is found using equation 1:

$$T_{90\%} = \frac{1.35V \times 0.1}{25} = 5.4mS$$

The transition from 90% VID to 100% VID occupies 0.5% of the total soft-start time, so TSS is essentially $T_{90\%}$.

The PGOOD delay (TDLY, Figure 3) can be programmed with a capacitor to GND on pin 16 (C_{DELAY}):

$$C_{DELAY}(\text{in nF}) = 1.8 \times TDLY(\text{in mS}) \quad (3)$$

For 12mS of TDLY, C_{DELAY} = 22nF.

C_{DELAY} is typically chosen to provide 1mS of "blanking" for the over-current shut-down (**see Over-Current Sensing**, on page 12).

The following conditions set the PGOOD pin low:

1. Under-voltage - VCORE is below a fixed voltage.
2. Chip shut-down due to over-temperature or over-current as defined below.

Converter Operation (see Figure 2)

At nominal current the converter operates in fixed frequency PWM mode. The output voltage is compared with a reference voltage set by the DAC, which appears on the SS pin. The derived error signal is amplified by an internally compensated error amplifier and applied to the inverting input of the PWM comparator. To provide output voltage droop for enhanced dynamic load regulation, a signal proportional to the output current is added to the voltage feedback signal at the + input of A1. Since the processor specifies a +100mV/-50mV tolerance on VCORE, a fixed positive offset of 30 mV is created with a 30µA current source and external 1K resistor. Phase load balancing is accomplished by adding a signal proportional to the difference of the two phase currents before the error amplifier (at nodes A and B). This feedback scheme in conjunction with a PWM ramp proportional to the input voltage allows for fast and stable loop response over a wide range of input voltage and output current variations. For the sake of efficiency and maximum simplicity, the current sense signal is derived from the voltage drop across the lower MOSFET during its conduction time. This current sense signal is used to set droop levels as well as for phase balancing and current limiting.

The PWM controller has a built-in duty cycle clamp in the path from the error amplifier to the PWM comparator. During a severe load step, the output signal from the error amp can go to its rail, pushing the duty cycle to almost 100% for a significant amount of time. This could cause a severe rise in the inductor current, especially at high battery voltage, and lead to a long recovery time or even failure of the converter. To prevent this, the output of the error amplifier is clamped to a fixed value after two clock cycles if a large output voltage excursion is detected. Sensitivity of this circuit is set in such a way as not to affect the PWM control during transients normally expected from the load.

Operation Mode Control

The mode-control circuit changes the converter's mode of operation from PWM to Hysteretic and visa versa, based on the voltage polarity of the SW node when the lower MOSFET is conducting and just before the upper MOSFET turns on. For continuous inductor current, the SW node is negative when the lower MOSFET is conducting and the converters operate in fixed-frequency PWM mode as shown in Figure 4. This mode of operation achieves high efficiency at nominal load. When the load current decreases to the point where the inductor current flows through the lower MOSFET in the 'reverse' direction, the SW node becomes positive, and the mode is changed to hysteretic, which achieves higher efficiency at low currents by decreasing the effective switching frequency.

To prevent accidental mode change or "mode chatter" the transition from PWM to Hysteretic mode occurs when the SW node is positive for eight consecutive clock cycles (see Figure 4). The polarity of the SW node is sampled at the end of the lower MOSFET's conduction time. At the transition between PWM and hysteretic mode both the upper and lower MOSFETs are turned off. The phase node will 'ring' based on the output inductor and the parasitic capacitance on the phase node and settle out at the value of the output voltage.

The boundary value of inductor current, where current becomes discontinuous, can be estimated by the following expression.

$$I_{LOAD(DIS)} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{2F_{SW}L_{OUT}V_{IN}} \quad (4)$$

Hysteretic Mode

Conversely, the transition from Hysteretic mode to PWM mode occurs when the SW node is negative for 8 consecutive cycles.

A sudden increase in the output current will also cause a change from hysteretic to PWM mode. This load increase causes an instantaneous decrease in the output voltage due to the voltage drop on the output capacitor ESR. If the load causes the output voltage (as presented at VSNS) to drop below the hysteretic regulation level (20mV below VREF), the mode is changed to PWM on the next clock cycle. This insures the full power required by the increase in output current.

In hysteretic mode, the PWM comparator and the error amplifier that provide control in PWM mode are inhibited and the hysteretic comparator is activated. In hysteretic mode the low side MOSFET is operated as a synchronous rectifier, where the voltage across $V_{DS(ON)}$ is monitored, and its gate switched off when $V_{DS(ON)}$ goes positive (current flowing back from the load) blocking reverse conduction

The hysteretic comparator initiates a PFM signal to turn on HDRV when the output voltage (at VSNS) falls below the lower threshold (10mV below VREF) and terminates the PFM signal when VSNS rises over the higher threshold (5mV above VREF).

The switching frequency is primarily a function of:

1. Spread between the two hysteretic thresholds
2. I_{LOAD}
3. Output Inductor and Capacitor ESR

A transition back to PWM (Continuous Conduction Mode or CCM) mode occurs when the inductor current rises sufficiently to stay positive for 8 consecutive cycles. This occurs when:

$$I_{LOAD(CCM)} = \frac{\Delta V_{HYSTERESIS}}{2\ ESR} \quad (5)$$

where $\Delta V_{HYSTERESIS}$ = 15mV and ESR is the equivalent series resistance of C_{OUT}.

Because of the different control mechanisms, the value of the load current where transition into CCM operation takes place is typically higher compared to the load level at which transition into hysteretic mode occurs.

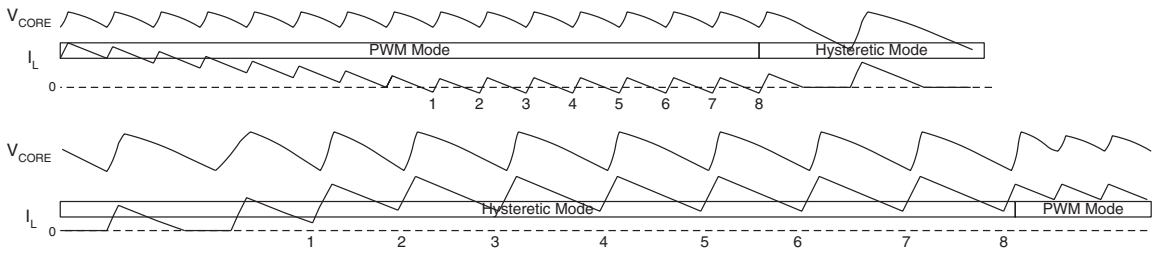


Figure 4. Transitioning between PWM and Hysteretic Mode

Current Processing Section

The following discussion refers to Figure 6.

Setting RSENSE

Each phase current is sampled about 200nS after the SW node crosses 0V. For proper converter operation, choose an RSENSE value of:

$$R_{SENSE} = \frac{R_{DS(ON)} \bullet I_{MAX}}{40\mu A}$$

which is about 1K for the components in Figure 1.

Active Droop

The core converter incorporates a proprietary output voltage droop method for optimum handling of fast load transients found in modern processors.

"Active droop" or voltage positioning is now widely used in the computer power applications. The technique is based on raising the converter voltage at light load in anticipation of a step increase in load current, and conversely, lowering VCORE in anticipation of a step decrease in load current.

With Active Droop, the output voltage varies with the load as if a resistor were connected in series with the converter's output, in other words, it's effect is to raise the output resistance of the converter.

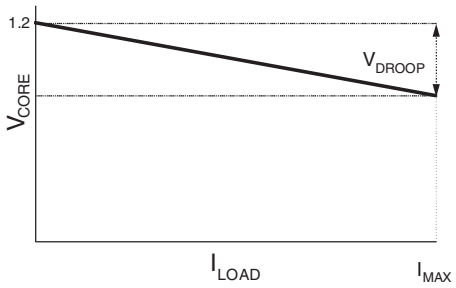


Figure 5. Active Droop

To get the most from the Active Droop, its magnitude should be scaled to match the output capacitor's ESR voltage drop.

$$V_{DROOP} = I_{MAX} \times ESR \quad (6)$$

Active Droop allows the size and cost of the output capacitors required to handle CPU current transients to be reduced. The reduction may be almost a factor of 2 when compared to a system without Active Droop.

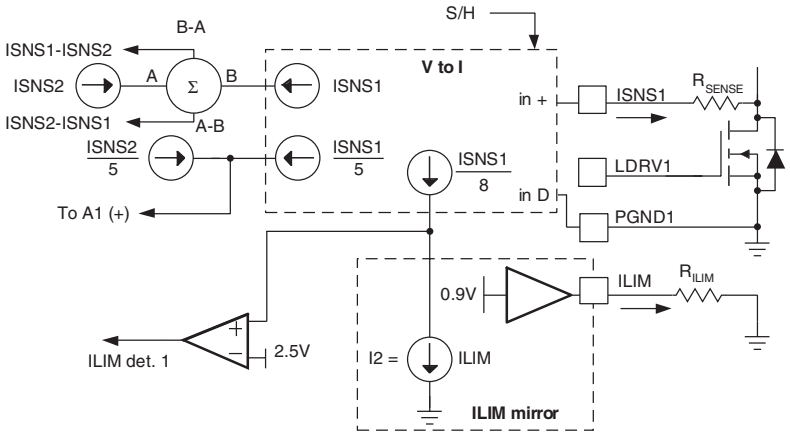


Figure 6. Current Limit and Active Droop Circuits

Additionally, the CPU power dissipation is also slightly reduced as it is proportional to the applied voltage squared and even slight voltage decrease translates to a measurable reduction in power dissipated.

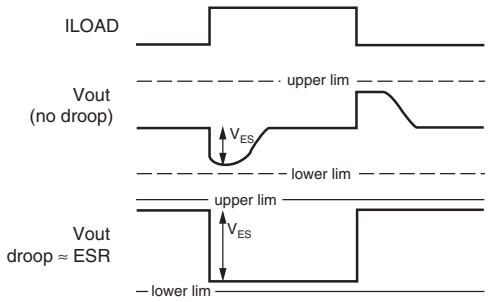


Figure 7. Effect of Active Droop on ESR

The processor regulation window including transients is specified as +100mV..–50mV. To accommodate the droop, the output voltage of the converter is raised by about 30mV at no load.

The converter response to the load step is shown in Figure 8. At zero load current, the output voltage is raised ~30mV above nominal value of 1.5V. When the load current increases, the output voltage droops down approximately 55mV. Due to use of Active Droop, the converter's output voltage adaptively changes with the load current allowing better utilization of the regulation window.

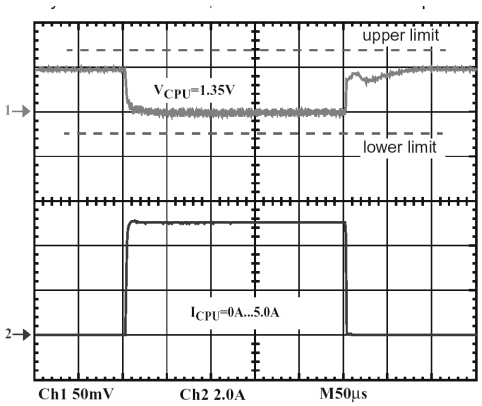


Figure 8. Converter response to 5A load step

The current through each R_{SENSE} resistor (ISNS) is sampled shortly after LDRV is turned on. That current is held for the remainder of the cycle, and then injected to produce an offset to VCORE+ through the external 1K resistor (R6 in Figure 1). This creates a voltage at the input to the error amplifier that rises with increasing current, causing the regulator's output to droop as the current increases.

$$V_{DROOP} = \frac{I_{LOAD} \bullet R_{DS(ON)}}{3 \bullet R_{SENSE}} \quad (7)$$

Gate Driver section

The gate control logic translates the internal PWM control signal into the MOSFET gate drive signals providing necessary amplification, level shifting and shoot-through protection. Also, it has functions that help optimize the IC performance over a wide range of operating conditions. Since MOSFET switching time can vary dramatically from type to type and with the input voltage, the gate control logic provides adaptive dead time by monitoring the gate-to-source voltages of both upper and lower MOSFETs. The lower MOSFET drive is not turned on until the gate-to-source voltage of the upper MOSFET has decreased to less than approximately 1 volt. Similarly, the upper MOSFET is not turned on until the gate-to-source voltage of the lower MOSFET has decreased to less than approximately 1 volt. This allows a wide variety of upper and lower MOSFETs to be used without a concern for simultaneous conduction, or shoot-through.

There must be a low – resistance, low – inductance path between the driver pin and the MOSFET gate for the adaptive dead-time circuit to work properly. Any delay along that path will subtract from the delay generated by the adaptive dead-time circit and a shoot-through condition may occur.

Frequency Loop Compensation

Due to the implemented current mode control, the modulator has a single pole response with -1 slope at frequency determined by load

$$F_{PO} = \frac{1}{2\pi R_O C_O} \quad (8)$$

where R_O is load resistance, C_O is load capacitance. For this type of modulator Type 2 compensation circuit is usually sufficient. To reduce the number of external components and simplify the design task, the PWM controller has an internally compensated error amplifier. Figure 9 shows a Type 2 amplifier and its response along with the responses of a current mode modulator and of the converter. The Type 2 amplifier, in addition to the pole at the origin, has a zero-pole pair that causes a flat gain region at frequencies between the zero and the pole.

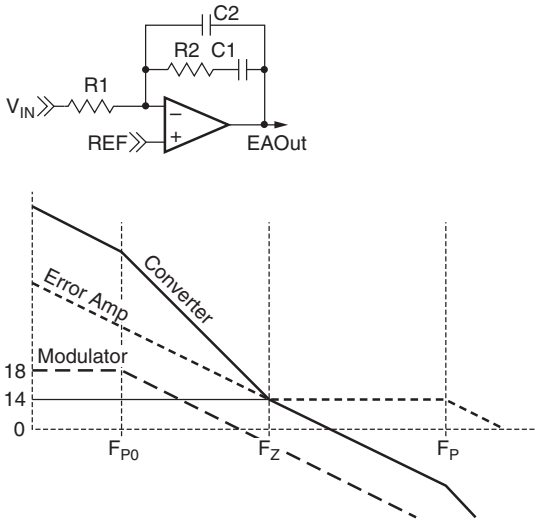


Figure 9. Compensation

$$F_Z = \frac{1}{2\pi R_2 C_1} = 6\ \text{kHz} \quad (9a)$$

$$F_P = \frac{1}{2\pi R_2 C_2} = 600\ \text{kHz} \quad (9b)$$

This region is also associated with phase 'bump' or reduced phase shift. The amount of phase shift reduction depends on how wide the region of flat gain is and has a maximum value of 90 degrees. To further simplify the converter compensation, the modulator gain is kept independent of the input voltage variation by providing feed-forward of VIN to the oscillator ramp.

The zero frequency, the amplifier high frequency gain and the modulator gain are chosen to satisfy most typical applications. The crossover frequency will appear at the point where the modulator attenuation equals the amplifier high frequency gain. The only task that the system designer has to complete is to specify the output filter capacitors to position the load main pole somewhere within one decade lower than the amplifier zero frequency. With this type of compensation plenty of phase margin is easily achieved due to zero-pole pair phase 'boost'.

Conditional stability may occur only when the main load pole is positioned too much to the left side on the frequency axis due to excessive output filter capacitance. In this case, the ESR zero placed within the 10kHz...50kHz range gives some additional phase 'boost'. Fortunately, there is an opposite trend in mobile applications to keep the output capacitor as small as possible.

Protection

The converter output is monitored and protected against short circuit (over-current), and over-voltage conditions.

Over-Current sensing (see Figure 10)

When the circuit's current limit signal ("ILIM det" as shown in Figure 6) goes high, a pulse-skipping circuit is activated and a 16-clock cycle counter is started. HDRV will be inhibited as long as the sensed current is higher than the ILIM value. This limits the current supplied by the DC input.

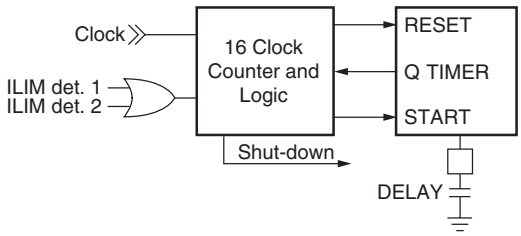


Figure 10. Over-current shut-down delay logic

If ILIM det goes high during counts 9-16 of the counter, the overcurrent delay timer is started and the 16-clock counter starts again. This timer delays the shut-down of the chip and its time is a function of the value of C_{DELAY}.

$$T_{HOLDOFF}(\text{in mS}) = \frac{C_{DELAY}(\text{in nF})}{19} \quad (10)$$

Over-current must detected at least once during the first 8 clock cycles and once during the 2nd 8 clock cycles of the 16-cycle counter for the timer to continue timing. If the over-current condition does not occur at least once per 8 clock counts during any clock counter cycle while the timer is high, the timer and the over-current detection circuit are reset, preventing shutdown. The clock counter coutinues to count and look for ILIM det pulses in this manner until either:

1. the IC is shut-down because the timer timed out:
   If the timer pulse is allowed to finish by timing out, the IC is shut-down and can only be restarted by removing power or toggling the EN pin.

2. ILIM det does not go high at least once per 8 clock counts. In this case, the timer and over-current shutdown logic are reset, and a chip shut-down is averted.

PGOOD will go LOW if the IC shuts down from over-current.

Setting the Current Limit

ISNS is compared to the current established when a 0.9 V internal reference drives the ILIM pin. The threshold is determined at the point when the

$$\frac{ISNS}{8} > \frac{0.9V}{R_{ILIM}} \text{ . Since } ISNS = \frac{I_{LOAD} \bullet R_{DS(ON)}}{R_{SENSE}}$$

therefore,

$$R_{ILIM} = \frac{0.9V}{I_{LIMIT}} \times \frac{8 \bullet (R_{SENSE})}{R_{DS(ON)}} \quad (11)$$

Since the tolerance on the current limit is largely dependent on the ratio of the external resistors it is fairly accurate if the voltage drop on the Switching Node side of R_{SENSE} is an accurate representation of the load current. When using the MOSFET as the sensing element, the variation of $R_{DS(ON)}$ causes proportional variation in the ISNS. This value not only varies from device to device, but also has a typical junction temperature coefficient of about 0.4% / °C (consult the MOSFET datasheet for actual values), so the actual current limit set point will decrease propotional to increasing MOSFET die temperature. The same discussion applies to the V_{DROOP} calculation.

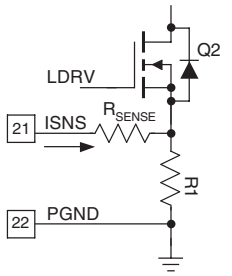


Figure 11. Improving current sensing accuracy

More accurate sensing can be achieved by using a resistor (R1) instead of the $R_{DS(ON)}$ of the FET as shown in Figure 11. This approach causes higher losses, but yields greater accuracy in both V_{DROOP} and I_{LIMIT}. R1 is a low value (e.g. 10mΩ) resistor.

The current limit (I_{LIMIT}) set point chosen needs to accommodate ripple current, slew current, and variability in the MOSFET's $R_{DS(ON)}$.

$$I_{LIMIT} > I_{LOAD} + C_{OUT}\frac{dV}{dt} \quad (12a)$$

Slew current ($C_{OUT}\frac{dV}{dt}$) is the current required for the output voltage to slew upwards during VID code changes, since the circuit will limit the regulator's output current by pulse skipping when I_{LIMIT} is reached. The $\frac{dV}{dt}$ term we used earlier in the discussion (set up by the C_{SS}) was 500mV/100µS or 5V/mS. Assuming C_{OUT} of 4000µF, the current required to slew C_{OUT} at this rate is:

$$C_{OUT}\frac{dV}{dt} = 4mF \bullet 5V/mS = 20A \quad (12b)$$

which is contributed roughly equally from each phase, therefore, 1/2 of the slew current comes from a single phase.

The over-current comparator is sampled just after LDRV is turned on, when the current is near its peak in the cycle. Assuming 20% inductor ripple current, we can then add 1/2 of the ripple current, or 10%. An additional factor of 1.2 accounts for the inaccuracy in the initial (room temperature) $R_{DS(ON)}$ of the MOSFETs with an additional factor of 1.4 to accommodate the rise of the MOSFET $R_{DS(ON)}$ when operating with T_J @ 125°C. With a maximum load current of 12.5A/phase, the target for I_{LIMIT} (per phase) would be:

$$I_{LIMIT} > 1.1 \bullet 1.2 \bullet 1.4 \bullet \left(12.5A + \frac{20A}{2}\right) \approx 42A \quad (12c)$$

so using equation 11, with $R_{DS(ON)}$ = 3mΩ for the 2 parallel FDS6688 MOSFETs, R_{ILIM} ≈ 56K:

Over-Voltage Protection

Should the output voltage exceed 2.35V due to an upper MOSFET failure, or for other reasons, the overvoltage protection comparator will force the LDRV high. This action actively pulls down the output voltage and, in the event of the upper MOSFET failure, will eventually blow the battery fuse. As soon as the output voltage drops below the threshold, the OVP comparator is disengaged.

This OVP scheme provides a 'soft' crowbar function which helps to tackle severe load transients and does not invert the output voltage when activated — a common problem for OVP schemes with a latch.

Over-Temperature Protection

The chip incorporates an over temperature protection circuit that shuts the chip down when a die temperature of 150°C is reached. Normal operation is restored at die temperature below 125°C with internal Power On Reset asserted, resulting in a full soft-start cycle.

Design and Component Selection Guidelines

As an initial step, define operating voltage range and minimum and maximum load currents for the controller. For this discussion,

IOUT Max	25A
VIN	5.5 to 21 V
VOUT	0.925 to 2 V

Output Inductor Selection

The minimum practical output inductor value is the one that keeps inductor current just on the boundary of continuous conduction at some minimum load. The industry standard practice is to choose the ripple current to be somewhere from 15% to 35% of the nominal current. At light load, the ripple current also determines the point where the converter will automatically switch to hysteretic mode of operation (I_{MIN}) to sustain high efficiency. The following equations help to choose the proper value of the output filter inductor.

$$\Delta I = 2 \times I_{MIN} = \frac{\Delta V_{OUT}}{ESR},$$

where ΔI is the inductor ripple current, which we will choose for 20% of the full load current (12.5A in each phase) and ΔV_{OUT} is the maximum output ripple voltage allowed.

$$L = \frac{V_{IN} - V_{OUT}}{F_{SW} \times \Delta I} \times \frac{V_{OUT}}{V_{IN}} \quad (13)$$

for this example we'll use:

V_{IN} = 20V, V_{OUT} = 1.5V
ΔI = 20% *12.5A (per phase) = 2.5A
F_{SW} = 300KHz.

Therefore,
L ≈ 1.8µH

The inductor's current rating should be chosen per the I_{LIMIT} calculated above. Some transient currents over the inductor current rating may be tolerable if the inductor's saturation characteristic $\left(\frac{dL}{dI}\right)$ is sufficiently "soft".

Output Capacitor Selection

The output capacitor serves two major functions in a switching power supply. Along with the inductor it filters the sequence of pulses produced by the switcher, and it supplies the load transient currents. The filtering requirements are a function of the switching frequency and the ripple current allowed, and are usually easy to satisfy in high frequency converters.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. Modern microprocessors produce transient load rates in excess of 10A/µs. High frequency ceramic capacitors placed beneath the processor socket initially supply the transient and reduce the slew rate seen by the bulk capacitors. The bulk capacitor values are generally determined by the total allowable ESR rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the processor power pins as physically possible. Consult with the processor manufacturer for specific decoupling requirements. Use only specialized low-ESR electrolytic capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a transient. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Input Capacitor Selection

The input capacitor should be selected by its ripple current rating. For a 2 phase converter, the RMS currents is calculated:

$$I_{RMS} = \frac{I_{PK}}{2}\sqrt{2D - 4D^2} \quad (14)$$

This equation produces the worst case value at maximum duty cycle. For our example, that occurs when VIN = 5.5V and VOUT = 2V. For 25A maximum output the maximum RMS current at C_{IN}:

$$I_{RMS(MAX)} = 5.6A$$

Power MOSFET Selection

For the example in the following discussion, we will be selecting components for:

VIN from 5V to 20V
V_{OUT} = 1.5V @ $I_{LOAD(MAX)}$ = 12.5A/phase

The FAN5240 converter's output voltage is very low with respect to the input voltage, therefore the Lower MOSFET (Q2) is conducting the full load current for most of the cycle. Therefore, Q2 should be selected to be a MOSFET with low $R_{DS(ON)}$ to minimize conduction losses.

In contrast, Q1 is on for a maximum of 20% (when VIN = 5V) of the cycle, and its conduction loss will have less of an impact. Q1, however, sees most of the switching losses, so Q1's primary selection criteria should be gate charge ($Q_{G(SW)}$).

High-Side Losses:

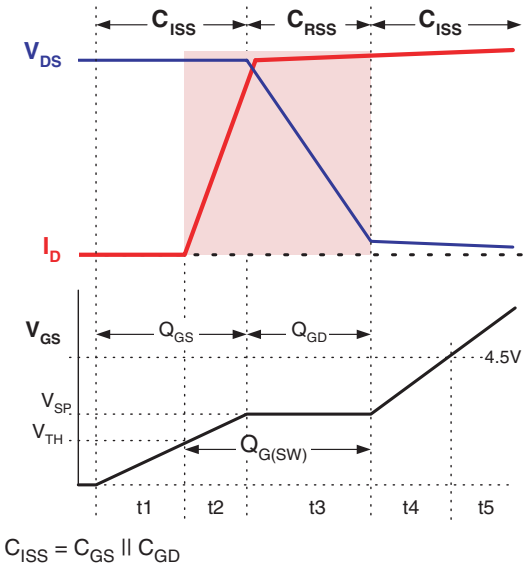


Figure 12. Switching losses and Q_G

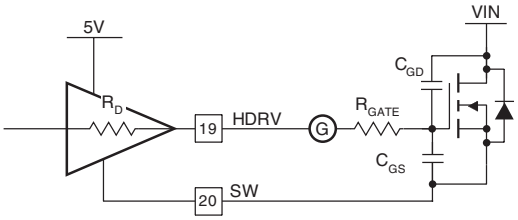


Figure 13. Drive Equivalent Circuit

Assuming switching losses are about the same for both the rising edge and falling edge, Q1's switching losses, as can be seen by Figure 12, are given by:

$$P_{UPPER} = P_{SW} + P_{COND} \quad (15a)$$

$$P_{SW} = \left(\frac{V_{DS} \times I_L}{2} \times 2 \times t_S\right) F_{SW} \quad (15b)$$

$$P_{COND} = \frac{V_{OUT}}{V_{IN}} \times I_{OUT}^{\ 2} \times R_{DS(ON)} \quad (15c)$$

where $R_{DS(ON)}$ is @$T_{J(MAX)}$ and:

t_S is the switching period (rise or fall time) and is predominantly the sum of t2, t3 (Figure 12), a function of the impedance of the driver and the $Q_{G(SW)}$ of the MOSFET. Since most of t_S occurs when $V_{GS} = V_{SP}$ we can use a constant current assumption for the driver to simplify the calculation of t_S :

$$t_S = \frac{Q_{G(SW)}}{I_{DRIVER}} \approx \frac{Q_{G(SW)}}{\left(\frac{VDD - V_{SP}}{R_{DRIVER} + R_{GATE}}\right)} \quad (16)$$

For the high-side MOSFET, V_{DS} = VIN, which can be as high as 20V in a typical portable application. Q2, however, switches on or off with its parallel shottky diode conducting, therefore $V_{DS} \approx 0.5V$. Since P_{SW} is proportional to V_{DS} , Q2's switching losses are negligible and we can select Q2 based on $R_{DS(ON)}$ only.

Care should also be taken to include the delivery of the MOSFET's gate power (P_{GATE}) in calculating the power dissipation required for the FAN5240:

$$P_{GATE} = Q_G \times VDD \times F_{SW} \quad (17)$$

Low-Side Losses

Conduction losses for Q2 are given by:

$$P_{COND} = (1 - D) \times I_{OUT}^{\ 2} \times R_{DS(ON)} \quad (18)$$

where $R_{DS(ON)}$ is the $R_{DS(ON)}$ of the MOSFET at the highest operating junction temperature and $D = \frac{V_{OUT}}{V_{IN}}$ is the minimum duty cycle for the converter. Since D_{MIN} is 5% for portable computers, (1-D) ≈ 1, further simplifying the calculation.

The maximum power dissipation ($P_{D(MAX)}$) is a function of the maximum allowable die temperature of the low-side MOSFET, the $\theta_{J\text{-}A}$, and the maximum allowable ambient temperature rise:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{J-A}}$$

$\theta_{J\text{-}A}$, depends primarily on the amount of PCB area that can be devoted to heat sinking (see FSC app note AN-1029 for SO-8 MOSFET thermal information).

Layout Considerations

Switching converters, even during normal operation, produce short pulses of current which could cause substantial ringing and be a source of EMI if layout constrains are not observed.

There are two sets of critical components in a DC-DC converter. The switching power components process large amounts of energy at high rate and are noise generators. The low power components responsible for bias and feedback functions are sensitive to noise.

A multi-layer printed circuit board is recommended. Dedicate one solid layer for a ground plane. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels.

Notice all the nodes that are subjected to high dV/dt voltage swing such as SW, HDRV and LDRV, for example. All surrounding circuitry will tend to couple the signals from these nodes through stray capacitance. Do not oversize copper traces connected to these nodes. Do not place traces connected to the feedback components adjacent to these traces. It is not recommended to use High Density Interconnect Systems, or micro-vias on these signals. The use of blind or buried vias should be limited to the low current signals only. The use of normal thermal vias is left to the discretion of the designer.

Keep the wiring traces from the IC to the MOSFET gate and source as short as possible and capable of handling peak currents of 2A. Minimize the area within the gate-source path to reduce stray inductance and eliminate parasitic ringing at the gate.

Locate small critical components like the soft-start capacitor and current sense resistors as close as possible to the respective pins of the IC.

The FAN5240 utilizes advanced packaging technology that will have lead pitch of 0.6mm. High performance analog semiconductors utilizing narrow lead spacing may require special considerations in PWB design and manufacturing. It is critical to maintain proper cleanliness of the area surrounding these devices. It is not recommended to use any type of rosin or acid core solder, or the use of flux in either the manufacturing or touch up process as these may contribute to corrosion or enable electromigration and/or eddy currents near the sensitive low current signals. When chemicals such as these are used on or near the PWB, it is suggested that the entire PWB be cleaned and dried completely before applying power.

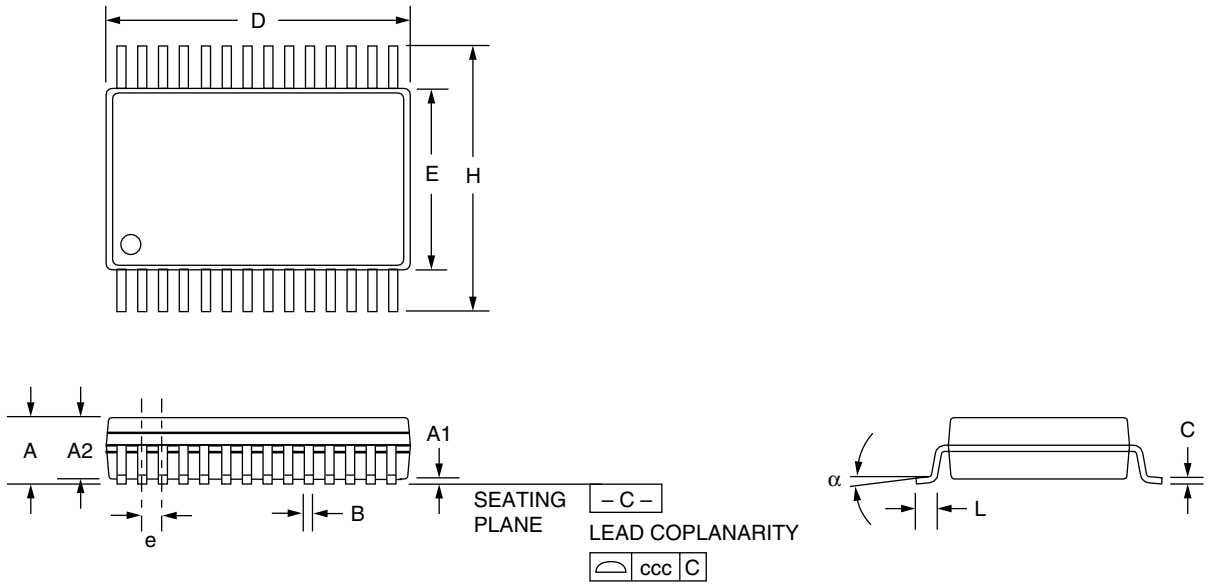
Mechanical Dimensions

28-Pin QSOP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	0.053	0.069	1.35	1.75	
A1	0.004	0.010	0.10	0.25	
A2	-	0.061	-	1.54	
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		
H	0.228	0.244	5.80	6.19	
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0°	8°	0°	8°	

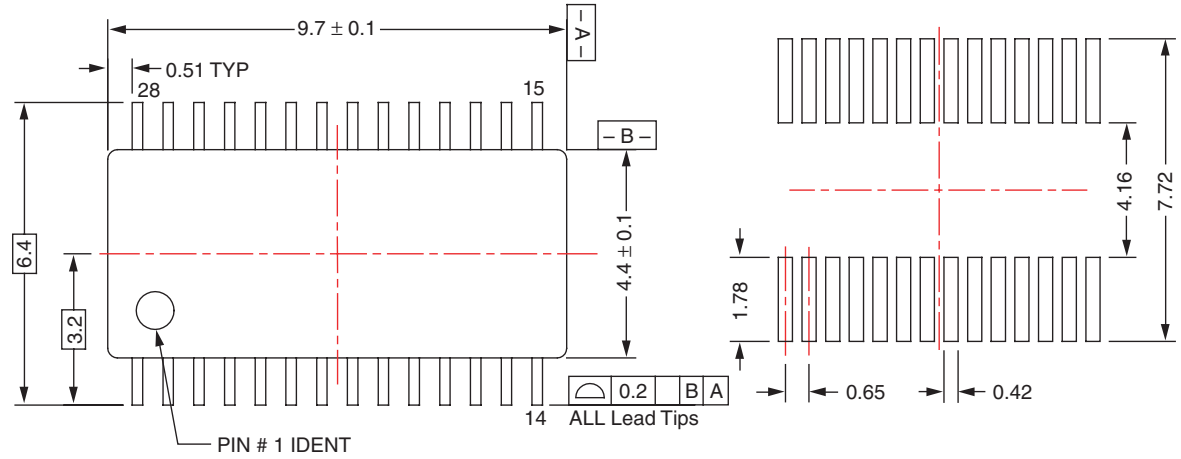
Notes:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamber on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the maximum number of terminals.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

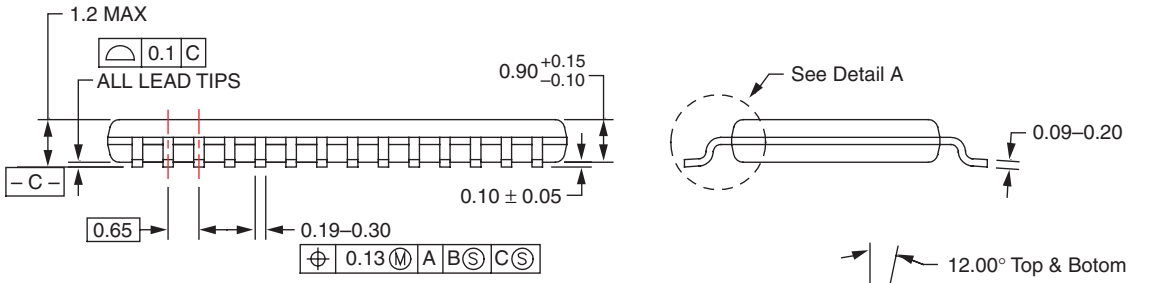


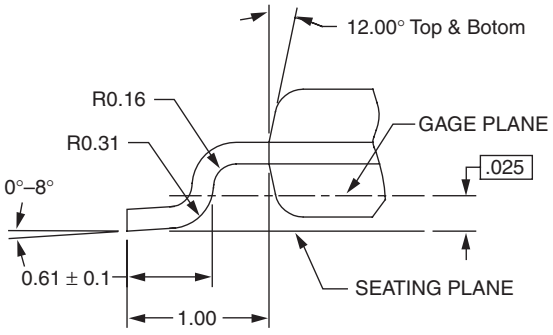
Mechanical Dimensions

28-Pin TSSOP



LAND PATTERN RECOMMENDATION





DIMENSIONS ARE IN MILLIMETERS

DETAIL A

NOTES:

A. Conforms to JEDEC registration MO-153, variation AB, Ref. Note 6, dated 7/93.
B. Dimensions are in millimeters.
C. Dimensions are exclusive of burrs, mold flash, and tie bar extensions.
D Dimensions and Tolerances per ANsI Y14.5M, 1982

Ordering Information

Part Number	Temperature Range	Package	Packing
FAN5240QSC	-10°C to 85°C	QSOP-28	Rails
FAN5240QSCX	-10°C to 85°C	QSOP-28	Tape and Reel
FAN5240MTC	-10°C to 85°C	TSSOP-28	Rails
FAN5240MTCX	-10°C to 85°C	TSSOP-28	Tape and Reel