

# FAN54300 — USB-Compliant, Dual-Power Input, Single-Cell, Li-Ion Switching Charger with USB-OTG Boost Regulator

## Features

- Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- Accepts USB or Dedicated Power Input Source
- 5 V, 300 mA Boost Mode for USB OTG from 2.5 to 4.5 V Battery Input
- Charge Voltage Accuracy:  $\pm 0.5\%$  at  $T_A=25^\circ\text{C}$   
 $\pm 1\%$  from  $T_A=0$  to  $125^\circ\text{C}$
- $\pm 5\%$  USB Input Current Regulation Accuracy
- $\pm 5\%$  Charge Current Regulation Accuracy
- 20 V Absolute Maximum Input Voltage
- 9.5 V Maximum Input Operating Voltage on VIN Pin, 6.5 V Maximum on VBUS Pin
- Up to 1.5 A Maximum Charge Rate
- Programmable Charge and Mode through High-Speed I<sup>2</sup>C Interface (3.4 Mb/s) with Fast Mode Plus Compatibility
  - Input Current
  - Fast-Charge / Termination Current
  - Charger Voltage
  - Safety Timer
  - Termination Enable
- 3 MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
- Small Footprint, 1  $\mu\text{H}$ , External Inductors
- Safety Timer with Reset Control
- Weak Input Sources Accommodated by Reducing Charging Current to Maintain Minimum V<sub>BUS</sub> Voltage
- Low Reverse Leakage from Battery Drain to VBUS or VIN
- Programmable LED Drive for Charge Indication
- Register and Slave Addresses Compatible with FAN540X and FAN542X Families

## Description

The FAN54300 combines two highly integrated switch-mode chargers and a boost regulator to minimize single-cell Li-Ion charging time from a USB and/or auxiliary power source.

Charging parameters and operating modes are programmable through an I<sup>2</sup>C Bus® interface that operates up to 3.4 Mbps. The charger and boost regulator circuits switch at 3 MHz to minimize the size of the external passive components.

The FAN54300 provides battery charging in three phases: conditioning, constant current, and constant voltage.

To ensure USB compliance and minimize charging time, the USB input current is limited to the value set through the I<sup>2</sup>C host. Charge termination is determined by a programmable minimum current level. A safety timer with reset control provides a safety backup for the I<sup>2</sup>C host.

The IC automatically restarts the charge cycle when the battery falls below an internal threshold. If the input source is removed, the IC enters a high-impedance mode, with leakage from the battery to the input prevented. Charge status is reported back to the host through the I<sup>2</sup>C port. Charge current is reduced when the die temperature reaches 120°C.

The FAN54300 can operate as a boost regulator on command from the system. The boost regulator includes a soft-start that limits inrush current from the battery.

The FAN54300 is available in a 30-bump, 0.4 mm pitch, wafer-level, chip-scale package (WLCSP).

## Applications

- Cell Phones, Smart Phones, PDAs
- Digital Cameras
- Portable Media Players

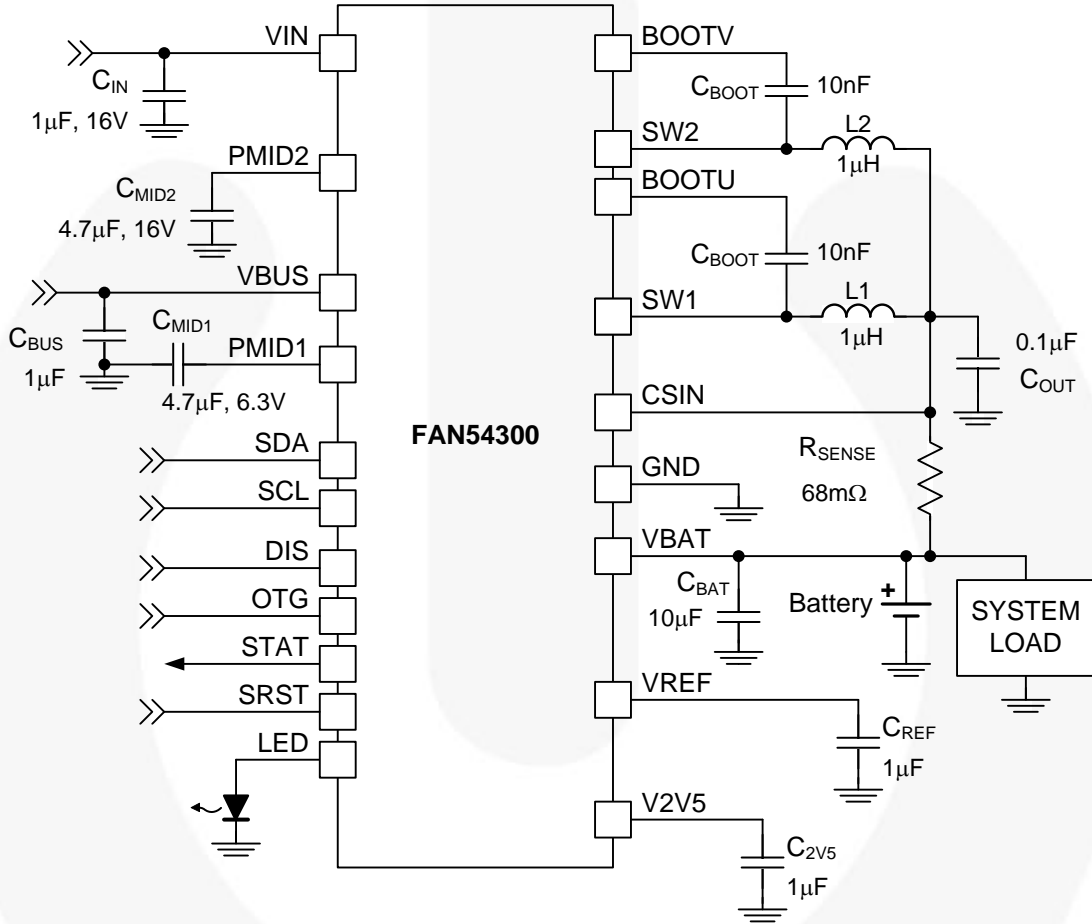
## Ordering Information

Part Number	Temperature Range	Package	Packing
FAN54300UCX	-40 to 85°C	30-Ball, WLCSP, 5x6 Array, 0.4mm Pitch, 586 $\mu\text{m}$ Package Height	Tape and Reel

**Table 1. Feature Summary**

Part Number	Automatic Charge	Battery Absent Charge
FAN54300	Yes	No

**Typical Application**



**Figure 1. Typical Application**

## Block Diagrams

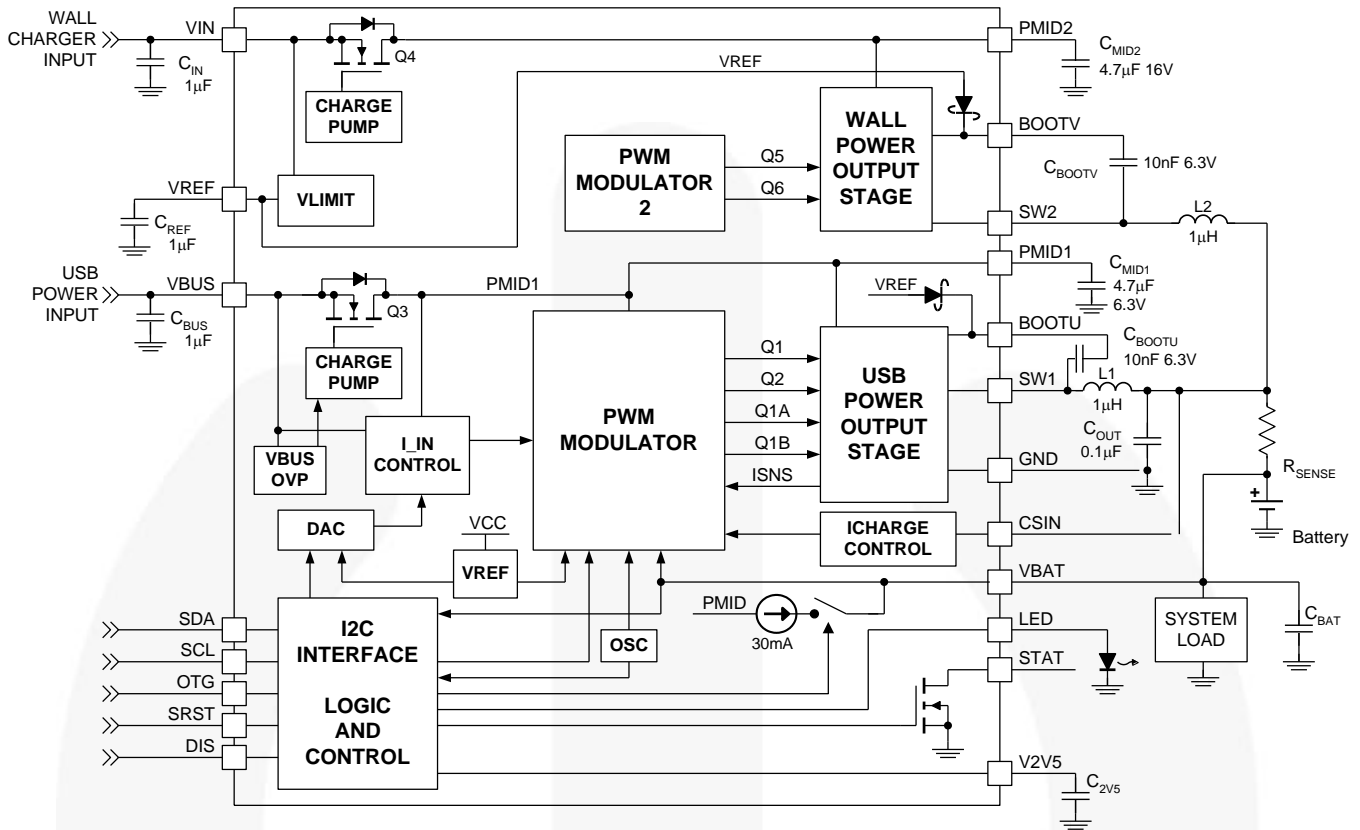


Figure 2. IC and System Block Diagram

Table 2. Recommended External Components

Component	Description	Vendor	Parameter	Typ.	Units
L1, L2:	Charge Currents to 1 A: 1 µH, 20%, 1.3 A, 2016	Murata: LQM2MPN1R0M	L	1.0	µH
			DCR	85	mΩ
	Charge Currents Above 1 A: 1 µH, 20%, 1.6 A, 2520	Murata: LQM2HPN1R0M	L	1.0	µH
			DCR	55	mΩ
C <sub>BAT</sub>	10 µF, 20%, 6.3 V, X5R, 0603	Murata: GRM188R60J106M	C	10	µF
C <sub>MID1,2</sub>	4.7 µF, 10%, 16 V, X5R, 0805	Murata: GRM21BR61C475K	C	4.7	µF
C <sub>IN</sub> , C <sub>BUS</sub>	1.0 µF, 10%, 16 V, X5R, 0603	Murata GRM188R61E105K	C	1.0	µF
C <sub>BOOT</sub>	10 nF, 10%, 6.3 V, X5R, 0201	Murata GRM033R70J103K	C	10	nF
C <sub>OUT</sub>	0.1 µF, 10%, 6.3 V, X5R, 0201	Murata GRM033R60J104K	C	0.1	µF
C <sub>2V5</sub> , C <sub>REF</sub>	1µF, 10%, 6.3 V, X5R, 0402	Murata GRM155R60J105M	C	1.0	µF

Block Diagrams (Continued)

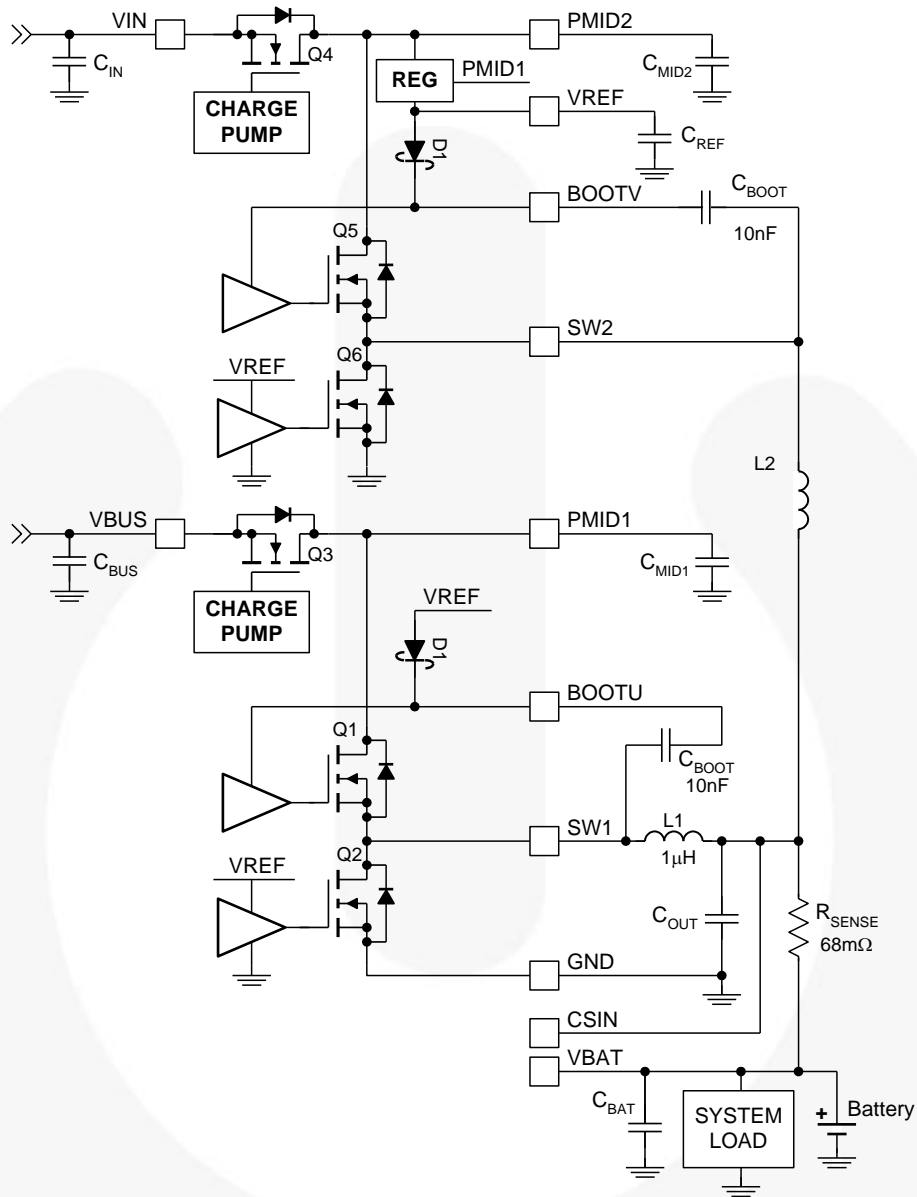


Figure 3. Power Output



## Pin Configuration

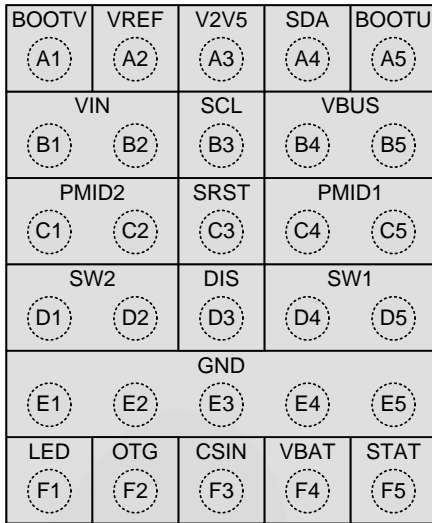


Figure 4. Pin Assignments (Top View)

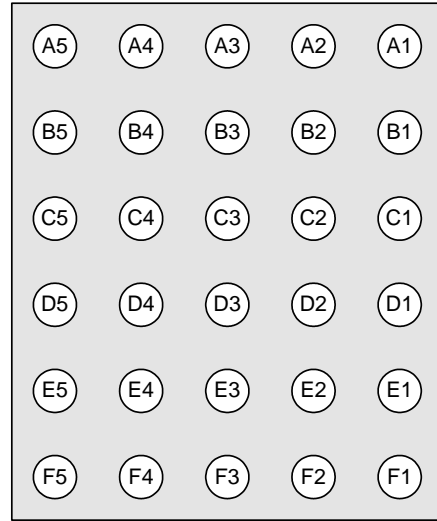


Figure 5. Pin Assignments (Bottom View)

## Pin Definitions

Pin #	Name	Description
A1	BOOTV	<b>BOOT.</b> High-side NMOS driver supply. Connect a 10nF capacitor from SW2 to this pin.
A2	VREF	<b>Bias Regulator Output.</b> Connect to a 1 $\mu$ F capacitor to PGND. This pin supplies the internal gate drive and power supply to the IC while charging. Up to 5 mA of current can be provided from this pin to drive external circuits. This pin is active when either $V_{IN}$ or $V_{BUS}$ are above $V_{BAT}$ .
A3	V2V5	<b>2.5 V Regulator.</b> Connect to a 1 $\mu$ F capacitor to PGND. Up to 5 mA can be provided from this pin to drive external circuits. This regulator is powered only when $V_{IN}$ is connected.
A4	SDA	<b>I<sup>2</sup>C Interface Serial Data.</b> This pin should not be left floating.
A5	BOOTU	<b>BOOT.</b> High-side NMOS driver supply. Connect a 10 nF capacitor from SW1 to this pin.
B1, B2	VIN	<b>Charger Input Voltage.</b> Bypass with a minimum of 1 $\mu$ F, 16 V capacitor to GND.
B3	SCL	<b>I<sup>2</sup>C Interface Serial Clock.</b> This pin should not be left floating.
B4, B5	VBUS	<b>USB Input Voltage.</b> Bypass with a 1 $\mu$ F, 16 V capacitor to GND.
C1, C2	PMID2	<b>Power Input Voltage for VIN Power Source.</b> Power input to the charger regulator, bypass point for the VIN input current sense, and high-voltage input switch. Bypass with a minimum of 4.7 $\mu$ F, 16 V capacitor to PGND.
C3	SRST	<b>Safety Reset.</b> When LOW, both safety registers are reset to their default values. When HIGH, the safety registers reset when $V_{BAT}$ drops below $V_{SHORT}$ .
C4, C5	PMID1	<b>Power Input Voltage for VBUS Power Source.</b> Power input to the VBUS switching charger regulator, bypass point for the VBUS input current sense, and high-voltage input switch. Bypass with a minimum of 4.7 $\mu$ F, 6.3 V capacitor to PGND.
D1, D2	SW2	<b>Switching Node for VIN Charger.</b> Connect to the output inductor.
D3	DIS	<b>Charge Disable.</b> When this pin is HIGH, charging is disabled and no timers are reset. When LOW, charging is controlled by the I <sup>2</sup> C registers. This pin does not affect the 32-second timer.
D4, D5	SW1	<b>Switching Node for VBUS Charger and OTG Boost.</b> Connect to the output inductor.
E1–E5	GND	<b>Ground.</b> Power return for gate drive and power transistors as well as IC signal ground. The connection from this pin to the bottoms of the $C_{PMID}$ capacitors should be as short as possible.
F1	LED	<b>Light Emitting Diode Output.</b> Up to 5 mA current source drive from the active PMID indicates the battery is charging.

Pin #	Name	Description
F2	OTG	<b>On The Go.</b> When unattended charging is indicated, the level on this pin sets the $I_{BUS}$ current limit. This pin is also used to put the IC into Boost Mode.
F3	CSIN	<b>Current-Sense Input.</b> Connect to sense resistor in series with the battery. The IC uses this node to sense current into the battery. Bypass this pin with a 0.1 $\mu\text{F}$ capacitor to PGND.
F4	VBAT	<b>Battery Voltage.</b> Connect to the positive (+) terminal of the battery pack. Bypass with a 10 $\mu\text{F}$ capacitor to PGND.
F5	STAT	<b>Status.</b> Open-drain output indicating charge status. The IC pulls this pin LOW when charging is in process.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V <sub>BUS</sub>	VBUS Voltage	Continuous	-1.4	20.0	V
		Pulsed, 100 ms Maximum Non-Repetitive	-2.0		
V <sub>IN</sub>	VIN Voltage		-2.0	20.0	V
V <sub>BOOTU</sub>	BOOTU Voltage		-0.7	20.0	V
V <sub>BOOTV</sub>	BOOTV Voltage		-0.7	20.0	V
V <sub>PMID1</sub>	PMID1 Voltage		-1.0	20.0	V
V <sub>SW1</sub>	SW1 Voltage		-0.7	6.5	V
V <sub>PMID2</sub>	PMID2 Voltage		-1.0	20.0	V
V <sub>SW2</sub>	SW2 Voltage		-0.7	12.0	V
V <sub>O</sub>	Other Pins		-0.3	6.5 <sup>(1)</sup>	V
$\frac{dV_{BUS}}{dt}$	Maximum Rate of V <sub>BUS</sub> Increase Above 5.5 V when IC Enabled			4	V/μs
$\frac{dV_{IN}}{dt}$	Maximum Rate of V <sub>IN</sub> Increase Above 9.5 V when IC Enabled			4	V/μs
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	2.0		kV
		Charged Device Model per JESD22-C101	1.5		kV
T <sub>J</sub>	Junction Temperature		-40	+150	°C
T <sub>STG</sub>	Storage Temperature		-65	+150	°C
T <sub>L</sub>	Lead Soldering Temperature, 10 Seconds			+260	°C

### Note:

1. Lesser of 6.5 V or V<sub>REF</sub> + 0.3 V.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V <sub>BUS</sub>	VBUS Supply Voltage	4	6	V
V <sub>IN</sub>	VIN Supply Voltage	4.0	9.5	V
T <sub>A</sub>	Ambient Temperature	-30	+85	°C
T <sub>J</sub>	Junction Temperature	0	+125	°C

## Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature T<sub>J(max)</sub> at a given ambient temperature T<sub>A</sub>.

Symbol	Parameter	Typical	Unit
θ <sub>JA</sub>	Junction-to-Ambient Thermal Resistance	60	°C/W
θ <sub>JB</sub>	Junction-to-PCB Thermal Resistance	20	°C/W

## Electrical Specifications

Unless otherwise specified: circuit of Figure 1, recommended operating temperature range for  $T_J$  and  $T_A$ ,  $V_{BUS}$  or  $V_{IN} = 5.0\text{ V}$ ,  $HZ1$ ,  $HZ2$ ,  $OPA\_MODE = 0$ , (Charger Mode).  $SCL$ ,  $SDA$ ,  $OTG = 0$  or  $1.8\text{ V}$ . Typical values are for  $T_J = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Power Supplies</b>						
$I_{VBUS}$	VBUS Current	PWM Switching, Open Battery, $TE=0$		33		mA
		PWM Not Switching ( $V_{BAT} > V_{OREG}$ )		3.6		mA
		$0^\circ\text{C} < T_J < 85^\circ\text{C}$ , $HZ1 = 1$ , $V_{BAT} > V_{LOWV}$		350	500	$\mu\text{A}$
		$0^\circ\text{C} < T_J < 85^\circ\text{C}$ , $HZ1 = 1$ , $V_{BAT} < V_{LOWV}$ , 32S Mode		350	500	$\mu\text{A}$
$I_{VIN}$	VIN Current	PWM Switching, Open Battery, $TE=0$		33		mA
		PWM Not Switching ( $V_{BAT} > V_{OREG}$ )		2.6		mA
		$0^\circ\text{C} < T_J < 85^\circ\text{C}$ , $HZ2 = 1$ , $V_{IN} > V_{LOWV}$		350	500	$\mu\text{A}$
		$0^\circ\text{C} < T_J < 85^\circ\text{C}$ , $HZ2 = 1$ , $V_{IN} < V_{LOWV}$ , 32S Mode		350	500	$\mu\text{A}$
$I_{BAT}$	Battery Discharge Current in High-Z Mode	$0^\circ\text{C} < T_J < 85^\circ\text{C}$ , $HZ1=HZ2 = 1$ or $DIS=1$ , $V_{BAT} = 4.2\text{ V}$			20	$\mu\text{A}$
		$0^\circ\text{C} < T_J < 85^\circ\text{C}$ , $V_{BAT} = 4.2\text{ V}$ , $V_{IN} = V_{BUS} = \text{Open or GND}$ , $HZ1=HZ2=1$ , $SDA = SCL = 1.8\text{ V}$ , No $I^2C$ Traffic			30	$\mu\text{A}$
<b>Charger Voltage Regulation</b>						
$V_{OREG}$	Charge Voltage Range		3.5		4.4	V
	Charge Voltage Accuracy	$T_A = 25^\circ\text{C}$	-0.5		+0.5	%
		$T_J = 0$ to $125^\circ\text{C}$	-1		+1	%
<b>Charging Current Regulation</b>						
$I_{OCHRG}$	Output Charge Current Range	$V_{LOWV} < V_{BAT} < V_{OREG}$ , $V_{BUS} > V_{SLP}$ , $R_{SENSE} = 68\text{ m}\Omega$	550		1500	mA
	Charge Current Accuracy Across $R_{SENSE}$	$20\text{ mV} \leq V_{IREG} \leq 40\text{ mV}$	92	97	102	% of Setting
		$V_{IREG} > 40\text{ mV}$	94	97	100	
<b>Weak-Battery Detection</b>						
$V_{LOWV}$	Weak-Battery Threshold Accuracy	$3.4 \leq V_{LOWV} \leq 3.7$	-5		+5	%
	Weak Battery Deglitch Time	Rising Voltage, 2 mV Overdrive		30		ms
<b>Logic Levels: DIS, SDA, SCL, OTG</b>						
$V_{IH}$	HIGH-Level Input Voltage		1.05			V
$V_{IL}$	LOW-Level Input Voltage				0.4	V
$I_{IN}$	Input Bias Current	Input Tied to GND or $V_{BAT}$		0.01	1.00	$\mu\text{A}$
<b>Charge Termination Detection</b>						
$I_{(TERM)}$	Termination Current Range	$V_{BAT} > V_{OREG} - V_{RCH}$ , $V_{BUS} > V_{SLP}$ , $R_{SENSE} = 68\text{ m}\Omega$	50		400	mA
	Termination Current Accuracy	$[V_{CSIN} - V_{BAT}]$ from 3 mV to 20 mV	-25%		+25%	
		$[V_{CSIN} - V_{BAT}]$ from 20 mV to 40 mV	-5%		+5%	
	Termination Current Deglitch Time	2 mV Overdrive		30		ms

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**Electrical Specifications** (Continued)

Unless otherwise specified: circuit of Figure 1, recommended operating temperature range for  $T_J$  and  $T_A$ ,  $V_{BUS}$  or  $V_{IN} = 5.0\text{ V}$ , HZ1, HZ2, OPA\_MODE = 0, (Charger Mode). SCL, SDA, OTG = 0 or 1.8V. Typical values are for  $T_J = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>VBUS Input Power Source Detection</b>						
$V_{BUS(MIN)1}$	$V_{BUS}$ Input Voltage Rising	To Start $V_{BUS}$ Validation	4.20	4.30	4.40	V
$V_{BUS(MIN)2}$	Min. $V_{BUS}$ to Pass Validation	During $V_{BUS}$ Validation Period	4.00	4.08	4.15	V
$V_{BUS(MIN)3}$	Min. $V_{BUS}$ During Charge	During Charging	3.64	3.71	3.78	V
$t_{VBUS\_VALID}$	$V_{BUS}$ Validation Time			30		ms
$VBUS_{LOAD}$	$V_{BUS}$ Load	$V_{BUS} = 5\text{ V}$ , Applied at $V_{BUS}$ Validation		50		mA
<b>VIN Input Power Source Detection</b>						
$V_{IN(MIN)1}$	$V_{IN}$ Input Voltage Rising	To Start $V_{IN}$ Validation	4.20	4.30	4.40	V
$V_{IN(MIN)2}$	Min. $V_{IN}$ to Pass Validation	During $V_{IN}$ Validation Period	4.00	4.08	4.15	V
$V_{IN(MIN)3}$	Min. $V_{IN}$ During Charge	During Charging	3.64	3.71	3.78	V
$t_{VBUS\_VALID}$	$V_{IN}$ Validation Time			30		ms
$V_{INLOAD}$	$V_{IN}$ Load	$V_{IN} = 5\text{ V}$ , Applied at $V_{IN}$ Validation		50		mA
<b>Input Current Limit</b>						
$I_{BUSLIM}$	VBUS Input Current-Limit Threshold	$I_{BUS}$ set to 100 mA	88	93	98	mA
		$I_{BUS}$ set to 500 mA	450	475	500	
<b>V<sub>2V5</sub> 2.5V Linear Regulator</b>						
$V_{2V5}$	2.5 V Regulator Output	$I_{2V5}$ from 0 to 5 mA, $V_{IN} > 4.75\text{ V}$	2.35	2.50	2.65	V
	Current Limit		6	8		mA
<b>V<sub>REF</sub> Bias Generator</b>						
$V_{REF}$	Bias regulator voltage	$V_{IN} > V_{IN(MIN)}$	3.5		6.0	V
	current limit		10	15		mA
<b>Battery Recharge Threshold</b>						
$V_{RCH}$	Recharge Threshold	Below $V_{(OREG)}$	100	120	150	mV
	Deglitch Time	$V_{BAT}$ falling below $V_{RCH}$ threshold		130		ms
<b>STAT Output</b>						
$V_{STAT(OL)}$	STAT Output LOW	$I_{STAT} = 10\text{ mA}$			0.4	V
$I_{STAT(OH)}$	STAT High Leakage Current	$V_{STAT} = 5\text{ V}$			1	$\mu\text{A}$
<b>LED Output</b>						
$I_{LED(ON)}$	LED Output Current Accuracy	$V_{LED}$ from 1.5 to 3.5 V, Max. $(V_{REF}, V_{BAT}) - V_{LED} > 100\text{ mV}$	-30		+30	%
$I_{LED(OFF)}$	LED Off-State Leakage Current	$V_{LED} = 0\text{ V}$			1	$\mu\text{A}$
<b>Battery Detection</b>						
$I_{DETECT}$	Battery Detection Current Before Charge Complete (Sink Current) <sup>(2)</sup>	Begins After Termination Detected and $V_{BAT} \leq V_{OREG} - V_{RCH}$		-0.45		mA
$t_{DETECT}$	Battery Detection time			262		ms

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**Electrical Specifications** (Continued)

Unless otherwise specified: circuit of Figure 1, recommended operating temperature range for  $T_J$  and  $T_A$ ,  $V_{BUS}$  or  $V_{IN} = 5.0\text{ V}$ ,  $HZ1, HZ2, OPA\_MODE = 0$ , (Charger Mode).  $SCL, SDA, OTG = 0$  or  $1.8\text{ V}$ . Typical values are for  $T_J = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Sleep Comparator</b>						
$V_{SLP}$	Sleep Mode Entry Threshold, $V_{BUS} - V_{BAT}$ or $V_{IN} - V_{BAT}$	$2.3\text{ V} \leq V_{BAT} \leq V_{OREG}$ , $V_{PWRIN}$ Falling	0	90	160	mV
$V_{SLP\_EXIT}$	Sleep Mode Exit Hysteresis	$2.3\text{ V} \leq V_{BAT} \leq V_{OREG}$		40		mV
	Deglintch Time for $V_{BUS}$ Rising Above $V_{SLP} + V_{SLP\_EXIT}$	Rising Voltage		30		ms
<b>Power Switches</b> (see Figure 3)						
$R_{DS(ON)}$	Q3 On Resistance (VBUS to PMID1)	$I_{BUS(LIMIT)} \geq 500\text{ mA}$		210	300	m $\Omega$
	Q1 On Resistance (PMID1 to SW1)			110	225	
	Q2 On Resistance (SW1 to GND)			130	225	
	Q4 On Resistance (VIN to PMID2)			160	225	
	Q5 On Resistance (PMID2 to SW2)			110	225	
	Q6 On Resistance (SW2 to GND)			190	350	
<b>Charger PWM Modulator</b>						
$f_{SW}$	Oscillator Frequency		2.7	3.0	3.3	MHz
$D_{MAX}$	Maximum Duty Cycle				100	%
$D_{MIN}$	Minimum Duty Cycle			0		%
$I_{SYNC}$	Synchronous to Non-Synchronous Current Threshold <sup>(3)</sup>	Low-Side MOSFET Cycle-by-Cycle Current Limit		-120		mA
<b>Boost Mode Operation (OPA_MODE = 1, HZ1 = 0)</b>						
$V_{BOOST}$	Boost Output Voltage at VBUS	$2.5\text{ V} < V_{BAT} < 4.5\text{ V}$ , 0-200 mA Load	4.80	5.05	5.17	V
		$2.7\text{ V} < V_{BAT} < 4.5\text{ V}$ , 0-300 mA Load	4.77	5.05	5.17	
$I_{BAT(BOOST)}$	Boost Mode Quiescent Current	PFM Mode, $V_{IN} = 3.6\text{ V}$ , $I_{OUT} = 0$		300	400	$\mu\text{A}$
$I_{LIMPK(BST)}$	Q2-Peak Current Limit		1160	1380	1550	mA
$V_{BAT(MAX)}$	Maximum Battery Input for Boost Operation	$V_{BAT}$ Rising	4.7			V
	Hysteresis	$V_{BAT}$ Falling		125		mV
$UVLO_{BST}$	Minimum Battery Voltage for Boost Operation	While Boost Active		2.42		V
		To Start Boost Regulator		2.58	2.70	
<b>VBUS, VIN Load Resistance</b>						
$R_{VBUS}$	VBUS to GND Resistance	Normal Operation	500	1000	1500	$\Omega$
		$V_{BUS}$ Validation	50	110	175	$\Omega$
$R_{VIN}$	VIN to GND Resistance	Normal Operation	500	1000	1500	$\Omega$
		$V_{IN}$ Validation	50	110	175	$\Omega$

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**Electrical Specifications** (Continued)

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Protection and Timers</b>						
$V_{BUS\text{OVP}}$	VBUS Over-Voltage Shutdown	$V_{BUS}$ Rising	6.12	6.31	6.50	V
	Hysteresis	$V_{BUS}$ Falling		100		mV
$V_{IN\text{OVP}}$	VIN Over-Voltage Shutdown	$V_{IN}$ Rising	9.5	10.0	10.5	V
	Hysteresis	$V_{IN}$ Falling		100		mV
$V_{SHORT}$	Battery Short-Circuit Threshold	$V_{BAT}$ Rising	2.00	2.05	2.10	V
	Hysteresis	$V_{BAT}$ Falling		100		
$I_{SHORT}$	Short-Circuit Current	$V_{BAT} < V_{SHORT}$	30	40	50	mA
$T_{SHUTDWN}$	Thermal Shutdown Threshold <sup>(4)</sup>	$T_J$ Rising		165		$^\circ\text{C}$
	Hysteresis <sup>(4)</sup>	$T_J$ Falling		10		
$T_{CF}$	Thermal Regulation Threshold <sup>(4)</sup>	Charge Current Reduction Begins		120		$^\circ\text{C}$
$t_{INT}$	Detection Interval			2.1		s
$t_{32SEC}$	32-Second Timer <sup>(5)</sup>	32-Second Mode	21.0		31.5	s
$t_{15MIN}$	15-Minute Timer	15-Minute Mode	12.0	13.5	15.0	min
$\Delta t_{LF}$	Low Frequency Timer Accuracy	Charger Inactive	-25		25	%

**Notes:**

- Refers to negative inductor current. At lower battery charging current, of about 20 mA, non-synchronous switching operation commences.
- Q2 and Q6 always turn on for  $\gg 60\text{ ns}$  and then turn off if the current is below  $I_{SYNC}$ .
- Guaranteed by design.
- This tolerance applies to all timers on the IC, including soft-start and deglitching timers.

## I<sup>2</sup>C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f <sub>SCL</sub>	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
		High-Speed Mode, C <sub>B</sub> ≤ 100 pF			3400	
		High-Speed Mode, C <sub>B</sub> ≤ 400 pF			1700	
t <sub>BUF</sub>	Bus-Free Time between STOP and START Conditions	Standard Mode		4.7		μs
		Fast Mode		1.3		
t <sub>HD;STA</sub>	START or Repeated START Hold Time	Standard Mode		4		μs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
t <sub>LOW</sub>	SCL LOW Period	Standard Mode		4.7		μs
		Fast Mode		1.3		μs
		High-Speed Mode, C <sub>B</sub> ≤ 100 pF		160		ns
		High-Speed Mode, C <sub>B</sub> ≤ 400 pF		320		ns
t <sub>HIGH</sub>	SCL HIGH Period	Standard Mode		4		μs
		Fast Mode		600		ns
		High-Speed Mode, C <sub>B</sub> ≤ 100 pF		60		ns
		High-Speed Mode, C <sub>B</sub> ≤ 400 pF		120		ns
t <sub>SU;STA</sub>	Repeated START Setup Time	Standard Mode		4.7		μs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
t <sub>SU;DAT</sub>	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		
		High-Speed Mode		10		
t <sub>HD;DAT</sub>	Data Hold Time	Standard Mode	0		3.45	μs
		Fast Mode	0		900	ns
		High-Speed Mode, C <sub>B</sub> ≤ 100 pF	0		70	ns
		High-Speed Mode, C <sub>B</sub> ≤ 400 pF	0		150	ns
t <sub>RCL</sub>	SCL Rise Time	Standard Mode		20+0.1C <sub>B</sub>	1000	ns
		Fast Mode		20+0.1C <sub>B</sub>	300	
		High-Speed Mode, C <sub>B</sub> ≤ 100 pF		10	80	
		High-Speed Mode, C <sub>B</sub> ≤ 400 pF		20	160	
t <sub>FCL</sub>	SCL Fall Time	Standard Mode		20+0.1C <sub>B</sub>	300	ns
		Fast Mode		20+0.1C <sub>B</sub>	300	
		High-Speed Mode, C <sub>B</sub> ≤ 100 pF		10	40	
		High-Speed Mode, C <sub>B</sub> ≤ 400 pF		20	80	
t <sub>RDA</sub> t <sub>RCL1</sub>	SDA Rise Time Rise Time of SCL after a Repeated START Condition and after ACK Bit	Standard Mode		20+0.1C <sub>B</sub>	1000	ns
		Fast Mode		20+0.1C <sub>B</sub>	300	
		High-Speed Mode, C <sub>B</sub> ≤ 100 pF		10	80	
		High-Speed Mode, C <sub>B</sub> ≤ 400 pF		20	160	

Continued on the following page...

## I<sup>2</sup>C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t <sub>FDA</sub>	SDA Fall Time	Standard Mode		20+0.1C <sub>B</sub>	300	ns
		Fast Mode		20+0.1C <sub>B</sub>	300	
		High-Speed Mode, C <sub>B</sub> ≤ 100 pF		10	80	
		High-Speed Mode, C <sub>B</sub> ≤ 400 pF		20	160	
t <sub>SU;STO</sub>	Stop Condition Setup Time	Standard Mode		4		μs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
C <sub>B</sub>	Capacitive Load for SDA, SCL				400	pF

### Timing Diagrams

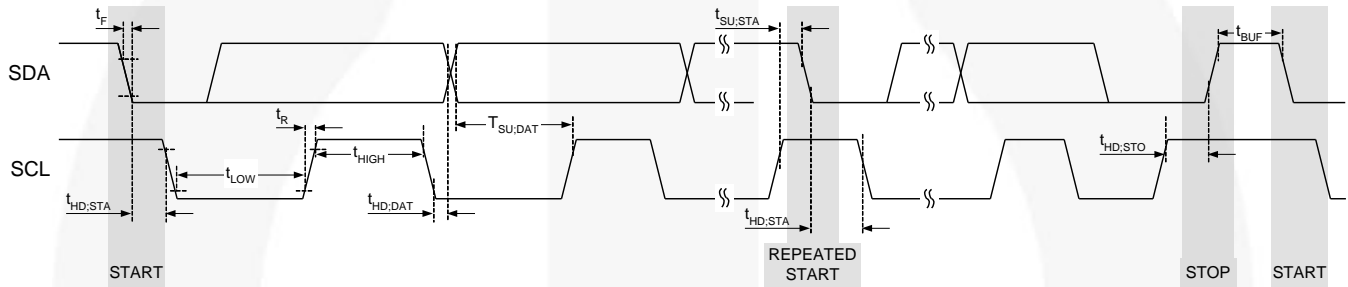
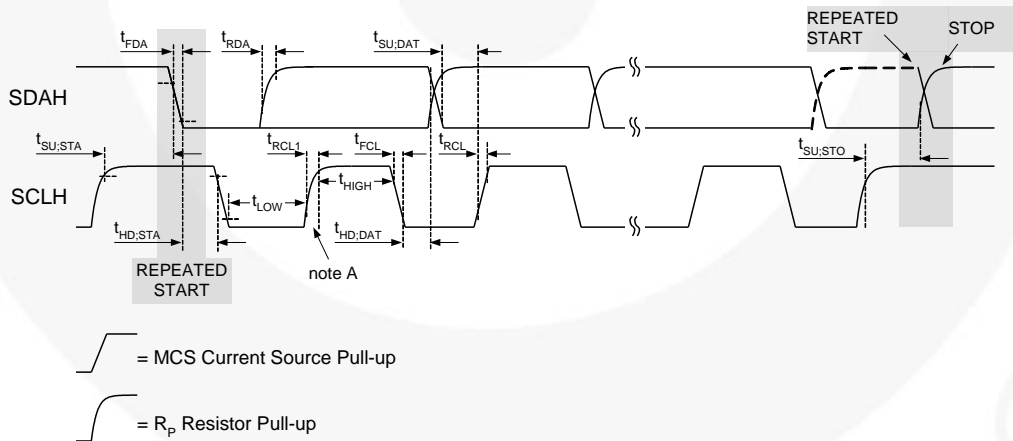


Figure 6. I<sup>2</sup>C Interface Timing for Fast and Slow Modes

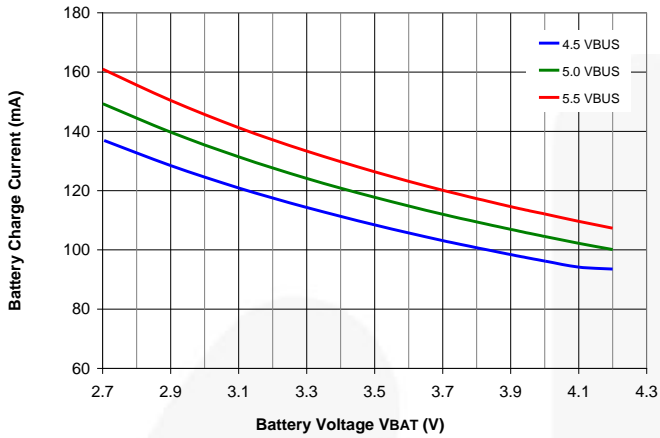


Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

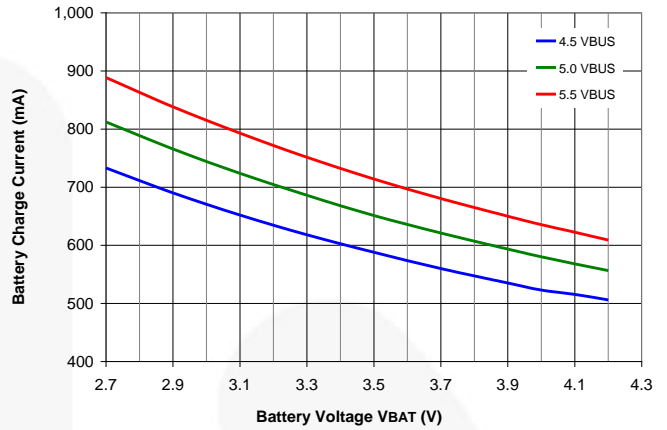
Figure 7. I<sup>2</sup>C Interface Timing for High-Speed Mode

## VBUS Charge Mode Typical Characteristics

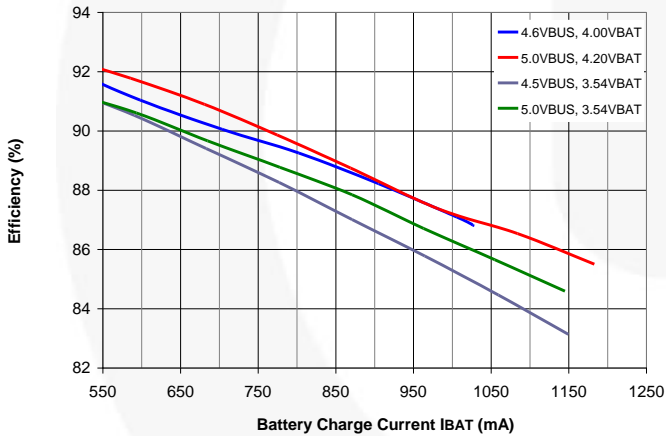
Unless otherwise specified, circuit of Figure 1,  $V_{\text{REG}}=4.2\text{ V}$ ,  $V_{\text{BUS}}=5.0\text{ V}$ , and  $T_{\text{A}}=25^{\circ}\text{C}$ .



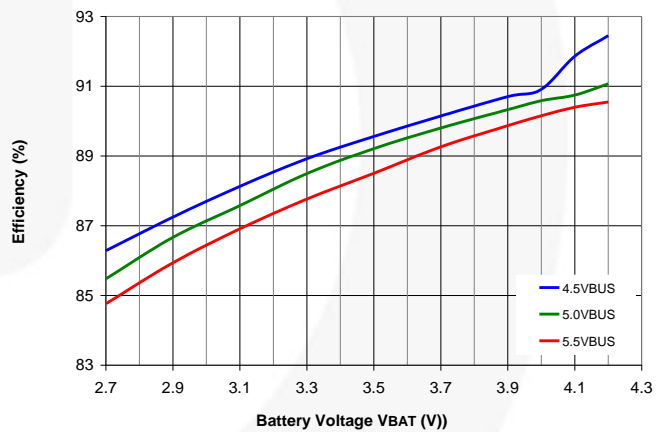
**Figure 8. Battery Charge Current vs.  $V_{\text{BUS}}$  with  $I_{\text{INLIM}}=100\text{ mA}$**



**Figure 9. Battery Charge Current vs.  $V_{\text{BUS}}$  with  $I_{\text{INLIM}}=500\text{ mA}$**



**Figure 10. Charger Efficiency, No  $I_{\text{INLIM}}$ ,  $I_{\text{CHARGE}}=1250\text{ mA}$**



**Figure 11. Charger Efficiency vs.  $V_{\text{BUS}}$ ,  $I_{\text{INLIM}}=500\text{ mA}$**

## VBUS Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1,  $V_{\text{REG}}=4.2\text{ V}$ ,  $V_{\text{BUS}}=5.0\text{ V}$ , and  $T_{\text{A}}=25^{\circ}\text{C}$ .

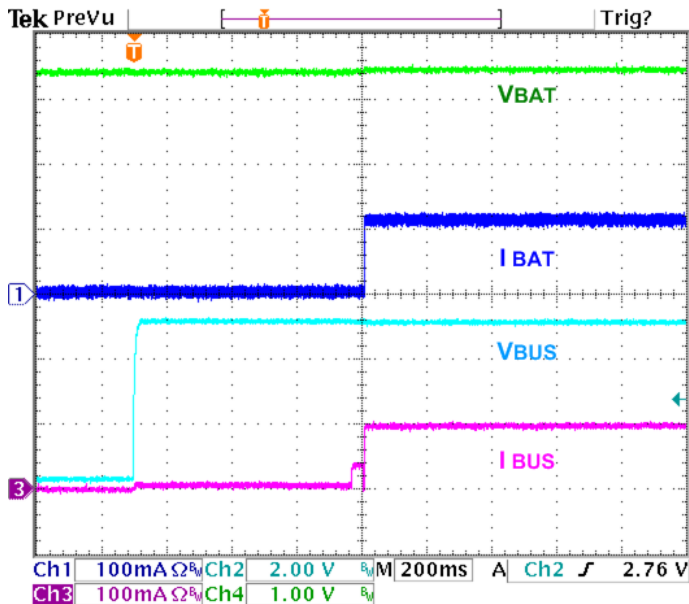


Figure 12. Auto-Charge Startup at  $V_{\text{BUS}}$  Plug-in,  $I_{\text{INLIM}}=100\text{ mA}$ ,  $\text{OTG}=1$ ,  $V_{\text{BAT}}=3.4\text{ V}$

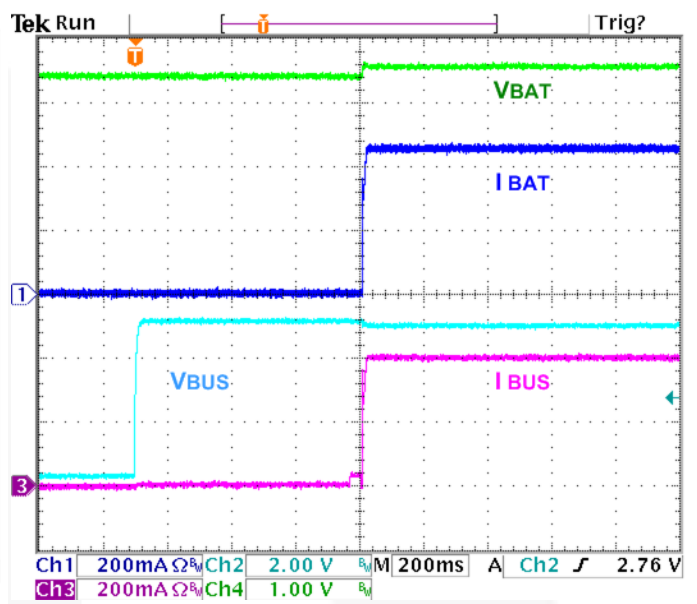


Figure 13. Auto-Charge Startup at  $V_{\text{BUS}}$  Plug-in,  $I_{\text{INLIM}}=500\text{ mA}$ ,  $\text{OTG}=1$ ,  $V_{\text{BAT}}=3.4\text{ V}$

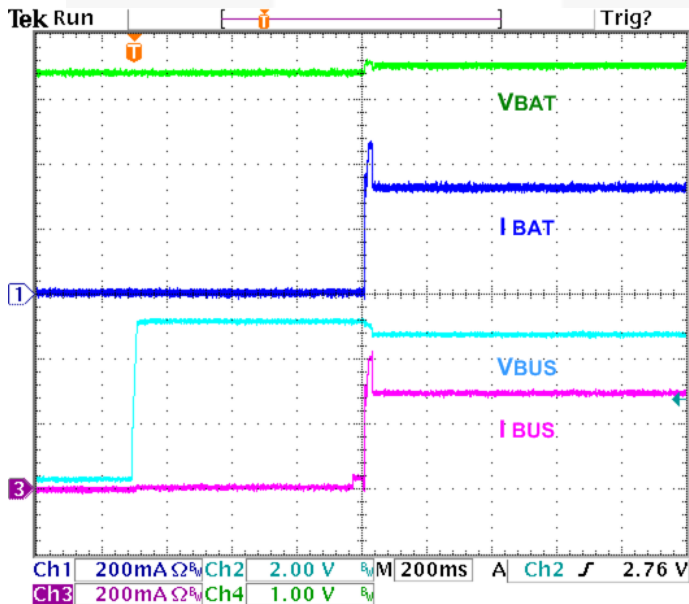


Figure 14. AutoCharge Startup with 300 mA Limited Charger / Adaptor,  $I_{\text{INLIM}}=500\text{ mA}$ ,  $\text{OTG}=1$ ,  $V_{\text{BAT}}=3.4\text{ V}$

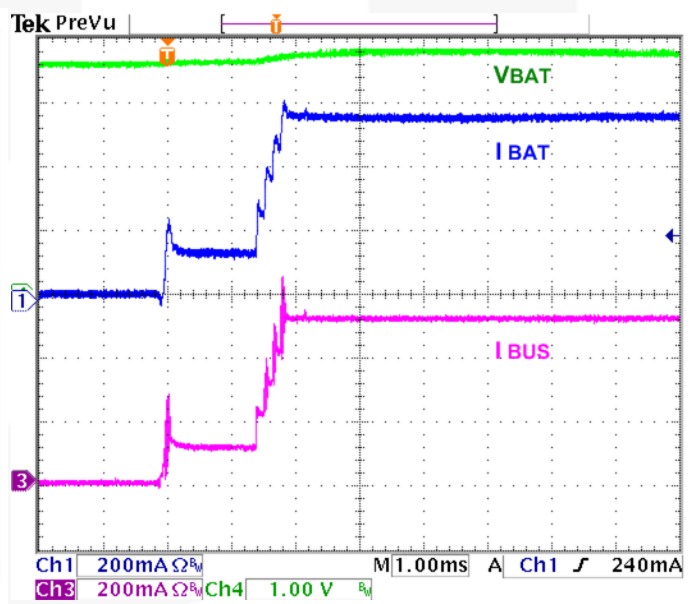


Figure 15. Charger Startup with HZ\_MODE Bit Reset,  $I_{\text{INLIM}}=500\text{ mA}$ ,  $I_{\text{OCHARGE}}=950\text{ mA}$ ,  $V_{\text{REG}}=4.2\text{ V}$ ,  $V_{\text{BAT}}=3.6\text{ V}$

## VBUS Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1,  $V_{\text{REG}}=4.2\text{ V}$ ,  $V_{\text{BUS}}=5.0\text{ V}$ , and  $T_{\text{A}}=25^{\circ}\text{C}$ .

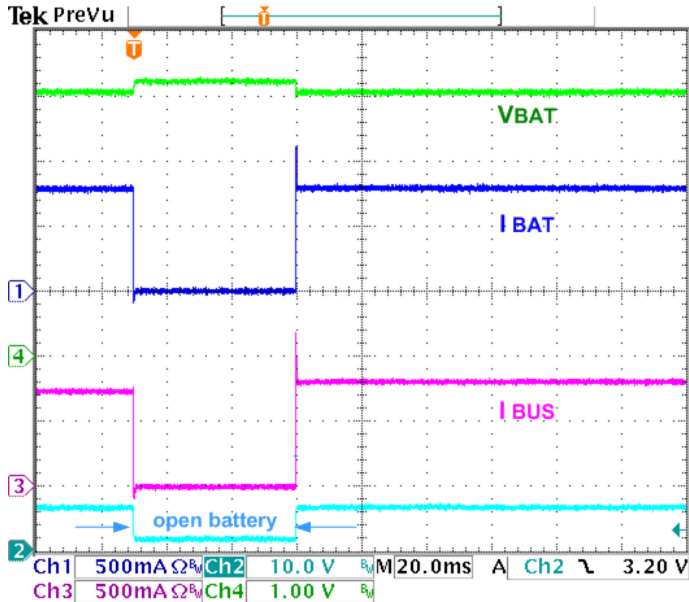


Figure 16. Battery Removal / Insertion during Charging,  $V_{\text{BAT}}=3.9\text{ V}$ ,  $I_{\text{CHARGE}}=950\text{ mA}$ , No  $I_{\text{INLIM}}$ ,  $\text{TE}=0$

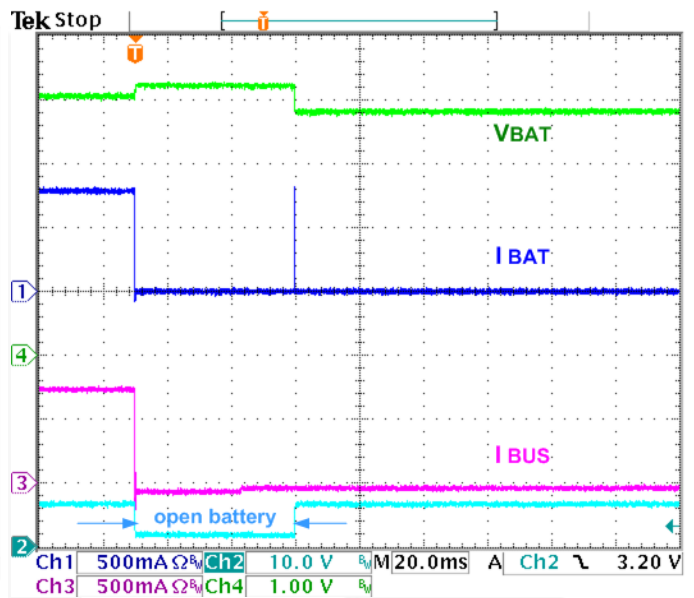


Figure 17. Battery Removal / Insertion during Charging,  $V_{\text{BAT}}=3.9\text{ V}$ ,  $I_{\text{CHARGE}}=950\text{ mA}$ , No  $I_{\text{INLIM}}$ ,  $\text{TE}=1$

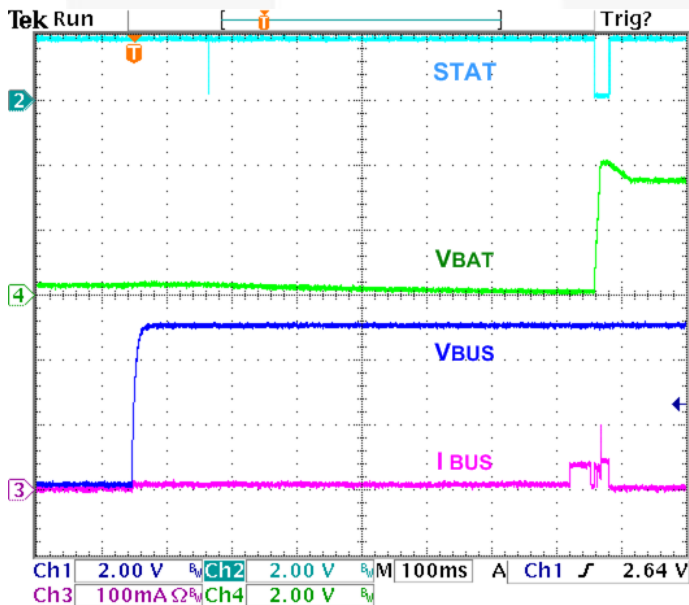


Figure 18. No Battery at  $V_{\text{BUS}}$  Power-up

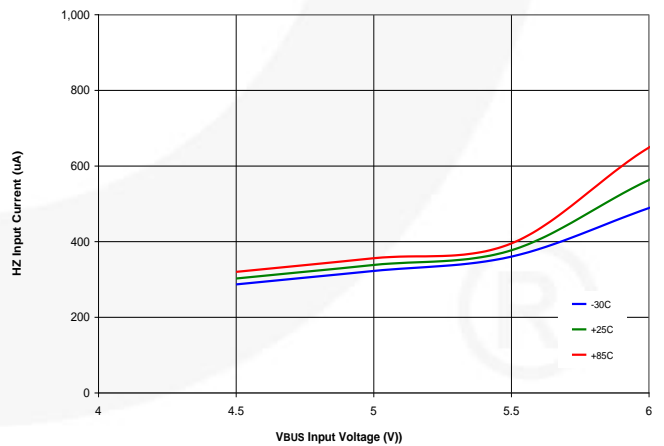


Figure 19. VBUS Current in High-Impedance Mode with Battery Open



## VIN Charger Characteristics

Unless otherwise specified, circuit of Figure 1,  $V_{OREG} = 4.2\text{ V}$ ,  $V_{IN} = 5.0\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

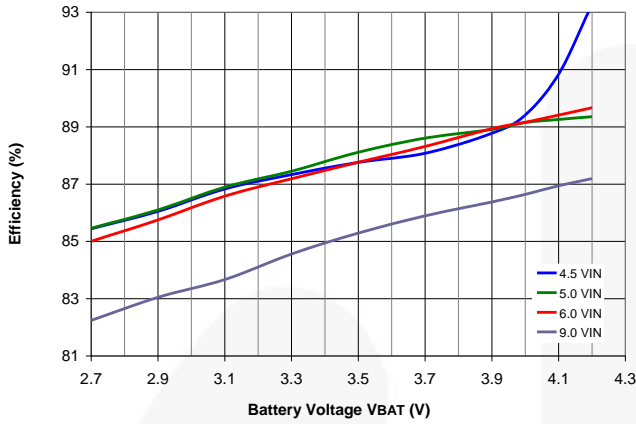


Figure 20. Charger Efficiency,  $I_{CHARGE}=950\text{ mA}$

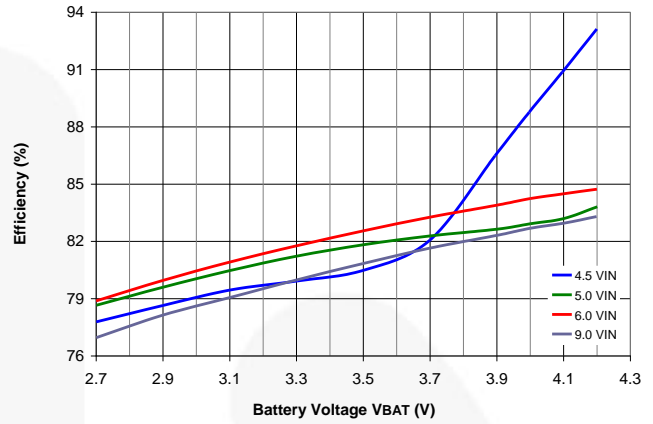


Figure 21. Charger Efficiency,  $I_{CHARGE}=1550\text{ mA}$

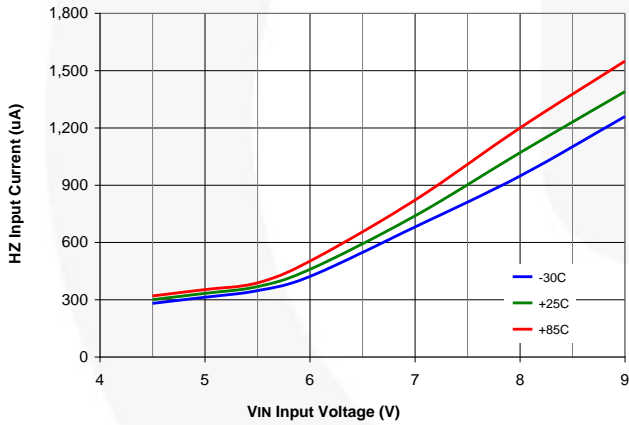


Figure 22.  $V_{IN}$  Current in High-Impedance Mode,  $V_{BAT}=3.6\text{ V}$

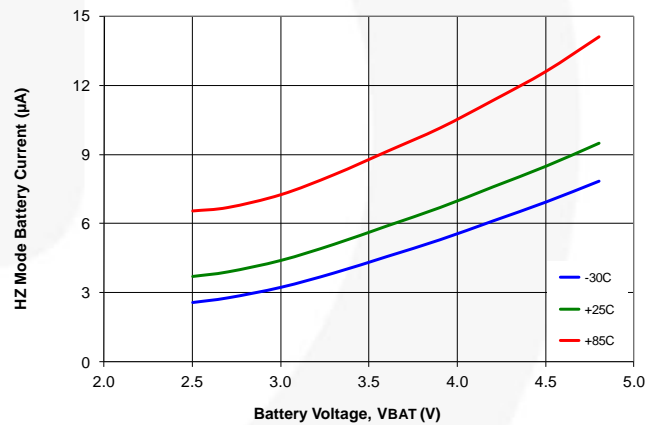


Figure 23. Battery Current in High-Impedance Mode,  $V_{BUS}=\text{Open}$ ,  $V_{IN}=\text{Open}$

## VIN Charger Characteristics

Unless otherwise specified, circuit of Figure 1,  $V_{OREG} = 4.2\text{ V}$ ,  $V_{IN} = 5.0\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

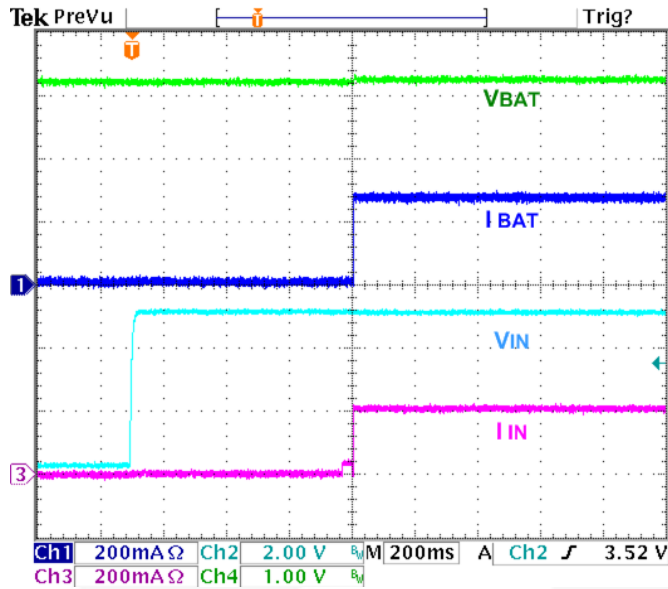


Figure 24. Auto-Charge Startup at  $V_{IN}$  Plug-in,  $V_{BAT}=3.2\text{ V}$ ,  $IO\_LEVELV = 1$

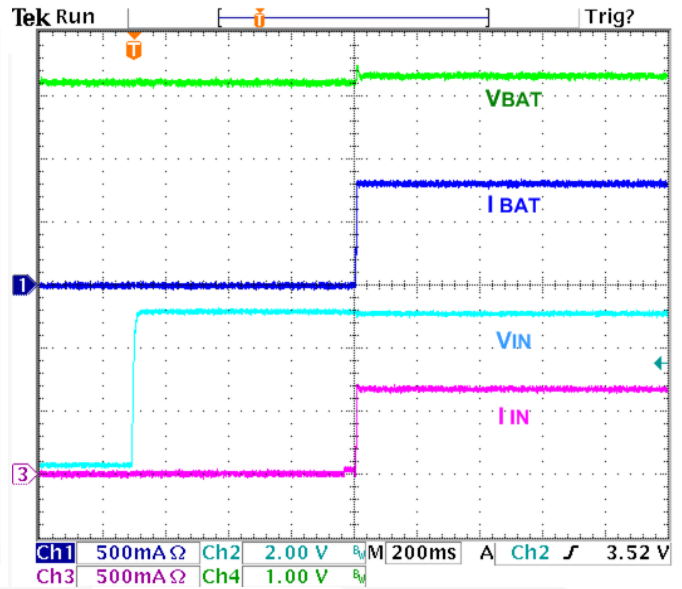


Figure 25. Auto-Charge Startup at  $V_{IN}$  Plug-in,  $V_{BAT}=3.2\text{ V}$ ,  $IOCHARGE=950\text{ mA}$

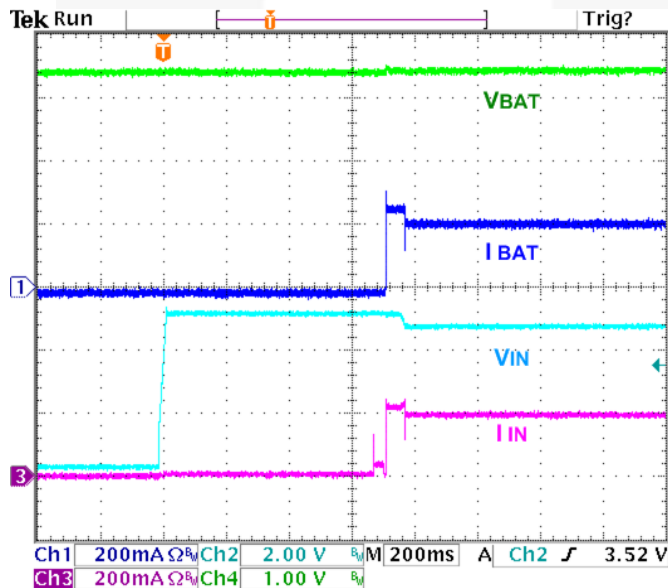


Figure 26. Auto-Charge Startup with 200 mA Limited Charger / Adaptor,  $V_{BAT}=3.4\text{ V}$

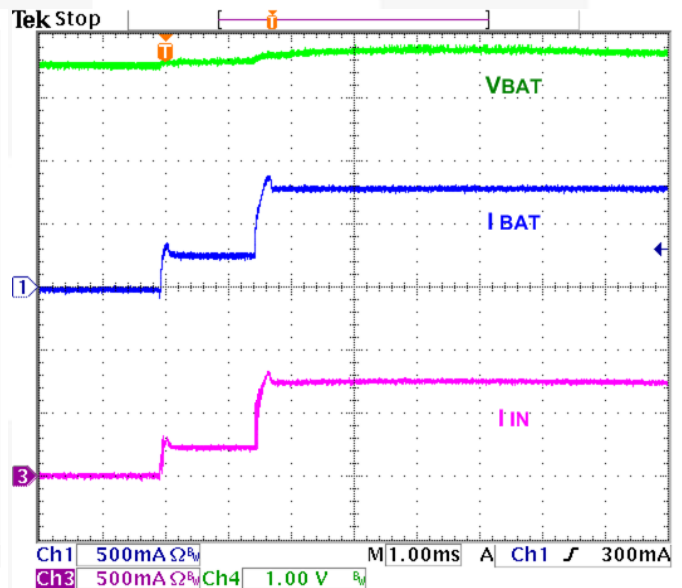


Figure 27. Charger Startup with  $HZ\_MODE$  Bit Reset,  $IOCHARGE=950\text{ mA}$ ,  $V_{OREG}=4.2\text{ V}$ ,  $V_{BAT}=3.6\text{ V}$

## VIN Charger Characteristics

Unless otherwise specified, circuit of Figure 1,  $V_{OREG} = 4.2\text{ V}$ ,  $V_{IN} = 5.0\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

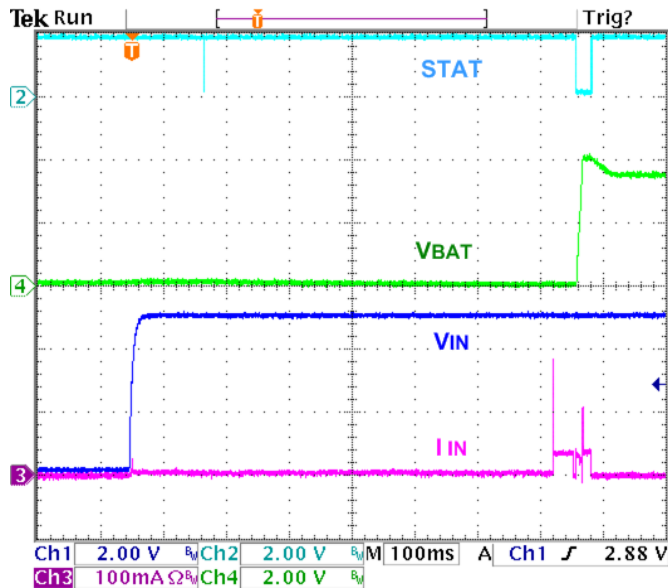


Figure 28. No Battery at  $V_{IN}$  Power-up

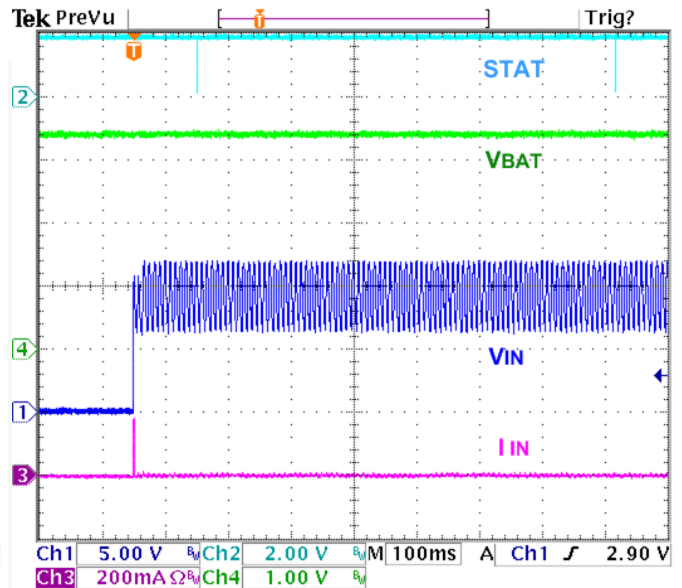


Figure 29. Non-Compliant Charger Rejection,  $V_{BAT} = 3.4\text{ V}$

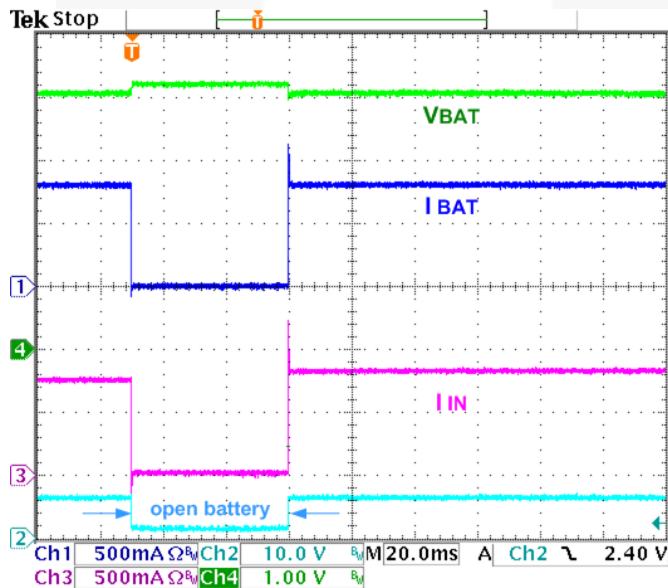


Figure 30. Battery Removal / Insertion During Charging,  $V_{BAT} = 3.9\text{ V}$ ,  $I_{CHARGE} = 950\text{ mA}$ ,  $TE = 0$

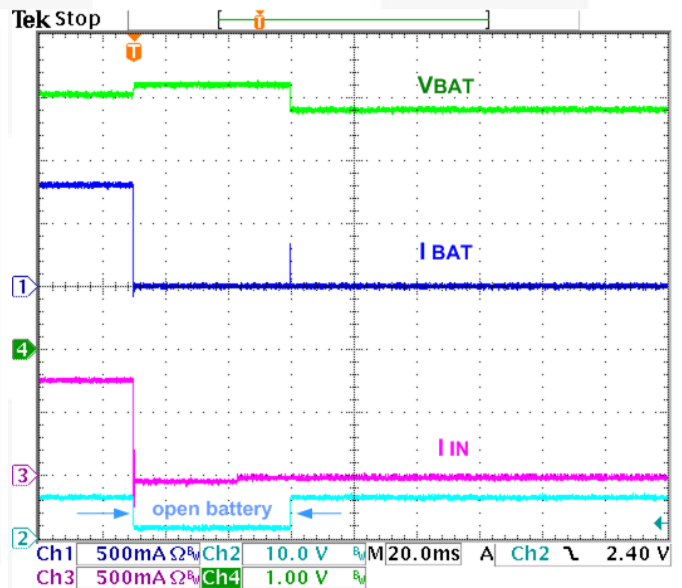


Figure 31. Battery Removal / Insertion During Charging,  $V_{BAT} = 3.9\text{ V}$ ,  $I_{CHARGE} = 950\text{ mA}$ ,  $TE = 1$

## Boost Mode Typical Characteristics

Unless otherwise specified, using the circuit of Figure 1,  $V_{BAT}=3.6\text{ V}$ ,  $T_A=25^\circ\text{C}$ .

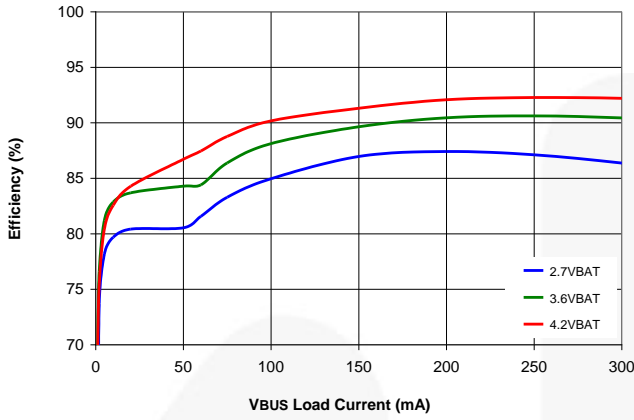


Figure 32. Efficiency vs.  $V_{BAT}$

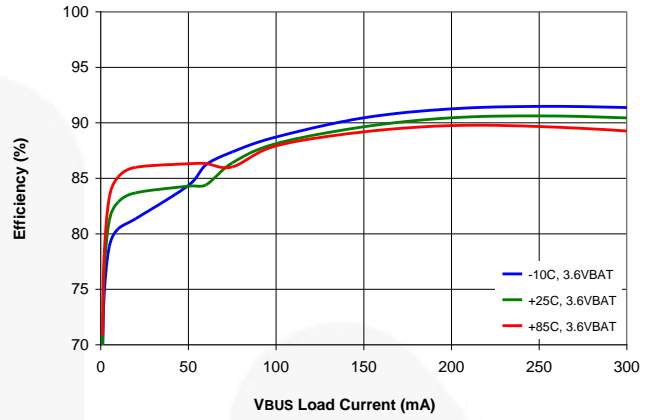


Figure 33. Efficiency Over Temperature

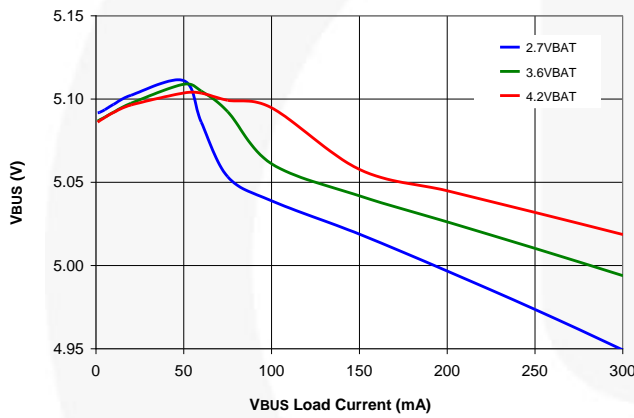


Figure 34. Output Regulation vs.  $V_{BAT}$

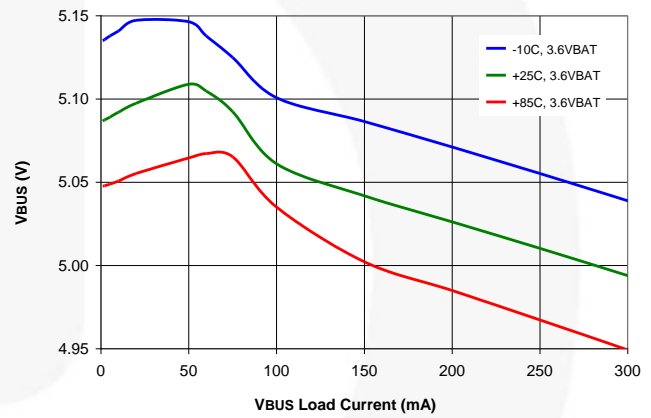


Figure 35. Output Regulation Over Temperature

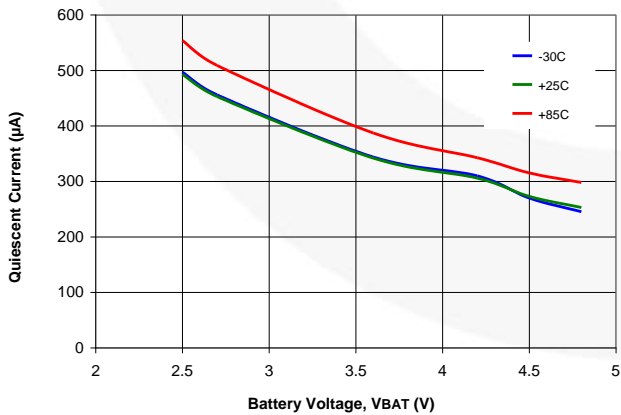


Figure 36. Quiescent Current

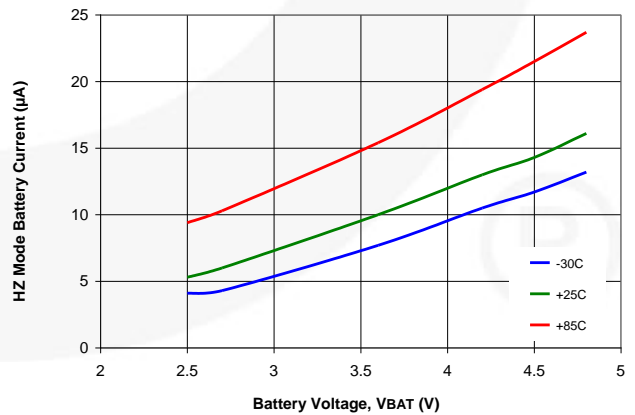


Figure 37. High-Impedance Mode Battery Current

## Boost Mode Typical Characteristics

Unless otherwise specified, using the circuit of Figure 1,  $V_{BAT}=3.6\text{ V}$ ,  $T_A=25^\circ\text{C}$ .

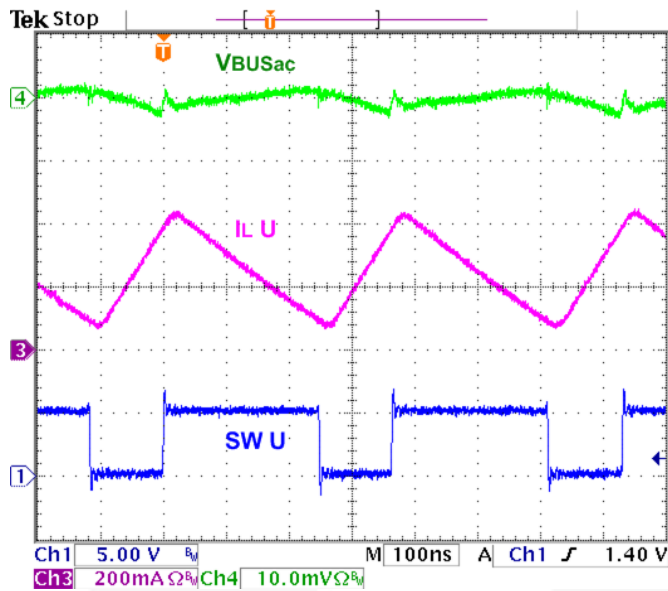


Figure 38. Boost PWM Waveform

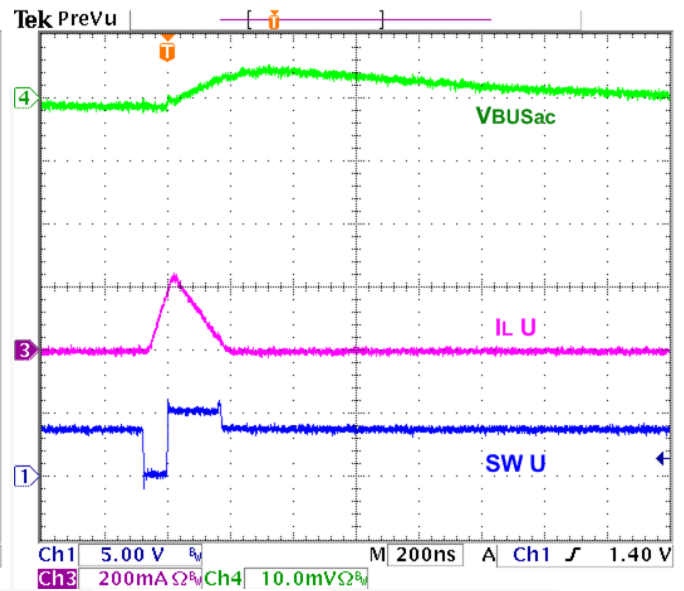


Figure 39. Boost PFM Waveform

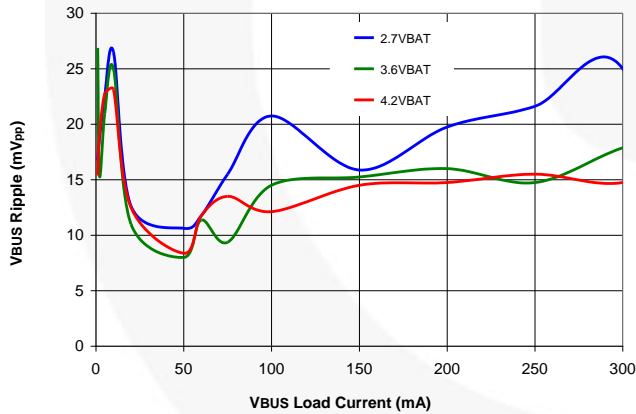


Figure 40. Output Ripple vs.  $V_{BAT}$

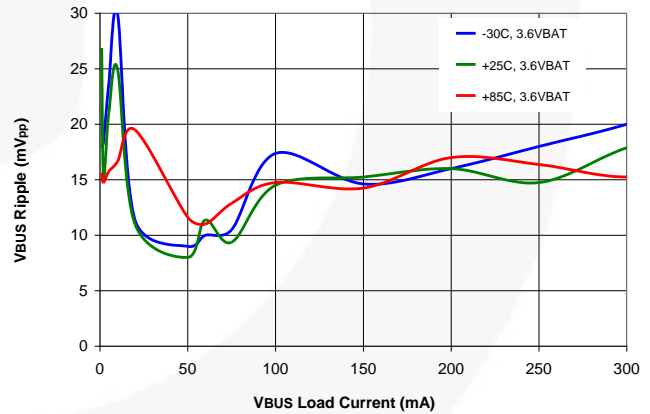


Figure 41. Output Ripple vs. Temperature

## Boost Mode Typical Characteristics

Unless otherwise specified, using the circuit of Figure 1,  $V_{BAT}=3.6\text{ V}$ ,  $T_A=25^\circ\text{C}$ .

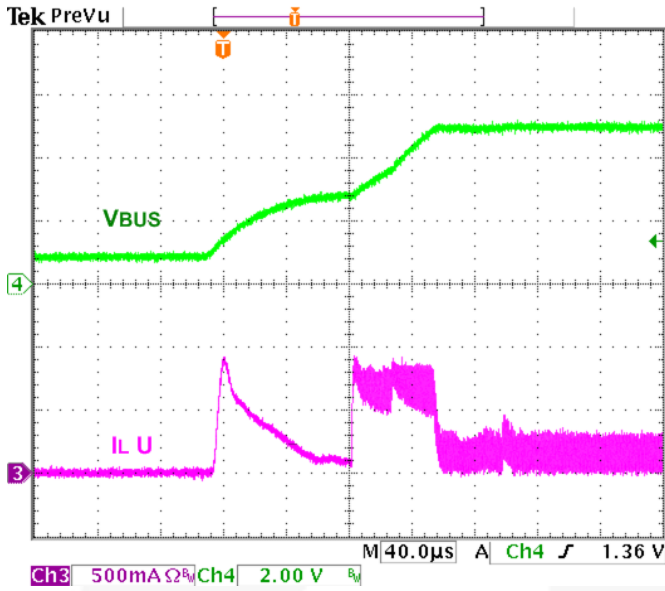


Figure 42. Startup, 3.6  $V_{BAT}$ , 50  $\Omega$  Load, Additional 10  $\mu\text{F}$ , X5R Across VBUS

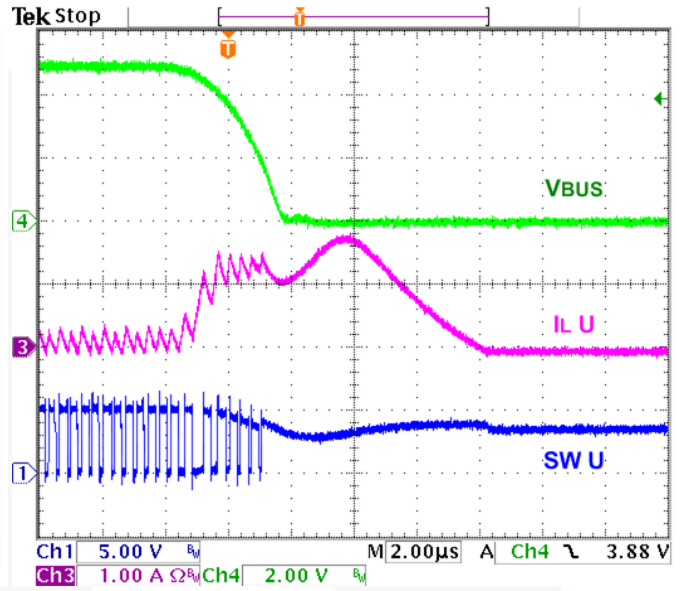


Figure 43.  $V_{BUS}$  Fault Response, 3.6  $V_{BAT}$

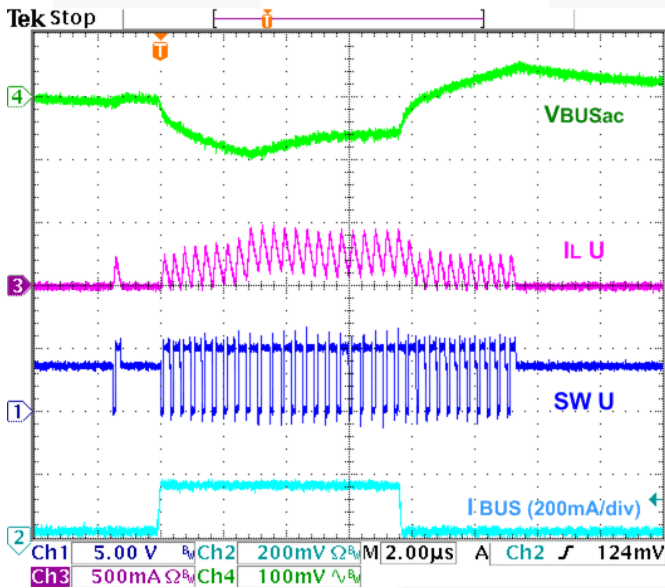


Figure 44. Load Transient, 5-155-5 mA,  $t_R=t_F=100\text{ ns}$

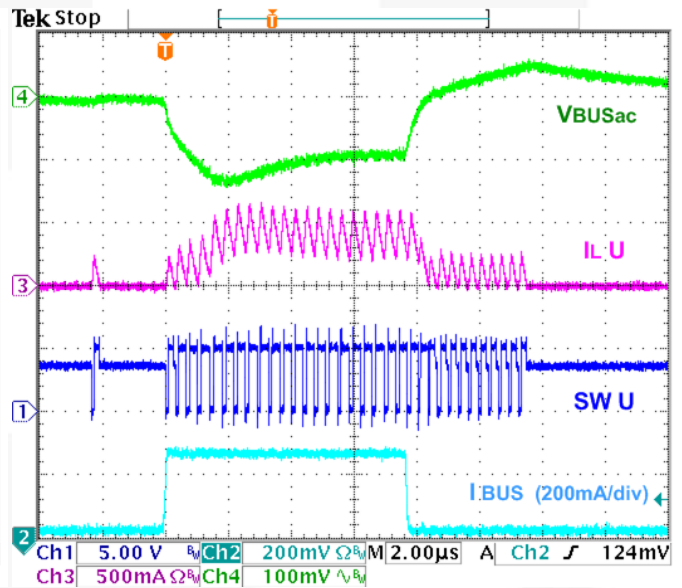


Figure 45. Load Transient, 5-255-5 mA,  $t_R=t_F=100\text{ ns}$

## Circuit Description / Overview

When charging batteries with a current-limited input source, such as USB, a switching charger's high efficiency over a wide range of output voltages minimizes charging time.

The FAN54300 combines two highly integrated synchronous buck regulators for charging from two separate power sources. The IC also includes a synchronous boost regulator, which can supply 5 V to USB On-The-Go (OTG) peripherals. The regulator employs synchronous rectification for both the charger and boost regulators to maintain high efficiency over a wide range of battery voltages and charge states.

In addition to its USB (VBUS) input, the FAN54300 allows a second power source (VIN) to be used for charging. This input source is typically a "wall wart" and can be up to 9.5 V input.

The FAN54300 has three operating modes:

- **Charge Mode:**  
Charges a single-cell Li-Ion or Li-polymer battery.
- **Boost Mode:**  
Provides 5 V power to USB-OTG with an integrated synchronous rectification boost regulator using the battery as input.
- **High-Impedance Mode:**  
Both the boost and charging circuits are off in this mode. Current flow from PWRIN (the charging power source) to the battery, or from the battery to PWRIN, are blocked in this mode. This mode consumes very little current from PWRIN or the battery.

When the IC is charging the battery from VIN, the boost regulator may be simultaneously enabled to supply 5 V for OTG peripherals.

## Charge Mode

In Charge Mode, FAN54300 employs five regulation loops:

1. VBUS input current: Limits the amount of current drawn from VBUS. This current is sensed internally and can be programmed through the I<sup>2</sup>C interface
2. Charging current: Limits the maximum charging current. This current is sensed using an external R<sub>SENSE</sub> resistor.
3. Charge voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage rises, the battery's internal impedance and R<sub>SENSE</sub> works in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the voltage across R<sub>SENSE</sub> drops below the I<sub>TERM</sub> threshold.
4. Temperature: If the IC's junction temperature reaches 120°C, charge current is continuously reduced until the IC's temperature stabilizes at 120°C.
5. An additional loop limits the amount of drop on VBUS or VIN to a programmable voltage (V<sub>SP</sub>) to accommodate current-limited wall chargers.

## Input Source Selection

The FAN54300 selects the power source (PWRIN) for charging according to the following criteria.

**Table 3. PWRIN: Charging Power Input Source Selection**

V <sub>IN</sub>	V <sub>BUS</sub>	PWRIN
VALID	INVALID	V <sub>IN</sub>
INVALID	VALID	V <sub>BUS</sub>
VALID	VALID	V <sub>IN</sub>

If charging is in progress with V<sub>BUS</sub> and V<sub>IN</sub> becomes valid, charging from VBUS stops and charging continues from V<sub>IN</sub>. Charging stops if HZ\_VIN is set when V<sub>IN</sub> becomes valid while charging with V<sub>BUS</sub>.

If VIN and VBUS are both connected and t<sub>15MIN</sub> expires, both CE# bits are set. To reinitiate t<sub>15MIN</sub> charging (autocharge) with a weak battery, both power sources must be unplugged, then a valid power source plugged in. If only one of the two connected sources are removed then connected with a weak battery, both CE# bits remain set.

## Fault Reporting and Register Reset

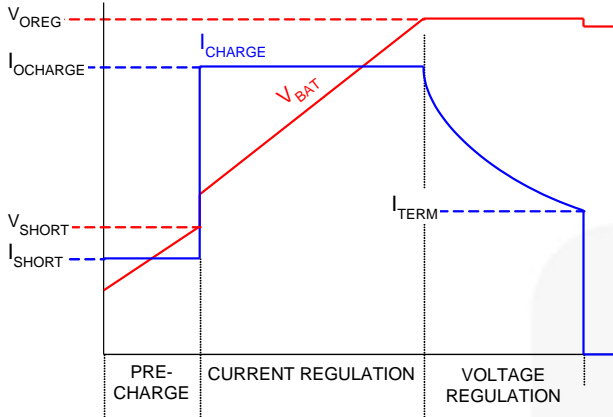
All faults that occur during charging or boost are reported only in the STATUS register (R0) associated with the active charging source at the time of the fault. Any register reset that occurs due to t<sub>32SEC</sub> overflow resets only the registers associated with the active charging source.

For example: Assume the IC is charging in 32-Second Mode with V<sub>IN</sub> as a source. The processor stops setting TMR\_RST, so t<sub>32SEC</sub> expires. The IC then resets only the \_V registers and goes into 15-Minute Mode charging with V<sub>IN</sub>. A timer fault is enunciated, but reported in the CONTROL0\_V register. CONTROL0\_U is unaffected by this event. When the t<sub>15MIN</sub> timer expires, the IC sets the CE#\_V bit, but leaves the CE#\_U bit unchanged.

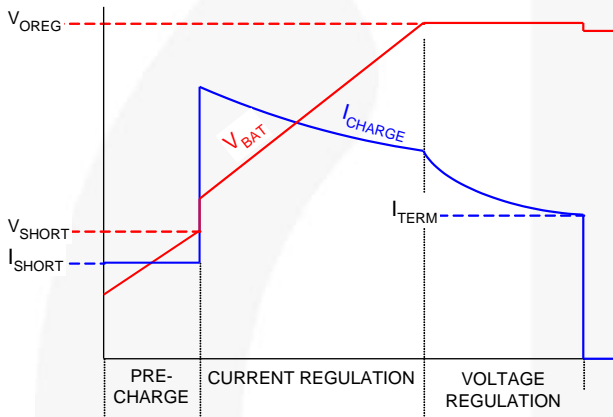
## Battery Charging Curve

If the battery voltage is below V<sub>SHORT</sub>, a linear current source "pre-charges" the battery until V<sub>BAT</sub> reaches V<sub>SHORT</sub>. The PWM charging circuits are then started and the battery is charged with a constant current if sufficient input power is available. The current slew rate is limited to prevent overshoot.

The FAN54300 is designed to work with a current-limited input source at PWRIN. During the current regulation phase of charging, PWRIN current limitations or the programmed charging current limit the amount of current available to charge the battery and power the system. The effect of input power limitations on I<sub>CHARGE</sub> can be seen in Figure 47.



**Figure 46. Charge Curve when PWRIN Limitations Don't Limit  $I_{CHARGE}$**



**Figure 47. Charge Curve when PWRIN Limits  $I_{CHARGE}$**

PWRIN limitations are controlled either by:

- **IBUSLIM:** These bits set the maximum amount of current that the charger draws from  $V_{BUS}$ ; OR
- **SP\_CHARGER:** For power-limited chargers, the FAN54300 limits current draw when the charging source drops to the voltage programmed by the SP\_CHARGER bits. This allows “travel adapters” to be accommodated without host software overhead. The SP\_CHARGER control loop applies to both  $V_{IN}$  and  $V_{BUS}$ .

Assuming  $V_{OREG}$  is programmed to the cell's fully charged “float” voltage, the current the battery accepts with the PWM regulator limiting its output (sensed at  $V_{BAT}$ ) to  $V_{OREG}$  declines and the charger enters the voltage regulation phase of charging. When the current declines to the programmed  $I_{TERM}$  value, the charge cycle is complete. Charge current termination can be disabled by resetting the TE bit.

### Charger Programmability

Throughout this document, any parameter that ends in “U” applies when charging from  $V_{BUS}$  and any parameter ending in “V” applies when charging from  $V_{IN}$ . Parameters set with slave address D6 are applied when charging from  $V_{BUS}$ . Parameters set with slave address D4 are applied when charging from  $V_{IN}$ .

The following charging and input power control parameters can be programmed by the host through  $I^2C$ .

**Table 4. Programmable Charging Parameters**

Parameter	Charging Source	Name	Register
Output Voltage Regulation	Either	OREG	REG2[7:2]
Battery Charging Current Limit	$V_{BUS}$	ICHGU	REG4[6:4]
	$V_{IN}$	ICHGV	REG4[6:3]
Input Current Limit	$V_{BUS}$	IBUSLIM	REG1[7:6]
Charge Termination Limit	Either	ITERM	REG4[2:0]
Special Charger Minimum Voltage	Either	VSP	REG5[2:0]

The charger output or “float” voltage can be programmed by the OREG bits from 3.5 V to 4.44 V in 20 mV increments.

**Table 5. OREG Bits ( REG2 [7:2] ) vs. Charger  $V_{OUT}$  ( $V_{OREG}$ ) Float Voltage**

Decimal	Hex	VOREG	Decimal	Hex	VOREG
0	00	3.50	32	20	4.14
1	01	3.52	33	21	4.16
<b>2</b>	<b>02</b>	<b>3.54</b>	34	22	4.18
3	03	3.56	35	23	4.20
4	04	3.58	36	24	4.22
5	05	3.60	37	25	4.24
6	06	3.62	38	26	4.26
7	07	3.64	39	27	4.28
8	08	3.66	40	28	4.30
9	09	3.68	41	29	4.32
10	0A	3.70	42	2A	4.34
11	0B	3.72	43	2B	4.36
12	0C	3.74	44	2C	4.38
13	0D	3.76	45	2D	4.40
14	0E	3.78	46	2E	4.42
15	0F	3.80	47	2F	4.44
16	10	3.82	48	30	4.44
17	11	3.84	49	31	4.44
18	12	3.86	50	32	4.44
19	13	3.88	51	33	4.44
20	14	3.90	52	34	4.44
21	15	3.92	53	35	4.44
22	16	3.94	54	36	4.44
23	17	3.96	55	37	4.44
24	18	3.98	56	38	4.44
25	19	4.00	57	39	4.44
26	1A	4.02	58	3A	4.44
27	1B	4.04	59	3B	4.44
28	1C	4.06	60	3C	4.44
29	1D	4.08	61	3D	4.44
30	1E	4.10	62	3E	4.44
31	1F	4.12	63	3F	4.44

**Note:**

6. All register default settings are noted by **bold typeface**.



## Charge Initiation

A new charge cycle begins when one of the following occurs:

- The battery voltage falls below  $V_{OREG} - V_{RCH}$
- A power source is connected (PWRIN POR) and battery voltage is below the weak-battery threshold ( $V_{LOWV}$ ).
- CE# and HZ\_MODE are both cleared, after having been set, and a power source is connected.

## Charge Current Limit

The default charge current is limited by the IOLEVEL bit (REG5[5]). When this bit is set (default), charge current is limited to 325 mA (22.1 mV across  $R_{SENSE}$ ) and the ICHG bits are ignored. Resetting IOLEVEL allows the ICHG bits to control the battery charge current limit.

Any attempt to write a value higher than 10 (0AH) results in a value of 10 (0AH) written to the ICHGV bits (see Table 24).

## Charge Termination Current Limit

Current charge termination is enabled when TE (REG1[3]) = 1. The current level is control by the ITERM bits (REG4[2:0]).

## PWM Controller in Charge Mode

The IC uses a current-mode PWM controller to regulate the output voltage and battery charge currents. A cycle-by-cycle current limit of nominally 2.3 A, sensed through Q1, is used to terminate  $t_{ON}$ . The synchronous rectifier, Q2, also has a current limit that turns off Q2 at 160mA to prevent current flow from the battery.

When the charge current drops below ~20 mA; the IC runs in Asynchronous Mode, which prevents reverse current from pumping up the input source.

## Safety Timer (see Figure 52)

At the beginning of the charging process, the IC starts the 15-minute timer ( $t_{15MIN}$ ). When this timer expires, charging is terminated and the CE# bit is set. Writing to any register through I<sup>2</sup>C stops the  $t_{15MIN}$  timer, which, in turn, starts a 32-second timer ( $t_{32SEC}$ ). Setting the TMR\_RST bit (REG0[1]) resets the  $t_{32SEC}$  timer. If the  $t_{32SEC}$  timer times out, all registers (except SAFETY) are set to their default values, a Timer Fault (110) is reported in the fault register, and charging resumes using the default values with the  $t_{15MIN}$  timer running.

Since there is only one  $t_{32SEC}$  timer on the IC, writing to either TMR\_RST bit in either CONTROL0\_U or CONTROL0\_V resets the timer. The  $t_{32SEC}$  timer starts with an I<sup>2</sup>C WRITE to either slave address. Timer faults are reported in both U and V registers. A  $t_{32SEC}$  fault resets U and V registers 1 – 5.

Normally, charging is controlled by the host with the  $t_{32SEC}$  timer running to ensure that the host is active. Charging with the  $t_{15MIN}$  timer running is used for charging that is unattended by the host, which would occur when  $V_{BAT}$  is insufficient to power the host processor. If the 15-minute timer expires, the IC turns off the charger and indicates a timer fault (110) on the FAULT bits (REG0[2:0]). This prevents overcharge if the host fails to reset the  $t_{32SEC}$  timer. The CE# bit is set in the registers where the power sources are connected. For example, if VIN and VBUS are both connected when the  $t_{15MIN}$  timer expires, CE#\_V and CE\_U are both set.

## Reset Bit

Setting the RESET bit (Reg4[7]) resets all registers for the slave address used to set the RESET bit. When the RESET bit is set, the  $t_{32SEC}$  timer is reset and stopped, charging stops and the IC goes to Charge Configuration Mode (see Figure 50). If  $V_{BAT} < V_{OREG}$ , charging begins in 15-Minute Mode 262 ms after the RESET bit is set.

## PWRIN Validation, Notification, and Non-Compliant Power Source Rejection

Whenever either VBUS\_CON or VIN\_CON bits have been set, the STAT pin pulses to notify the host processor of a change in status on the input power supply.

Before attempting to charge, the IC attempts to validate its input source by loading the appropriate source with 110  $\Omega$  to ensure that the source stays between 4.4 V and  $V_{IN_{OVP}}$  for 32 ms. If the input source fails validation, STAT enunciates a fault and the fault bits are set according to the condition of the input source (OVP or poor input source). The PWRIN validation sequence always occurs before charging is initiated or re-initiated (for example, after a PWRIN OVP fault, a  $V_{RCH}$  recharge initiation, or resetting the HZ bit). The 32 ms validation time ensures that unfiltered 50/60 Hz chargers and other non-compliant chargers are rejected.

## 2.5 V Regulator Operation

When the VIN\_CON bit is set, indicating that the VIN power source has been plugged in, the V2V5 regulator is enabled.

## USB-Friendly Boot Sequence (see Figure 48)

At PWRIN POR, when the battery voltage is above the weak-battery threshold ( $V_{LOW}$ ), the IC goes into Charge Configuration Mode unless the  $t_{32SEC}$  timer is enabled by an I<sup>2</sup>C write. In that case, the IC begins to charge with the existing register settings.

If  $V_{BAT} < V_{LOW}$ , the IC goes into Charge Configuration Mode if the  $t_{32SEC}$  timer is not enabled. If  $V_{BAT} < V_{OREG}$ , the registers reset and charging begins in 15-Minute Mode. During 15-Minute Mode, the charger uses an input current limit controlled by the OTG pin when charging from VBUS (100mA if OTG is LOW and 500mA if OTG is HIGH).

Even if charging from VIN, the charging current is limited to 325 mA (22.14 mV across 68m $\Omega$ ) after the registers are reset. This feature can revive a cell whose voltage is too low for reliable host operation until the battery has sufficient charge for the host to boot up and set charge parameters. Charging continues in the absence of host communication even after the battery has reached  $V_{OREG}$ , with a default value of 3.54 V, and the charger remains active until  $t_{15MIN}$  times out.

Once the host processor begins writing to the IC, charging parameters are set by the host, which must continually reset the  $t_{32SEC}$  timer to continue charging using programmed charging parameters. If  $t_{32SEC}$  times out, the register defaults are loaded, the FAULT bits are set to 110, STAT is pulsed, and charging continues with default charge parameters.

At PWRIN POR, if  $V_{BAT} < V_{LOW}$  and HZ or CE# were set previously, the IC goes into HZ state, which causes the registers to reset, clearing the HZ and CE# bits when  $t_{32SEC}$  expires and beginning  $t_{15MIN}$  charging unless the host processor sets the TMR\_RST bit.

### VBUS Current Limiting

To minimize charging time without overloading VBUS's current limitations, the IC's VBUS current limit can be programmed with the IBUSLIM bits ( REG1[7:6] ).

The OTG pin establishes the VBUS current limit during 15-Minute Mode charging.

### Operational Flow Charts

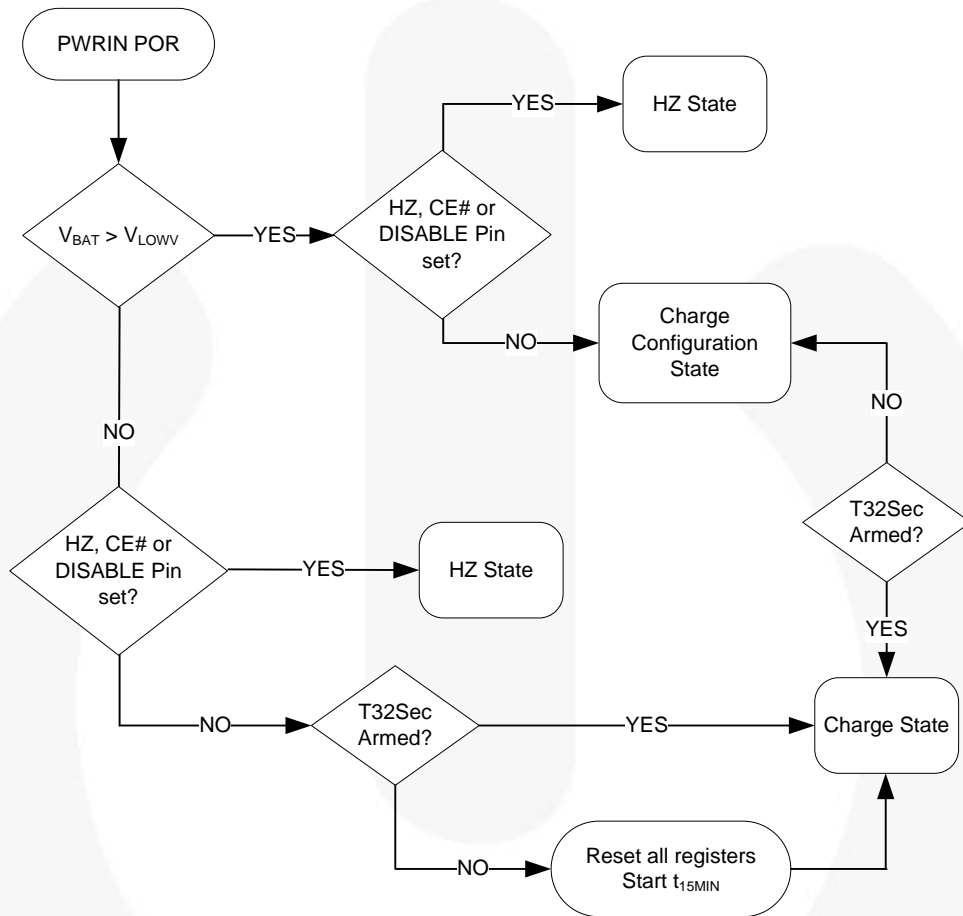


Figure 48. Charger PWRIN POR Flow Chart



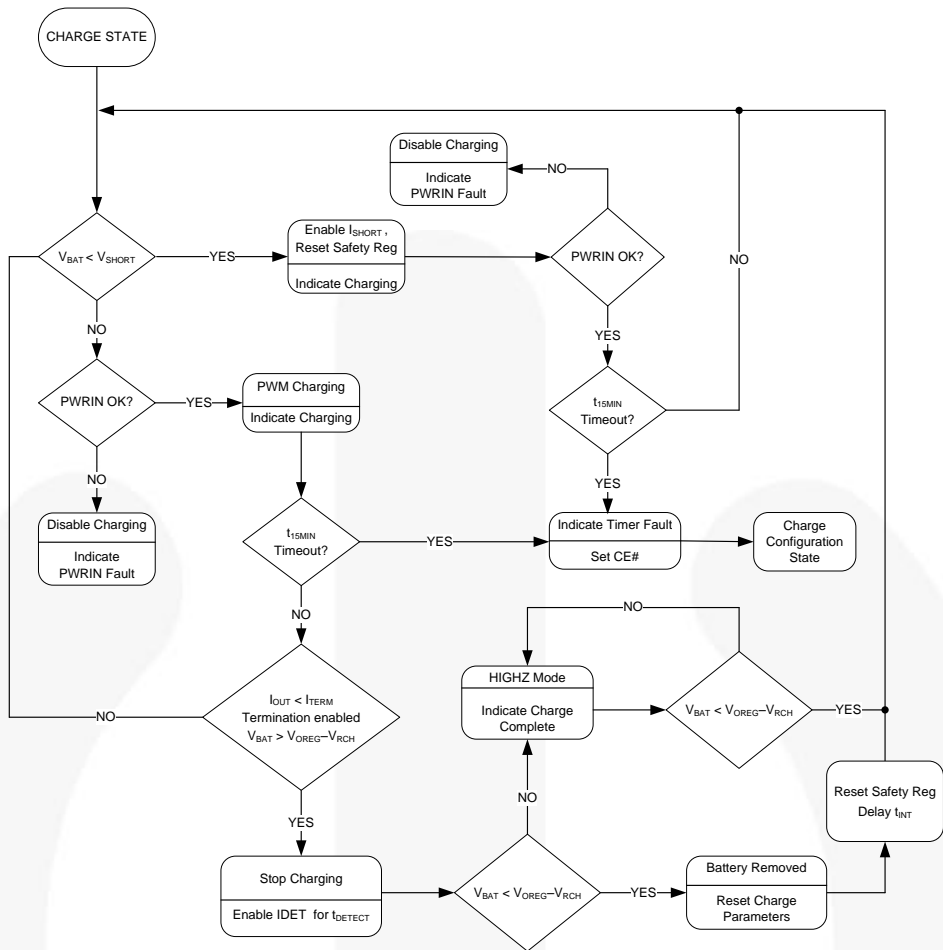


Figure 49. Charge Mode Flow Chart

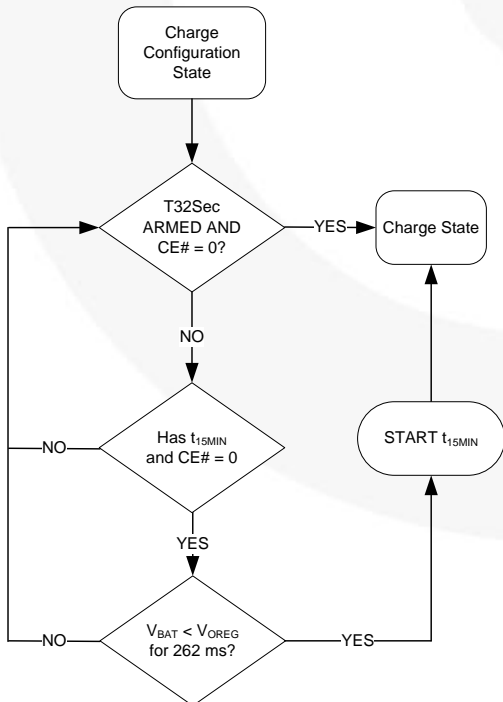


Figure 50. Charge Configuration Flow Chart

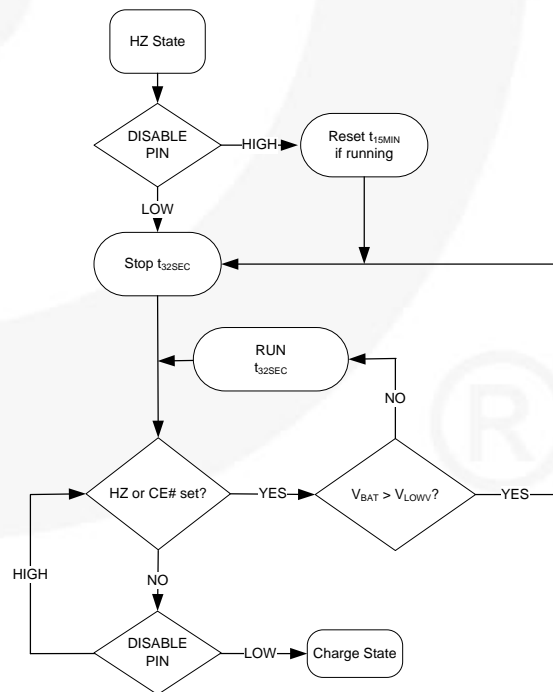


Figure 51. HZ-State Flow Chart

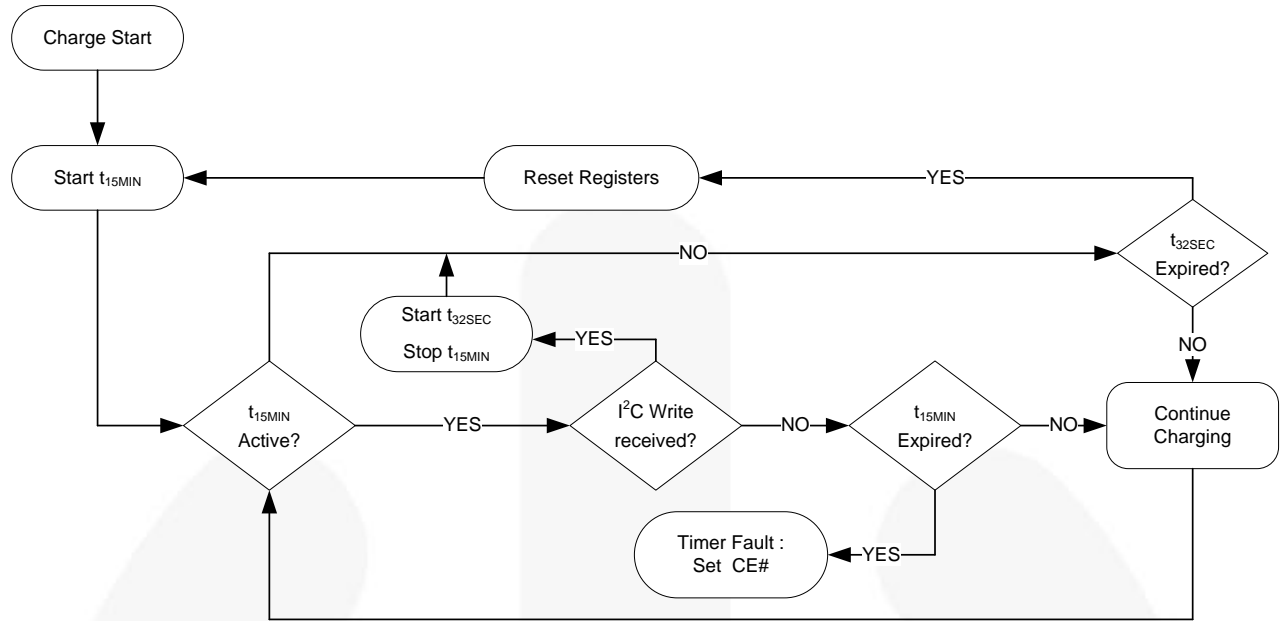


Figure 52. Timer Flow Chart

### Special Charger

The IC limits input current in case a current-limited charger is supplying  $V_{BUS}$  or  $V_{IN}$ . The IC slowly increases the charging current until either:

- $I_{BUSLIM}$  or  $I_{CHARGE}$  is reached; or
- $V_{PWRIN} = V_{SP}$  where  $V_{PWRIN}$  is the selected input power source (see Table 4).

If  $V_{PWRIN}$  collapses to  $V_{SP}$  when current is ramping up, the IC charges with an input current that keeps  $V_{PWRIN} = V_{SP}$ . When the  $V_{SP}$  control loop is limiting the charge current, the SP bit (REG5[4]) is set.  $V_{SP}$  default value is 4.53 V, but it can be programmed by REG5[2:0].

### Safety Settings

A SAFETY register (REG6) prevents the values in OREG (REG2[7:2]) and ICHG (REG4[6:3]) from exceeding the values of the VSAFE and ISAFE values.

After  $V_{BAT}$  rises above  $V_{SHORT}$ , the SAFETY register is loaded with its default value and may be written only before any other register is written. After writing to any other register, the SAFETY register is locked until  $V_{BAT}$  falls below  $V_{SHORT}$ . The SAFETY register is reset whenever the SRST pin is LOW.

ISAFE and VSAFE establish values that limit the maximum values of ICHG and OREG used by the control logic. If the host attempts to write a value higher than VSAFE or ISAFE to OREG or ICHG, respectively; the VSAFE, ISAFE value appears as the OREG, ICHG register value, respectively.

For the SAFETY\_U register, any attempt to write an ISAFE value higher than 10 (0AH) results in a value of 10 being written to the ISAFE bits. See Table 21 for VSAFE values and Table 20 and Table 26 for ISAFE values.

### Thermal Regulation and Protection

When the IC's junction temperature reaches  $T_{CF}$  (about 120°C) the charger reduces its output current to prevent overheating. If the temperature continues to increase, the current is reduced to 0 when the junction is 10°C above  $T_{CF}$ . If the temperature increases beyond  $T_{SHUTDOWN}$ , charging is suspended, the FAULT bits are set to 101, and SAT is pulsed. In Suspend Mode, all timers stop and the state of the IC's logic is preserved. Charging resumes after the die cools to about 10°C below  $T_{SHUTDOWN}$ .

### Charge Mode Input Supply Protection

#### Sleep Mode

When  $V_{BUS}$  and  $V_{IN}$  are both below  $V_{BAT}$ , the IC enters Sleep Mode. To prevent the battery from discharging into  $V_{BUS}$ , reverse current is prevented by body switching Q1 when PMID1 falls below  $V_{BAT}$ .

Similarly, when  $V_{IN}$  falls below  $V_{BAT}$ , Q4 turns off, blocking battery current flow into  $V_{IN}$ .

#### Input Supply Low-Voltage Detection

The IC continuously monitors  $V_{PWRIN}$  during charging. If the input voltage for the active charging source falls below 3.7 V, the IC terminates charging, pulses the STAT pin, sets STAT bits to 11, and sets the FAULT bits to 011 for the appropriate input source.

If the power source recovers above the  $V_{IN(MIN)}$  rising threshold after timer  $t_{INT}$  (about two seconds), the charging process is repeated. This prevents the USB power bus from collapsing or oscillating when the IC is connected to a suspended USB port or an OTG device with low current capability.

### Input Over-Voltage Detection

When  $V_{BUS}$  exceeds its OVP threshold, the IC:

1. Turns off Q3;
2. Suspends charging from  $V_{BUS}$ ; and
3. Sets the FAULTU bits to 001, STATU bits to 11, and pulses the STAT pin.

When  $V_{BUS}$  falls to about 150 mV below  $V_{BUS_{OVP}}$ , the fault is cleared, and charging resumes after  $V_{BUS}$  is revalidated.

If  $V_{IN}$  exceeds its OVP threshold, the IC:

1. Turns off Q4;
2. Suspends charging from  $V_{IN}$ ; and
3. Sets the FAULTV bits to 001, STATV bits to 11, and pulses the STAT pin.

### Charge Mode Battery Detection & Protection

#### $V_{BAT}$ Over-Voltage Protection

The OREG voltage regulation loop prevents  $V_{BAT}$  from overshooting the OREG voltage by more than 50 mV when the battery is removed. When the PWM charger is running with no battery, the TE bit is not set, and a battery is inserted that's charged to a voltage higher than  $V_{OREG}$ ; PWM pulses stop. If no further pulses occur for 30 ms, the IC sets the FAULT bits to 100, STAT bits to 11, and pulses the STAT pin.

#### Battery Detection During Charging

The IC can detect presence, absence, or removal of a battery. During normal charging, once  $V_{BAT}$  is greater than  $V_{OREG} - V_{RCH}$  and the termination charge current is detected; the IC terminates charging and sets the STAT bits to 10. It then turns on a discharge current,  $I_{DETECT}$ , for  $t_{DETECT}$ . If  $V_{BAT}$  is still above  $V_{OREG} - V_{RCH}$ , the battery is present and the IC sets the FAULT bits to 000. If  $V_{BAT}$  is below  $V_{OREG} - V_{RCH}$ , the battery is absent and the IC:

1. Sets the registers to their default values;
2. Sets the FAULT bits to 111; and
3. Resumes charging with default values after delay  $t_{INT}$ .

#### Battery Detection During Power-up

At PWRIN POR, if the charger is in 15-Minute Mode (no  $I^2C$  writes from the host detected), the IC starts a 32 ms timer when  $V_{BAT}$  crosses  $V_{SHORT}$  and starts PWM charging. If  $V_{BAT}$  exceeds 3.7 V within a 32 ms period, the IC determines that the battery is not present and:

1. Enters Charge Configuration Mode;
2. Sets the FAULT bits to 111 (no battery) and resets the SAFETY registers; and
3. Disables auto-charging until the next PWRIN POR.

#### Battery Short-Circuit Protection

If the battery voltage is below the short-circuit threshold ( $V_{SHORT}$ ); a linear current source,  $I_{SHORT}$ , supplies  $V_{BAT}$  until  $V_{BAT} > V_{SHORT}$ .

### Charger Status / Fault Status

The STAT pin indicates the operating condition of the IC and provides a fault indicator for interrupt-driven systems. When a fault condition occurs, the STAT pin pulses LOW for 125  $\mu$ s. If a new fault replaces the prior fault, STAT issues a new pulse.

The FAULT bits ( R0[2:0] ) indicate the type of fault in Charge Mode (see Table 14). FAULT bits return to 000 once R0 is read if the fault condition has cleared.

#### Charge Mode Control Bits

When set, the HZ\_VBUS and HZ\_VIN bits prevent charging from the VBUS or VIN input sources, respectively. The DIS pin prevents all charging when set, regardless of the state of the HZ bits.

**Table 6. DIS Pin and HZ Bit Functionality**

Charging	DIS PIN	HZ
ENABLE	0	0
DISABLE	X	1
DISABLE	1	X

### Boost Mode

Boost Mode can be enabled when the IC is in 32-Second Mode (host sets TMR\_RST before the  $t_{32SEC}$  expired ) with the OTG pin and OPA\_MODE bits as indicated in Table 7. The OTG ACTIVE state is 1 if OTG\_PL = 1, and 0 when OTG\_PL = 0.

If boost is active using the OTG pin, boost mode is initiated even if the HZ\_VBUS = 1. The HZ\_VBUS bit overrides the OPA\_MODE bit.

**Table 7. Enabling Boost**

OTG_E N	OTG PIN	HZ_VBU S	OPA_MOD E	BOOS T
1	ACTIVE	X	X	Enabled
1	X	0	1	Enabled
1	$\overline{\text{ACTIVE}}$	0	0	Disabled
1	$\overline{\text{ACTIVE}}$	X	0	Disabled
0	X	1	X	Disabled

To remain in Boost Mode, the TMR\_RST bit must be set by the host before the  $t_{32SEC}$  timer expires. If  $t_{32SEC}$  times out in Boost Mode; the IC reverts to High-Impedance Mode, pulses the STAT pin, sets the FAULT bits to 110, and resets the BOOST bit. POR or USB activity clears the fault condition.

The IC can operate its boost regulator while simultaneously charging from VIN. If the IC is charging from VIN when the boost regulator is enabled, charging pauses until the boost soft-start has completed.

## Boost PWM Control

The IC uses a minimum on-time, and computed minimum off-time, to regulate  $V_{BUS}$ . The computed off-time is designed to keep the switching frequency constant near 3 MHz when the regulator's inductor current is continuous (CCM).

The regulator achieves excellent transient response by employing current-mode modulation. This technique causes the regulator to exhibit a load line. During CCM Mode, the output voltage drops slightly as the input current rises. With a constant  $V_{BAT}$ , this appears as a constant output resistance.

The “droop” caused by the output resistance when a load is applied allows the regulator to respond smoothly to load transients with no undershoot from the load line. This can be seen in Figure 34.

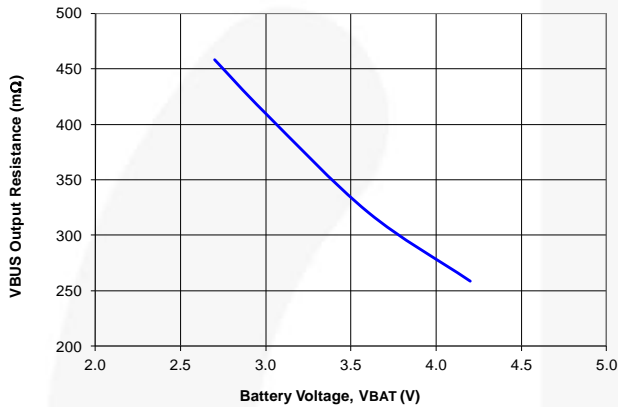


Figure 53. Output Resistance ( $R_{OUT}$ )

$V_{BUS}$  as a function of  $I_{LOAD}$  can be computed when the regulator is in PWM Mode (continuous conduction) as:

$$V_{BUS} = 5.05 - R_{OUT} \cdot I_{LOAD} \quad \text{EQ. 1}$$

At 3.6  $V_{BAT}$  and  $I_{LOAD} = 300$  mA,  $V_{BUS}$  would droop to about:

$$V_{BUS} = 5.05 - 0.32 \cdot 0.3 = 4.95V \quad \text{EQ. 2}$$

At 2.7  $V_{BAT}$ , with  $I_{LOAD} = 200$  mA,  $V_{BUS}$  would droop to about:

$$V_{BUS} = 5.05 - 0.45 \cdot 0.2 = 4.96V \quad \text{EQ. 3}$$

## Pulse Frequency Modulated (PFM) Mode

If  $V_{BUS} > V_{REF_{BOOST}}$  (nominally 5.05 V) when the minimum off time has ended, the regulator enters PFM Mode. Boost pulses are inhibited until  $V_{BUS} < V_{REF_{BOOST}}$ . The minimum on-time is increased to enable the output to pump up sufficiently with each PFM boost pulse. The regulator behaves like a constant on-time regulator, with the bottom of its output voltage ripple at 5.05 V in PFM Mode. Since PFM voltage ripple is typically 20 mV<sub>P-P</sub>,  $V_{BUS(PFM)}$  is nominally 5.06 V.

Table 8. Boost PWM Operating States

State	Description	Invoked When:
SCHK	Short-Circuit Check	$V_{BAT} > V_{BUS}$ and $V_{BUS} < 1V$
LIN1	Linear Startup	$V_{BAT} > 1V$
SS	Boost Soft-Start	$V_{BUS} < V_{BST}$
BST	Boost Operating Mode	$V_{BAT} > V_{UVLO}$ and SS completed

## Shutdown State

When the boost regulator is shut down, Q3 is off, preventing current flow from  $V_{BAT}$  to  $V_{BUS}$ . Q1 is also off, which prevents current flow from  $V_{BUS}$  to  $V_{BAT}$ .

## SCHK State

The SCHK state turns on a switch with an on-resistance of about 120  $\Omega$  from  $V_{BAT}$  to  $V_{BUS}$  and waits for  $V_{BUS}$  to rise to about 1 V before proceeding with boost soft-start. This prevents high current drain from the battery, which could occur if Q3 is turned on into a short circuit. If  $V_{BUS}$  fails to rise above 1 V within 8 ms, a boost overload fault is enunciated.

## LIN1 State

A portion of Q3 is turned on (on-resistance = 1  $\Omega$ ) to charge  $V_{BUS}$  from 1V to  $V_{PMID1}$ .  $V_{PMID1}$  is about 0.7 V below  $V_{BAT}$ . This state ends when  $V_{PMID1} - V_{BUS} < 0.4$  V. If  $V_{BUS}$  fails to achieve  $V_{PMID1} - 0.4$  V within 512  $\mu$ s, a boost overload fault is enunciated.

## SS State

When  $V_{BUS} > V_{PMID1} - 0.4$  V, the boost regulator begins switching. The output slews up until  $V_{BUS}$  is within 10% of its setpoint; at which time, the regulation loop is closed and the boost reference is digitally stepped to 5.07 V.

If the output fails to achieve 90% of its setpoint ( $V_{BST}$ ) within 512  $\mu$ s, a boost overload fault is enunciated.

## BST State

This is the normal operating mode of the regulator.

## Thermal

If the die temperature reaches 120°C while the boost and charger are both operating, charging stops for at least 10 ms, then resumes when the die temperature falls below 120°C.

### Boost Fault States

A BOOST fault is enunciated by the STAT pin pulsing and FAULT status bits under any of the following conditions.

**Table 9. Fault Status Bits during Boost Mode**

Fault Bit			Fault Description
B2	B1	B0	
0	0	0	Normal (no fault)
0	0	1	$V_{BUS} > V_{BUS_{OVP}}$
0	1	0	$V_{BUS}$ fails to achieve the voltage required to advance to the next state during soft-start or sustained (>32 ms) current limit during the BST state.
0	1	1	$V_{BAT} < UVLO_{BST}$
1	0	0	N/A: This code will not appear
1	0	1	Thermal shutdown
1	1	0	Timer fault
1	1	1	N/A: This code will not appear

Once a fault is triggered, the OPA\_MODE bit is reset.

If the boost was started by setting the OTG pin and OTG\_EN bits, the boost attempts to restart after a fault following a "cool-off" time of 128 ms.

### VREF

The VREF pin provides bias current to the charging circuit while VIN is the power source. This pin follows PMID2, but its voltage is limited to 5.8 V. Up to 5 mA of current can be drawn from the VREF pin to power external devices.

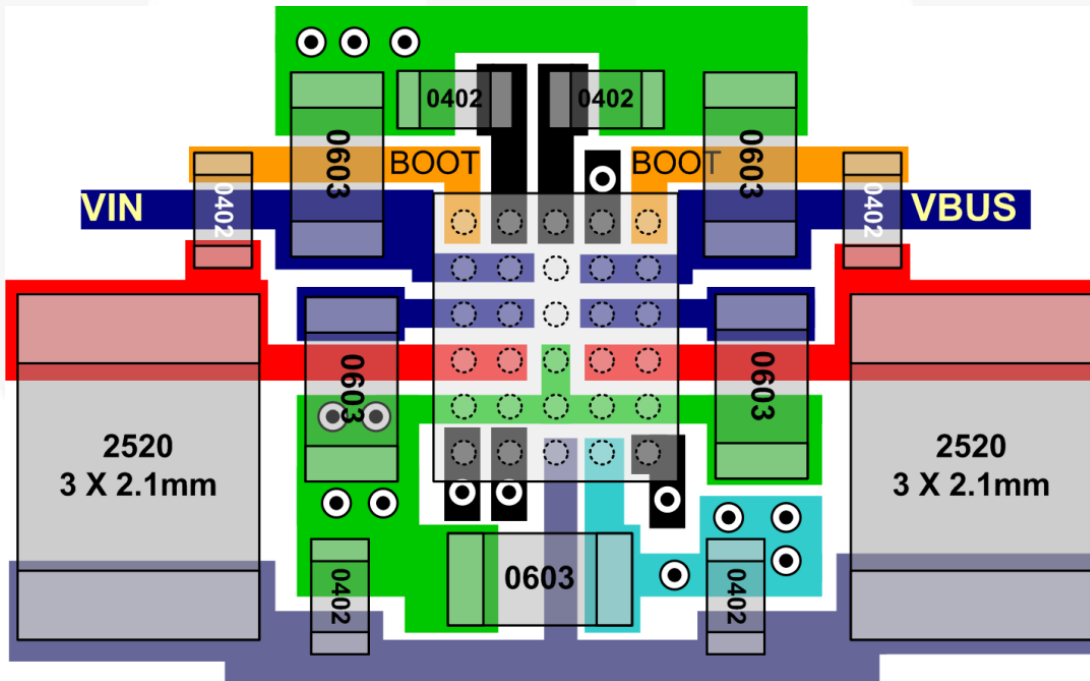
### LED Control

An LED driver provides a constant current to drive the anode of a charge indicator LED. The LED flashes during charging. The LED\_CONTROL register provides control of the LED driver and can be programmed to flash the LED when charging is disabled.

LED\_CONTROL is reset whenever the IC begins charging in 15-Minute Mode. This occurs after VBUS or VIN POR with a weak battery when  $t_{32SEC}$  is not running or when  $t_{32SEC}$  expires.

### Recommended PCB Layout

To limit the high-voltage excursions and stresses on the chargers' internal switching MOSFETs, it is critical to limit the total loop length from PMID back to the GND return, including the length of the CMID bypass capacitors. The layout below achieves this goal.



**Figure 54. Recommended Layout for High-Current Charging, Using 2520 Inductors**

## I<sup>2</sup>C Interface

The serial interface is compatible with Standard, Fast, Fast Plus, and High-Speed Modes per the I<sup>2</sup>C-Bus® specifications. The SCL line is an input and its SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

### Bus Timing

As shown in Figure 55, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

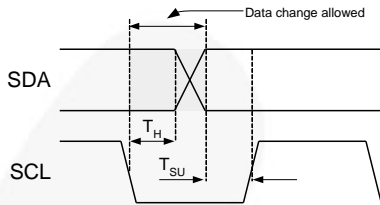


Figure 55. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 56.

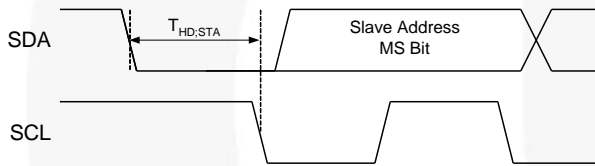


Figure 56. Start Bit

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 57.

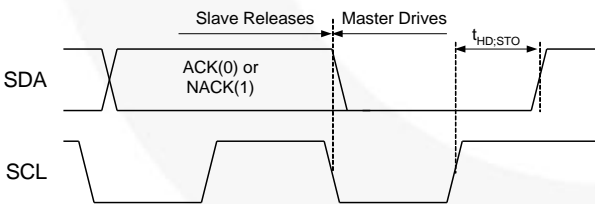


Figure 57. Stop Bit

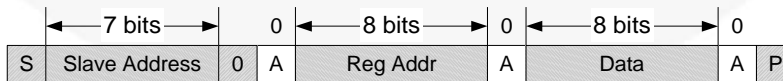


Figure 59. Write Transaction



Figure 60. Read Transaction

During a read from the FAN54300 (see Figure 60), the master issues a “REPEATED START” after sending the register address and before resending the slave address. The REPEATED START is a 1-to-0 transition on SDA while SCL is HIGH, as shown in Figure 58.

### High-Speed (HS) Mode

The protocols for High-Speed (HS), Low-Speed (LS), and Fast-Speed (FS) Modes are identical, except the bus speed for HS Mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a START condition. The master code is sent in Fast or Fast-Plus Mode (less than 1 MHz clock). Slaves do not ACK this transmission.

The master then generates a REPEATED START condition (see Figure 58) that causes all slaves on the bus to switch to HS Mode. The master then sends I<sup>2</sup>C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a stop bit (Figure 57) is sent by the master. While in HS Mode, packets are separated by REPEATED START conditions (Figure 58).

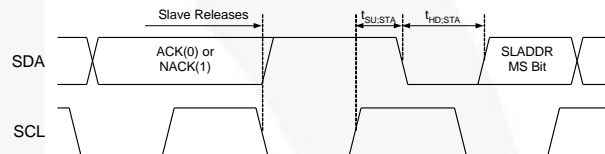


Figure 58. Repeated Start Timing

### Read and Write Transactions

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus. All addresses and data are MSB first.

Table 10. Bit Definitions for Figure 59 and Figure 60

Symbol	Definition
S	START, see Figure 56.
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\bar{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	Repeated START, see Figure 58
P	STOP, see Figure 57.



## Register Descriptions

**Table 11. I<sup>2</sup>C Slave Address**

Hex	7	6	5	4	3	2	1	0	
D4	1	1	0	1	0	1	0	R/W	VIN Charger
D6	1	1	0	1	0	1	1	R/W	USB Charger

**Table 12. I<sup>2</sup>C Register Address**

Name	Register Address	Slave Address	Affects	7	6	5	4	3	2	1	0
CONTROL0_U	0	D6	USB	0	0	0	0	0	0	0	0
CONTROL1_U	1	D6	USB	0	0	0	0	0	0	0	1
OREG_U	2	D6	USB	0	0	0	0	0	0	1	0
IC_INFO_U	3	D6	Both	0	0	0	0	0	0	1	1
IBAT_U	4	D6	USB	0	0	0	0	0	1	0	0
SP_CHARGER_U	5	D6	USB	0	0	0	0	0	1	0	1
SAFE_U	6	D6	USB	0	0	0	0	0	1	1	0
CONTROL0_V	0	D4	VIN	0	0	0	0	0	0	0	0
CONTROL1_V	1	D4	VIN	0	0	0	0	0	0	0	1
OREG_V	2	D4	VIN	0	0	0	0	0	0	1	0
IC_INFO_V	3	D4	Both	0	0	0	0	0	0	1	1
IBAT_V	4	D4	VIN	0	0	0	0	0	1	0	0
SP_CHARGER_V	5	D4	VIN	0	0	0	0	0	1	0	1
SAFE_V	6	D4	VIN	0	0	0	0	0	1	1	0
LED_CONTROL	7	D4/D6	Both	0	0	0	0	0	1	1	1
CHARGE_STATUS	8	D4/D6	Both	0	0	0	0	1	0	0	0
INPUT_STATUS	9	D4/D6	Both	0	0	0	0	1	0	0	1
DIE_REV	14	D4/D6	Both	0	0	0	1	0	1	0	0

## Register Bit Definitions

Bit	Name	Type	Description																																																		
<b>CONTROL0_U</b>			<b>Reg Addr: 0 Slave Addr: D6 Default = x1xx xxxx</b>																																																		
7	TMR_RST	W	Writing a 1 resets the $t_{32SEC}$ timer. Writing a 0 has no effect.																																																		
	OTG	R	Returns the OTG pin level (1 = OTG pin HIGH)																																																		
6	EN_STU	R/W	0: STAT pin does not go LOW when charging from USB source. 1: <b>STAT pin function is enabled.</b>																																																		
5:4	STAT_U	R	USB charger status																																																		
			<b>Table 13. USB Charger Status Bits</b>																																																		
			00	Normal (no fault) / Ready																																																	
			01	Charge in progress from USB source																																																	
			10	Charge done																																																	
11	USB charger fault																																																				
3	BOOST	R	0: <b>OTG boost is not active.</b> 1: OTG boost is active.																																																		
2:0	FAULT_U	R	Delineates USB Charger and OTG Boost Faults																																																		
			<b>Table 14. USB Fault Bits</b>																																																		
			<table border="1"> <thead> <tr> <th colspan="3">Bits</th> <th rowspan="2">Charger Mode</th> <th rowspan="2">Boost Mode</th> </tr> <tr> <th>2</th> <th>1</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Normal (no fault)</td> <td>Normal (no fault)</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td><math>V_{BUS} &gt; V_{BUS_{OVP}}</math></td> <td><math>V_{BUS} &gt; V_{BUS_{OVP}}</math></td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Sleep Mode: <math>V_{BUS} &lt; V_{BAT}</math></td> <td>Boost overload</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Poor USB input source</td> <td><math>V_{BAT} &lt; UVLO_{BST}</math></td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Battery OVP</td> <td>N/A: This code will not appear</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Thermal shutdown</td> <td>Thermal shutdown</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Timer fault</td> <td>Timer fault</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>No battery</td> <td>N/A: This code will not appear</td> </tr> </tbody> </table>			Bits			Charger Mode	Boost Mode	2	1	0	0	0	0	Normal (no fault)	Normal (no fault)	0	0	1	$V_{BUS} > V_{BUS_{OVP}}$	$V_{BUS} > V_{BUS_{OVP}}$	0	1	0	Sleep Mode: $V_{BUS} < V_{BAT}$	Boost overload	0	1	1	Poor USB input source	$V_{BAT} < UVLO_{BST}$	1	0	0	Battery OVP	N/A: This code will not appear	1	0	1	Thermal shutdown	Thermal shutdown	1	1	0	Timer fault	Timer fault	1	1	1	No battery	N/A: This code will not appear
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			1	0	0	Battery OVP	N/A: This code will not appear																																														
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1	1	0	Timer fault	Timer fault																																																	
1	1	1	No battery	N/A: This code will not appear																																																	

### Note:

7. Default values are in **bold** text.



Bit	Name	Type	Description										
<b>CONTROL1_U</b>			<b>Reg Addr: 1</b> <b>Slave Addr: D6</b> <b>Default = 0011 0000</b>										
7:6	IBUSLIM	R/W	USB bus current limit <b>Table 15. IBUSLIM: USB bus current limit</b> <table border="1"> <thead> <tr> <th>[7:6]</th> <th>IBUS Current Limit</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>100 mA</td> </tr> <tr> <td>01</td> <td>500 mA</td> </tr> <tr> <td>10</td> <td>800 mA</td> </tr> <tr> <td>11</td> <td>No limit</td> </tr> </tbody> </table>	[7:6]	IBUS Current Limit	00	100 mA	01	500 mA	10	800 mA	11	No limit
[7:6]	IBUS Current Limit												
00	100 mA												
01	500 mA												
10	800 mA												
11	No limit												
5:4	VLOWV_U	R/W	Weak Battery Threshold. This register determines $V_{LOWV}$ threshold when $V_{BUS}$ is charging. <b>Table 16. <math>V_{LOWV}</math>: Weak Battery Threshold</b> <table border="1"> <thead> <tr> <th>[5:4]</th> <th>IBUS Current Limit</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>3.4 V</td> </tr> <tr> <td>01</td> <td>3.5 V</td> </tr> <tr> <td>10</td> <td>3.6 V</td> </tr> <tr> <td>11</td> <td>3.7 V</td> </tr> </tbody> </table>	[5:4]	IBUS Current Limit	00	3.4 V	01	3.5 V	10	3.6 V	11	3.7 V
[5:4]	IBUS Current Limit												
00	3.4 V												
01	3.5 V												
10	3.6 V												
11	3.7 V												
3	TE_U	R/W	<b>0: Charge termination is disabled when charging from USB.</b> 1: Charge termination is enabled for USB charging.										
2	CE#_U	R/W	<b>0: USB charger is enabled.</b> 1: USB charger is disabled. This bit is set when $t_{15MIN}$ expires, regardless of which input source is charging.										
1	HZ_U	R/W	<b>0: USB charger is not in High-Impedance Mode.</b> 1: USB charger is in High-Impedance Mode.										
0	OPA_MODE	R/W	<b>0: Boost Mode disabled unless enabled with the OTG pin and OTG_EN HIGH.</b> 1: Boost Mode enabled unless HZ_U is set.										
<b>OREG_U</b>			<b>Reg Addr: 2</b> <b>Slave Addr: D6</b> <b>Default = 0000 1010</b>										
7:2	OREGU	R/W	Charger output “float” voltage when charging from USB source. Programmable from 3.5 to 4.44 V in 20 mV increments. Defaults to 000010 (3.54 V) (see Table 5).										
1	OTG_PL	R/W	<b>0: OTG pin is active LOW.</b> <b>1: OTG pin is active HIGH.</b>										
0	OTG_EN	R/W	<b>0: OTG pin does not enable boost when HIGH.</b> 1: OTG pin enables boost when HIGH.										
<b>IC_INFO_U</b>			<b>Reg Addr: 3</b> <b>Slave Addr: D4 or D6</b> <b>Default = 100x x000</b>										
7:5	VENDOR	R	<b>100:</b> Identifies Fairchild as the supplier.										
4:3	PN_U	R	Part number bits. FAN54300 = 10										
2:0	REV	R	IC Revision. Revision is 1.X where X is the decimal of these 3 bits.										
<b>DIE_REV</b>			<b>Reg Addr: 14H</b> <b>Slave Addr: D4 or D6</b> <b>Default = 0000 XXXX</b>										
7:4	Reserved	R	These bits return 0.										
3:0	REV_D	R	Die revision. These bits uniquely identify the full revision of the IC. REV bits change whenever there is a significant design change. REV_D bits change whenever any masks are revised.										

Bit	Name	Type	Description																																																								
<b>IBAT_U</b>			<b>Reg Addr: 4                      Slave Addr: D6    Default = 0000 1001</b>																																																								
7	RESETU	W	Writing a 1 resets all registers programmed with slave address D4, except the Safety register (Reg6), to their defaults. Writing a 0 has no effect. Read returns 0.																																																								
6:4	ICHGU	R/W	<p>Sets the maximum charge current (<math>I_{CHARGE}</math>) when charging from VBUS when IO_LEVELU = 0.</p> <p><b>Table 17. <math>I_{CHARGE}</math> as a Function of the ICHGU Bits and <math>R_{SENSE}</math> Resistor Value</b></p> <table border="1"> <thead> <tr> <th rowspan="2">BIN</th> <th rowspan="2">HEX</th> <th rowspan="2"><math>V_{RSENSE}</math> (mV)</th> <th colspan="2"><math>I_{CHARGE}</math> (mA)</th> <th rowspan="2">IOREF</th> </tr> <tr> <th>68m<math>\Omega</math></th> <th>100m<math>\Omega</math></th> </tr> </thead> <tbody> <tr><td>000</td><td>00</td><td>37.4</td><td>550</td><td>374</td><td>704</td></tr> <tr><td>001</td><td>01</td><td>44.2</td><td>650</td><td>442</td><td>832</td></tr> <tr><td>010</td><td>02</td><td>51.0</td><td>750</td><td>510</td><td>960</td></tr> <tr><td>011</td><td>03</td><td>57.8</td><td>850</td><td>578</td><td>1088</td></tr> <tr><td>100</td><td>04</td><td>64.6</td><td>950</td><td>646</td><td>1216</td></tr> <tr><td>101</td><td>05</td><td>71.4</td><td>1,050</td><td>714</td><td>1344</td></tr> <tr><td>110</td><td>06</td><td>78.2</td><td>1,150</td><td>782</td><td>1472</td></tr> <tr><td>111</td><td>07</td><td>85.0</td><td>1,250</td><td>850</td><td>1600</td></tr> </tbody> </table> <p>Note that when charging from a USB source, charger current is limited to 1250 mA (<math>R_{SENSE} = 68m\Omega</math>).</p>	BIN	HEX	$V_{RSENSE}$ (mV)	$I_{CHARGE}$ (mA)		IOREF	68m $\Omega$	100m $\Omega$	000	00	37.4	550	374	704	001	01	44.2	650	442	832	010	02	51.0	750	510	960	011	03	57.8	850	578	1088	100	04	64.6	950	646	1216	101	05	71.4	1,050	714	1344	110	06	78.2	1,150	782	1472	111	07	85.0	1,250	850	1600
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3	Reserved	R	This bit returns 1.																																																								
2:0	ITERMU	R/W	<p>Sets the current at which charging terminates when charging from VBUS if the TE bit is set.</p> <p><b>Table 18. <math>I_{CHARGE}</math> Termination Current as a Function of ITERM bits and <math>R_{SENSE}</math> Resistor Value</b></p> <table border="1"> <thead> <tr> <th rowspan="2">BIN</th> <th rowspan="2">HEX</th> <th rowspan="2"><math>V_{RSENSE}</math> (mV)</th> <th colspan="2"><math>I_{TERM}</math> (mA)</th> </tr> <tr> <th>68m<math>\Omega</math></th> <th>100m<math>\Omega</math></th> </tr> </thead> <tbody> <tr><td>000</td><td>00</td><td>3.3</td><td>49</td><td>33</td></tr> <tr><td>001</td><td>01</td><td>6.6</td><td>97</td><td>66</td></tr> <tr><td>010</td><td>02</td><td>9.9</td><td>146</td><td>99</td></tr> <tr><td>011</td><td>03</td><td>13.2</td><td>194</td><td>132</td></tr> <tr><td>100</td><td>04</td><td>16.5</td><td>243</td><td>165</td></tr> <tr><td>101</td><td>05</td><td>19.8</td><td>291</td><td>198</td></tr> <tr><td>110</td><td>06</td><td>23.1</td><td>340</td><td>231</td></tr> <tr><td>111</td><td>07</td><td>26.4</td><td>388</td><td>264</td></tr> </tbody> </table>	BIN	HEX	$V_{RSENSE}$ (mV)	$I_{TERM}$ (mA)		68m $\Omega$	100m $\Omega$	000	00	3.3	49	33	001	01	6.6	97	66	010	02	9.9	146	99	011	03	13.2	194	132	100	04	16.5	243	165	101	05	19.8	291	198	110	06	23.1	340	231	111	07	26.4	388	264									
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Bit	Name	Type	Description
<b>SP_CHARGER_U</b>			<b>Reg Addr: 5                      Slave Addr: D6    Default = 0x1x x100</b>
7	Reserved	R	This bit returns 0.
6	VBUS_CON	R	Mirror of INPUT_STATUS[5] (see INPUT_STATUS register description)
5	IO_LEVEL	R/W	<p>0: Output current is controlled by IOCHARGE bits for charging from VBUS.</p> <p><b>When charging from VBUS, the voltage across <math>R_{SENSE}</math> for output current control is set to 22.1 mV (325 mA for <math>R_{SENSE} = 68 m\Omega</math>, 221 mA for 100 m<math>\Omega</math>).</b></p>
4	SPU	R	<p>Special charger loop is not active. Input power source is able to stay above <math>V_{SP}</math>. SPU = 0 when VBUS is not PWM charging.</p> <p>1: Special charger loop is active and controlling the charging current.</p>
3	VIN_CON	R	Mirror of INPUT_STATUS[7] (see INPUT_STATUS register description)

Bit	Name	Type	Description																																																																				
2:0	VSPU	R/W	<p>Sets the special charger control loop reference voltage when charging from <math>V_{BUS}</math>. If <math>V_{BUS}</math> falls below this voltage, battery current is reduced until the input voltage is at or above <math>V_{SP}</math>.</p> <p><b>Table 19. <math>V_{SP}</math> Special Charger Reference Voltage</b></p> <table border="1"> <thead> <tr> <th>DEC</th> <th>BIN</th> <th><math>V_{SP}</math></th> </tr> </thead> <tbody> <tr><td>0</td><td>000</td><td>4.21</td></tr> <tr><td>1</td><td>001</td><td>4.29</td></tr> <tr><td>2</td><td>010</td><td>4.37</td></tr> <tr><td>3</td><td>011</td><td>4.45</td></tr> <tr><td><b>4</b></td><td><b>100</b></td><td><b>4.53</b></td></tr> <tr><td>5</td><td>101</td><td>4.61</td></tr> <tr><td>6</td><td>110</td><td>4.69</td></tr> <tr><td>7</td><td>111</td><td>4.77</td></tr> </tbody> </table>	DEC	BIN	$V_{SP}$	0	000	4.21	1	001	4.29	2	010	4.37	3	011	4.45	<b>4</b>	<b>100</b>	<b>4.53</b>	5	101	4.61	6	110	4.69	7	111	4.77																																									
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6:4	ISAFEU	R/W	<p>Any attempt to write a value to ICHGU higher than the contents of ISAFEU sets ICHGU = ISAFEU.</p> <p><b>Table 20. USB Charging <math>I_{CHARGE}</math> Limit as a Function of the ISAFEU Bits</b></p> <table border="1"> <thead> <tr> <th rowspan="2">BIN</th> <th rowspan="2">HEX</th> <th rowspan="2"><math>V_{RSENSE}</math> (mV)</th> <th colspan="2"><math>I_{SAFE}</math> (mA)</th> </tr> <tr> <th>68m<math>\Omega</math></th> <th>100m<math>\Omega</math></th> </tr> </thead> <tbody> <tr><td>000</td><td>00</td><td>37.4</td><td>550</td><td>374</td></tr> <tr><td>001</td><td>01</td><td>44.2</td><td>650</td><td>442</td></tr> <tr><td>010</td><td>02</td><td>51.0</td><td>750</td><td>510</td></tr> <tr><td>011</td><td>03</td><td>57.8</td><td>850</td><td>578</td></tr> <tr><td><b>100</b></td><td><b>04</b></td><td><b>64.6</b></td><td><b>950</b></td><td><b>646</b></td></tr> <tr><td>101</td><td>05</td><td>71.4</td><td>1,050</td><td>714</td></tr> <tr><td>110</td><td>06</td><td>78.2</td><td>1,150</td><td>782</td></tr> <tr><td>111</td><td>07</td><td>85.0</td><td>1,250</td><td>850</td></tr> </tbody> </table>	BIN	HEX	$V_{RSENSE}$ (mV)	$I_{SAFE}$ (mA)		68m $\Omega$	100m $\Omega$	000	00	37.4	550	374	001	01	44.2	650	442	010	02	51.0	750	510	011	03	57.8	850	578	<b>100</b>	<b>04</b>	<b>64.6</b>	<b>950</b>	<b>646</b>	101	05	71.4	1,050	714	110	06	78.2	1,150	782	111	07	85.0	1,250	850																					
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3:0	VSAFEU	R/W	<p>Any attempt to write a value to OREGU that is higher than the value in the Max. OREG column (below) results in OREGU = Max OREG.</p> <p><b>Table 21. <math>V_{OREG}</math> Limit as a Function of the VSAFEU Bits when Charging from <math>V_{BUS}</math></b></p> <table border="1"> <thead> <tr> <th>DEC</th> <th>BIN</th> <th>Max OREG (REG2[7:2])</th> <th>VOREG MAX</th> </tr> </thead> <tbody> <tr><td><b>0</b></td><td><b>0000</b></td><td><b>100011</b></td><td><b>4.20</b></td></tr> <tr><td>1</td><td>0001</td><td>100100</td><td>4.22</td></tr> <tr><td>2</td><td>0010</td><td>100101</td><td>4.24</td></tr> <tr><td>3</td><td>0011</td><td>100110</td><td>4.26</td></tr> <tr><td>4</td><td>0100</td><td>100111</td><td>4.28</td></tr> <tr><td>5</td><td>0101</td><td>101000</td><td>4.30</td></tr> <tr><td>6</td><td>0110</td><td>101001</td><td>4.32</td></tr> <tr><td>7</td><td>0111</td><td>101010</td><td>4.34</td></tr> <tr><td>8</td><td>1000</td><td>101011</td><td>4.36</td></tr> <tr><td>9</td><td>1001</td><td>101100</td><td>4.38</td></tr> <tr><td>10</td><td>1010</td><td>101101</td><td>4.40</td></tr> <tr><td>11</td><td>1011</td><td>101110</td><td>4.42</td></tr> <tr><td>12</td><td>1100</td><td>101111</td><td>4.44</td></tr> <tr><td>13</td><td>1101</td><td>110000</td><td>4.44</td></tr> <tr><td>14</td><td>1110</td><td>110001</td><td>4.44</td></tr> <tr><td>15</td><td>1111</td><td>110010</td><td>4.44</td></tr> </tbody> </table>	DEC	BIN	Max OREG (REG2[7:2])	VOREG MAX	<b>0</b>	<b>0000</b>	<b>100011</b>	<b>4.20</b>	1	0001	100100	4.22	2	0010	100101	4.24	3	0011	100110	4.26	4	0100	100111	4.28	5	0101	101000	4.30	6	0110	101001	4.32	7	0111	101010	4.34	8	1000	101011	4.36	9	1001	101100	4.38	10	1010	101101	4.40	11	1011	101110	4.42	12	1100	101111	4.44	13	1101	110000	4.44	14	1110	110001	4.44	15	1111	110010	4.44
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Bit	Name	Type	Description																																							
<b>CONTROL0_V</b>			<b>Reg Addr: 0</b> <b>Slave Addr: D4</b> <b>Default = x1xx 0xxx</b>																																							
	TMR_RST SRST	W R	Writing a 1 resets the $t_{32SEC}$ timer. Writing a 0 has no effect. Returns the SRST pin level (1 = SRST pin HIGH).																																							
6	EN_STV	R/W	0: STAT pin does not go LOW when charging from $V_{IN}$ source. 1: <b>STAT pin function is enabled for <math>V_{IN}</math> source.</b>																																							
5:4	STAT_V	R	<b>Table 22. VIN Charger Status Bits</b> <table border="1" style="margin-left: 20px;"> <tr><td>00</td><td>Normal (no fault)</td></tr> <tr><td>01</td><td>Charge in progress from VIN source</td></tr> <tr><td>10</td><td>Charge Done</td></tr> <tr><td>11</td><td>VIN charger fault</td></tr> </table>	00	Normal (no fault)	01	Charge in progress from VIN source	10	Charge Done	11	VIN charger fault																															
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3	Reserved	R	This bit returns 0.																																							
2:0	FAULT_V	R	Delineates VIN Charger Faults <b>Table 23. VIN Charger Fault Bits</b> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th colspan="3">Bits</th> <th rowspan="2">Charger Mode</th> </tr> <tr> <th>2</th> <th>1</th> <th>0</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>Normal (no fault)</td></tr> <tr><td>0</td><td>0</td><td>1</td><td><math>V_{IN} &gt; V_{IN_{OVP}}</math></td></tr> <tr><td>0</td><td>1</td><td>0</td><td>Sleep Mode: <math>V_{IN} &lt; V_{BAT}</math></td></tr> <tr><td>0</td><td>1</td><td>1</td><td>Poor VIN input source</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>Battery OVP</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>Thermal shutdown</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>Timer fault</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>No battery</td></tr> </tbody> </table>	Bits			Charger Mode	2	1	0	0	0	0	Normal (no fault)	0	0	1	$V_{IN} > V_{IN_{OVP}}$	0	1	0	Sleep Mode: $V_{IN} < V_{BAT}$	0	1	1	Poor VIN input source	1	0	0	Battery OVP	1	0	1	Thermal shutdown	1	1	0	Timer fault	1	1	1	No battery
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<b>CONTROL1_V</b>			<b>Reg Addr: 1</b> <b>Slave Addr: D4</b> <b>Default = 0111 0000</b>																																							
7:6	Reserved	R/W	These bits have no effect on IC operation. Input current is not limited by the IC when charging from VIN.																																							
5:4	VLOWV_V	R/W	See Table 16. <i>VLOWV: Weak Battery Threshold</i>																																							
3	TE_V	R/W	0: <b>Charge termination is disabled when charging from VIN.</b> 1: Charge termination is enabled for VIN charging.																																							
2	CE#_V	R/W	0: <b>VIN charger is enabled.</b> 1: VIN charger is disabled. This bit is set when $t_{15MIN}$ expires, regardless of which input source is charging.																																							
1	HZ_V	R/W	0: <b>VIN charger is not in High-Impedance Mode.</b> 1: VIN charger is in High-Impedance Mode.																																							
0	Reserved	R	This bit returns 0.																																							
<b>OREG_V</b>			<b>Reg Addr: 2</b> <b>Slave Addr: D4</b> <b>Default = 0000 1010</b>																																							
7:2	OREGV	R/W	Charger output “float” voltage when charging from VIN source. Programmable from 3.5 to 4.44 V in 20 mV increments. Defaults to 000010 (3.54 V) (see Table 5).																																							
1:0	Reserved	R	These bits return 10.																																							
<b>IC_INFO_V</b>			<b>Reg Addr: 3</b> <b>Slave Addr: D4</b> <b>Default = 100x x000</b>																																							
7:5	VENDOR	R	<b>100: Identifies Fairchild as the supplier.</b>																																							
4:3	PN_V	R	Part number bits: FAN54300 = 00																																							
2:0	REV	R	IC Revision: Revision is 1.X, where X is the decimal of these 3 bits.																																							

Bit	Name	Type	Description																																																														
<b>IBAT_V</b>			<b>Reg Addr: 4</b> <b>Slave Addr: D4</b> <b>Default = 0000 0001</b>																																																														
7	RESETV	W	Writing a 1 resets all registers programmed with slave address D4, except the Safety register (Reg6), to their defaults. Writing a 0 has no effect. Read returns 0.																																																														
6:3	ICHGV	R/W	<p>Sets the maximum charge current (<math>I_{CHARGE}</math>) when charging from VIN when IO_LEVELV = 0.</p> <p><b>Table 24. <math>I_{CHARGE}</math> Current as a Function of the ICHGV Bits and <math>R_{SENSE}</math> Resistor Value</b></p> <table border="1"> <thead> <tr> <th rowspan="2">BIN</th> <th rowspan="2">HEX</th> <th rowspan="2"><math>V_{RSENSE}</math> (mV)</th> <th colspan="2"><math>I_{CHARGE}</math> (mA)</th> </tr> <tr> <th>68m<math>\Omega</math></th> <th>100m<math>\Omega</math></th> </tr> </thead> <tbody> <tr><td>0000</td><td>00</td><td>37.4</td><td>550</td><td>374</td></tr> <tr><td>0001</td><td>01</td><td>44.2</td><td>650</td><td>442</td></tr> <tr><td>0010</td><td>02</td><td>51.0</td><td>750</td><td>510</td></tr> <tr><td>0011</td><td>03</td><td>57.8</td><td>850</td><td>578</td></tr> <tr><td>0100</td><td>04</td><td>64.6</td><td>950</td><td>646</td></tr> <tr><td>0101</td><td>05</td><td>71.4</td><td>1,050</td><td>714</td></tr> <tr><td>0110</td><td>06</td><td>78.2</td><td>1,150</td><td>782</td></tr> <tr><td>0111</td><td>07</td><td>85.0</td><td>1,250</td><td>850</td></tr> <tr><td>1000</td><td>08</td><td>91.8</td><td>1,350</td><td>918</td></tr> <tr><td>1001</td><td>09</td><td>98.6</td><td>1,450</td><td>986</td></tr> <tr><td>1010</td><td>0A</td><td>105.4</td><td>1,550</td><td>1,054</td></tr> </tbody> </table> <p>Any attempt to write a value higher than 1010 results in ICHGV = 1010.</p>	BIN	HEX	$V_{RSENSE}$ (mV)	$I_{CHARGE}$ (mA)		68m $\Omega$	100m $\Omega$	0000	00	37.4	550	374	0001	01	44.2	650	442	0010	02	51.0	750	510	0011	03	57.8	850	578	0100	04	64.6	950	646	0101	05	71.4	1,050	714	0110	06	78.2	1,150	782	0111	07	85.0	1,250	850	1000	08	91.8	1,350	918	1001	09	98.6	1,450	986	1010	0A	105.4	1,550	1,054
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2:0	ITERMV	R/W	<p>Sets the current at which charging terminates if the TE bit is set:</p> <p><b>Table 25. <math>I_{CHARGE}</math> Termination Current as a Function of the ITERM bits and <math>R_{SENSE}</math> Resistor Value</b></p> <table border="1"> <thead> <tr> <th rowspan="2">BIN</th> <th rowspan="2">HEX</th> <th rowspan="2"><math>V_{RSENSE}</math> (mV)</th> <th colspan="2"><math>I_{TERM}</math> (mA)</th> </tr> <tr> <th>68m<math>\Omega</math></th> <th>100m<math>\Omega</math></th> </tr> </thead> <tbody> <tr><td>000</td><td>00</td><td>3.3</td><td>49</td><td>33</td></tr> <tr><td>001</td><td>01</td><td>6.6</td><td>97</td><td>66</td></tr> <tr><td>010</td><td>02</td><td>9.9</td><td>146</td><td>99</td></tr> <tr><td>011</td><td>03</td><td>13.2</td><td>194</td><td>132</td></tr> <tr><td>100</td><td>04</td><td>16.5</td><td>243</td><td>165</td></tr> <tr><td>101</td><td>05</td><td>19.8</td><td>291</td><td>198</td></tr> <tr><td>110</td><td>06</td><td>23.1</td><td>340</td><td>231</td></tr> <tr><td>111</td><td>07</td><td>26.4</td><td>388</td><td>264</td></tr> </tbody> </table>	BIN	HEX	$V_{RSENSE}$ (mV)	$I_{TERM}$ (mA)		68m $\Omega$	100m $\Omega$	000	00	3.3	49	33	001	01	6.6	97	66	010	02	9.9	146	99	011	03	13.2	194	132	100	04	16.5	243	165	101	05	19.8	291	198	110	06	23.1	340	231	111	07	26.4	388	264															
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Bit	Name	Type	Description
<b>SP_CHARGER_V</b>			<b>Reg Addr: 5</b> <b>Slave Addr: D4</b> <b>Default = 0x1x x100</b>
7	Reserved	R	This bit returns 0.
6	VIN_CON	R	Mirror of INPUT_STATUS[7] (see INPUT_STATUS register description)
5	IO_LEVELV	R/W	0: Output current is controlled by IOCHARGE bits for charging from VIN. When charging from VIN, the voltage across $R_{SENSE}$ for output current control is set to 22.1mV (325mA for $R_{SENSE} = 68m\Omega$ , 221mA for 100m $\Omega$ ).
4	SPV	R	Special charger loop is not active. $V_{IN}$ is able to stay above $V_{SP}$ . SPV = 0 when VIN is not PWM charging. 1: Special charger loop is active and controlling the charging current.
3	EN_LEVEL	R	0: DISABLE (DIS) pin is LOW. 1: DISABLE (DIS) pin is HIGH
2:0	VSPV	R/W	Sets the special charger control loop reference voltage when charging from VIN. If $V_{IN}$ falls below this voltage, battery current is reduced until the input voltage is at or above $V_{SP}$ (see Table 19).

Bit	Name	Type	Description																																																														
<b>SAFE_V</b> <span style="float: right;">Reg Addr: 6</span> <span style="float: right;">Slave Addr: D4</span> <span style="float: right;">Default = 0100 0000</span>																																																																	
7:4	ISAFEV	R/W	<p>Any attempt to write a value to ICHGV higher than the contents of ISAFEV sets ICHGV = ISAFEV. Any attempt to write a value higher than 1010 to ISAFEV results in ISAFEV = 1010.</p> <p><b>Table 26. I<sub>CHARGE</sub> Limit as a Function of the ISAFEV Bits when Charging from VIN</b></p> <table border="1"> <thead> <tr> <th rowspan="2">BIN</th> <th rowspan="2">HEX</th> <th rowspan="2">V<sub>RSENSE</sub> (mV)</th> <th colspan="2">I<sub>SAFE</sub> (mA)</th> </tr> <tr> <th>68mΩ</th> <th>100mΩ</th> </tr> </thead> <tbody> <tr><td>0000</td><td>00</td><td>37.4</td><td>550</td><td>374</td></tr> <tr><td>0001</td><td>01</td><td>44.2</td><td>650</td><td>442</td></tr> <tr><td>0010</td><td>02</td><td>51.0</td><td>750</td><td>510</td></tr> <tr><td>0011</td><td>03</td><td>57.8</td><td>850</td><td>578</td></tr> <tr><td><b>0100</b></td><td><b>04</b></td><td><b>64.6</b></td><td><b>950</b></td><td><b>646</b></td></tr> <tr><td>0101</td><td>05</td><td>71.4</td><td>1,050</td><td>714</td></tr> <tr><td>0110</td><td>06</td><td>78.2</td><td>1,150</td><td>782</td></tr> <tr><td>0111</td><td>07</td><td>85.0</td><td>1,250</td><td>850</td></tr> <tr><td>1000</td><td>08</td><td>91.8</td><td>1,350</td><td>918</td></tr> <tr><td>1001</td><td>09</td><td>98.6</td><td>1,450</td><td>986</td></tr> <tr><td>1010</td><td>0A</td><td>105.4</td><td>1,550</td><td>1,054</td></tr> </tbody> </table>	BIN	HEX	V <sub>RSENSE</sub> (mV)	I <sub>SAFE</sub> (mA)		68mΩ	100mΩ	0000	00	37.4	550	374	0001	01	44.2	650	442	0010	02	51.0	750	510	0011	03	57.8	850	578	<b>0100</b>	<b>04</b>	<b>64.6</b>	<b>950</b>	<b>646</b>	0101	05	71.4	1,050	714	0110	06	78.2	1,150	782	0111	07	85.0	1,250	850	1000	08	91.8	1,350	918	1001	09	98.6	1,450	986	1010	0A	105.4	1,550	1,054
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3:0	VSAFEV	R/W	Any attempt to write a value to OREGV that is higher than the value in the Max OREG column below results in OREGV = Max OREG (see Table 21).																																																														

Bit	Name	Type	Description								
<b>LED_CONTROL</b> <span style="float: right;">Reg Addr: 7</span> <span style="float: right;">Slave Addr: D4 or D6</span> <span style="float: right;">Default = 1000 0010</span>											
7:6	I_LED	R/W	<p>Sets LED behavior</p> <p><b>Table 27. LED Control Bits</b></p> <table border="1"> <tbody> <tr><td>00</td><td>LED is off</td></tr> <tr><td>01</td><td>LED current = 1.13 mA</td></tr> <tr><td><b>10</b></td><td><b>LED current = 2.25mA</b></td></tr> <tr><td>11</td><td>LED current = 4.50 mA</td></tr> </tbody> </table>	00	LED is off	01	LED current = 1.13 mA	<b>10</b>	<b>LED current = 2.25mA</b>	11	LED current = 4.50 mA
00	LED is off										
01	LED current = 1.13 mA										
<b>10</b>	<b>LED current = 2.25mA</b>										
11	LED current = 4.50 mA										
5	Reserved	R	This bit returns 0.								
4	LED_ON	R/W	<p><b>0:</b> LED is only active when charging.  <b>1:</b> LED is active regardless of charging status.</p>								
3:2	LED_TON	R/W	<p>Sets LED blink t<sub>ON</sub></p> <p><b>Table 28. LED ON-Time</b></p> <table border="1"> <tbody> <tr><td><b>00</b></td><td>131 ms</td></tr> <tr><td>01</td><td>262 ms</td></tr> <tr><td>10</td><td>524 ms</td></tr> <tr><td>11</td><td>Constant ON</td></tr> </tbody> </table>	<b>00</b>	131 ms	01	262 ms	10	524 ms	11	Constant ON
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01	262 ms										
10	524 ms										
11	Constant ON										
1:0	LED_TOFF	R/W	<p>Sets LED blink t<sub>OFF</sub></p> <p><b>Table 29. LED OFF-Time</b></p> <table border="1"> <tbody> <tr><td>00</td><td>393 ms</td></tr> <tr><td>01</td><td>786 ms</td></tr> <tr><td><b>10</b></td><td><b>1573 ms</b></td></tr> <tr><td>11</td><td>3146 ms</td></tr> </tbody> </table>	00	393 ms	01	786 ms	<b>10</b>	<b>1573 ms</b>	11	3146 ms
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11	3146 ms										



Bit	Name	Type	Description
<b>CHARGE_STATUS</b>			<b>Reg Addr: 8</b> <b>Slave Addr: D4 or D6</b>
7	ITERM_CMP	R	0: If TE = 1, $(V_{CSIN} - V_{BAT}) < V_{ITERM}$ . If TE = 0, $(V_{CSIN} - V_{BAT}) < 1$ mV. 1: If TE = 0, $(V_{CSIN} - V_{BAT}) > V_{ITERM}$ . If TE = 0, $(V_{CSIN} - V_{BAT}) > 1$ mV.
6	T_120	R	0: The die temperature is below 120°C. 1: The die temperature is above 120°C.
5	ICHG	R	0: ICHARGE loop is controlling charge current (charger is in CC Mode). 1: ICHARGE loop is not controlling charge current.
4	IBUS	R	0: IBUS is limiting charge current. 1: IBUS loop is not controlling charge current. This bit always = 1 when charging from VIN.
3	CV	R	1 indicates that the constant-voltage loop (OREG) is controlling the charger and that all current limiting loops have released. Deglitched 32ms.
2	LINCHG	R	0: Charger is not in Linear Mode 1: Charger is in Linear Mode ( $V_{BAT} < V_{SHORT}$ ).
1:0	Reserved	R	These bits always return 0.
<b>INPUT_STATUS</b>			<b>Reg Addr: 9</b> <b>Slave Addr: D4 or D6</b>
7	VIN_CON	R	0: $V_{IN}$ has been less than $V_{BAT}$ for at least 100ms ( $V_{IN}$ is disconnected). 1: $V_{IN} > V_{BAT}$ and $V_{IN} > 4.5$ V for at least 4ms ( $V_{IN}$ is connected). This bit is mirrored in SP_CHARGER_U[3] and SP_CHARGER_V[6].
6	VIN_VALID	R	0: $V_{IN}$ has not passed validation. 1: $V_{IN}$ has passed validation and can be used as a charging source.
5	VBUS_CON	R	0: $V_{BUS}$ has been less than $V_{BAT}$ for at least 100ms ( $V_{BUS}$ is disconnected). 1: $V_{BUS} > V_{BAT}$ and $V_{BUS} > 4.5$ V for at least 4ms ( $V_{BUS}$ is connected).
4	VBUS_VALID	R	0: $V_{BUS}$ has not passed validation. 1: $V_{BUS}$ has passed validation and can be used as a charging source. This bit is mirrored in SP_CHARGER_U[6].
3	SOURCE	R	0: $V_{IN}$ is used for IC power and charging. 1: $V_{BUS}$ is used for IC power and charging.
2:0	Reserved	R	These bits always return 0.



## Physical Dimensions

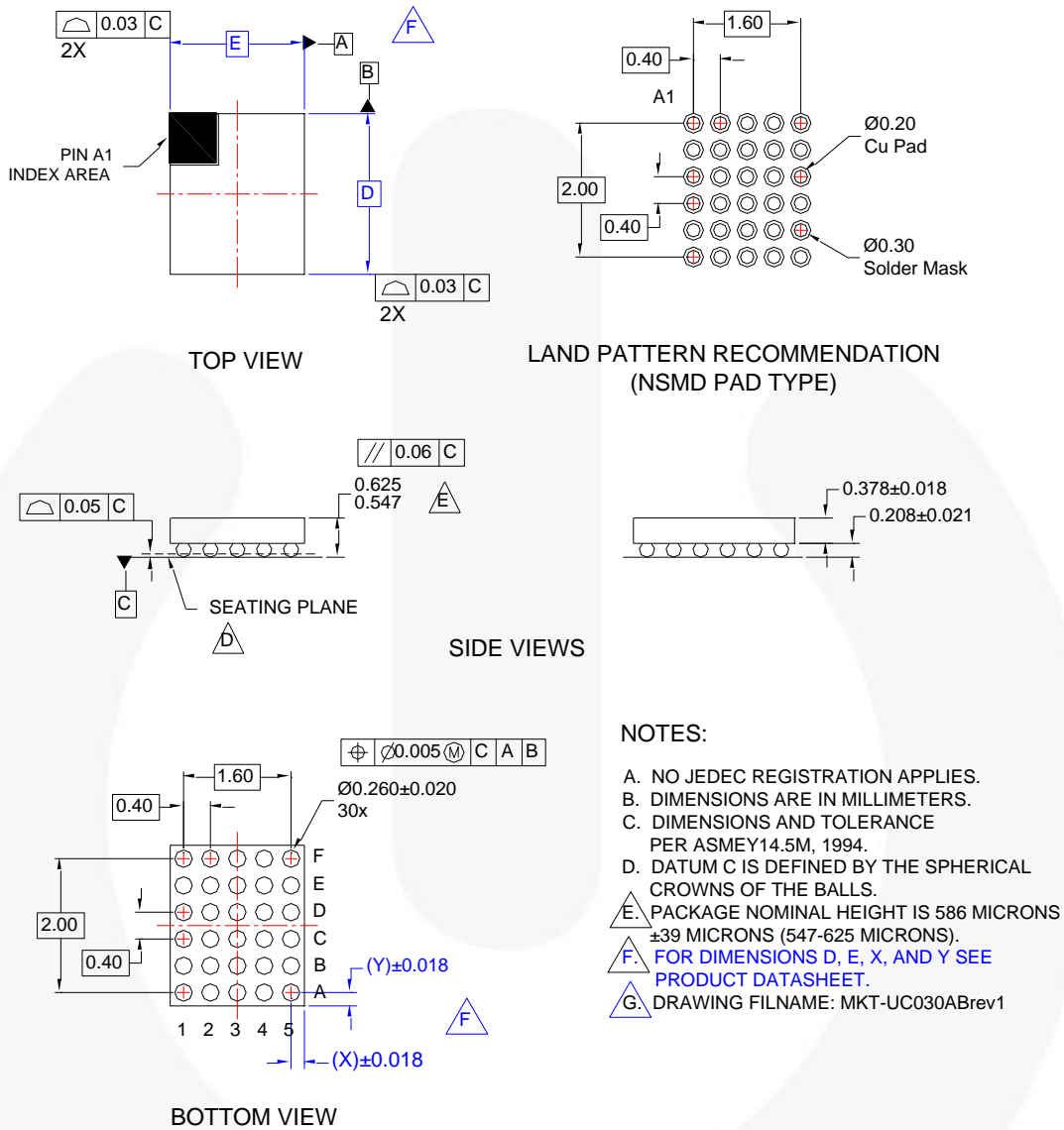


Figure 61. 30-Ball, WLCSP, 5x6 Array, 0.4 mm Pitch, 586  $\mu$ m Package Height

## Product-Specific Dimensions

Product	D	E	X	Y
FAN54300UCX	2.460 $\pm$ 0.030 mm	2.26 $\pm$ 0.030 mm	0.330 mm	0.230 mm



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