

FAN7535

PFC & Ballast Control IC

Features

- PFC, Ballast Control, and Half-Bridge Driver in One IC
- PFC Driver Current Capability: +500mA/-800mA
- Critical Conduction Mode Control Type PFC
- Internal Clamping Zener Diode (PFC): 23V
- Under-Voltage Lockout with 3.5V of Hysteresis (PFC)
- Internal Clamping Zener Diode (Ballast): 15V
- Lower di/dt Gate Driver for Better Noise Immunity
- Under-Voltage Lockout with 1.8V Hysteresis (Ballast)
- Ballast Driver Current Capability: +350mA/-650mA
- Programmable Preheat Time & Frequency
- Programmable Run Frequency
- Programmable Ignition Sweep Time
- Internal Active ZVS Control
- Internal Protection Function (Latch Mode)

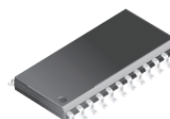
Applications

- Fluorescent Lamp Ballast

Description

FAN7535 provides simple, high-performance, active power factor correction (PFC), and ballast control. The FAN7535 is optimized for all kinds of fluorescent lamps, which require minimum board area and reduced external components. The FAN7535 PFC control block to reduce the input current THD lower than conventional CRM boost PFC methods. An innovative Active Zero Voltage Switching (AZVS) block reduces the switching power loss. A dedicated timing section in the FAN7535 allows the user set the necessary parameters for proper lamp preheat and ignition.

24-SOP



Ordering Information

Part Number	Package	Operating Temperature Range	Packing Method
FAN7535M	24-SOP	-25°C ~ 125°C	Tube
FAN7535MX			Tape & Reel



All packages are lead free per JEDEC: J-STD-020B standard.

Typical Application Diagrams

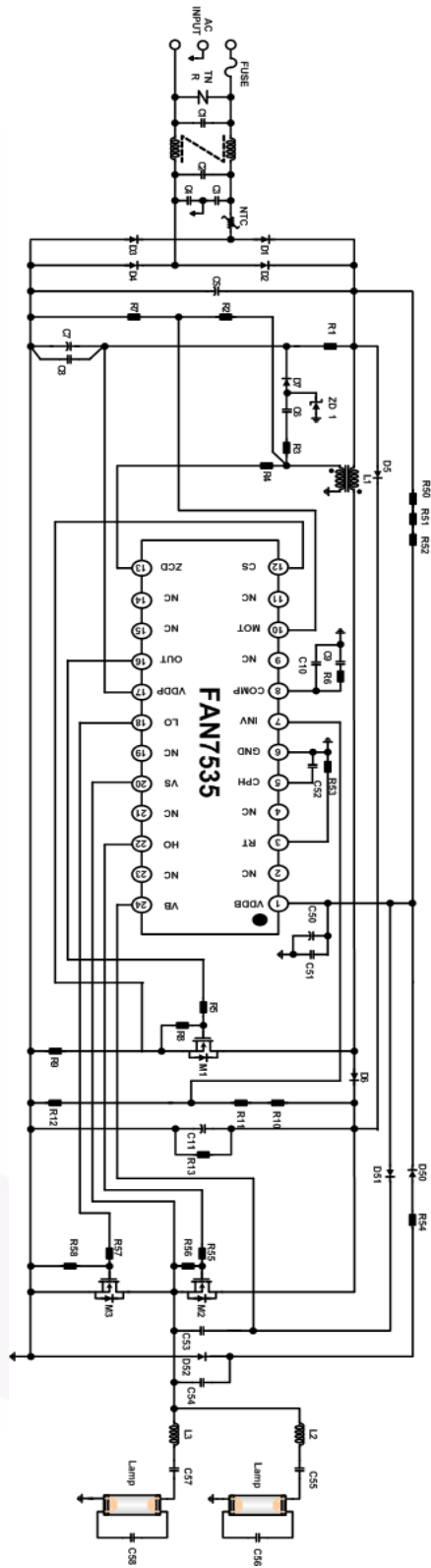


Figure 1. Typical Application Circuit for Fluorescent Lamp

Internal Block Diagram

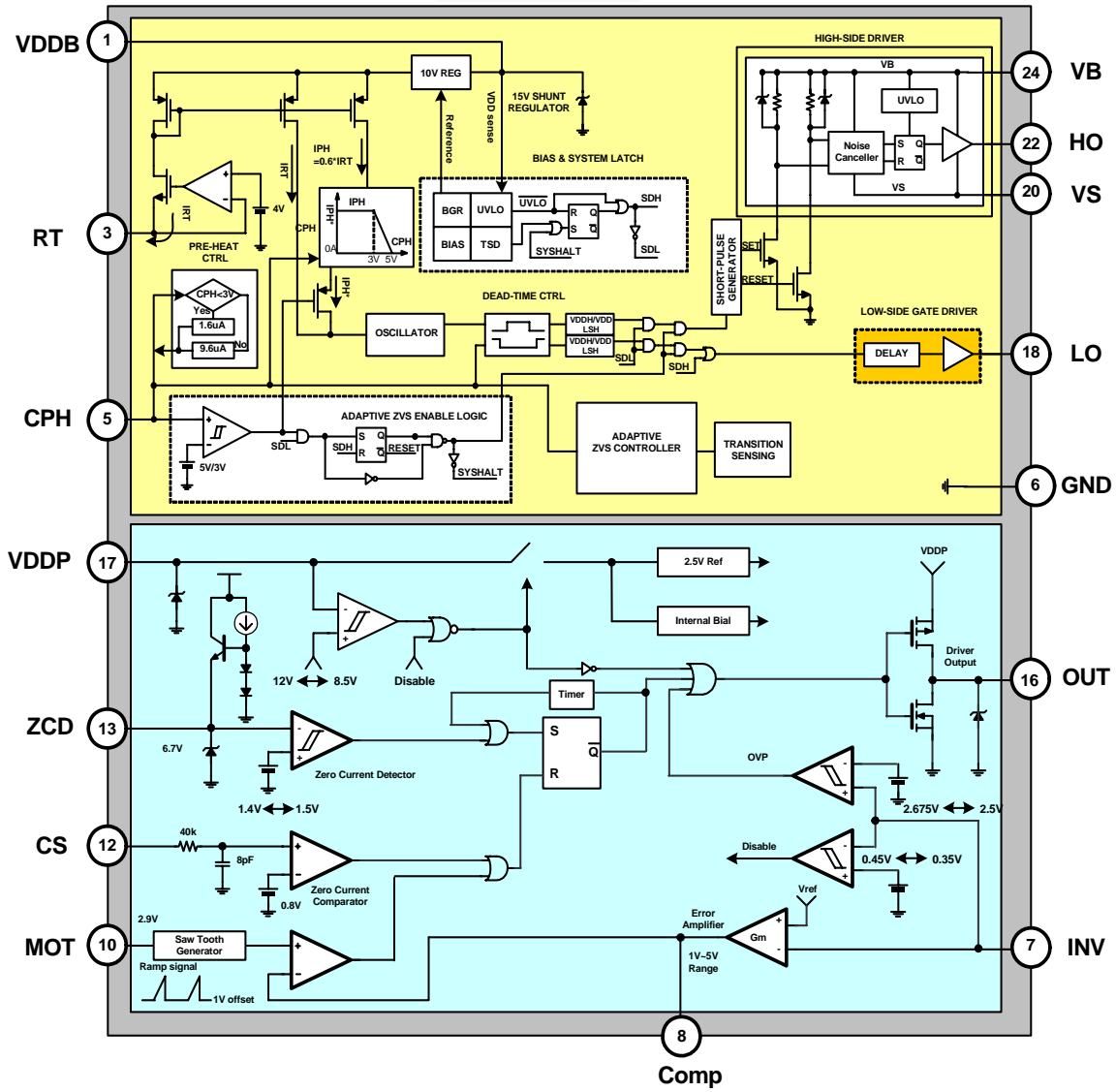


Figure 2. Functional Block Diagram (2chips-1PKG)

Pin Configuration

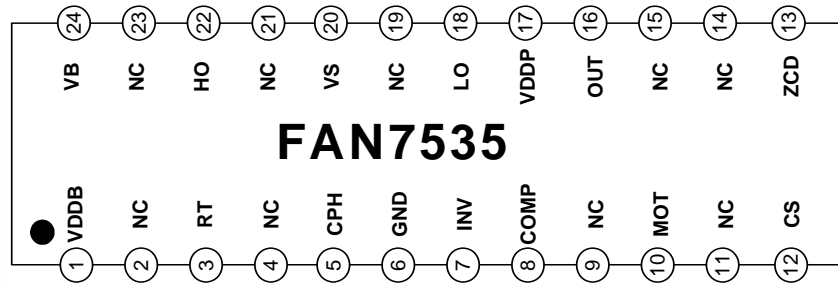


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	VDDDB	Supply voltage for ballast part
2	NC	No connection
3	RT	Oscillator frequency set resistor
4	NC	No connection
5	CPH	Preheating time set capacitor
6	GND	Ground for ballast part & PFC part
7	INV	Inverting input of the error amplifier
8	COMP	Output of the transconductance error amplifier
9	NC	No connection
10	MOT	Set the slope of the internal ramp
11	NC	No connection
12	CS	Input of the over-current protection comparator
13	ZCD	Input of the zero current detection block
14	NC	No connection
15	NC	No connection
16	OUT	Gate driver output
17	VDDP	Supply voltage for PFC block
18	LO	Low-side output
19	NC	No connection
20	VS	High-side floating supply return
21	NC	No connection
22	HO	High-side output
23	NC	No connection
24	VB	High-side floating supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability.

The absolute maximum ratings are stress ratings only. $T_A=25^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
PFC PART					
V_{DDP}	Supply Voltage		V_Z		V
I_{OH}, I_{OL}	Peak Drive Output Current	-800		+500	mA
I_{CLAMP}	Driver Output Clamping Diodes $V_O > V_{CC}$ or $V_O < -0.3V$		± 10		
I_{DET}	Detector Clamping Diodes		± 10		
V_{IN}	Error Amplifier, MOT, CS Input Voltages	-0.3		6.0	V
BALLAST PART					
V_B	High-side Floating Supply	-0.3		625.0	V
V_S	High-side floating supply return	-0.3		600.0	
V_{IN}	RT, CPH Pins Input Voltage	-0.3		8.0	
V_{CL}	Clamping Voltage		V_{CL}		mA
I_{CL}	Clamping Current Level		25		
dV_S/dt	Allowable Offset Voltage Slew Rate			50	V/ns
Common					
T_{OPR}	Operating Temperature Range	-25		+125	$^{\circ}\text{C}$
T_{STG}	Storage Temperature Range	-65		+150	
P_D	Total Power Dissipation		1.5		W
θ_{JA}	Thermal Resistance (Junction-to-Air)			83	$^{\circ}\text{C}/\text{W}$

Caution:

Do not supply a low-impedance voltage source to the internal clamping Zener diode between the GND and the VDDDB and VDDP pins of this device. Use a common supply between the two ICs (PFC, Ballast) only under careful attention.

Electrical Characteristics

$V_{DDP}=14V$, $T_A = 25^{\circ}C$, unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
PFC PART⁽¹⁾						
UNDER-VOLTAGE LOCKOUT SECTION						
$V_{th(start)}$	Start Threshold Voltage	V_{DDP} Increasing	11	12	13	V
$V_{th(stop)}$	Stop Threshold Voltage	V_{DDP} Decreasing	7.5	8.5	9.5	
$H_{Y(UVLO)}$	UVLO Hysteresis		3.0	3.5	4.0	
V_Z	Zener Voltage	$I_{DDP} = 20mA$	20	22	24	
SUPPLY CURRENT SECTION						
I_{st}	Start-up Supply Current	$V_{DDP} = V_{TH(START)} - 0.2V$		40	70	mA
I_{DDP}	Operating Supply Current	Output not switching		1.5	3.0	mA
$I_{DDP(dyn)}$	Dynamic Operating Supply Current	50kHz, $C_L = 1nF$		2.5	4.0	
$I_{DD(dis)}$	Operating Current at Disable	$V_{INV} = 0V$	20	65	95	mA
ERROR AMPLIFIER SECTION						
V_{ref1}	Voltage Feedback Input Threshold1	$T_A = 25^{\circ}C$	2.465	2.500	2.535	V
DV_{ref1}	Line Regulation	$14V \leq V_{DDP} \leq 20V$		0.1	10.0	mV
$DV_{ref3}^{(1)}$	Temperature Stability of V_{REF}			20		
$I_{b(ea)}$	Input Bias Current	$1V \leq V_{inv} \leq 4V$	-0.5		0.5	mA
I_{source}	Output Source Current	$V_{inv} = V_{ref1} - 0.1V$		-12		
I_{sink}	Output Sink Current	$V_{inv} = V_{ref1} + 0.1V$		12		
$V_{eao(H)}$	Output Upper Clamp Voltage	$V_{inv} = V_{ref1} - 0.1V$	5.4	6.0	6.6	V
$V_{eao(Z)}$	Zero Duty Cycle Output Voltage		0.9	1.0	1.1	
$g_m^{(2)}$	Transconductance		90	115	140	μmho
MAXIMUM ON-TIME SECTION						
V_{MOT}	Maximum On-Time Voltage	$R_{MOT} = 40.5\Omega$	2.784	2.900	3.016	V
T_{ON-MAX}	Maximum On-Time Programming	$R_{MOT} = 40.5\Omega, T_A = 25^{\circ}C$	19	24	29	μs
CURRENT-SENSE SECTION						
$V_{CS(LIMIT)}$	Current Sense Input Threshold Voltage Limit		0.7	0.8	0.9	V
$I_{b(cs)}$	Input Bias Current	$0V \leq V_{CS} \leq 1V$	-1.0	-0.1	1.0	mA
$Td_{(cs)}^{(1)}$	Current Sense Delay to Output			350	500	ns

Notes:

1. Please refer to the FAN7529 datasheet and AN-6026 application note for more detailed information. Available on Fairchild's website at:

[Datasheet: http://www.fairchildsemi.com/ds/FA%2FFAN7529.pdf](http://www.fairchildsemi.com/ds/FA%2FFAN7529.pdf)

[Application Note: http://www.fairchildsemi.com/an/AN/AN-6026.pdf](http://www.fairchildsemi.com/an/AN/AN-6026.pdf)

2. This parameter, although guaranteed, is not 100% tested in production.

Electrical Characteristics (Continued)V_{DDP} = 14V, T_A = 25°C, unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
ZERO CURRENT DETECT SECTION						
V _{th(ZCD)} ⁽³⁾	Input Voltage Threshold		1.35	1.50	1.65	V
HY _(ZCD) ⁽³⁾	Detect Hysteresis		0.05	0.10	0.15	
V _{clamp(h)}	Input High Clamp Voltage	I _{DET} = 3mA	6.0	6.7	7.4	
V _{clamp(l)}	Input Low Clamp Voltage	I _{DET} = -3mA	0	0.65	1.00	
I _{b(ZCD)}	Input Bias Current	1V ≤ V _{ZCD} ≤ 5V	-1.0	-0.1	1.0	mA
I _{source(ZCD)} ⁽³⁾	Source Current Capability	T _A = 25°C			-10	mA
I _{sink(ZCD)} ⁽³⁾	Sink Current Capability	T _A = 25°C			10	
T _{DEAD} ⁽³⁾	Maximum Delay, ZCD to Output Turn-on		100		200	
OUTPUT SECTION						
V _{oh}	Output Voltage High	I _O = -100mA, T _A = 25°C	9.2	11.0	12.8	V
V _{ol}	Output Voltage Low	I _O = 100mA, T _A = 25°C		1.0	2.5	
T _r ⁽³⁾	Rising Time	C _I = 1nF		50	100	ns
T _f ⁽³⁾	Falling Time	C _I = 1nF		50	100	
V _{O(MAX)}	Maximum Output Voltage	V _{DDP} = 20V, I _O = 100mA	11.5	13.0	14.5	V
V _{O(UVLO)}	Output Voltage with UVLO Activated	V _{DDP} = 5V, I _O = 100mA			1	
RESTART TIMER SECTION						
t _{d(rst)}	Restart Time Delay		50	150	300	ms
OVER-VOLTAGE PROTECTION SECTION						
V _{OVP}	OVP Threshold Voltage	T _A = 25°C	2.620	2.675	2.730	V
HY _(OVP)	OVP Hysteresis	T _A = 25°C	0.120	0.175	0.230	
ENABLE SECTION						
V _{th(en)}	Enable Threshold Voltage		0.40	0.45	0.50	V
HY _(en)	Enable Hysteresis		0.05	0.10	0.15	

Note:

3. These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (Continued)

V_{BIAS} (V_{DDB} , V_{BS}) = 14.0V, T_A = 25°C, unless otherwise specified.

Symbol	Characteristics	Condition	Min.	Typ.	Max.	Unit
BALLAST PART⁽⁴⁾						
Supply Voltage Section						
$V_{DDTH(ST+)}$	V_{DDB} UVLO Positive Going Threshold	V_{DDB} Increasing	12.4	13.4	14.4	V
$V_{DDTH(ST-)}$	V_{DDB} UVLO Negative Going Threshold	V_{DDB} Decreasing	10.8	11.6	12.4	
$V_{DDHY(ST)}$	V_{DDB} -side UVLO Hysteresis			1.8		
V_{CL}	Supply Clamping Voltage	$I_{DDB} = 10mA$	14.8	15.2		
I_{ST}	Start-up Supply Current	$V_{DDB} = 12V$		150		μA
$I_{DDB(dyn)}$	Dynamic Operating Supply Current	50kHz, $C_L = 1nF$		3.2		mA
High-Side Supply Section (V_B-V_S)						
$V_{HSTH(ST+)}$	High-side UVLO Positive Going Threshold	V_{BS} Increasing	8.5	9.2	10.0	V
$V_{HSTH(ST-)}$	High-side UVLO Negative Going Threshold	V_{BS} Decreasing	7.9	8.6	9.5	
$V_{HSHY(ST)}$	High-side UVLO Hysteresis			0.6		
I_{HST}	High-side Quiescent Supply Current	$V_{BS} = 14V$		50		μA
I_{HD}	High-side Dynamic Operating Supply Current	50kHz, $C_L = 1nF$		1		mA
I_{LK}	Offset Supply Leakage Current	$V_B = V_S = 600V$			45	μA
Oscillator Section						
V_{MPH}	CPH Pin Preheating Voltage Range		2.5	3.0	3.5	V
I_{PH}	CPH Pin Charging Current During Preheating	$V_{CPH} = 1V$	1.25	2.00	2.85	μA
I_{IG}	CPH Pin Charging Current During Ignition	$V_{CPH} = 4V$	8	12	16	
V_{MO}	CPH Pin Voltage Level at Running Mode			7.0		V
f_{PRE}	Preheating Frequency	$R_T = 80k\Omega$, $V_{CPH} = 2V$	72	85	98	kHz
f_{OSC}	Running Frequency	$R_T = 80k\Omega$	48.2	53.0	57.8	kHz
DT_{MAX}	Maximum Dead Time	$V_{CPH} = 1V$, $V_S = GND$ in Preheat Mode		3.1		μs
DT_{MIN}	Minimum Dead Time	$V_{CPH} = 6V$, $V_S = GND$ in Run Mode		1.0		μs
Output Section						
I_{OH+}	High-side Driver Sourcing Current	$PW = 10\mu s$	250	350		mA
I_{OH-}	High-side Driver Sinking Current	$PW = 10\mu s$	500	650		
I_{OL+}	Low-side Driver Sourcing Current	$PW = 10\mu s$	250	350		
I_{OL-}	Low-side Driver Sink Current	$PW = 10\mu s$	500	650		
t_{HOR}	High-side Driver Turn-on Rising Time	$C_L = 1nF$, $V_{BS} = 15V$		45		ns
t_{HOL}	High-side Driver Turn-off Rising Time	$C_L = 1nF$, $V_{BS} = 15V$		25		
t_{LOR}	Low-side Driver Turn-on Rising Time	$C_L = 1nF$, $V_{BS} = 15V$		45		
t_{LOL}	Low-side Driver Turn-off Rising Time	$C_L = 1nF$, $V_{BS} = 15V$		25		
$V_S^{(5)}$	Maximum Negative V_S Swing Range for Signal Propagation to High-side Output			-9.8		V

Electrical Characteristics (Continued)

V_{BIAS} (V_{DDB} , V_{BS}) = 14.0V, T_A = 25°C, unless otherwise specified.

Symbol	Characteristics	Condition	Min.	Typ.	Max.	Unit
Protection Section						
V_{CPHSD}	Shutdown Voltage	$V_{RT} = 0$ After Run Mode	2.6			V
I_{SD}	Shutdown Current			250	450	μ A
TSD ⁽⁵⁾	Thermal Shutdown			165		°C

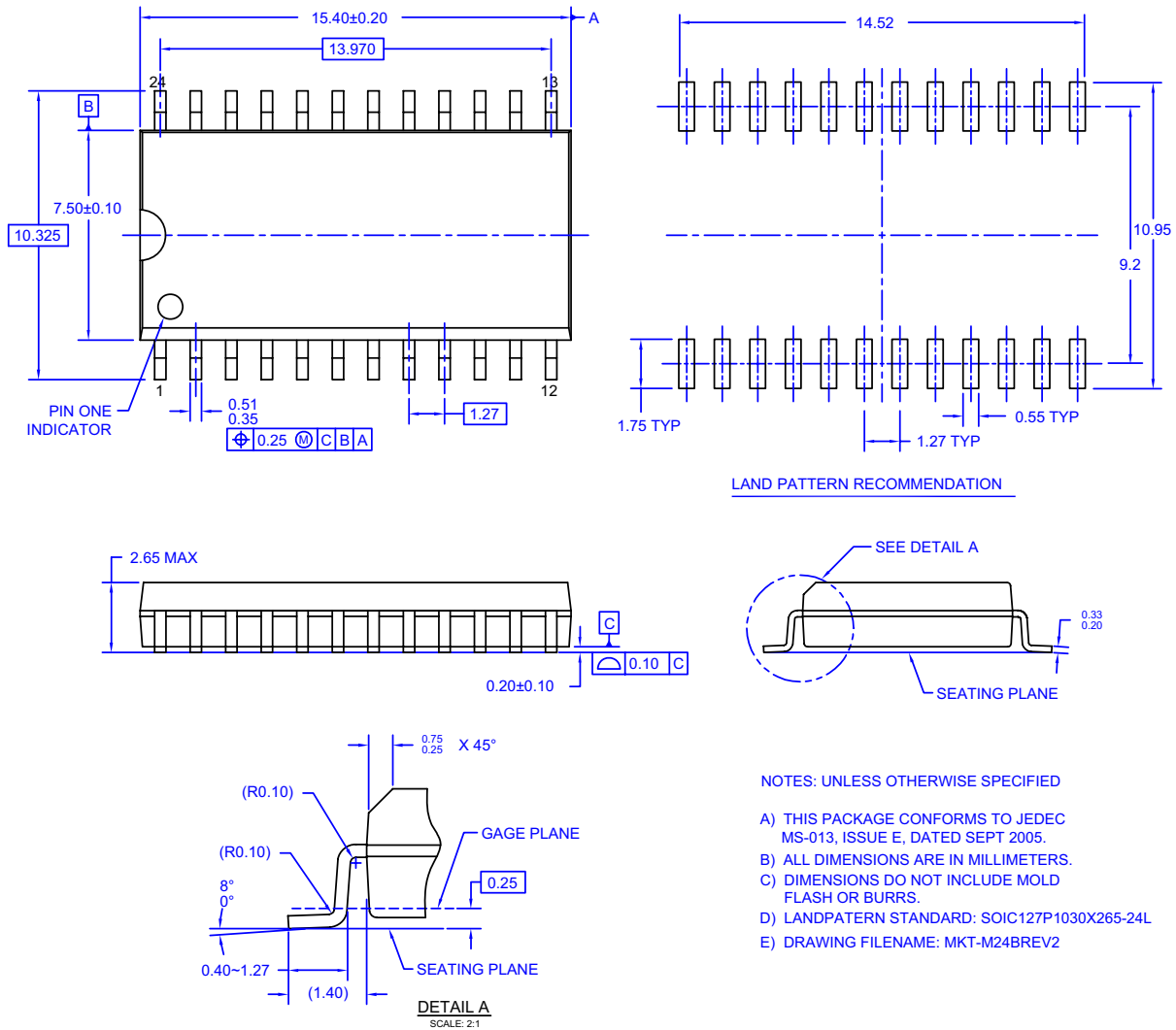
Notes:

- Please refer to the FAN7711 datasheet for more detailed information. Available on Fairchild's website at:
[Datasheet: http://www.fairchildsemi.com/ds/FA%2FFAN7711.pdf](http://www.fairchildsemi.com/ds/FA%2FFAN7711.pdf)
- This parameter, although guaranteed, is not 100% tested in production.

Component List for 32W Two Lamps

Part	Value	Note	Part	Value	Note
Resistor			C55	15nF/630V	Miller Capacitor
R1	330k Ω	1/2W	C56	2.7nF/1kV	Miller Capacitor
R2	750k Ω	1/4W	C57	15nF/630V	Miller Capacitor
R3	100 Ω	1/2W	C58	2.7nF/1kV	Miller Capacitor
R4	20k Ω	1/4W	Diode		
R5	47 Ω	1/4W	D1	1N4007	1kV,1A
R6	10k Ω	1/4W	D2	1N4007	1kV,1A
R7	50k Ω	1/4W	D3	1N4007	1kV,1A
R8	47k Ω	1/4W	D4	1N4007	1kV,1A
R9	0.3 Ω	1W	D5	UF4007	Ultra Fast,1kV,1A
R10	1M Ω	1/4W	D6	UF4007	Ultra Fast,1kV,1A
R11	1M Ω	1/4W	D7	1N4148	100V,1A
R12	12.6k Ω	1/4W,1%	D8	1N4148	100V,1A
R13	220k Ω	2W	D50	UF4007	Ultra Fast,1kV,1A
R50	150k Ω	1/4W	D51	UF4007	Ultra Fast,1kV,1A
R51	150k Ω	1/4W	D52	UF4007	Ultra Fast,1kV,1A
R52	150k Ω	1/4W	ZD1	IN4746A	Zener 18V, 1W
R53	90k Ω	1/4W,1%	MOSFET		
R54	10 Ω	1/4W	M1	FQPF5N60C	500V,6A
R55	47 Ω	1/4W	M2	FQPF5N50C	500V,5A
R56	47k Ω	1/4W	M3	FQPF5N50C	500V,5A
R57	47 Ω	1/4W	Fuse		
R58	47k Ω	1/4W	Fuse	3A/250V	
Capacitor			TNR		
C1	47nF/275V _{AC}	Box Capacitor	TNR	471	
C2	150nF/275V _{AC}	Box Capacitor	NTC		
C3	2200pF/3kV	Ceramic Capacitor	NTC	10D-09	
C4	2200pF/3kV	Ceramic Capacitor	Line Filter		
C5	0.22 μ F/630V	Miller Capacitor	LF1	40mH	
C6	12nF/50V	Ceramic Capacitor	Transformer		
C7	22 μ F/50V	Electrolytic Capacitor	L1	0.94mH (75T:10T)	EI2820
C8	39pF/50V	Ceramic Capacitor	Inductor		
C9	1 μ F/50V	Ceramic Capacitor	L2	3.2mH (130T)	EI2820
C10	0.1 μ F/50V	Ceramic Capacitor	L3	3.2mH (130T)	EI2820
C11	47 μ F/450V	Electrolytic Capacitor	IC		
C50	10 μ F/50V	Electrolytic Capacitor	U1	FAN7535	Fairchild Semiconductor
C51	1 μ F/50V	Ceramic Capacitor			
C52	0.47 μ F/25V	Ceramic Capacitor, 5%			
C53	100nF/50V	Ceramic Capacitor			
C54	470pF/1kV	Ceramic Capacitor			

Package Dimensions



M24BREV2

Figure 4. 24-Lead Small Outline Package (SOP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.


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<http://www.fairchildsemi.com/packaging/>



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- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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