

# FAN8005D2

## 3-CH Motor Driver

### Features

- 3-Channel BTL (Balanced transformer-less) driver
- Built-in variable regulator with reset (Series-REG)
- Built-in thermal shutdown circuit
- Built-in power save circuit
- Built-in general OP-amp
- Operating supply voltage: 4.5V ~ 5.5V
- Corresponds to 3.3V or 5V DSP

### Description

The FAN8005D2 is a monolithic integrated circuit, suitable for a 3-ch motor driver which drives focus actuator, tracking actuator, and sled motor of a CD-media system.

28-SSOPH-300



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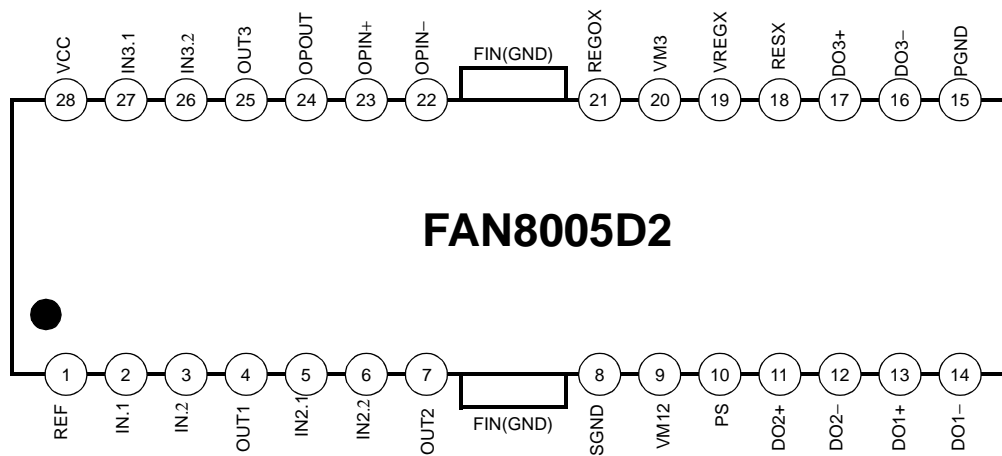
### Typical Applications

- Compact disk player
- Digital video disk player
- Compact disk ROM

### Ordering Information

Device	Package	Operating Temp.
FAN8005D2	28-SSOPH-300	-35°C ~ +85°C
FAN8005D2TF	28-SSOPH-300	-35°C ~ +85°C

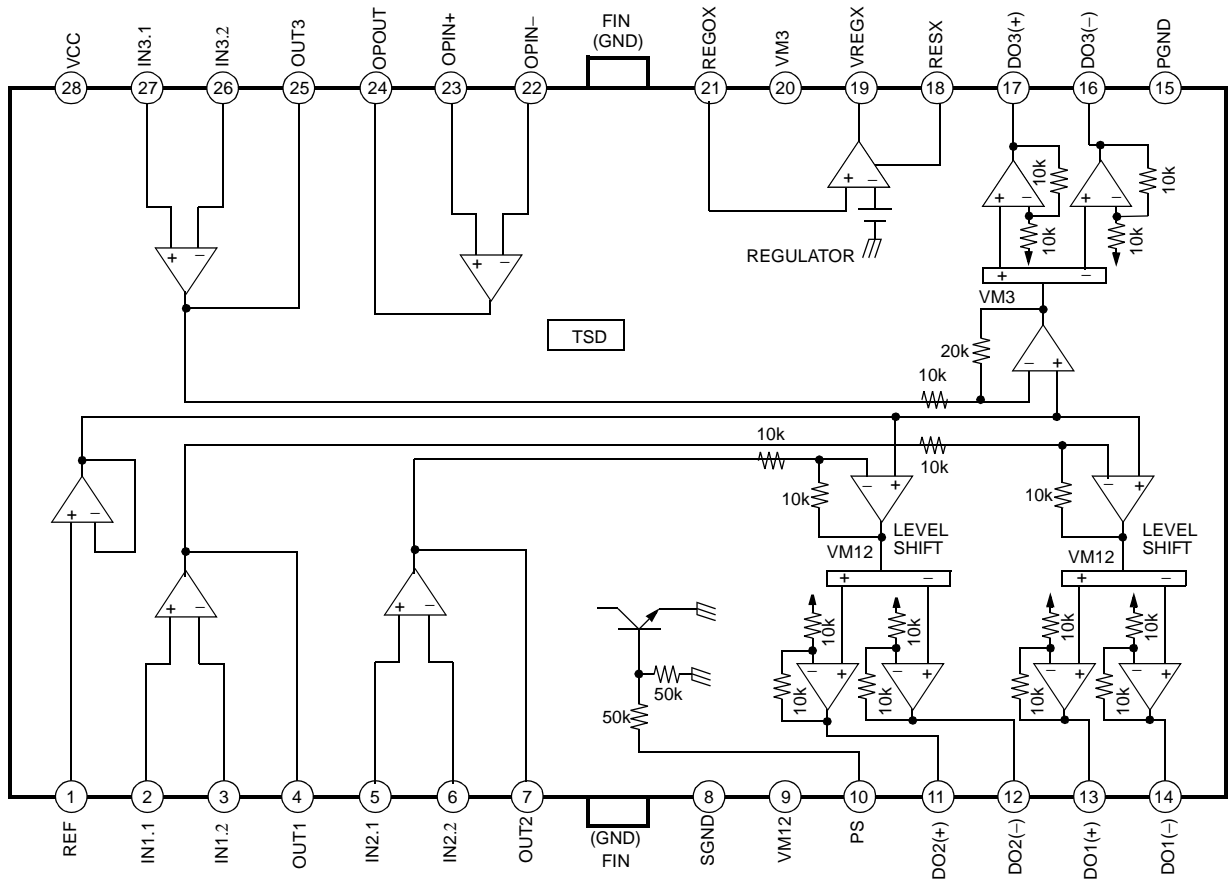
## Pin Assignments



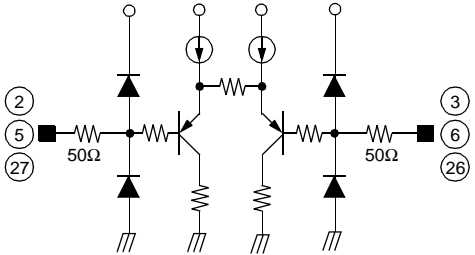
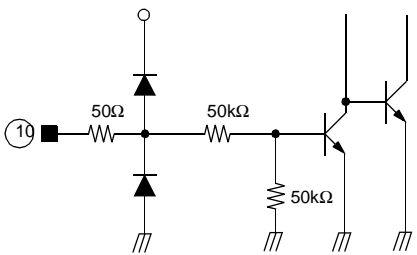
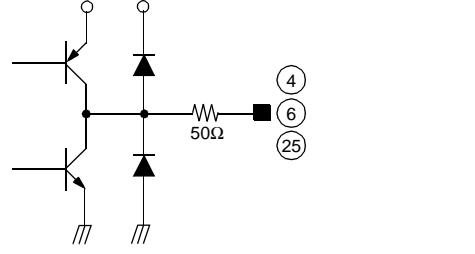
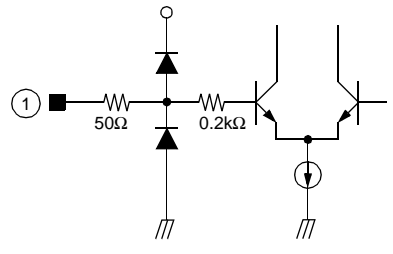
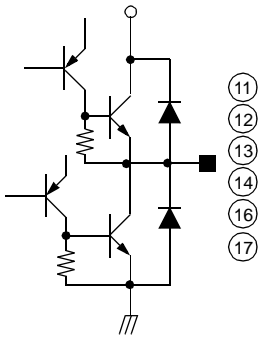
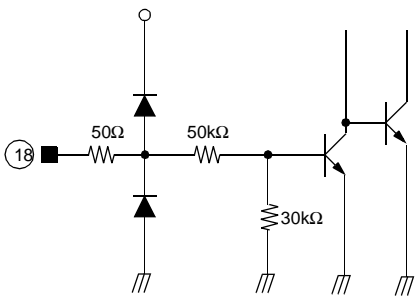
## Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	REF	I	Bias voltage input
2	IN1.1	I	Op-amp CH1 input (+)
3	IN1.2	I	Op-amp CH1 input (-)
4	OUT1	O	Op-amp CH1 output
5	IN2.1	I	Op-amp CH2 input (+)
6	IN2.2	I	Op-amp CH2 input (-)
7	OUT2	O	Op-amp CH2 output
8	SGND	-	Signal ground
9	VM12	-	BTL CH1, 2 supply voltage
10	PS	I	Power save
11	DO2+	O	Drive2 output (+)
12	DO2-	O	Drive2 output (-)
13	DO1+	O	Drive1 output (+)
14	DO1-	O	Drive1 output (-)
15	PGND	-	Power ground
16	DO3-	O	Drive3 output (-)
17	DO3+	O	Drive3 output (+)
18	RESX	I	Regulator reset
19	VREGX	O	Op-amp output
20	VM3	-	BTL CH3 supply voltage
21	REGOX	I	Op-amp input(+)
22	OPIN-	I	Op-amp input (-)
23	OPIN+	I	Op-amp input (+)
24	OPOUT	O	Op-amp output
25	OUT3	O	Op-amp CH3 output
26	IN3.2	I	Op-amp CH3 input (-)
27	IN3.1	I	Op-amp CH3 input (+)
28	VCC	-	Supply voltage

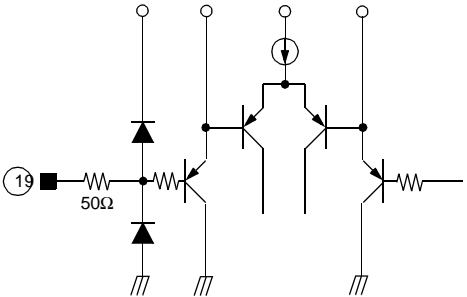
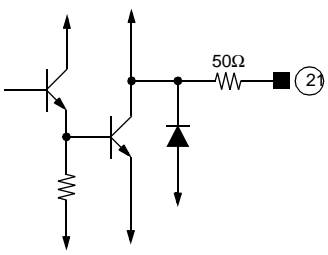
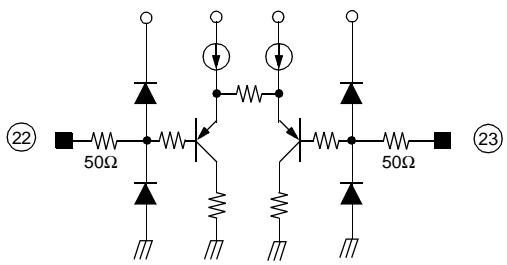
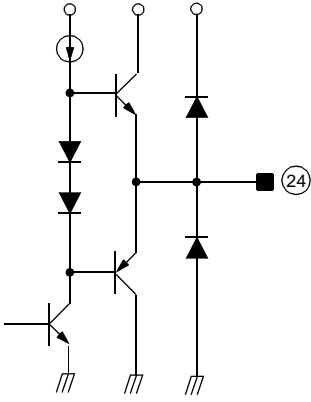
# Internal Block Diagram



## Equivalent Circuits

Error amp input	Power save input
 <p>The diagram shows an input node connected to a 50Ω resistor, which is in series with a diode connected to ground. This node is also connected to a 50Ω resistor leading to another node. This second node is connected to a diode to ground and the base of a PNP transistor. The emitter of this transistor is connected to a 50kΩ resistor to ground and the base of an NPN transistor. The emitter of the NPN transistor is connected to a 50Ω resistor to ground. The collector of the NPN transistor is connected to a diode to ground and a 50Ω resistor leading to a final node. This final node is connected to a diode to ground and a 50Ω resistor to ground. Pin numbers 2, 5, 27, 3, 6, and 26 are indicated.</p>	 <p>The diagram shows an input node connected to a 50Ω resistor to ground and a diode to ground. This node is also connected to a 50kΩ resistor leading to another node. This second node is connected to a diode to ground and the base of a PNP transistor. The emitter of this transistor is connected to a 50kΩ resistor to ground and the base of an NPN transistor. The emitter of the NPN transistor is connected to ground. The collector of the NPN transistor is connected to ground. Pin number 10 is indicated.</p>
Error amp output	Signal reference input
 <p>The diagram shows an output node connected to a diode to ground and the collector of a PNP transistor. The emitter of this transistor is connected to ground. The base of the PNP transistor is connected to a 50Ω resistor leading to a node. This node is connected to a diode to ground and the base of an NPN transistor. The emitter of the NPN transistor is connected to ground. The collector of the NPN transistor is connected to ground. Pin numbers 4, 6, and 25 are indicated.</p>	 <p>The diagram shows an input node connected to a 50Ω resistor to ground and a diode to ground. This node is also connected to a 0.2kΩ resistor leading to another node. This second node is connected to a diode to ground and the base of a PNP transistor. The emitter of this transistor is connected to a 50kΩ resistor to ground and the base of an NPN transistor. The emitter of the NPN transistor is connected to ground. The collector of the NPN transistor is connected to ground. Pin number 1 is indicated.</p>
Power output	Regulator reset
 <p>The diagram shows a power output stage with a diode to ground and the collector of a PNP transistor. The emitter of this transistor is connected to a 50kΩ resistor to ground and the base of an NPN transistor. The emitter of the NPN transistor is connected to a 50kΩ resistor to ground and the base of another PNP transistor. The emitter of this second PNP transistor is connected to ground. The collector of the second PNP transistor is connected to a diode to ground and a 50Ω resistor to ground. Pin numbers 11, 12, 13, 14, 16, and 17 are indicated.</p>	 <p>The diagram shows an input node connected to a 50Ω resistor to ground and a diode to ground. This node is also connected to a 50kΩ resistor leading to another node. This second node is connected to a diode to ground and the base of a PNP transistor. The emitter of this transistor is connected to a 30kΩ resistor to ground and the base of an NPN transistor. The emitter of the NPN transistor is connected to ground. The collector of the NPN transistor is connected to ground. Pin number 18 is indicated.</p>

## Equivalent Circuits (Continued)

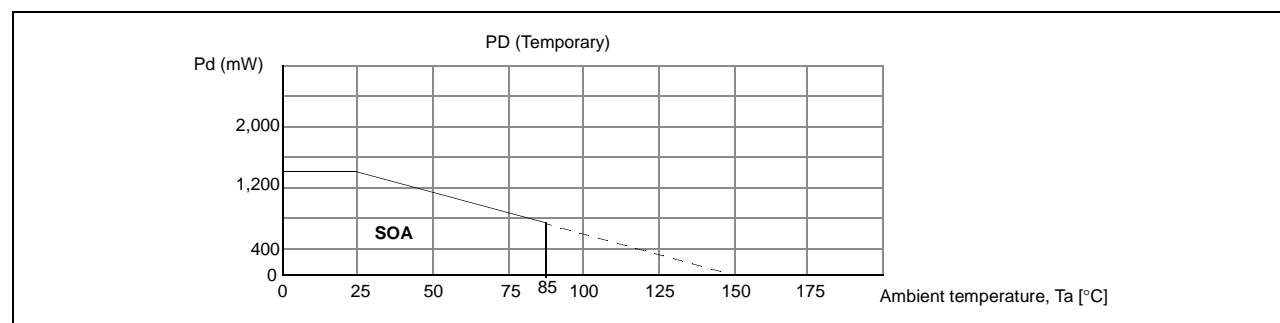
Regulator	Regulator output
	
General op amp input	General op amp output
	

## Absolute Maximum Ratings ( Ta=25°C)

Parameter	Symbol	Value	Unit
Maximum supply voltage	$V_{CCmax}$	7	V
Power dissipation	$P_D$	@1.4	W
Operating temperature range	$T_{OPR}$	-35 ~ +85	°C
Storage temperature range	$T_{STG}$	-55 ~ +150	°C

### Notes:

1. When mounted on a 76.2mm × 114mm × 1.57mm PCB (Phenolic resin material).
2. Power dissipation reduces 11.2mW / °C for using above Ta = 25°C
3. Do not exceed PD and SOA (Safe operating area).



## Recommended Operating Conditions ( Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VCC	4.5	-	5.5	V

## Electrical Characteristics

(Unless otherwise specified,  $T_a=25^\circ\text{C}$ ,  $V_{CC}=V_{M12}=V_{M3}=5\text{V}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Quiescent current	$I_{CC}$	$V_{IN}=0\text{V}$	-	13	-	mA
Power save on current	$I_{PS}$	PS pin=GND	-	-	1	mA
Power save on voltage	$V_{PSon}$	-	-	-	0.5	V
Power save off voltage	$V_{PSoff}$	-	2	-	-	V
<b>BTL DRIVE CIRCUIT</b>						
Output offset voltage 1	$V_{OO1}$	$V_{IN}=2.5\text{V}$ (CH1,2)	-50	-	+50	mV
Output offset voltage 2	$V_{OO2}$	$V_{IN}=2.5\text{V}$ (CH3)	-60	-	+60	mV
Maximum output voltage 1	$V_{OM1}$	$V_{CC}=5\text{V}$ , $R_L=8\Omega$ (CH1, 2)	2.7	3.5	-	V
Maximum output voltage 2	$V_{OM2}$	$V_{CC}=5\text{V}$ , $R_L=24\Omega$ (CH3)	3	3.8	-	V
Closed loop voltage gain 1	$G_{VC1}$	$f=1\text{kHz}$ , $V_{IN}=0.1V_{RMS}$ (CH1, 2)	10.5	12	13.5	dB
Closed loop voltage gain 2	$G_{VC2}$	$f=1\text{kHz}$ , $V_{IN}=0.1V_{RMS}$ (CH3)	16	18	20	dB
Ripple rejection ratio	RR	$V_{IN}=0.1V_{RMS}$ , $f=120\text{Hz}$	-	60	-	dB
Slew rate	SR	$V_O=2\text{V}_{p-p}$ , $f=120\text{kHz}$	-	1	-	$\text{V}/\mu\text{s}$
<b>ERROR AMP CIRCUIT</b>						
Input offset voltage	$V_{OFOP}$	-	-20	-	+20	mV
Input bias current	$I_{BOP}$	-	-	-	300	nA
High level output voltage	$V_{OHOP}$	$V_{CC}=5\text{V}$ , $R_L=10\text{k}\Omega$	4.5	4.8	-	V
Low level output voltage	$V_{OLOP}$	$V_{CC}=5\text{V}$ , $R_L=10\text{k}\Omega$	-	0.2	0.5	V
Output sink current	$I_{SINK}$	$V_{CC}=5\text{V}$ , $R_L=1\text{k}\Omega$	1	3	-	mA
Output source current	$I_{SOURCE}$	$V_{CC}=5\text{V}$ , $R_L=1\text{k}\Omega$	1	3	-	mA
Slew rate	$SR_{OP}$	$f=120\text{kHz}$ , $2\text{V}_{p-p}$	-	1	-	$\text{V}/\mu\text{s}$
<b>GENERAL OP AMP CIRCUIT</b>						
Input offset voltage	$V_{OFOP}$	-	-20	-	+20	mV
Input bias current	$I_{BOP}$	-	-	-	300	nA
High level output voltage	$V_{OHOP}$	$V_{CC}=5\text{V}$ , $R_L=1\text{k}\Omega$	3	4	-	V
Low level output voltage	$V_{OLOP}$	$V_{CC}=5\text{V}$ , $R_L=1\text{k}\Omega$	-	1	1.3	V
Output sink current	$I_{SINK}$	$V_{CC}=5\text{V}$ , $R_L=50\Omega$	2	5	-	mA
Output source current	$I_{SOURCE}$	$V_{CC}=5\text{V}$ , $R_L=50\Omega$	2	5	-	mA
Open loop voltage gain	$G_{VO}$	$V_{IN}=-75\text{dB}$ , $f=1\text{kHz}$	-	75	-	dB
Ripple rejection ratio	$RR_{OP}$	$V_{IN}=-20\text{dB}$ , $f=120\text{Hz}$	-	65	-	dB
Slew rate	$SR_{OP}$	$f=120\text{kHz}$ , $2\text{V}_{p-p}$	-	1	-	$\text{V}/\mu\text{s}$
Common mode rejection ratio	CMRR	$V_{IN}=-20\text{dB}$ , $f=1\text{kHz}$	-	80	-	dB
<b>VARIABLE REGULATOR CIRCUIT</b>						
Regulator output voltage	$V_{REG}$	$I_L=100\text{mA}$	3.0	-	4.5	V
Load regulation	$\Delta V_{R1}$	$I_L=0 \rightarrow 200\text{mA}$	-40	-	10	mV
Line regulation	$\Delta V_{CC}$	$I_L=200\text{mA}$ , $V_{CC}=5 \rightarrow 8\text{V}$	-20	-	30	mV



## Application Information

### 1. Reference Input & Power Save Function

Pin 1 (REF) is a reference input pin.

- Reference input  
The applied voltage at the reference input pin must be between 1.5V and 3.5V, when  $V_{CC}=5V$ .
- Power save input  
The following input conditions must be satisfied for the power save function.

Power save on voltage	Below 0.5V	Power save function operation
Power save off voltage	Above 2V	Normal operation

### 2. Protection Function

Thermal shutdown (TSD)

- If the chip temperature rises above 175°C, the thermal shutdown (TSD) circuit is activated and the output circuit is in the mute state, that is off state. The TSD circuit has a temperature hysteresis of 25°C.

### 3. Regulator & Reset Function

The regulator configuration with the external components is illustrated in figure 1.

- The external circuit is composed of the KSB772 PNP transistor and a capacitor about 33μF, and two feedback resistors R1, R2.  
The capacitor operates both as a ripple eliminator and as a compensator of the feedback loop.
- The output voltage (REG OUT) is

$$V_{out} = \left(1 + \frac{R1}{R2}\right) \times 2.5$$

- When the voltage of pin18 (Vreset) is 0V, the regulator reset function is activated, and the output voltage (REG OUT) becomes 0V. Otherwise, if the voltage of pin 18 is 5V, the regulator operates properly.

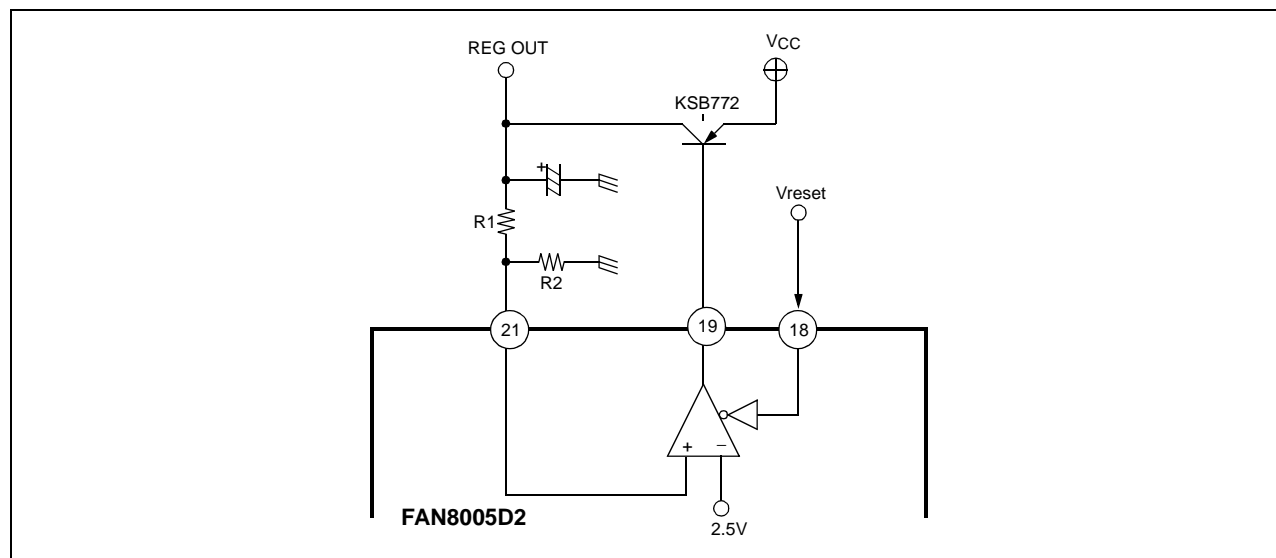
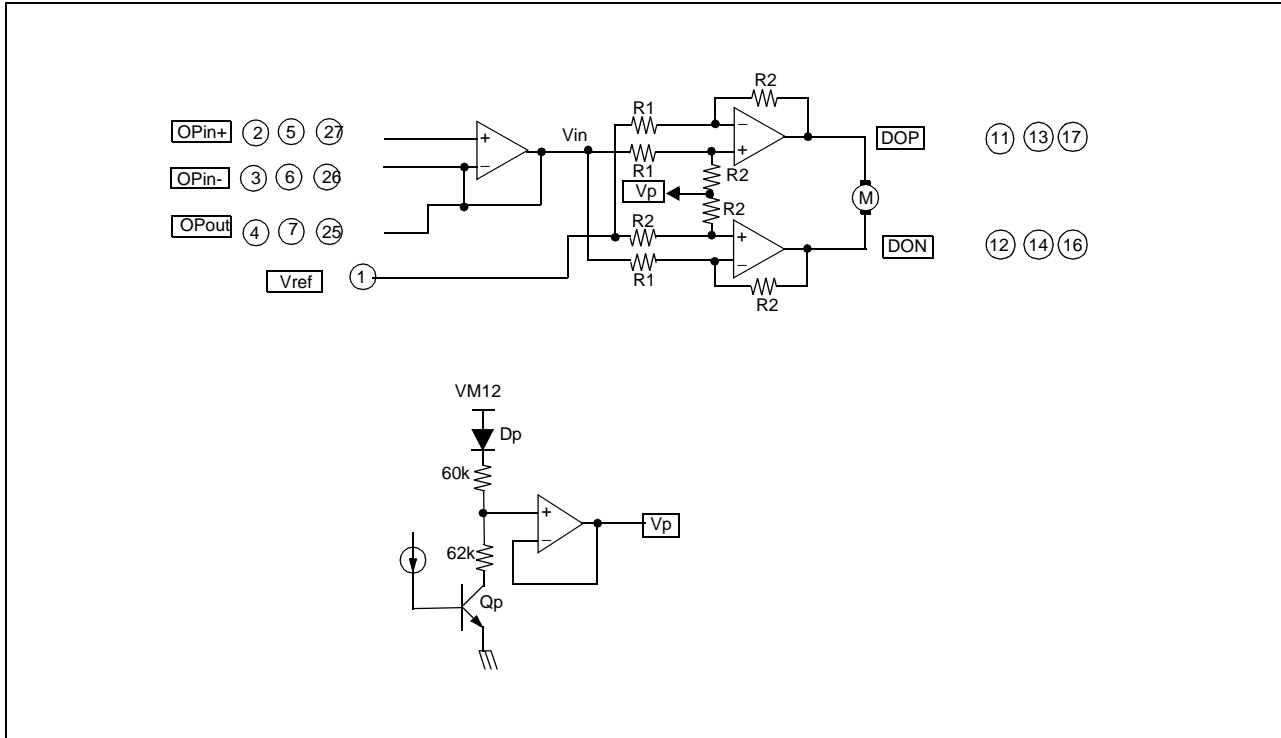


Figure 1. Regulator circuit

4. Focus / Tracking Actuator Sled Motor Drive Part



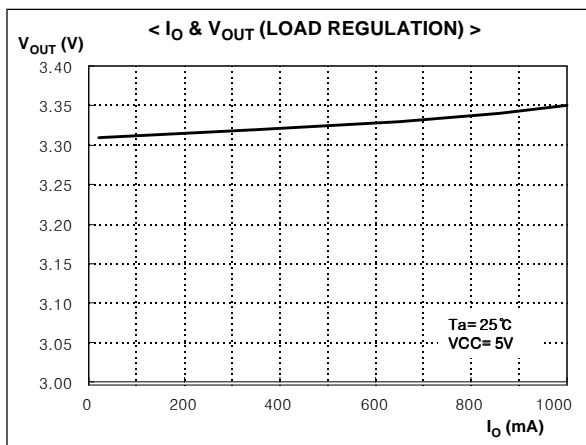
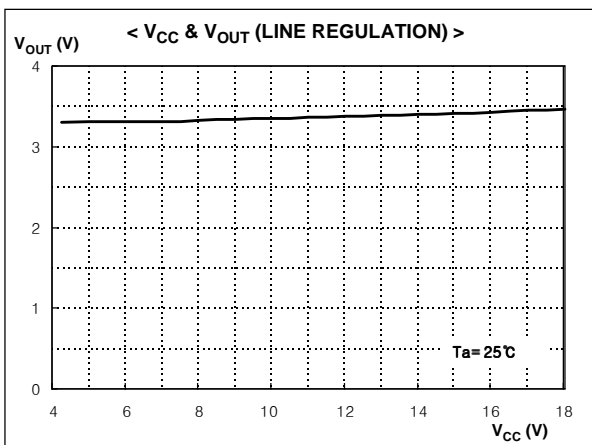
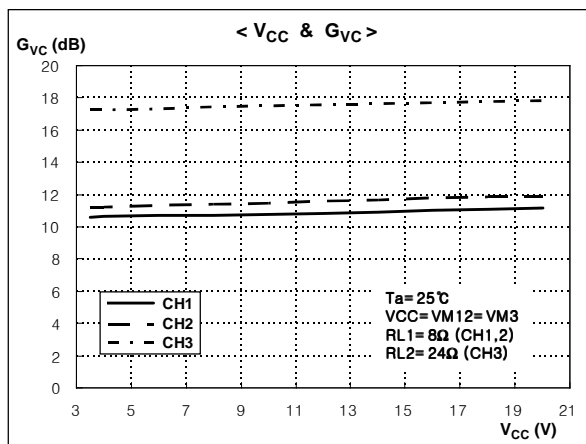
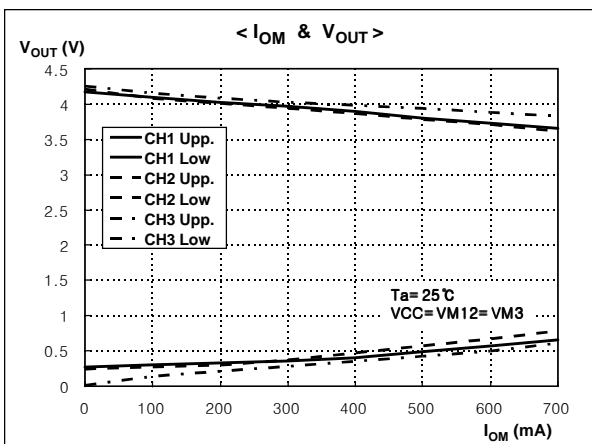
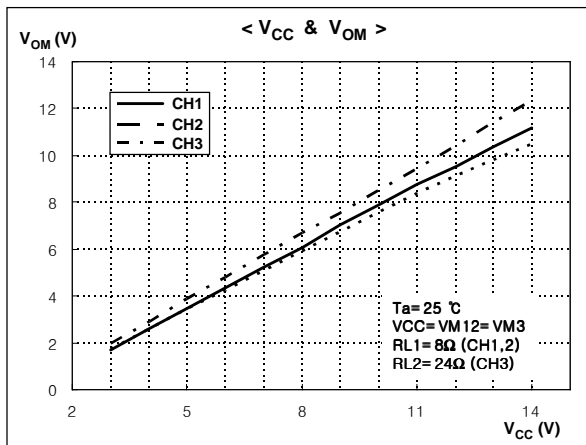
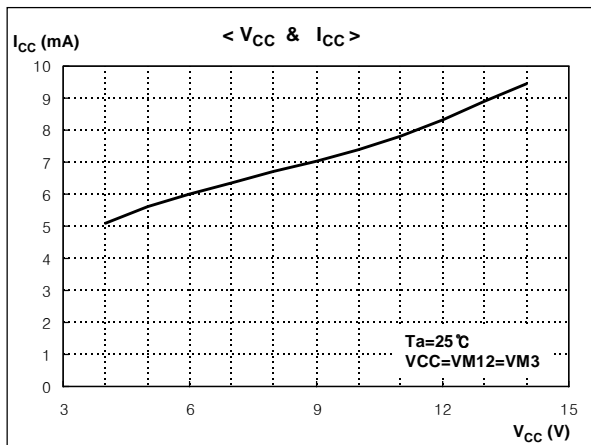
- The voltage, Vref is the reference voltage given by the external bias voltage of the pin 1.
- The input signal (Vin) through pins 3,6 and 26 are amplified one time and then fed to the output stage. (assume that input opamp was used as a buffer)
- The total closed loop voltage gain is as follows (assume that R2=2R1)

$$\begin{aligned}
 V_{in} &= V_{ref} + \Delta V \\
 DOP &= V_p + 2\Delta V \\
 DON &= V_p - 2\Delta V \\
 V_{out} &= DOP - DON = 4\Delta V \\
 \text{Gain} &= 20\log \frac{V_{out}}{\Delta V} = 20\log 4 = 12\text{dB}
 \end{aligned}$$

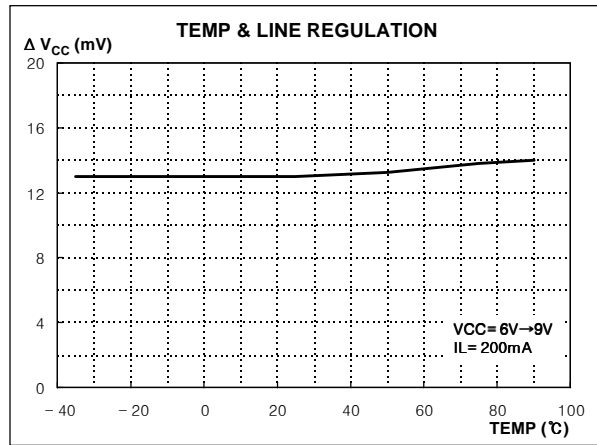
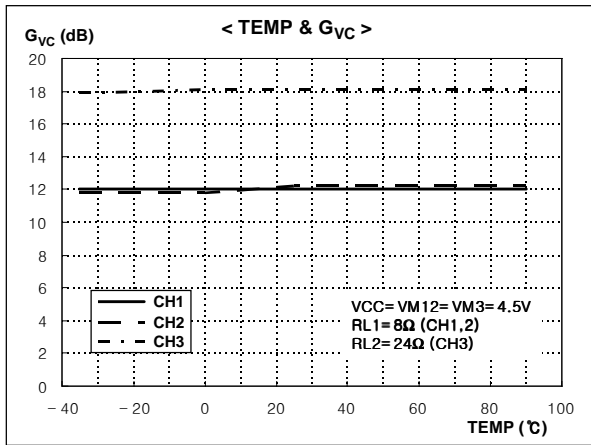
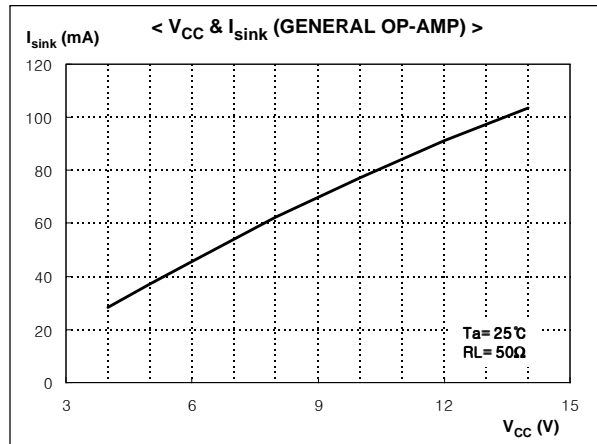
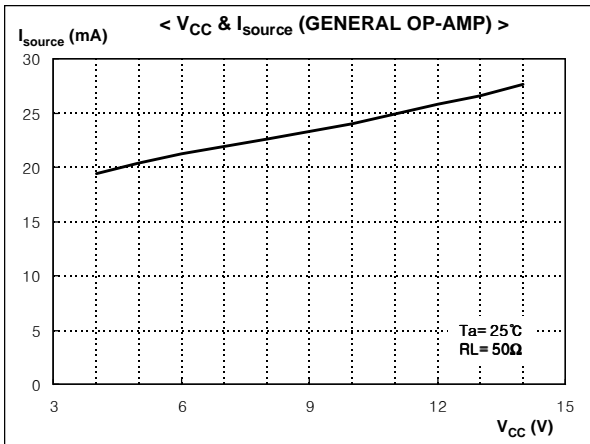
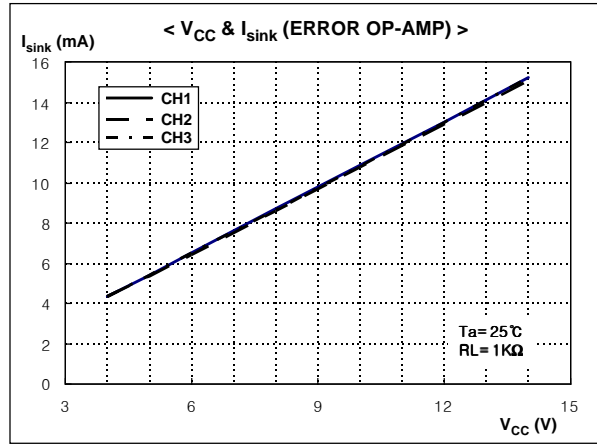
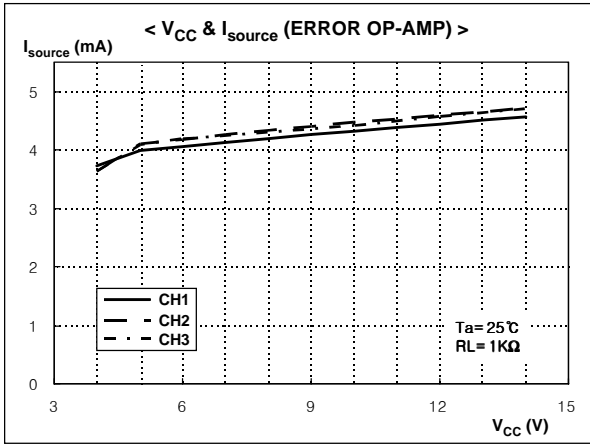
- To change the total closed loop voltage gain, Use the input opamp as an amplifier
- The output stage is the balanced transformerless (BTL) driver.
- The bias voltage Vp is expressed as ;

$$\begin{aligned}
 V_p &= (PVCC1 - VDp - V_{cesatQp}) \times \frac{62k}{60k + 62k} + V_{cesatQp} \\
 &= \frac{PVCC1 - VDp + V_{cesatQp}}{1.97} + V_{cesatQp} \quad \text{----- (1)}
 \end{aligned}$$

# Typical Performance Characteristics

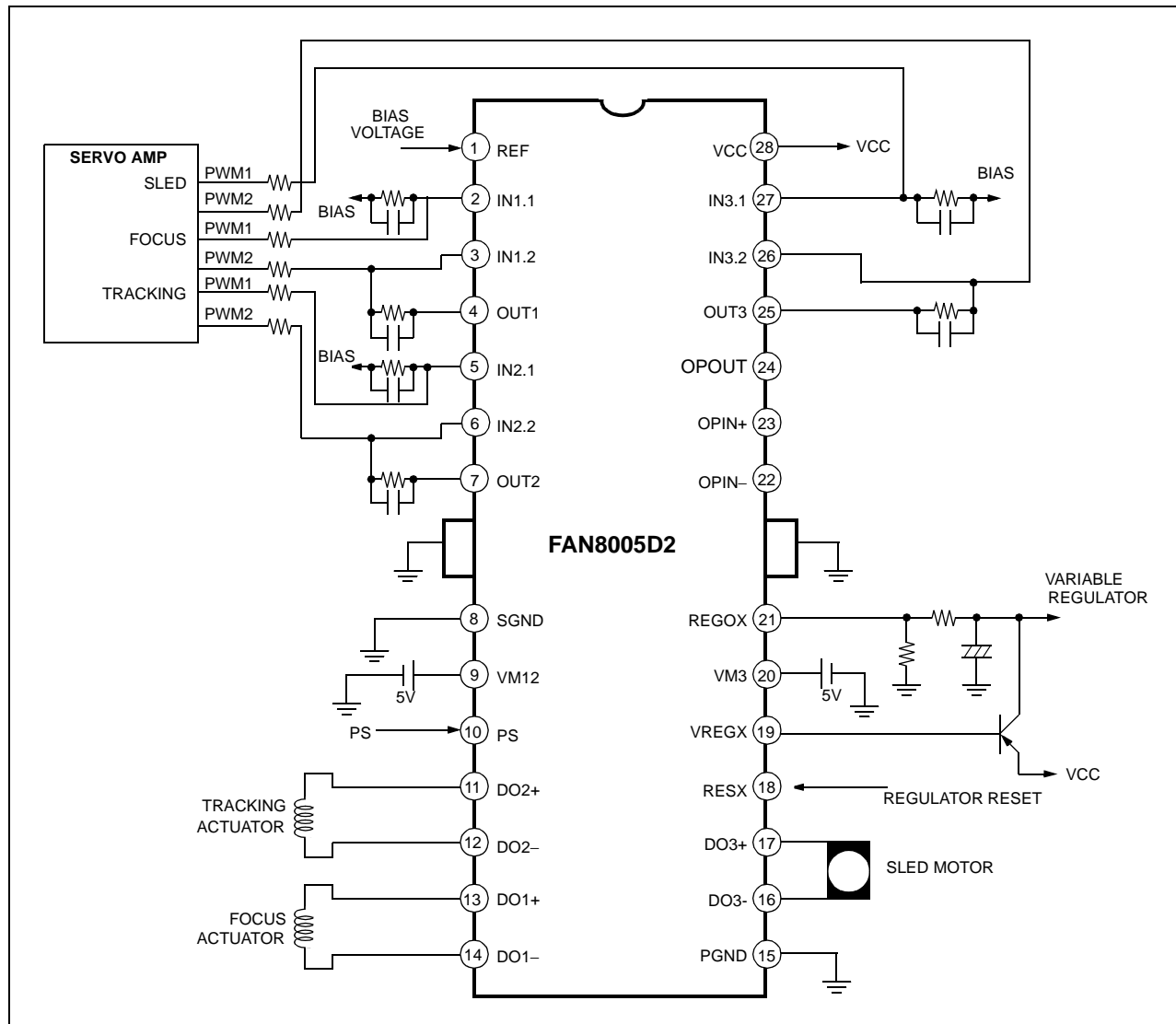


## Typical Performance Characteristics (Continued)



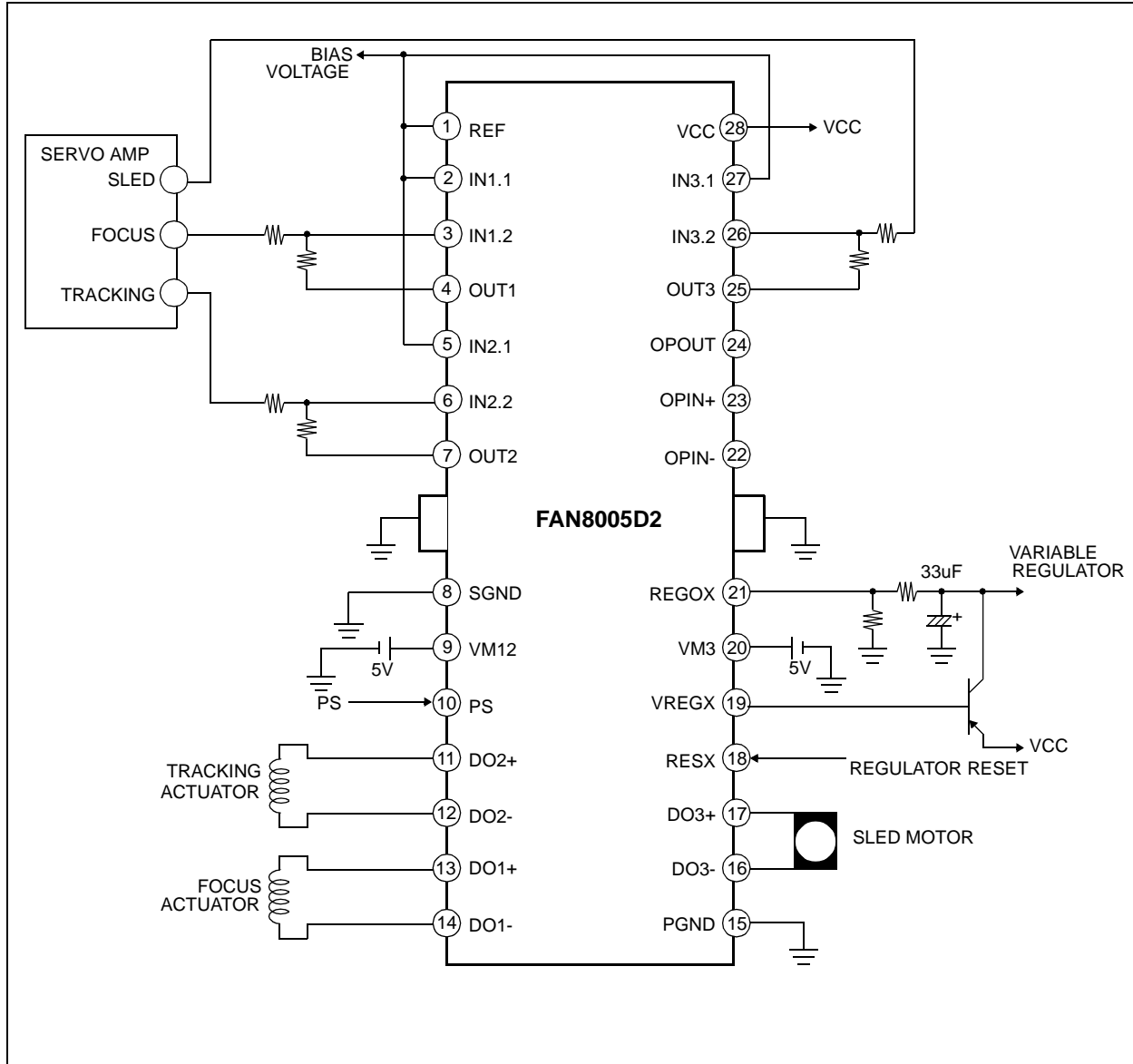
# Application Circuits 1

(Differential PWM control mode)



## Application Circuits 2

(Voltage control mode)





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