

FAN8036

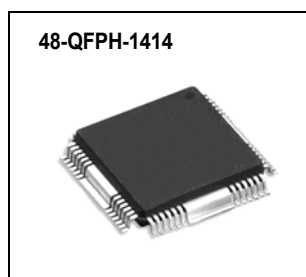
5-CH Motor Driver + 2-Regulator

Features

- 4-CH Balanced Transformerless (BTL) Driver
- 1-CH (Forward Reverse) Control DC Motor Driver
- Operating Supply Voltage (4.5V ~ 13.2V)
- Built in Thermal Shut Down Circuit (TSD)
- Built in Channel Mute Circuit
- Built in Power Save Mode Circuit
- Built in TSD Monitor Circuit
- Built in 2 Regulators
- Built in 2-OP AMPs

Description

The FAN8036 is a monolithic integrated circuit suitable for a 5-CH motor driver which drives the tracking actuator, focus actuator, sled motor, spindle motor, and tray motor of the CDP/CAR-CD/DVDP systems.



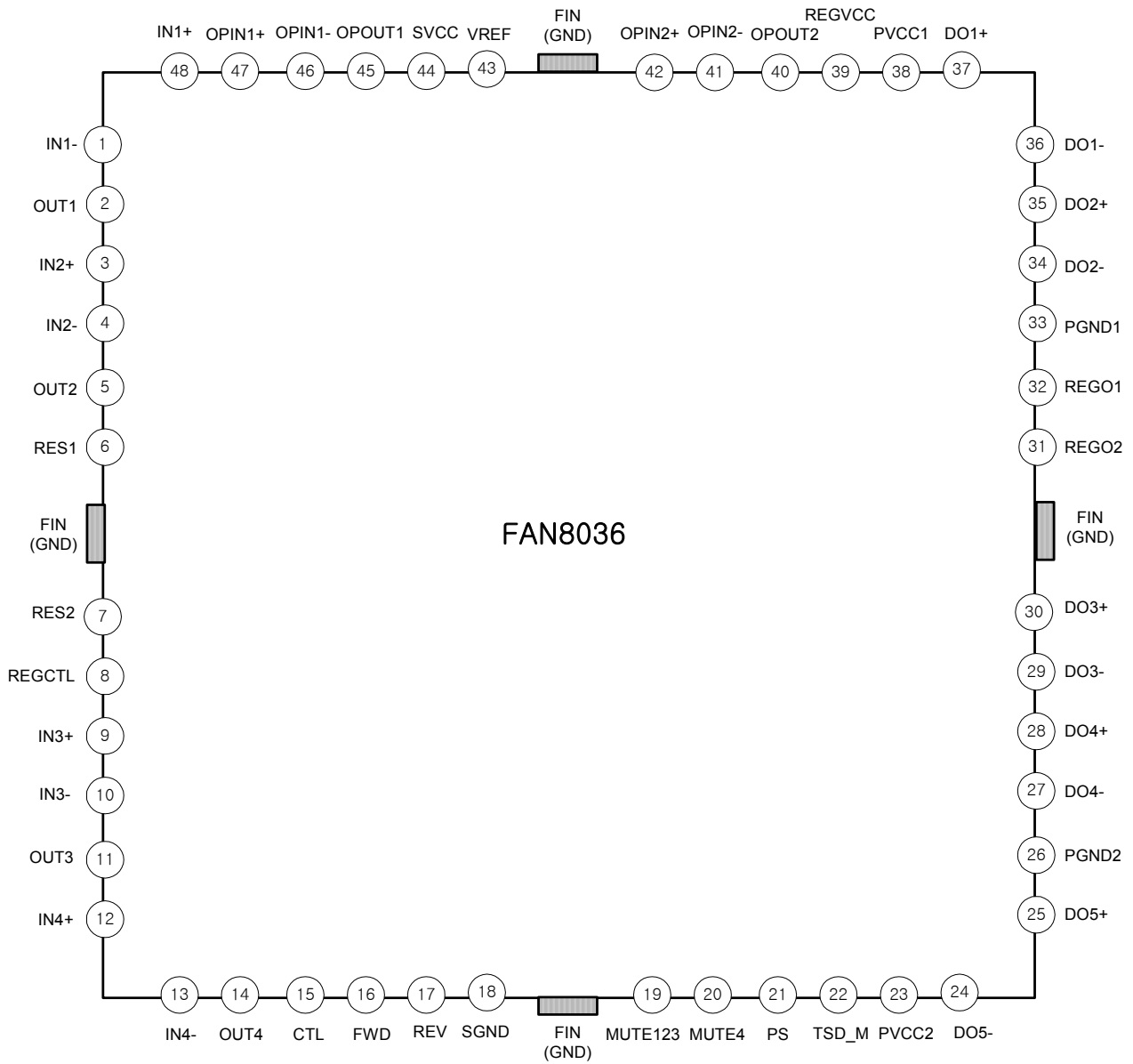
Typical Application

- Compact Disk Player
- Video Compact Disk Player
- Car Compact Disk Player
- Digital Video Disk Player

Ordering Information

Device	Package	Operating Temperature
FAN8036L	48-QFPH-1414	-35°C ~ +85°C
FAN8036_NL	48-QFPH-1414	-35°C ~ +85°C

Pin Assignments



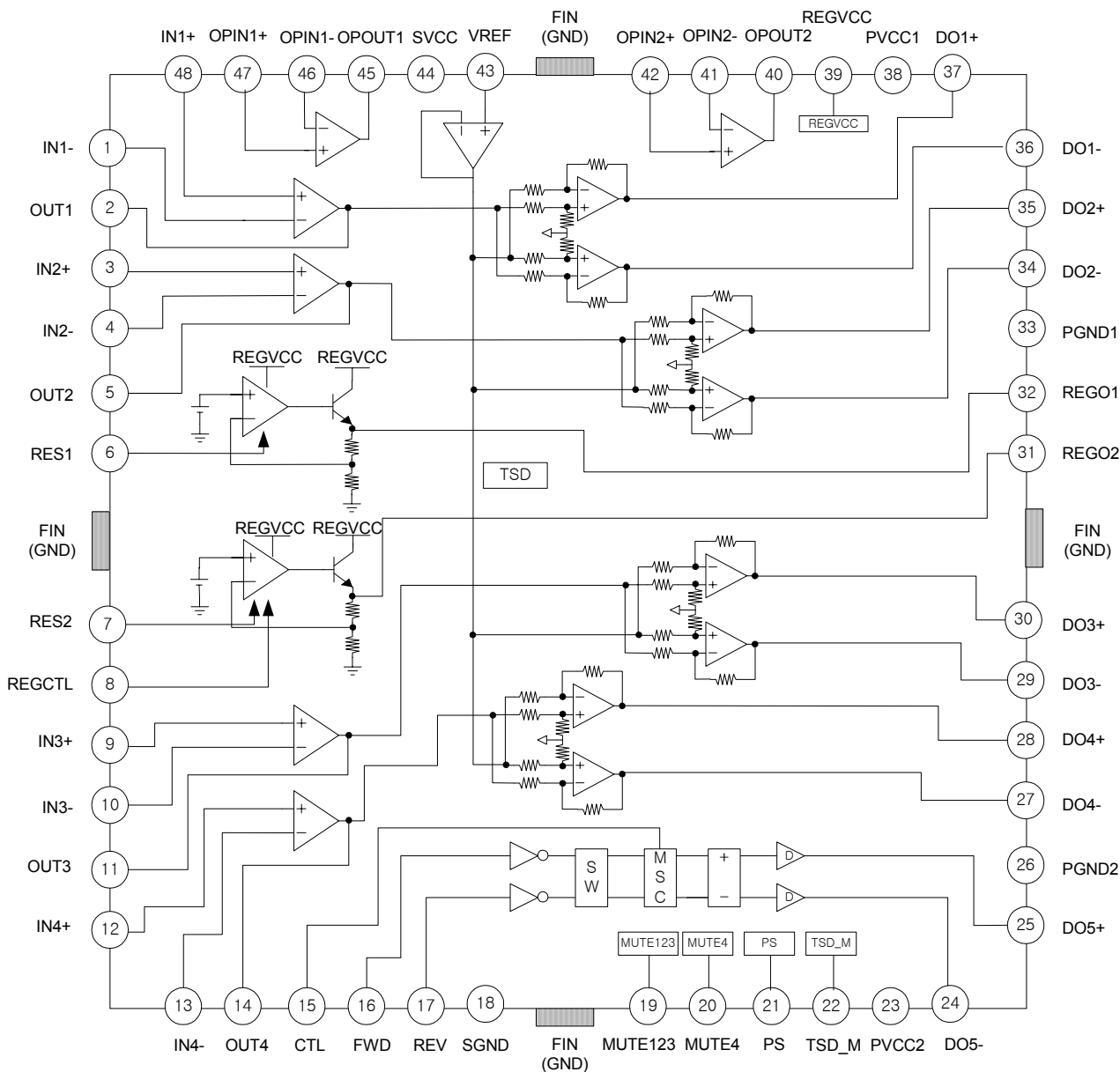
Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	IN1-	I	CH1 OP-AMP Input (-)
2	OUT1	O	CH1 OP-AMP Output
3	IN2+	I	CH2 OP-AMP Input (+)
4	IN2-	I	CH2 OP-AMP Input (-)
5	OUT2	O	CH2 OP-AMP Output
6	RES1	I	Regulator1 Reset
7	RES2	I	Regulator2 Reset
8	REGCTL	I	Regulator2 Control Voltage
9	IN3+	I	CH3 OP-AMP Input (+)
10	IN3-	I	CH3 OP-AMP Input (-)
11	OUT3	O	CH3 OP-AMP Output
12	IN4+	I	CH4 OP-AMP Input (+)
13	IN4-	I	CH4 OP-AMP Input (-)
14	OUT4	O	CH4 OP-AMP Output
15	CTL	I	CH5 Motor Speed Control
16	FWD	I	CH5 Forward Input
17	REV	I	CH5 Reverse Input
18	SGND	-	Signal Ground
19	MUTE123	I	Mute for CH1,2,3
20	MUTE4	I	Mute for CH4
21	PS	I	Power Save
22	TSD-M	O	TSD Monitor
23	PVCC2	-	Power Supply Voltage 2 (for CH3,CH4,CH5)
24	DO5-	O	CH5 Drive Output (-)
25	DO5+	O	CH5 Drive Output (+)
26	PGND2	-	Power Ground 2 (for CH3,CH4,CH5)
27	DO4-	O	CH4 Drive Output (-)
28	DO4+	O	CH4 Drive Output (+)
29	DO3-	O	CH3 Drive Output (-)
30	DO3+	O	CH3 Drive Output (+)
31	REGO2	O	Regulator2 Output
32	REGO1	O	Regulator1 Output

Pin Definitions (Continued)

Pin Number	Pin Name	I/O	Pin Function Description
33	PGND1	-	Power Ground 1 (for CH1, CH2)
34	DO2-	O	CH2 Drive Output (-)
35	DO2+	O	CH2 Drive Output (+)
36	DO1-	O	CH1 Drive Output (-)
37	DO1+	O	CH1 Drive Output (+)
38	PVCC1	-	Power Supply Voltage 1 (for CH1, CH2)
39	REGVCC	-	Regulator Supply Voltage (Regulator1,2)
40	OPOUT2	O	Normal OP-AMP2 Output
41	OPIN2-	I	Normal OP-AMP2 Input (-)
42	OPIN2+	I	Normal OP-AMP2 Input (+)
43	VREF	I	Bias Voltage Input
44	SVCC	-	Signal & OPAMPs Supply Voltage
45	OPOUT1	O	Normal OP-AMP1 Output
46	OPIN1-	I	Normal OP-AMP1 Input (-)
47	OPIN1+	I	Normal OP-AMP1 Input (+)
48	IN1+	I	CH1 OP-AMP Input (+)

Internal Block Diagram



Equivalent Circuits

Description	Pin No	Internal Circuit
<p>BTL INPUT & OP AMP1 INPUT</p>	<p>48,3,9,12,47 1,4,10,13,46</p>	
<p>OP AMP2 INPUT</p>	<p>41,42</p>	
<p>VREF</p>	<p>43</p>	
<p>BTL OP AMP OUT OP AMP1 OUT</p>	<p>2,5,11,14,45</p>	

Equivalent Circuits (Continued)

Description	Pin No	Internal Circuit
OP AMP2 OUT	40	
MUTE123,4	19,20	
CTL	15	
TSD-M	22	

Equivalent Circuits (Continued)

Description	Pin No	Internal Circuit
PS	21	
FWD,REV	16,17	
BTL CH1,2,3,4 OUTPUT	27,28,29,30, 34,35,36,37	
BTL CH5 OUTPUT	24,25	

Equivalent Circuits (Continued)

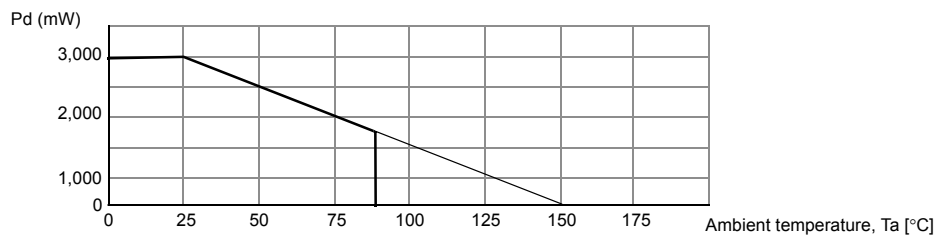
Description	Pin No	Internal Circuit
REGO1,2	31,32	
RES1,2	6,7	
REGCTL	8	

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Value	Unit
Maximum Supply Voltage	SVCCMAX	18	V
	PVCC1	18	V
	PVCC2	18	V
	REGVCC	18	V
Power Dissipation	P _D	3 ^{note}	W
Operating Temperature	TOPR	-35 ~ +85	°C
Storage Temperature	TSTG	-55 ~ +150	°C
Maximum Output Current	IOMAX	1	A

Note:

1. When mounted on the PCB of which size is 114mm × 76mm × 1.6mm.
2. Power dissipation is derated with the rate of -24mW/°C for TA ≥ 25°C.
3. Do not exceed PD and SOA.



Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Supply Voltage	SVCC	4.5	-	13.2	V
	PVCC1	SVCC	-	13.2	V
	PVCC2	SVCC	-	13.2	V
	REGVCC	7	-	13.2	V

Electrical Characteristics

(SVCC = 5V, PVCC1 = PVCC2 = 8V, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Quiescent Circuit Current	ICC	Under no-load	-	20	-	mA
Power Save On Current	IPS ^{*note1}	Under no-load	-	-	1	mA
Power Save On Voltage	VPSON	Pin21 = Variation	-	-	0.5	V
Power Save Off Voltage	VPSOFF	Pin21 = Variation	2	-	-	V
Mute123 On Voltage	VMON123	Pin19 = Variation	-	-	0.5	V
Mute123 Off Voltage	VMOFF123	Pin19 = Variation	2	-	-	V
Mute4 On Voltage	VMON4	Pin20 = Variation	-	-	0.5	V
Mute4 Off Voltage	VMOFF4	Pin20 = Variation	2	-	-	V
BTL DRIVER CIRCUIT						
Output Offset Voltage	VOO	VIN = 2.5V	-100	-	+100	mV
Maximum Output Voltage1	VOM1	RL = 10Ω, CH1,2	4.5	6.0	-	V
Maximum Output Voltage2	VOM2	RL = 18Ω, CH3,4,5	5.5	6.5	-	V
Closed-loop Voltage Gain	AVF	VIN = 0.1Vrms	16.8	18	19.2	dB
Ripple Rejection Ratio ^{*note2}	RR	VIN = 0.1Vrms, f = 120Hz	-	60	-	dB
Slew Rate ^{*note2}	SR	Square, Vout = 4Vp-p	1	2	-	V/μs
INPUT OPAMP CIRCUIT						
Input Offset Voltage1	VOF1	-	-10	-	+10	mV
Input Bias Current1	IB1	-	-	-	400	nA
High Level Output Voltage1	VOH1	-	4.4	4.7	-	V
Low Level Output Voltage1	VOL1	-	-	0.2	0.5	V
Output Sink Current1	ISINK1	RL = 50Ω	1	2	-	mA
Output Source Current1	ISOU1	RL = 50Ω	1	2	-	mA
Common Mode Input Range1 ^{*note2}	Vicm1	-	-0.3	-	4.0	V
Open Loop Voltage Gain1 ^{*note2}	GVO1	VIN = -75dB	-	80	-	dB
Ripple Rejection Ratio1 ^{*note2}	RR1	VIN = -20dB, f = 120Hz	-	65	-	dB
Common Mode Rejection Ratio1 ^{*note2}	CMRR1	VIN = -20dB	-	80	-	dB
Slew Rate1 ^{*note2}	SR1	Square, Vout = 3Vp-p	-	1.5	-	V/μs

Note :

- When the voltage at pin 39 goes below 0.5V, the power save circuit makes the main bias current sources stop operating. As a result, the whole circuits are disable. (The whole circuits mean the driver circuit, the input OP amp circuit, and the normal OP amp circuit.)
- Guaranteed field.(No EDS/Final test)

Electrical Characteristics (Continued)

(SVCC = 5V, PVCC1 = PVCC2 = 8V, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
NORMAL OP AMP CIRCUIT 1						
Input Offset Voltage 2	VOF2	-	-10	-	+10	mV
Input Bias Current 2	IB2	-	-	-	400	nA
High Level Output Voltage 2	VOH2	-	4.4	4.7	-	V
Low Level Output Voltage 2	VOL2	-	-	0.2	0.5	V
Output Sink Current 2	ISINK2	RL = 50Ω	2	4	-	mA
Output Source Current 2	ISOU2	RL = 50Ω	2	4	-	mA
Common Mode Input Range 2 ^{*note}	Vicm2	-	-0.3	-	4.0	V
Open Loop Voltage Gain 2 ^{*note}	GVO2	VIN = -75dB	-	80	-	dB
Ripple Rejection Ratio 2 ^{*note}	RR2	VIN = -20dB, f = 120Hz	-	65	-	dB
Common Mode Rejection Ratio 2 ^{*note}	CMRR2	VIN = -20dB	-	80	-	dB
Slew Rate 2 ^{*note}	SR2	Square, Vout = 3Vp-p	-	1.5	-	V/μs
NORMAL OP AMP CIRCUIT 2						
Input Offset Voltage 3	VOF3	-	-15	-	+15	mV
Input Bias Current 3	IB3	-	-	-	400	nA
High Level Output Voltage 3	VOH3	-	3	3.8	-	V
Low Level Output Voltage 3	VOL3	-	-	1.0	1.5	V
Output Sink Current 3	ISINK3	RL = 50Ω	10	-	-	mA
Output Source Current 3	ISOU3	RL = 50Ω	10	-	-	mA
Open Loop Voltage Gain 3 ^{*note}	GVO3	VIN = -75dB	-	80	-	dB
Ripple Rejection Ratio 3 ^{*note}	RR3	VIN = -20dB, f = 120Hz	-	65	-	dB
Common Mode Rejection Ratio 3 ^{*note}	CMRR3	VIN = -20dB	-	80	-	dB
Slew Rate 3 ^{*note}	SR3	Square, Vout = 3Vp-p	-	1.5	-	V/μs
TRAY DRIVE CIRCUIT						
Input High Level Voltage	VIH	-	2	-	-	V
Input Low Level Voltage	VIL	-	-	-	0.5	V
Output Voltage 1	VO1	PVCC2 = 8V, VCTL = 3V, RL = 45Ω	-	6	-	V
Output Voltage 2	VO2	PVCC2 = 8V, VCTL = 1.5V, RL = 10Ω	-	3	-	V
Output Load Regulation	ΔVRL	VCTL=3V, IL=100mA → 400mA	-	300	700	mV
Output Offset Voltage 1	VOO1	VIN = 5V, 5V	-40	-	+40	mV
Output Offset Voltage 2	VOO2	VIN = 0V, 0V	-40	-	+40	mV

Note: Guaranteed field.(No EDS/Final test)

Electrical Characteristics (Continued)

(SVCC = 5V, PVCC1 = PVCC2 = 8V, TA = 25°C, unless otherwise specified)

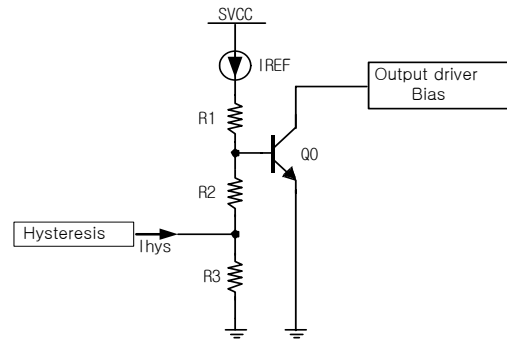
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
REGULATOR1 CIRCUIT (REGVCC=8V)						
Load regulation	ΔV_{RL1}	$I_L=0 \rightarrow \square 200\text{mA}$	-80	0	0	mV
Line regulation	ΔV_{CC1}	$I_L=200\text{mA}, V=7\text{V} \rightarrow \square 9\text{V}$	-20	0	+30	mV
Regulator output voltage 1	VREG1	$I_L=100\text{mA}$	4.75	5.0	5.25	V
Regulator reset on voltage 1	Reson1	Pin6=Variation	-	-	0.5	V
Regulator reset off voltage 1	Resoff1	Pin6=Variation	2	-	SVCC	V
Ripple Rejection 1 ^{*note}	RR1	Vin=1Vp-p, f=120Hz	-	55	-	dB
REGULATOR2 CIRCUIT (REGVCC=8V)						
Load regulation	ΔV_{RL2}	$I_L=0 \rightarrow \square 200\text{mA}$	-80	0	0	mV
Line regulation	ΔV_{CC2}	$I_L=200\text{mA}, V=7\text{V} \rightarrow \square 9\text{V}$	-20	0	+30	mV
Regulator output voltage 2 range	VREG2R	$I_L=100\text{mA}$	1.5	-	4.5	V
Regulator output voltage 2	VREG2	$I_L=100\text{mA}, V_{REGCTL}=0\text{V}$	1.482	1.56	1.638	V
		$I_L=100\text{mA}, V_{REGCTL}=1.9\text{V}$	3.135	3.3	3.465	V
Regulator reset on voltage 2	Reson2	Pin7=Variation	-	-	0.5	V
Regulator reset off voltage 2	Resoff2	Pin7=Variation	2	-	SVCC	V
Control Gain	GREGCTL	-	0.75	0.95	1.15	V/V
Ripple Rejection 2 ^{*note}	RR2	Vin=1Vp-p, f=120Hz	-	55	-	dB

Note: Guaranteed field.(No EDS/Final test)

Application Information

1. Thermal Shutdown

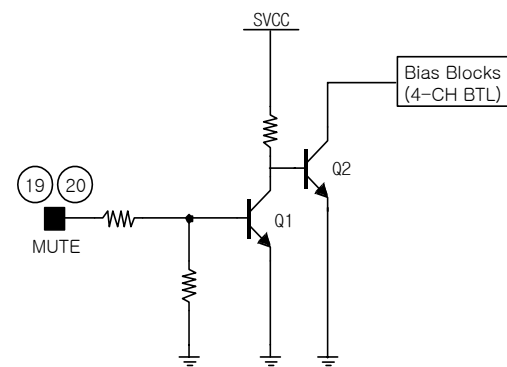
- The TSD circuit is activated at the junction temperature of 160°C and deactivated at 135°C with the hysteresis of 25°C. During the thermal shutdown, the TSD circuit keeps all the output driver off.



2. CH Mute Function

- When the mute pin is high, the TR Q1 is on and Q2 is off, so the bias circuit is enabled. When the mute pin is low (GND), the TR Q1 is off and Q2 is on, so the bias circuit is disabled.
- During the mute on state, all the circuit blocks except for the variable regulator remain off, and the low power quiescent state is established.
- Truth table is as follows;

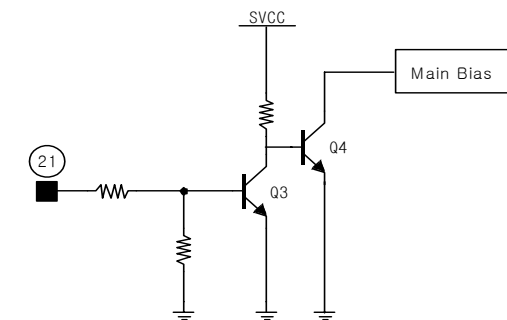
Pin 19, 20	Mute
High	Mute-Off
Low	Mute-On



3. Power Save Function

- When the pin21 is high, the TR Q3 becomes on and Q4 off, so the bias circuit is enabled. When the pin21 is low (GND), the TR Q3 becomes off and Q4 is on, so the bias circuit is disabled.
- During the power save on state, this function keeps all the circuit blocks off, and the low power quiescent state is established.
- Truth table is as follows;

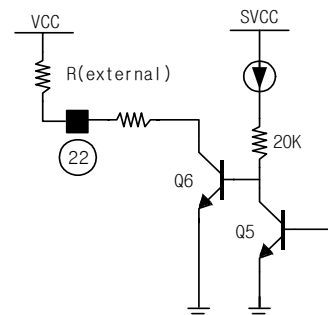
Pin21	Power Save
High	Power Save Off
Low	Power Save On



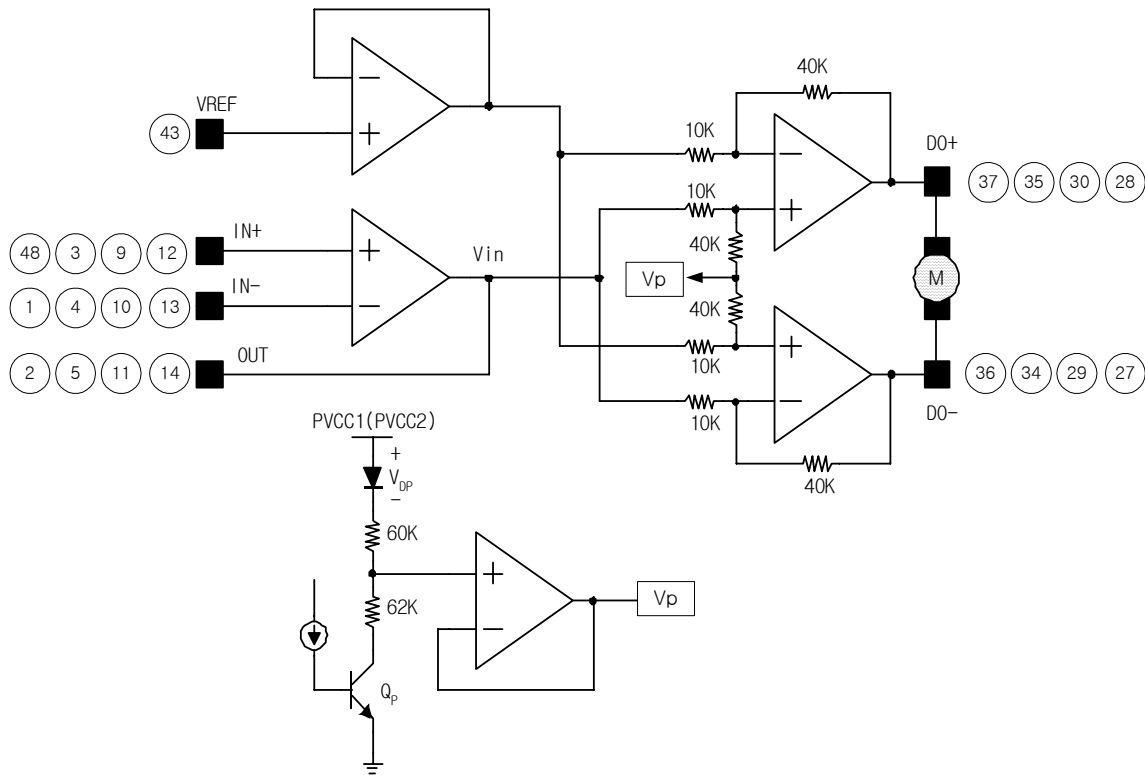
4. TDS Monitor Function

- Pin 22 is TSD monitor pin, which detects the state of the TSD block and generates the TSD-monitor signal.
- In the normal state Q5 is on, and Q6 is off. When the TSD block is activated Q5 becomes off, and thus the voltage of pin22 keeps low.
- Truth table is as follows;

TSD	Pin22
TSD Off	High
TSD On	Low



5. Focus, Tracking Actuator, Spindle, Sled Motor Drive Part



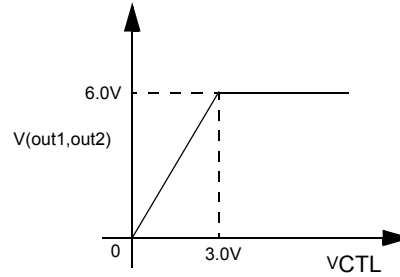
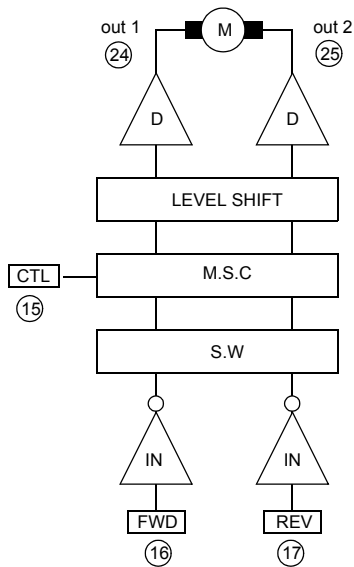
- The Vref at pin 43 is for eliminating the dc components from the input signals and can set by an external circuit.
- The voltage gain from Vin to output is as follows ;

$$\begin{aligned}
 V_{in} &= V_{ref} + \Delta V \\
 DOP &= V_D + 4\Delta V \\
 DON &= V_D - 4\Delta V \\
 V_{out} &= DOP - DON = 8\Delta V \\
 \text{Gain} &= 20\log \frac{V_{out}}{\Delta V} = 20\log 8 = 18\text{dB}
 \end{aligned}$$

- Where ΔV means just ac component.
- The total input to output voltage gain is the sum of the input OP amp network gain and 18dB.
- The output stage is the balanced transformerless (BTL) driver.
- The bias voltage V_p is expressed as ;

$$\begin{aligned}
 V_P &= (PVCC1 - V_{DP} - V_{CESAT} Q_P) \times \frac{62k}{60k + 62k} + V_{CESAT} Q_P \\
 &= \frac{PVCC1 - V_{DP} - V_{CESAT} Q_P}{1.97} + V_{CESAT} Q_P \quad \text{----- (1)}
 \end{aligned}$$

6. Tray, Changer,panel Motor Drive Part



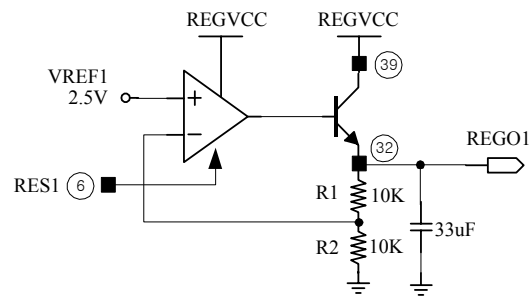
• Rotational direction control

The forward and reverse rotational direction is controlled by FWD (pin16) and REV (pin17) and the input conditions are as follows;

INPUT		OUTPUT		
FWD	REV	OUT 1	OUT 2	State
H	H	Vp	Vp	Brake
H	L	H	L	Forward
L	H	L	H	Reverse
L	L	-	-	High impedance

- Where Vp(Power reference voltage) is approximately 3.75V at PVCC2=8V according to equation (1).
- Motor speed control (When SVCC=5V, PVCC2=8V)
 - The maximum torque is obtained when the pin15(CTL) is open.
 - If the voltage of the pin15 (CTL) is 0V, the motor will not operate.
 - When the control voltage (pin15) is between 0 and 3.0V, the differential output voltage V(out1,out2) is about two times of control voltage. The output gain is 6dB.
 - When the control voltage is greater than 3.0V, the output voltage is saturated at the 6.0V because of the output swing limitation.

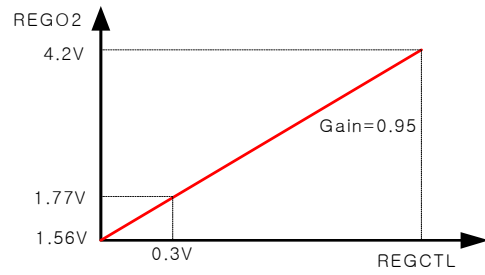
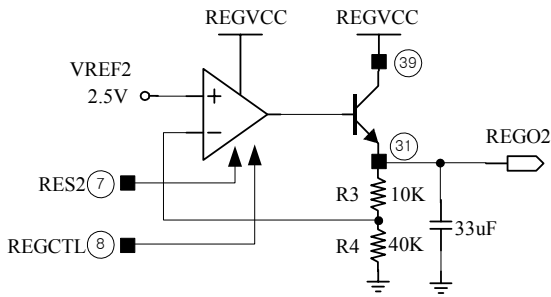
7. Regulator1 Part



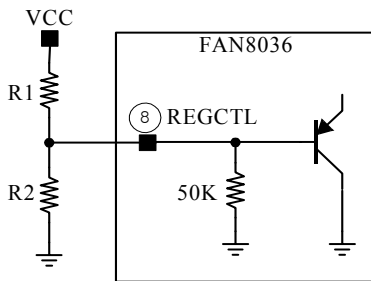
- The output voltage of the regulator1 is fixed to 5V.
- When power save on or TSD on, regulator1 is disabled.
- Truth table is as follows;

RES1(Pin6)	REGO1
HIGH	Active
LOW	Deactive

8. Regulator2 Part



- The output of the regulator2 is variable.
- The input impedance of the REGCTL pin is 50kΩ.
- The REGCTL input circuit is as follows;



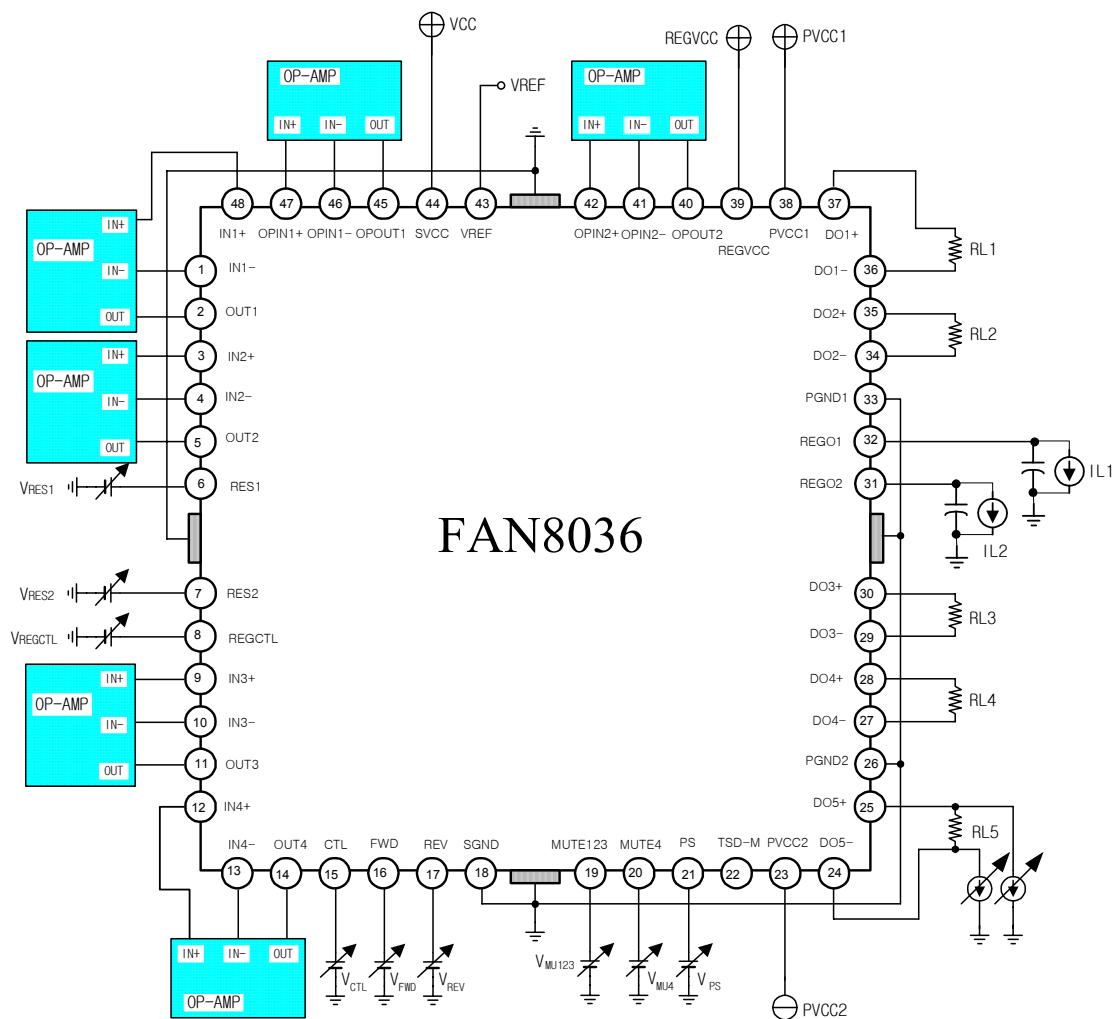
- The output voltage(VREGO2) is decided as follows;

$$VREGO2 = (1.56V + V_{REGCTL}) \times 0.95$$

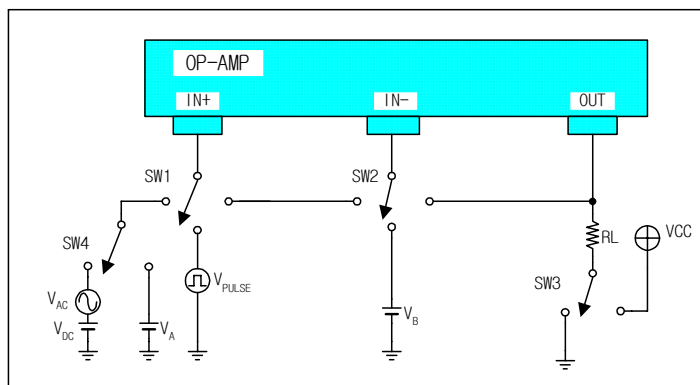
- When the REGCTL pin is connect to the ground or open, the regulator output voltage become 1.56V.
- When power save on or TSD on, regulator2 is disabled.
- Truth table is as follows;

RES2(Pin7)	REGO2
HIGH	Active
LOW	Deactive

Test Circuits

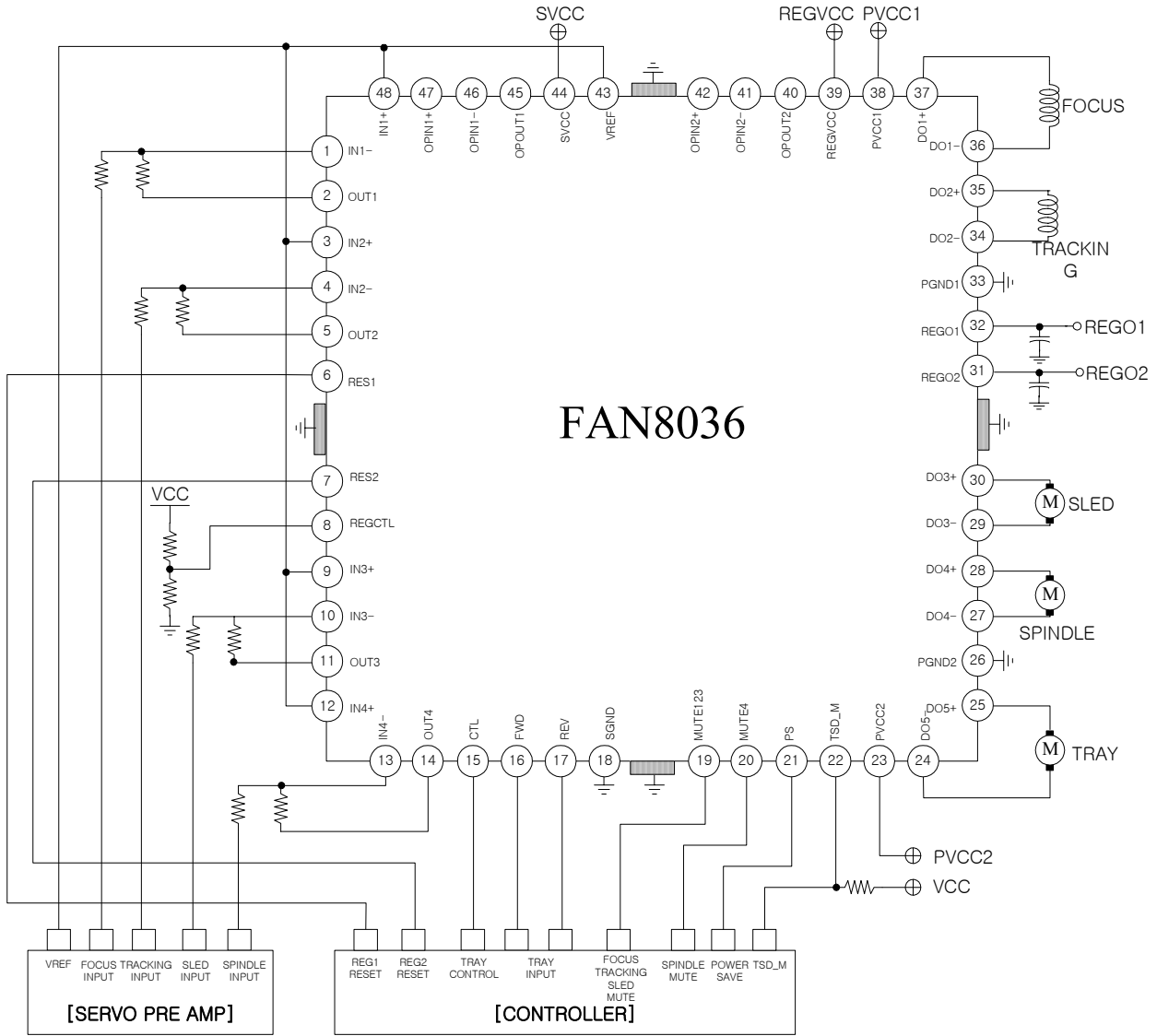


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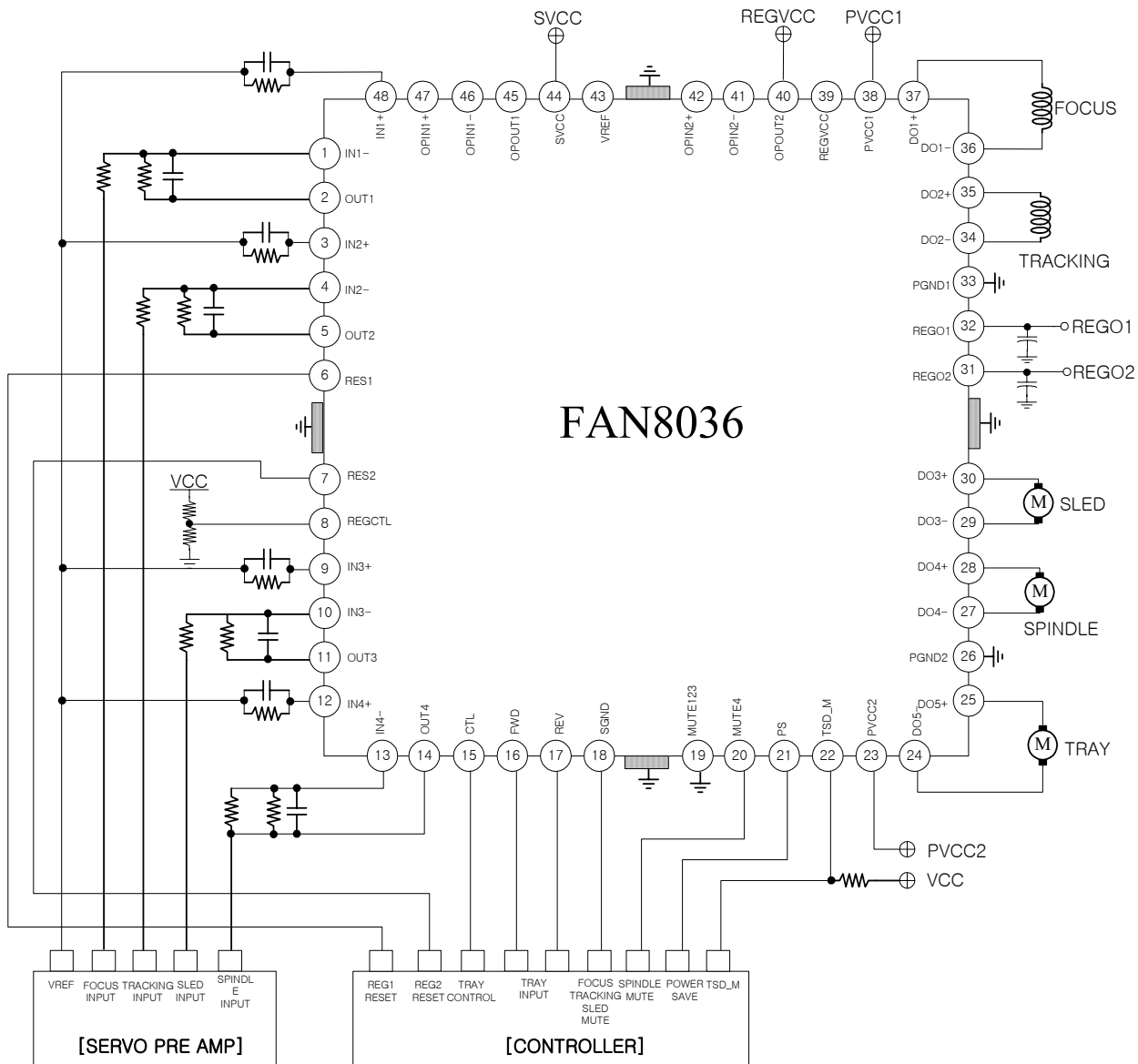
Typical Application Circuits 1

[Voltage control mode]



Typical Application Circuits 2

[Differential PWM control mode]



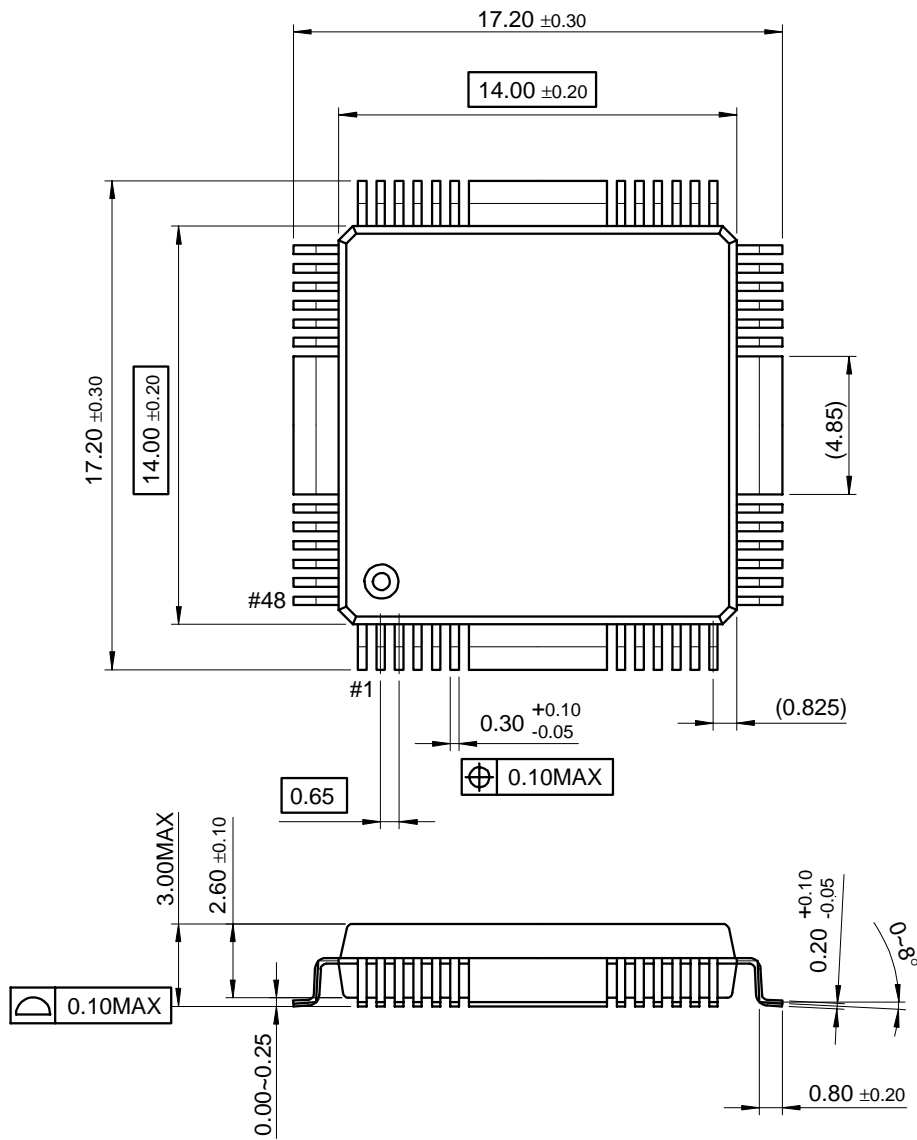
Notes:

Radiation pin is connected to the internal GND of the package.

Mechanical Dimensions

Package

48-QFPH-1414



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