QLogic Corporation

FAS368M Fast Architecture SCSI Processor

Data Sheet

Features

- Compliance with ANSI X3T10/1142D *SCSI Parallel Interconnect-2 (SPI-2)* standard
- Compliance with ANSI SCSI configured automatically (SCAM) protocol levels 1 and 2
- Sustained SCSI data transfer rates of up to:
  - 40 Mbytes/sec synchronous (Ultra and wide SCSI)
  - 14 Mbytes/sec asynchronous (wide SCSI)
- Synchronous DMA timing; DMA speed of 50 Mbytes/sec
- $\overline{\text{REQ}}$ and $\overline{\text{ACK}}$ programmable assertion and deassertion control
- Support for hot plugging
- Target and initiator block transfer sequences
- Bus idle timer
- Split-bus architecture
- Pipelined command structure
- On-chip, single-ended SCSI transceivers (48-mA drivers)
- On-chip, multimode, low voltage differential (LVD) drivers
- On-chip differential sense decoder
- Initiator and target roles
- Active negation
- 16-bit recommand counter
- Differential mode
- SCSI bus reset watchdog timer

Product Description

The FAS368M is a new addition to the QLogic fast architecture SCSI processor (FAS) chip family. The FAS368M supports internal multimode LVD and single-ended (SE) transceivers, which allow the chip to support LVD and SE operations in initiator and target roles.

The FAS368M is a single-chip controller for use in host and peripheral applications. To ensure firmware compatibility and provide FAS366U customers a seamless upgrade path, the FAS368M uses the same SCSI core, foundry, and process as the FAS366U. Note that the FAS368M package size, pin out, and transceivers differ from the FAS366U. The FAS368M block diagram is shown in figure 1.

The FAS368M implements QLogic's new SCSI target and initiator block transfer sequences. The block sequences reduce firmware overhead and are composed of the following new commands: Target Block Sequence (including the bus idle timer), Initiator Block Sequence, Load/Unload Block Registers sequences, Abort Block Sequence, and Disconnect Abort Block Sequence.

The FAS368M supports both single-ended and differential mode SCSI operations and operates in initiator and target roles. The FAS368M has been optimized for interaction with a DMA controller and the controlling microprocessor.

The versatile split-bus architecture supports various microprocessor and DMA bus configurations. A separate 8-bit microprocessor bus (PAD) provides access to all internal registers, and a 16-bit DMA bus (DB) provides a path for DMA transfers through the FIFO. Each bus is protected by a parity bit (byte-wide parity) to improve data integrity. During data transfer, the microprocessor has instant access to status and has the ability to execute commands.

SCAM Implementation

The FAS368M supports levels 1 and 2 of the SCAM protocol. Refer to the latest revision of X3T10/855D, Annex B. The SCAM protocol requires direct access and control over the SCSI data bus and several of the SCSI phase and control signals. The majority of the SCAM protocol can be implemented in firmware at microprocessor speeds. The following SCAM features are supported in the hardware:

- Arbitration without an ID
- Slow response to selection with an unconfirmed ID
- Detection of and response to SCAM selection

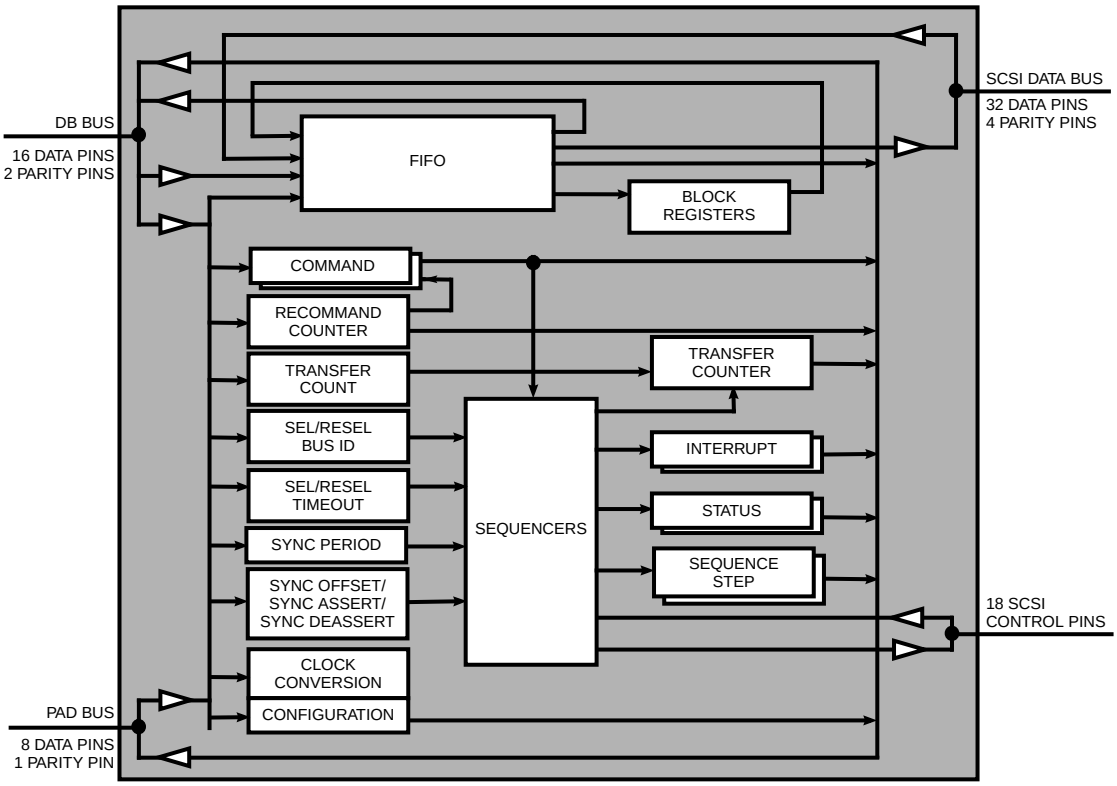

Figure 1. FAS368MBlock Diagram

Fast DMA Protocol

Fast DMA protocol is required for supporting the full bandwidth of Ultra, wide SCSI.

The DREQ signal initiates DMA transfers and runs asynchronous to the user's clock. For read operations, $\overline{\text{DACK}}$ acts as a chip select to enable the FAS368M drivers onto the DMA bus. The chip select role of $\overline{\text{DACK}}$ helps support the burst timing of fast DMA mode. $\overline{\text{DACK}}$ selects the FAS368M after DREQ is asserted and is removed either after DREQ is deasserted or when the DMA transfer is paused.

$\overline{\text{DBRD}}$ requests data from the FAS368M and $\overline{\text{DBWR}}$ validates data sent to the FAS368M. Data is valid around the rising (trailing) edge of $\overline{\text{DBRD}}$ or $\overline{\text{DBWR}}$.

DMA transfers are terminated by deasserting DREQ. Deassertion of DREQ is triggered by the leading edge of $\overline{\text{DBRD}}$ or $\overline{\text{DBWR}}$ (see timing parameter t1 in figures 2 and 3) under any of the following conditions:

- To prevent FIFO overrun conditions
- To prevent FIFO underrun conditions
- When the required amount of data has been transferred

When DREQ is deasserted, the FAS368M ignores $\overline{\text{DBRD}}$ and $\overline{\text{DBWR}}$. Data transfers do not take place unless DREQ is asserted.

The FAS368M does not generate parity on the incoming DMA bus. Correct parity must always be supplied with the data.

The DMA interface signals are listed in table 1. DMA timing is listed in table 2 and illustrated in figures 2 and 3.

Table 1. DMA Interface Signals

Pin	Type	Active Level	Description
DREQ	O	High	The FAS368M DMA request line begins and ends DMA cycles.
$\overline{\text{DACK}}$	I	Low	The acknowledge is used as a chip select to activate FAS368M drivers and to acknowledge acceptance of DREQ.
$\overline{\text{DBRD}}$	I	Rising edge	The trailing edge accepts data from the FAS368M for DMA read operations.

Table 1. DMA Interface Signals (Continued)

Pin	Type	Active Level	Description
$\overline{DBWR}$	I	Rising edge	The trailing edge strobes data into the FAS368M FIFO on DMA write operations.
DB15-0	I/O	N/A	This is the DMA data bus.

Table 2. DMA Timing

Symbol	Description	Min. (ns)	Max. (ns)
t1	$\overline{DBRD}$/$\overline{DBWR}$ low to DREQ low[a]		12
t2	$\overline{DACK}$ high to DREQ high	2	
t3	$\overline{DACK}$ high to $\overline{DACK}$ low	40	
tR1	$\overline{DACK}$ low to $\overline{DBRD}$ low	tR5	
tR2	$\overline{DBRD}$ assertion pulse width	15	
tR3	$\overline{DBRD}$ deassertion pulse width	15	
tR4	$\overline{DBRD}$ high to $\overline{DACK}$ high[b]	tR3	
tR5	$\overline{DBRD}$ low to $\overline{DBRD}$ low cycle	40	
tR6	$\overline{DACK}$ low to DB15-0 read on[c]	2	

Table 2. DMA Timing (Continued)

Symbol	Description	Min. (ns)	Max. (ns)
tR7	$\overline{DACK}$ high to DB15-0 read off[c]		15
tR8	$\overline{DBRD}$ low to DB15-0 read valid[c]		15
tR9	$\overline{DBRD}$ low to DB15-0 read invalid[c]	0	
tW1	$\overline{DACK}$ low to $\overline{DBWR}$ low	tW5	
tW2	$\overline{DBWR}$ assertion pulse width	15	
tW3	$\overline{DBWR}$ deassertion pulse width	15	
tW4	$\overline{DBWR}$ high to $\overline{DACK}$ high[d]	tW3	
tW5	$\overline{DBWR}$ low to $\overline{DBWR}$ low cycle	40	
tW6	DB15-0 write setup to $\overline{DBWR}$ high	10	
tW7	DB15-0 write hold from $\overline{DBWR}$ high	5	

Table Notes

[a] DREQ loading is 30 pf.

[b] $\overline{DBRD}$ low to $\overline{DACK}$ high ≥ tR5

[c] Data loading is 50 pf.

[d] $\overline{DBWR}$ low to $\overline{DACK}$ high ≥ tW5

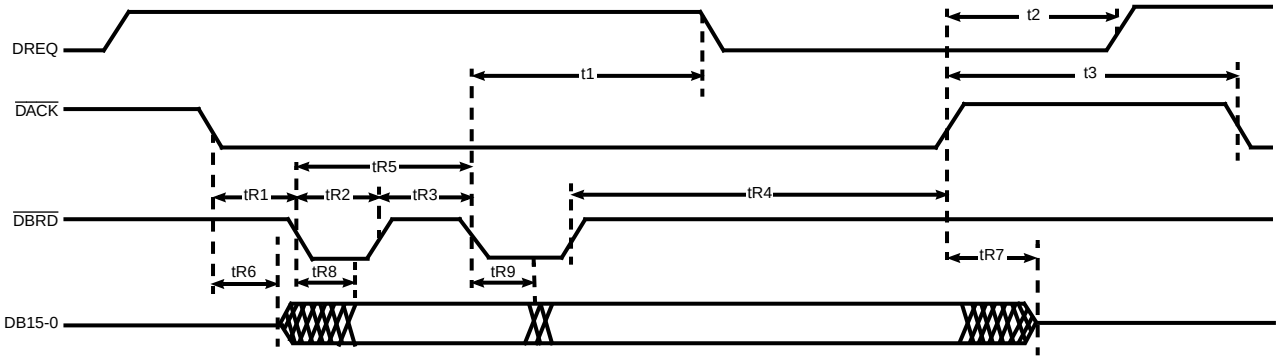

Figure 2. DMA Read Cycle

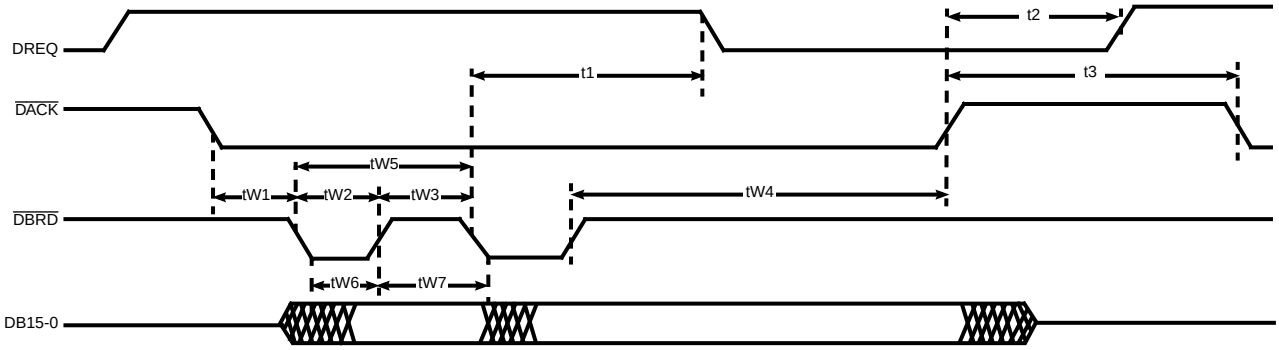

Figure 3. DMA Write Cycle

Interfaces

The FAS368M interfaces consist of the microprocessor bus and the SCSI bus. Pins that support these interfaces and other chip operations are shown in figure 4.

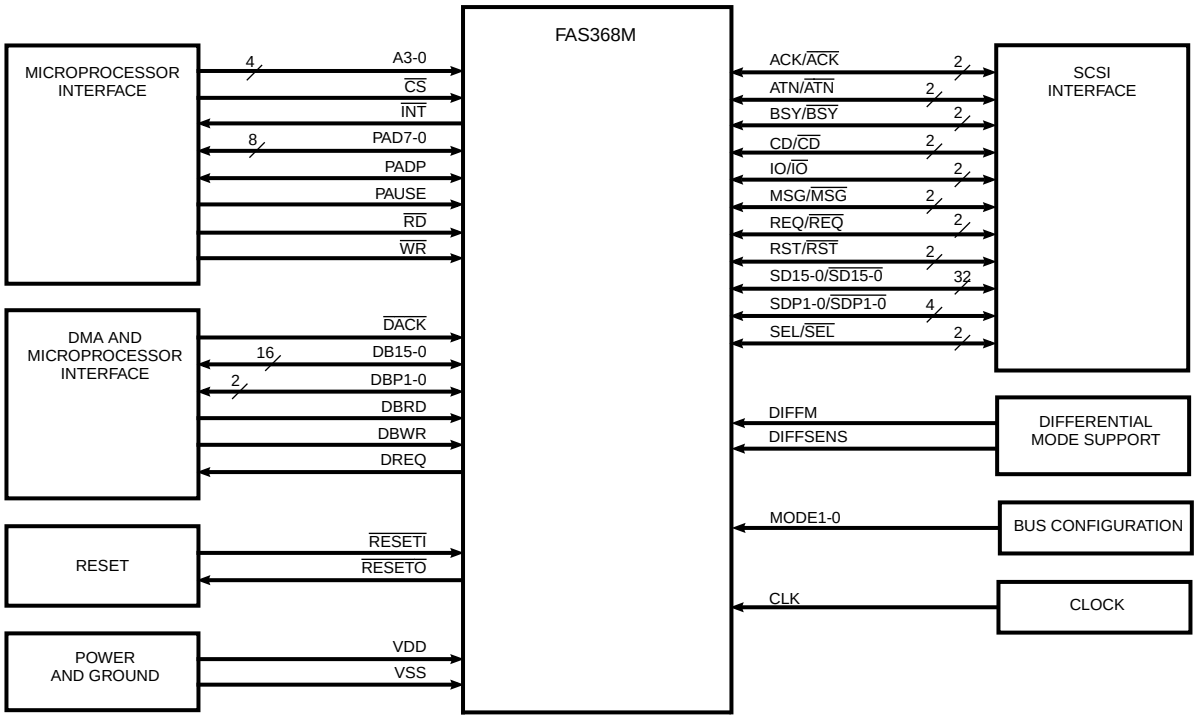

Figure 4. FAS368M Functional Signal Grouping

Packaging

The FAS368M is available in a 144-pin thin quad flat pack (TQFP). The mechanical drawings are illustrated in figure 3.

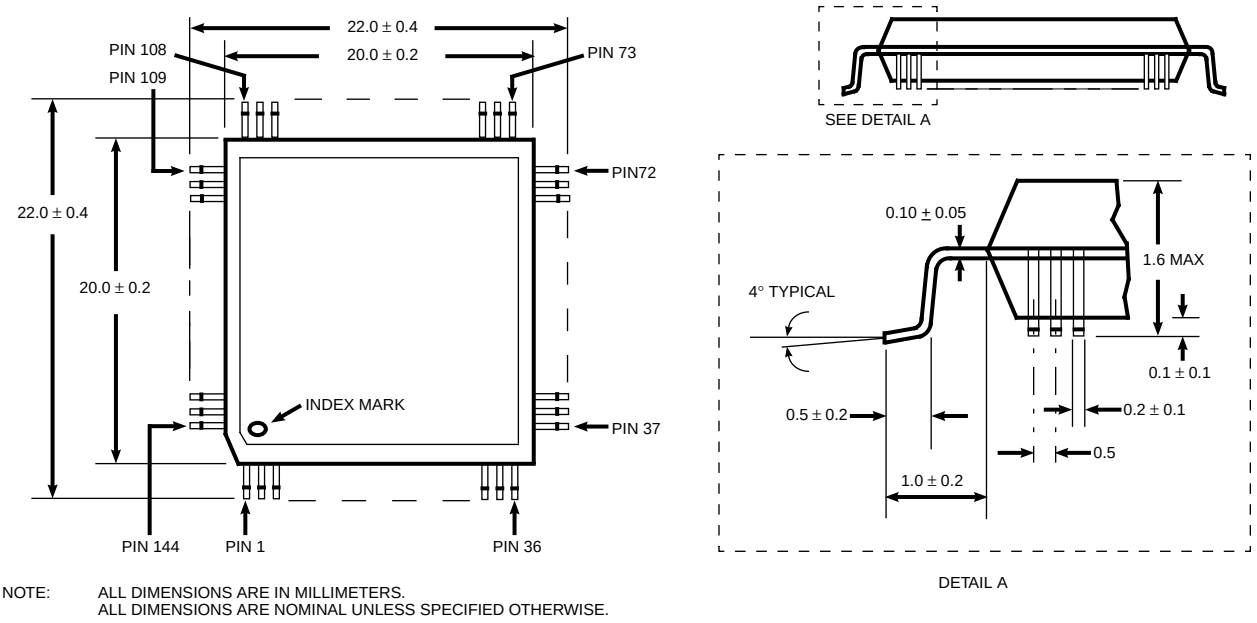

Figure 3. FAS368M Mechanical Drawings

Electrical Characteristics

Table 4. Operating Conditions

Symbol	Description	Minimum	Maximum	Unit
VDD	Supply voltage (5 volt)	4.75	5.25	V
VDD	Supply voltage (3 volt)	3.3 V - 5%	3.3 V + 5%	V
IDD[a]	Supply current (static IDD)		1	mA
IDD[b]	Supply current (dynamic IDD)		TBD	mA
TA	Ambient temperature	0	70	^{o}C

Table Notes

Conditions that not within the operating conditions but within the absolute maximum stress ratings may cause the chip to malfunction.

Capacitance in and out (CIN, COUT) is 15 pF maximum for all pins.

[a]Static IDD is measured with no clocks running and all inputs forced to VDD, all outputs unloaded, all bidirectional pins configured as inputs, and LVD mode disabled.

[b]Dynamic IDD is dependent on the application.