

DATA SHEET

FBL22040

3.3V BTL8-bit TTL to BTL transceiver

Product specification
IC23 Data Handbook

1998 Dec 07

3.3V BTL 8-bit TTL to BTL transceiver

FBL22040

FEATURES

- Resistor version of FB2040
- 8-bit BTL transceivers
- Separate I/O on TTL A-port
- Inverting
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω.
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flat Pack
- Same pin and function as FBL2040 except for a 30Ω series termination resistor
- The A outputs include a series resistor of 30Ω making external terminating resistors unnecessary

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | | TYPICAL | UNIT |
|------------------------|-----------------------------------|-----------------------------|------------|------|
| t_{PLH} t_{PHL} | Propagation delay AIn to Bn | | 4.4 3.1 | ns |
| t_{PLH} t_{PHL} | Propagation delay Bn to AOn | | 3.4 3.2 | ns |
| C_{OB} | Output capacitance (B0 – B7 only) | | 4 | pF |
| I_{OL} | Output current (B0 – B7 only) | | 100 | mA |
| I_{CC} | Supply current | Standby | 4 | mA |
| | | AIn to Bn (outputs Low) | 8 | |
| | | Bn to AOn (outputs Low) | 18 | |
| | | AIn to Bn (outputs High) | 13 | |
| | | Bn to AOn (outputs High) | 16 | |

ORDERING INFORMATION

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 3V \pm 10\%$; $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$ | DRAWING NUMBER |
|-------------------------------------|---|----------------|
| 52-pin Plastic Quad Flat Pack (QFP) | FBL22040BB | SOT379-1 |

ABSOLUTE MAXIMUM RATINGS

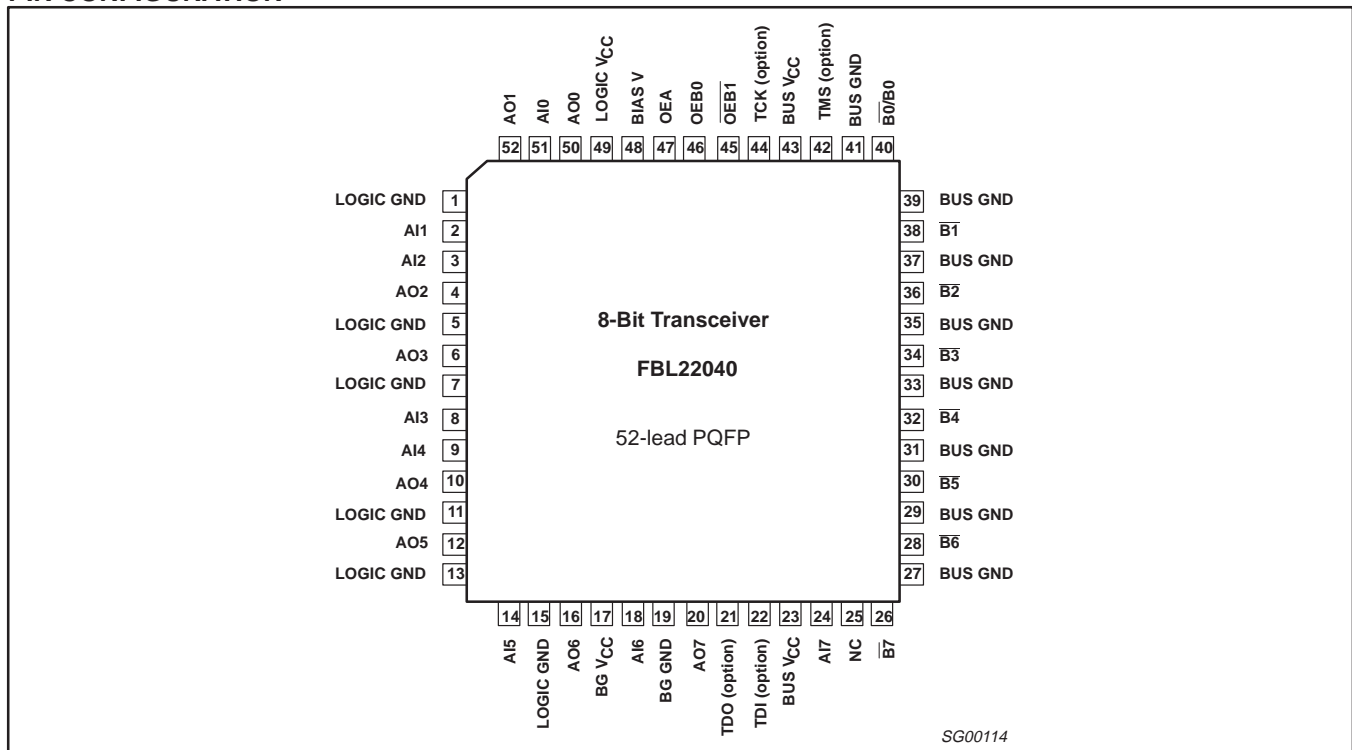
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

| SYMBOL | PARAMETER | | RATING | UNIT |
|-----------|--|--------------------------|--------------|-------------|
| V_{CC} | Supply voltage | | -0.5 to +4.6 | V |
| V_{IN} | Input voltage | A10 – A17, OE0, OE1, OEA | -0.5 to +7.0 | V |
| | | B0 – B7 | -0.5 to +3.5 | |
| I_{IN} | Input current | | -18 to +5.0 | mA |
| V_{OUT} | Voltage applied to output in High output state | | -0.5 to +7.0 | V |
| I_{OUT} | Current applied to output in Low output state | A0 – A7 | 24, -24 | mA |
| | | B0 – B7 | 200 | |
| T_{amb} | Operating free-air temperature range | | -40 to +85 | $^{\circ}C$ |
| T_{STG} | Storage temperature | | -65 to +150 | $^{\circ}C$ |

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FBL22040

PIN CONFIGURATION



DESCRIPTION

The FBL22040 is an 8-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FBL22040 is an inverting transceiver.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1Vp-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

The A-port operates at TTL levels with separate I/O. The 3-state A-port drivers are enabled when OEA goes High after an extra 6ns delay which is built in to provide a break-before-make function. When OEA goes Low, A-port drivers become High impedance without any extra delay. During power on/off cycles, the A-port drivers are held in a High impedance state when V_{CC} is below 1.3V.

The B-port has two output enables, OEB0 and $\overline{\text{OEB1}}$. When OEB0 is High and $\overline{\text{OEB1}}$ is Low the output is enabled. When OEB0 is Low

or if $\overline{\text{OEB1}}$ is High, the B-port is inactive and is at the level of the backplane signal.

To support live insertion, OEB0 is held Low during power on/off cycles to insure glitch free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 3.3V level while V_{CC} is Low. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated in the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble-shoot.

The LOGIC V_{CC} and BUS V_{CC} pins are also isolated internally to minimize noise and may be externally decoupled separately or simply tied together.

JTAG boundary scan pins are provided with signals TMS, TCK, TDI and TDO. TMS and TCK are no-connects (no bond wires) and TDI and TDO are shorted together internally. Boundary scan functionality is not implemented at this time.

3.3V BTL 8-bit TTL to BTL transceiver

FBL22040

PIN DESCRIPTION

| SYMBOL | PIN NUMBER | TYPE | NAME AND FUNCTION |
|-----------------------------------|-----------------------------------|--------|--|
| AI0 – AI7 | 51, 2, 3, 8, 9, 14, 18, 24 | Input | Data inputs (TTL) |
| AO0 – AO7 | 50, 52, 4, 6, 10, 12, 16, 20 | Output | 3-state outputs (TTL) |
| $\overline{B}0$ – $\overline{B}7$ | 40, 38, 36, 34, 32, 30, 28, 26 | I/O | Data inputs/Open Collector outputs. High current drive (BTL) |
| OEB0 | 46 | Input | Enables the B outputs when High |
| $\overline{OEB}1$ | 45 | Input | Enables the B outputs when Low |
| OEA | 47 | Input | Enables the A outputs when High |
| BUS GND | 41, 39, 37, 35, 33, 31, 29, 27 | GND | Bus ground (0V) |
| LOGIC GND | 1, 5, 7, 11, 13, 15 | GND | Logic ground (0V) |
| BUS V _{CC} | 23, 43 | Power | Positive supply voltage |
| LOGIC V _{CC} | 49 | Power | Positive supply voltage |
| BG V _{CC} | 17 | Power | Band Gap threshold voltage reference |
| BG GND | 19 | GND | Band Gap threshold voltage reference ground |
| BIAS V | 48 | Power | Live insertion pre-bias pin |
| TMS | 42 | Input | Test Mode Select (optional, if not implemented then no-connect) |
| TCK | 44 | Input | Test Clock (optional, if not implemented then no-connect) |
| TDI | 22 | Input | Test Data In (optional, if not implemented then shorted to TDO) |
| TDO | 21 | Output | Test Data Out (optional, if not implemented then shorted to TDI) |
| NC | 25 | NC | No Connect |

FUNCTION TABLE

| MODE | INPUTS | | | | | OUTPUTS | |
|---------------------------------|--------|-------------------|------|-------------------|-----|---------|-------------------|
| | AIn | $\overline{B}n^*$ | OEB0 | $\overline{OEB}1$ | OEA | AOn | $\overline{B}n^*$ |
| AIn to $\overline{B}n$ | L | — | H | L | L | Z | H** |
| | H | — | H | L | L | Z | L |
| | L | — | H | L | H | L | H** |
| | H | — | H | L | H | H | L |
| Disable $\overline{B}n$ outputs | X | X | L | X | X | X | H** |
| | X | X | X | H | X | X | H** |
| $\overline{B}n$ to AOn | X | L | L | X | H | H | Input |
| | X | H | X | H | H | L | Input |
| | X | L | X | H | H | H | Input |
| | X | H | L | X | H | L | Input |
| Disable AOn outputs | — | X | X | X | L | Z | X |

H** = Goes to level of pull-up voltage

B* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

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FBL22040

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | | LIMITS | | | UNIT |
|-----------|--------------------------------------|--|--------|------|------|------|
| | | | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | | 3.0 | 3.3 | 3.6 | V |
| V_{IH} | High-level input voltage | Except $\overline{B0}$ – $\overline{B7}$ | 2.0 | | | V |
| | | $B0$ – $B7$ | 1.62 | 1.55 | | |
| V_{IL} | Low-level input voltage | Except $\overline{B0}$ – $\overline{B7}$ | | | 0.8 | V |
| | | $B0$ – $B7$ | | | 1.47 | |
| I_{IK} | Input clamp current | | | | -18 | mA |
| I_{OH} | High-level output current | $AO0$ – $AO7$ | | | -12 | mA |
| I_{OL} | Low-level output current | $AO0$ – $AO7$ | | | +12 | mA |
| | | $\overline{B0}$ – $\overline{B7}$ | | | 100 | |
| C_{OB} | Output capacitance on B port | | | 6 | 7 | pF |
| T_{amb} | Operating free-air temperature range | | -40 | | +85 | °C |

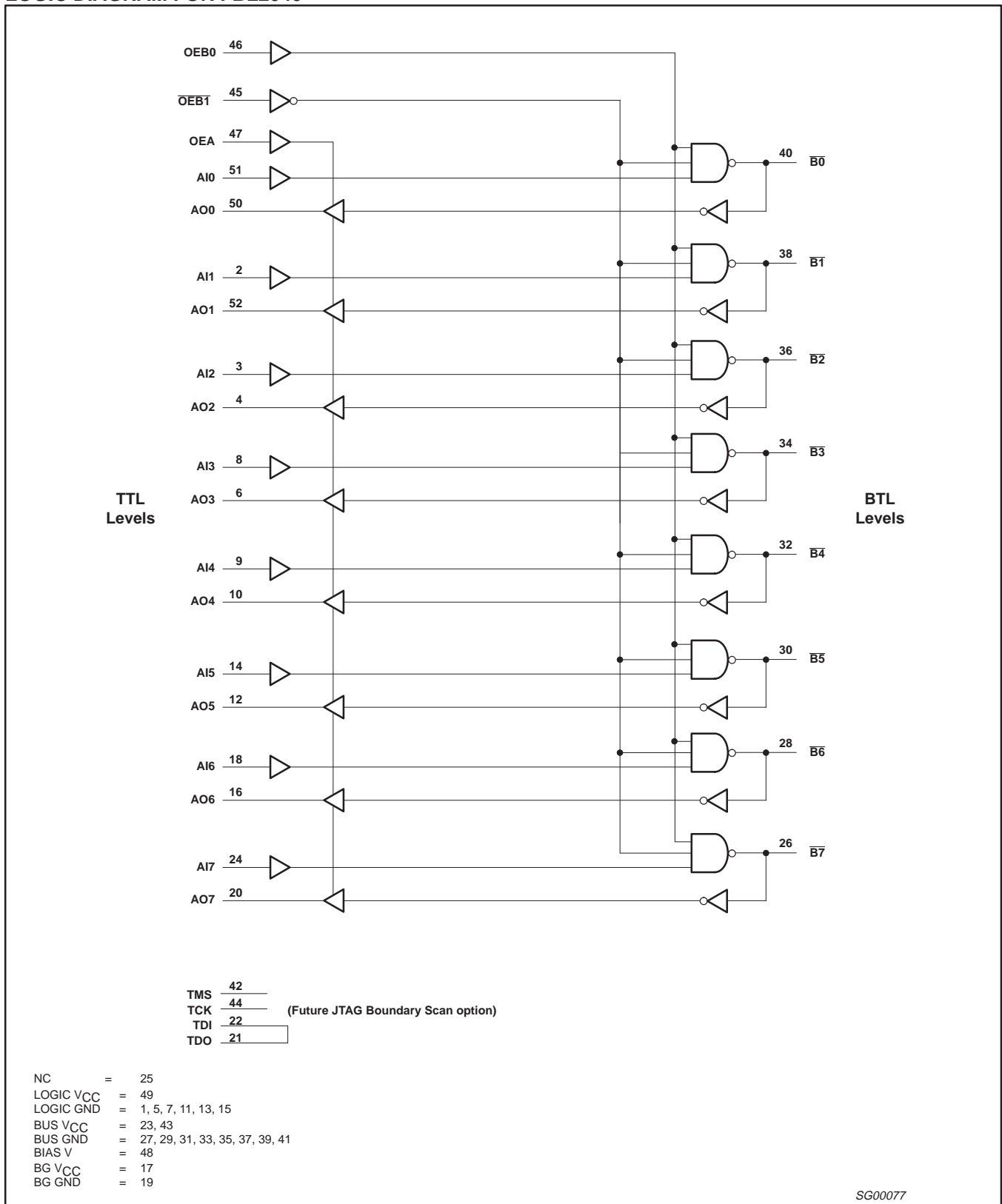
LIVE INSERTION SPECIFICATIONS

| SYMBOL | PARAMETER | | LIMITS | | | UNIT |
|-----------------|---|--|--------|------|-----|------|
| | | | MIN | TYP | MAX | |
| V_{BIASV} | Bias pin voltage | Voltage difference between the Bias voltage and V_{CC} after the PCB is plugged in. | – | – | 0.5 | V |
| I_{BIASV} | Bias pin (I_{BIASV}) input DC current | $V_{CC} = 0$ V, Bias $V = 3.6$ V | | | 1.2 | mA |
| | | $V_{CC} = 3.3$ V, Bias $V = 3.6$ V | | | 10 | μA |
| V_{Bn} | Bus voltage during prebias | $\overline{B0}$ – $\overline{B8} = 0$ V, Bias $V = 3.3$ V | 1.62 | | 2.1 | V |
| I_{LM} | Fall current during prebias | $\overline{B0}$ – $\overline{B8} = 2$ V, Bias $V = 1.3$ to 2.5 V | | | 1 | μA |
| I_{HM} | Rise current during prebias | $\overline{B0}$ – $\overline{B8} = 1$ V, Bias $V = 3$ to 3.6 V | -1 | | | μA |
| I_{Bn}^{PEAK} | Peak bus current during insertion | $V_{CC} = 0$ to 3.3 V, $\overline{B0}$ – $\overline{B8} = 0$ to 2.0 V, Bias $V = 2.7$ to 3.6 V, $OEB0 = 0.8$ V, $t_r = 2$ ns | | | 10 | mA |
| I_{OLOFF} | Power up current | $V_{CC} = 0$ to 3.3 V, $OEB0 = 0.8$ V | | | 100 | μA |
| | | $V_{CC} = 0$ to 1.2 V, $OEB0 = 0$ to 5 V | | | 100 | |
| t_{GR} | Input glitch rejection | $V_{CC} = 3.3$ V | 1.0 | 1.35 | | ns |

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FBL22040

LOGIC DIAGRAM FOR FBL22040



3.3V BTL 8-bit TTL to BTL transceiver

FBL22040

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

| SYMBOL | PARAMETER | | TEST CONDITIONS ¹ | LIMITS | | | UNIT | |
|------------------------|---------------------------|---------------------------------|--|------------------|------------------|-----------|---------------|----|
| | | | | MIN | TYP ² | MAX | | |
| I_{OH} | High level output current | $\overline{B0} - \overline{B7}$ | $V_{CC} = \text{MAX}, V_{IL} = \text{MAX}, V_{OH} = 1.9\text{V}$ | | | 100 | μA | |
| I_{OFF} | Power-off output current | $\overline{B0} - \overline{B7}$ | $V_{CC} = 0\text{V}, V_{IL} = \text{MAX}, V_{OH} = 1.9\text{V}$ | | | 100 | μA | |
| | | | $V_{CC} = 0\text{V}, V_{IL} = \text{MAX}, V_{OH} = 1.9\text{V}@85^\circ\text{C}$ | | | 300 | | |
| V_{OH} | High-level output voltage | AO0 – AO7 ³ | $V_{CC} = \text{MIN to MAX}; I_{OH} = -100\mu\text{A}$ | V_{CC} -0.2 | | | V | |
| | | | $V_{CC} = \text{MIN}; I_{OH} = -4\text{mA}$ | 2.4 | | | V | |
| | | | $V_{CC} = \text{MIN}; I_{OH} = -12\text{mA}$ | 2.0 | | | V | |
| V_{OL} | Low-level output voltage | AO0 – AO7 ³ | $V_{CC} = \text{MIN}; I_{OL} = 4\text{mA}$ | | | 0.4 | V | |
| | | | $V_{CC} = \text{MIN}; I_{OL} = 12\text{mA}$ | | | 0.8 | V | |
| | | $\overline{B0} - \overline{B7}$ | $V_{CC} = \text{MIN}, I_{OL} = 4\text{mA}$ | 0.5 | | | V | |
| | | | $V_{CC} = \text{MIN}, I_{OL} = 100\text{mA}$ | 0.75 | 1.0 | 1.20 | | |
| V_{IK} | Input clamp voltage | | $V_{CC} = \text{MIN}, I_I = I_{IK} = -18\text{mA}$ | | -0.85 | -1.2 | V | |
| I_I | Input leakage current | Control pins | $V_{CC} = 3.6\text{V}; V_I = V_{CC}$ or 100mV | | | ± 1.0 | μA | |
| | | Control/ AI0 – AI7 | $V_{CC} = 0\text{V}$ or 3.6V; $V_I = 5.5\text{V}$ | | | 10 | | |
| | | AI0 – AI7 | $V_{CC} = 3.6\text{V}; V_I = V_{CC}$ | | | 1 | | |
| | | Note 4 | $V_{CC} = 3.6\text{V}; V_I = 100\text{mV}$ | | | -5 | | |
| I_{IH} | High-level input current | $\overline{B0} - \overline{B7}$ | $V_{CC} = \text{MAX}, V_I = 1.9\text{V}$ | | | 100 | μA | |
| | | | $V_{CC} = \text{MAX}, V_I = 3.5\text{V}$, note 5 | 100 | | | | mA |
| | | | $V_{CC} = \text{MAX}, V_I = 3.75\text{V}$, Note 5 @ -40°C | 100 | | | | |
| I_{IL} | Low-level input current | $\overline{B0} - \overline{B7}$ | $V_{CC} = \text{MAX}, V_I = 0.75\text{V}$ | | | -100 | μA | |
| I_{OZH} | Off-state output current | AO0 – AO7 | $V_{CC} = \text{MAX}, V_O = 3\text{V}$ | | | 5 | μA | |
| I_{OZL} | Off-state output current | AO0 – AO7 | $V_{CC} = \text{MAX}, V_O = 0.5\text{V}$ | | | -5 | μA | |
| I_{CCZ} | Supply current | | $V_{CC} = \text{MAX}$, outputs disabled, $V_I = \text{GND}$ or 0.0 | | 16 | 31 | mA | |
| I_{CCH} I_{CCL} | Supply current (total) | B→A | $V_{CC} = \text{MAX}$, outputs High, $V_I = \text{GND}$ or 0.0 | | 16 | 35 | | |
| | | | $V_{CC} = \text{MAX}$, outputs Low, $V_I = \text{GND}$ or 0.0 | | 18 | 39 | | |
| I_{CCH} I_{CCL} | Supply current (total) | A→B | $V_{CC} = \text{MAX}$, outputs High, $V_I = \text{GND}$ or 0.0 | | 13 | 30 | | |
| | | | $V_{CC} = \text{MAX}$, outputs Low, $V_I = \text{GND}$ or 0.0 | | 8 | 16 | | |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
- All typical values are at $V_{CC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$.
- Due to test equipment limitations, actual test conditions are $V_{IH} = 1.8\text{V}$ and $V_{IL} = 1.3\text{V}$ for the B side.
- Unused pins are at V_{CC} or GND.
- For B port input voltage between 3 and 5 volt; I_{IH} will be greater than 100mA but the part will continue to function normally (clamping circuit is Active). This is not a tested condition.

3.3V BTL 8-bit TTL to BTL transceiver

FBL22040

AC ELECTRICAL CHARACTERISTICS INDUSTRIAL AND COMMERCIAL (A TO B)

| SYMBOL | PARAMETER | TEST CONDITION | $T_{amb} = +25^{\circ}\text{C}, V_{CC} = 3.3\text{V}, R_L = 9\Omega$ | | | $T_{amb} = -40 \text{ to } +85^{\circ}\text{C}, V_{CC} = 3.3\text{V} \pm 10\%, R_L = 9\Omega$ | | UNIT |
|------------------------|--|----------------|--|------------|------------|---|------------|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| t_{PLH} t_{PHL} | Propagation delay, AIn to $\bar{B}n$ | | 1.0 1.2 | 2.7 3.0 | 5.7 5.1 | 1.0 1.0 | 6.3 5.6 | ns |
| t_{PLH} t_{PHL} | OEB0 to $\bar{B}n$ | | 1.4 2.0 | 3.1 4.1 | 5.0 6.4 | 1.0 1.9 | 6.1 6.9 | ns |
| t_{PLH} t_{PHL} | $\overline{\text{OEB}}\bar{1}$ to $\bar{B}n$ | | 1.5 1.4 | 3.3 3.2 | 5.3 5.0 | 1.0 1.1 | 6.0 5.8 | ns |
| t_{TLH} t_{THL} | Transition time, $\bar{B}n$ Port (1.3V to 1.8V) | | 1.0 1.2 | 1.7 1.9 | 2.5 2.5 | 3.5 3.5 | 0.5 0.5 | ns |
| $t_{sk}(O)$ | Output skew between receivers in same package | | 0.5 | 1.0 | | | 1.5 | ns |
| $t_{sk}(P)$ | Pulse skew $ t_{PHL} - t_{PLH} $ MAX | | 0.3 | 1.0 | | | 1.5 | ns |

AC ELECTRICAL CHARACTERISTICS INDUSTRIAL AND COMMERCIAL (A TO B)

| SYMBOL | PARAMETER | TEST CONDITION | $T_{amb} = +25^{\circ}\text{C}, V_{CC} = 3.3\text{V}, R_L = 16.5\Omega$ | | | $T_{amb} = -40 \text{ to } +85^{\circ}\text{C}, V_{CC} = 3.3\text{V} \pm 10\%, R_L = 16.5\Omega$ | | UNIT |
|------------------------|--|----------------|---|------------|------------|--|------------|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| t_{PLH} t_{PHL} | Propagation delay, AIn to $\bar{B}n$ | | 1.2 1.2 | 2.8 2.8 | 4.4 4.6 | 1.0 1.1 | 5.2 5.1 | ns |
| t_{PLH} t_{PHL} | OEB0 to $\bar{B}n$ | | 1.8 1.8 | 3.6 3.8 | 5.6 5.9 | 1.2 1.7 | 6.5 6.2 | ns |
| t_{PLH} t_{PHL} | $\overline{\text{OEB}}\bar{1}$ to $\bar{B}n$ | | 1.6 1.3 | 3.4 3.0 | 6.2 4.8 | 1.0 1.0 | 6.0 5.6 | ns |
| t_{TLH} t_{THL} | Transition time, $\bar{B}n$ Port (1.3V to 1.8V) | | 1.0 1.2 | 1.7 1.9 | 2.5 2.5 | 0.5 0.5 | 3.0 3.0 | ns |
| $t_{sk}(O)$ | Output skew between receivers in same package | | 0.5 | 1.0 | | | 1.5 | ns |
| $t_{sk}(P)$ | Pulse skew $ t_{PHL} - t_{PLH} $ MAX | | 0.3 | 1.0 | | | 1.5 | ns |

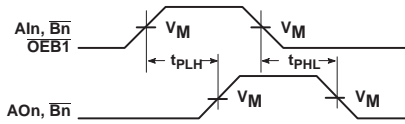
AC ELECTRICAL CHARACTERISTICS INDUSTRIAL AND COMMERCIAL (B TO A)

| SYMBOL | PARAMETER | TEST CONDITION | $T_{amb} = +25^{\circ}\text{C}, V_{CC} = 3.3\text{V}$ | | | $T_{amb} = -40 \text{ to } +85^{\circ}\text{C}, V_{CC} = 3.3\text{V} \pm 10\%$ | | UNIT |
|------------------------|---|----------------|---|------------|------------|--|------------|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| t_{PLH} t_{PHL} | Propagation delay, $\bar{B}n$ to AOn | | 2.4 2.3 | 4.4 4.2 | 6.6 6.3 | 2.1 2.1 | 7.4 7.3 | ns |
| t_{PLH} t_{PHL} | OEA to AOn | | 2.9 2.2 | 4.9 4.1 | 7.0 6.1 | 2.5 1.4 | 7.9 6.7 | ns |
| t_{PLH} t_{PHL} | OEA to AOn | | 2.8 1.2 | 4.7 2.9 | 6.7 4.6 | 2.5 1.0 | 7.3 5.3 | ns |
| t_{TLH} t_{THL} | Transition time, AOn Port (10% to 90% or 90% to 10%) | | 1.3 1.7 | 2.2 2.6 | 2.5 2.5 | 0.9 0.8 | 3.0 3.0 | ns |
| $t_{sk}(O)$ | Output skew between receivers in same package | | 0.5 | 1.0 | | | 1.5 | ns |
| $t_{sk}(P)$ | Pulse skew $ t_{PHL} - t_{PLH} $ MAX | | 0.3 | 1.0 | | | 1.5 | ns |

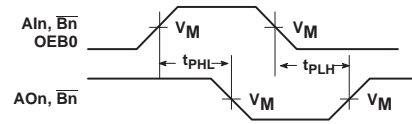
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FBL22040

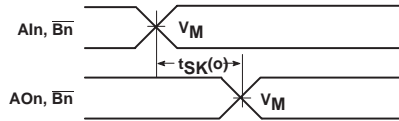
AC WAVEFORMS



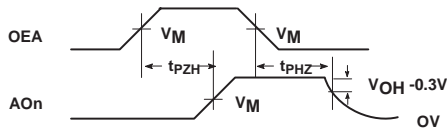
Waveform 1. Propagation Delay for Data or Output Enable to Output



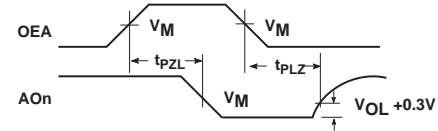
Waveform 2. Propagation Delay for Data or Output Enable to Output



Waveform 3. Output Skews



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

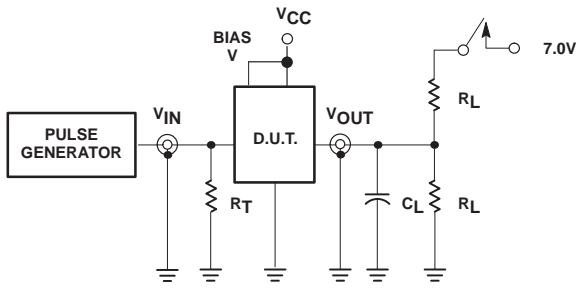
NOTE: $V_M = 1.55V$ for \overline{Bn} , $V_M = 1.5V$ for all others.

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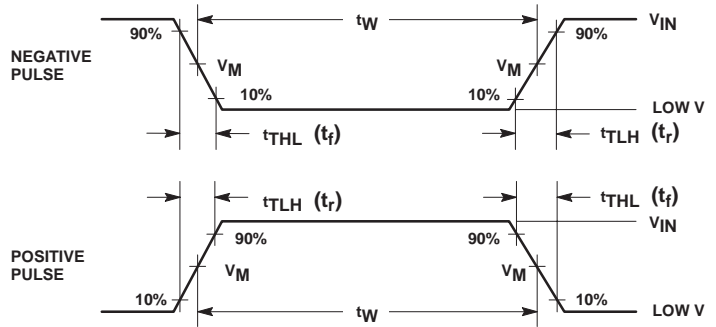
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FBL22040

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs on A Port



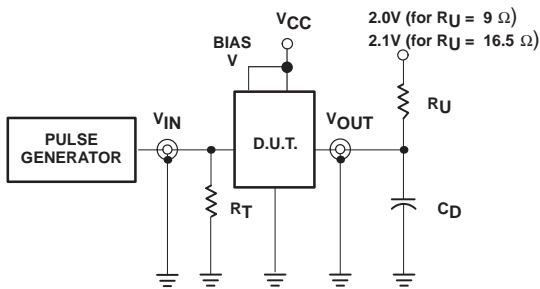
$V_M = 1.55V$ for \overline{Bn} , $V_M = 1.5V$ for all others.

Input Pulse Definitions

SWITCH POSITION

| TEST | SWITCH |
|-----------------------|--------|
| t_{PLZ} , t_{PZL} | closed |
| All other | open |

| Family FB+ | INPUT PULSE REQUIREMENTS | | | | | |
|---------------|--------------------------|-------|-----------|-------|-----------|-----------|
| | Amplitude | Low V | Rep. Rate | t_W | t_{TLH} | t_{THL} |
| A Port | 3.0V | 0.0V | 1MHz | 500ns | 2.5ns | 2.5ns |
| B Port | 2.0V | 1.0V | 1MHz | 500ns | 2.5ns | 2.5ns |



Test Circuit for Outputs on B Port

DEFINITIONS:

- R_L = Load Resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
- C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_U = Pull up resistor; see AC CHARACTERISTICS for value.

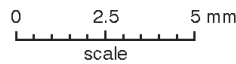
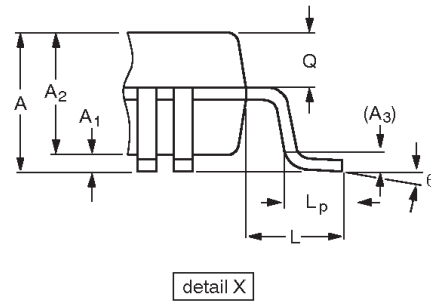
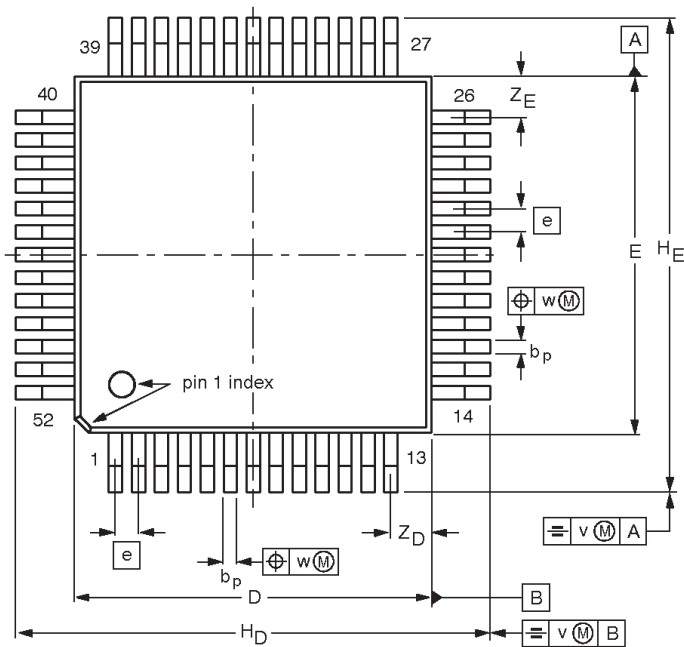
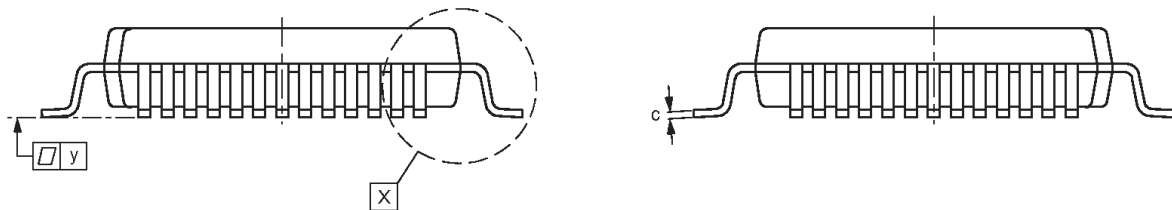
SG00059

3.3V BTL 8-bit TTL TO BTL transceiver

74FBL22040

QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm

SOT379-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _D | H _E | L | L _p | Q | v | w | y | Z _D ⁽¹⁾ | Z _E ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|----------------|------|----------------|--------------|------|------|------|-------------------------------|-------------------------------|----------|
| mm | 2.45 | 0.45 0.25 | 2.10 1.95 | 0.25 | 0.38 0.22 | 0.23 0.13 | 10.1 9.9 | 10.1 9.9 | 0.65 | 13.45 12.95 | 13.45 12.95 | 1.60 | 0.95 0.65 | 1.05 0.90 | 0.20 | 0.12 | 0.10 | 1.24 0.95 | 1.24 0.95 | 7° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|------|--|---------------------|------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT379-1 | | MO-108 | | | | 95-02-04 |

3.3V BTL 8-bit TTL TO BTL transceiver

74FBL22040

Data sheet status

| Data sheet status | Product status | Definition [1] |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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