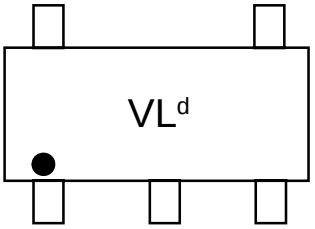
Noninverting Buffer / CMOS Logic Level Shifter

FC74VHC1G50 is a single gate noninverting buffer fabricated with silicon gate CMOS technology.
It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.
The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.
The FC74VHC1G50 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage.
This allows the 74VHC1G50 to be used to interface 5 V circuits to 3 V circuits.

- High Speed: t_{PD} = 3.5 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2 uA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- CMOS–Compatible Outputs: V_{OH} > 0.8 V_{CC} ; V_{OL} < 0.1 V_{CC} @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 104; Equivalent Gates = 26

SC–70/SC–88A/SOT–353
DF SUFFIX

MARKING DIAGRAMS



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	NC
2	IN A
3	GND
4	OUT Y
5	V_{CC}

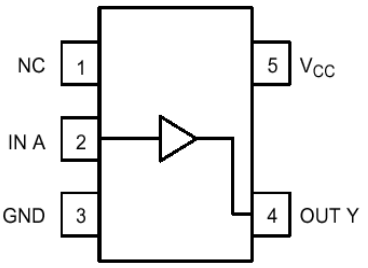


Figure 1. Pinout (Top View)

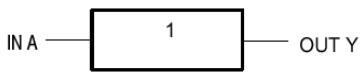


Figure 2. Logic Symbol

FUNCTION TABLE

Inputs	Output
A	**Y**
L	L
H	H

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		– 0.5 to + 7.0	V
V_{IN}	DC Input Voltage		– 0.5 to +7.0	V
V_{OUT}	DC Output Voltage	V_{CC}=0	– 0.5 to +7.0	V
		High or Low State	–0.5 to V_{CC} + 0.5	
I_{IK}	Input Diode Current		–20	mA
I_{OK}	Output Diode Current	V_{OUT} < GND; V_{OUT} > V_{CC}	+20	mA
I_{OUT}	DC Output Current, per Pin		+ 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND		+50	mA
P_D	Power dissipation in still air		200	mW
Θ_{JA}	Thermal resistance		333	°C/W
T_L	Lead Temperature, 1 mm from Case for 10 s		260	°C
T_J	Junction Temperature Under Bias		+ 150	°C
T_{stg}	Storage temperature		–65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2)	>2000	V
		Machine Model (Note 3)	> 200	
		Charged Device Model (Note 4)	N/A	
$I_{LATCH-UP}$	Latch–Up Performance	Above V_{CC} and Below GND at 125°C (Note 5)	± 500	mA

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22–A114–A
3. Tested to EIA/JESD22–A115–A
4. Tested to JESD22–C101–A
5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		3.0	5.5	V
V_{IN}	DC Input Voltage		0.0	5.5	V
V_{OUT}	DC Output Voltage	V_{CC} = 0	0.0	5.5	V
		High Low State	0.0	V_{CC}	
T_A	Operating Temperature Range		– 55	+ 125	°C
t_r ,t_f	Input Rise and Fall Time	V_{CC} = 3.3 ± 0.3 V	0	100	ns/V
		V_{CC} = 5.0 ± 0.5 V	0	20	

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

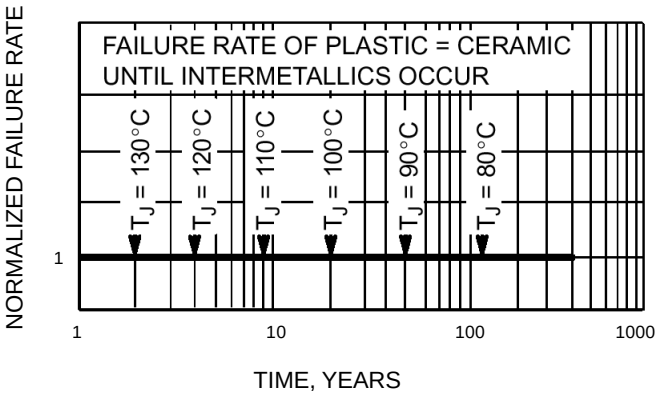


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	Typ	Max	$T_A \leq$ 85°C Min	Max	−55°C≤T_A≤125°C Min	Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0	1.5			1.5		1.5		V
			3.0	2.1			2.1		2.1		
			4.5	3.15			3.15		3.15		
			5.5	3.85			3.85		3.85		
V_{IL}	Maximum Low–Level Input Voltage		2.0			0.5		0.5		0.5	V
			3.0			0.9		0.9		0.9	
			4.5			1.35		1.35		1.35	
			5.5			1.65		1.65		1.65	
V_{OH}	Minimum High–Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OH} = – 50 μA	3.0	2.9	3.0		2.9		2.9		V
			4.5	4.4	4.5		4.4		4.4		
		V_{IN} = V_{IH} or V_{IL} I_{OH} = –4 mA	3.0	2.58			2.48		2.34		
		I_{OH} = –8 mA	4.5	3.94			3.80		3.66		
V_{OL}	Maximum Low–Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	3.0		0.0	0.1		0.1		0.1	V
			4.5		0.0	0.1		0.1		0.1	
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4 mA	3.0			0.36		0.44		0.52	
		I_{OL} = 8 mA	4.5			0.36		0.44		0.52	
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	0 to5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: V_{IN} = 3.4 V	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5 V	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_r = t_f = 3.0 ns

Symbol	Parameter	Test Conditions	T_A = 25°C Min	Typ	Max	$T_A \leq$ 85°C Min	Max	−55°C≤T_A≤125°C Min	Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Y	V_{CC} = 3.3± 0.3 V C_L = 15 pF		4.5	10.0		11.0		13.0	ns
		C_L = 50 pF		6.3	13.5		15.0		17.5	
		V_{CC} = 5.0± 0.5 V C_L = 15 pF		3.5	6.7		7.5		8.5	
		C_L = 50 pF		4.3	7.7		8.5		9.5	
C_N	Maximum Input Capacitance			5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 6)	12	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

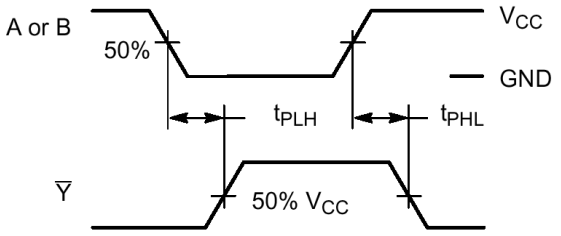
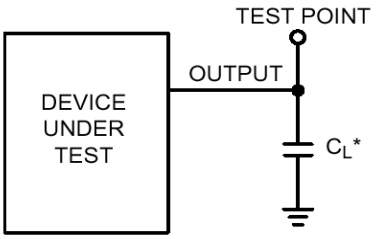


Figure 4. Switching Waveforms

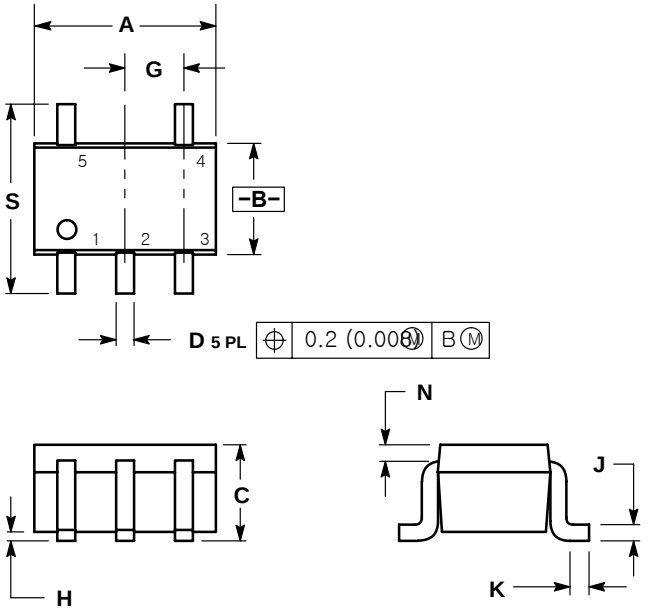


*Includes all probe and jig capacitance

Figure 5. Test Circuit

PACKAGE DIMENSIONS

SC70−5/SC−88A/SOT−353 DF SUFFIX



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.070	0.087	1.80	2.20
B	0.040	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	−−−	0.004	−−−	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDERING FOOTPRINT*