Panasonic

FC8V22080L

Gate resistor installed Dual N-channel MOS FET

For lithium-ion secondary battery protection circuits

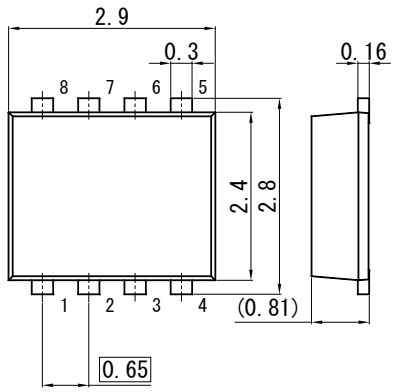
■ Features

- Low drain-source ON resistance:Rds(on) typ. = 13 mΩ(VGS = 4.5 V)
- Built-in gate resistor
- Halogen-free / RoHS compliant
  (EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)

■ Marking Symbol: 4D

■ Packaging

Embossed type (Thermo-compression sealing) : 3 000 pcs / reel (standard)



1. Source(FET1) 5. Darin(FET1,2)
2. Gate(FET1) 6. Darin(FET1,2)
3. Source(FET2) 7. Darin(FET1,2)
4. Gate(FET2) 8. Darin(FET1,2)

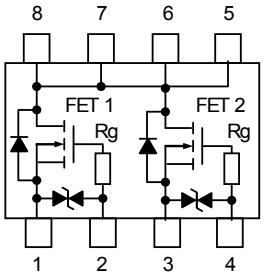
Panasonic	WMini8-F1
JEITA	SC-115
Code	-

■ Absolute Maximum Ratings Ta = 25 °C

Parameter		Symbol	Rating	Unit
Drain-source Voltage		VDS	24	V
Gate-source Voltage		VGS	±12	V
Drain Current	DC *1	ID1	7	A
	DC *2	ID2	10	A
	Pulse *3	IDp	70	A
Total power dissipation	Ta = 25 °C, DC *1	PD1	1.0	W
	Ta = 25 °C, DC *2	PD2	2.0	
	Ta = 25 °C, t = 10 s *1	PD3	1.2	
Channel Temperature		Tch	150	°C
Storage Temperature Range		Tstg	-55 to +150	°C
Thermal resistance (ch-a)		Rth(ch-a)	125	°C/W

Note *1 Mounted on FR4 board (25.4 mm × 25.4 mm × t0.8 mm)
Copper foil of the drain portion should have a area of 300mm^2 or more.
*2 Mounted on Ceramic substrate (70 mm × 70 mm × t1.0 mm).
*3 t = 10 μs, Duty Cycle ≤ 1 %

Internal Connection



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Established : 2013-01-10
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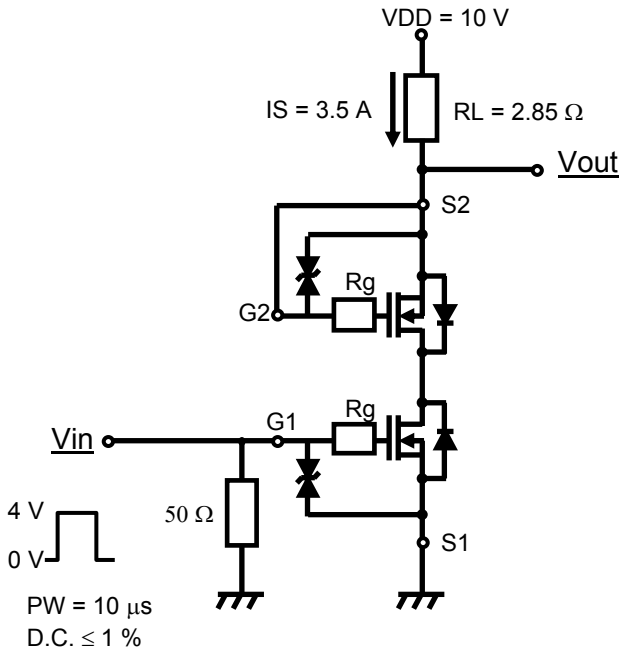
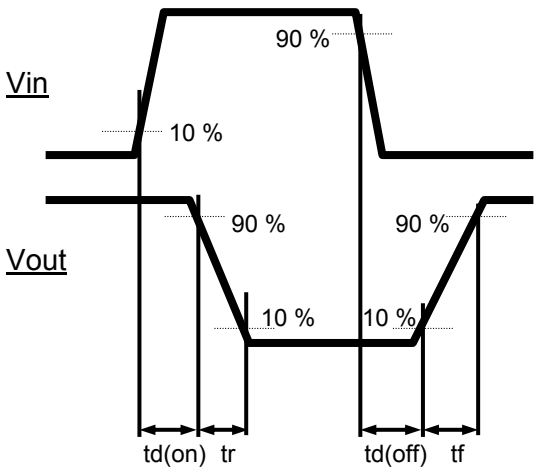
■ Electrical Characteristics Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	24			V
Zero Gate Voltage Drain Current	IDSS	VDS = 24 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VSS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = 0.33 mA, VDS = 10 V	0.40	0.90	1.4	V
Drain-source On-state Resistance	RDS(on)1	ID = 3.5 A, VGS = 4.5 V	9.8	13	16.2	mΩ
	RDS(on)2	ID = 3.5 A, VGS = 3.8 V	10	13.8	18.1	
	RDS(on)3	ID = 3.5 A, VGS = 3.1 V	10.8	15.5	22.1	
	RDS(on)4	ID = 3.5 A, VGS = 2.5 V	12	18.5	32.9	
Body Diode Forward Voltage	VSD	IF = 7.0 A, VGS = 0 V		0.8	1.2	V
Input Capacitance *1	Ciss	VDS = 10 V, VGS = 0 V, f = 1 MHz		860		pF
Output Capacitance *1	Coss			85		
Reverse Transfer Capacitance *1	Crss			70		
Turn-on delay Time *1,*2	td(on)	VDD = 10 V, VGS = 0 to 4.0 V, ID = 3.5 A		0.3		μs
Rise Time *1,*2	tr			0.6		
Turn-off delay Time *1,*2	td(off)	VDD = 10 V, VGS = 4.0 to 0 V, ID = 3.5 A		2.2		μs
Fall Time *1,*2	tf			1.1		
Total Gate Charge *1	Qg	VDD = 10 V, VGS = 0 to 4.0 V, ID = 7.0 A		7.8		nC
Gate-source Charge *1	Qgs			2.8		
Gate-drain Charge *1	Qgd			1.8		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.
*1 Assured by design
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time





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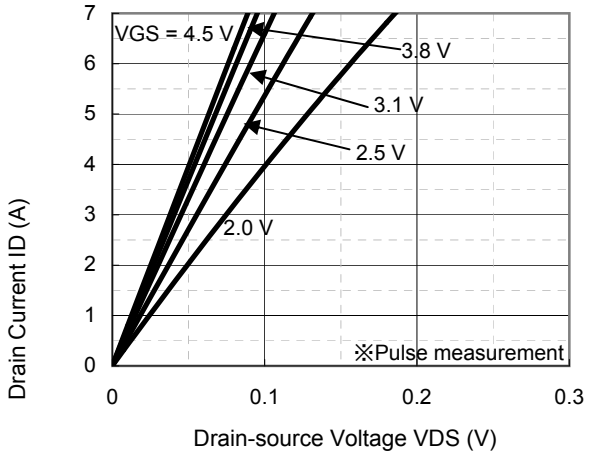
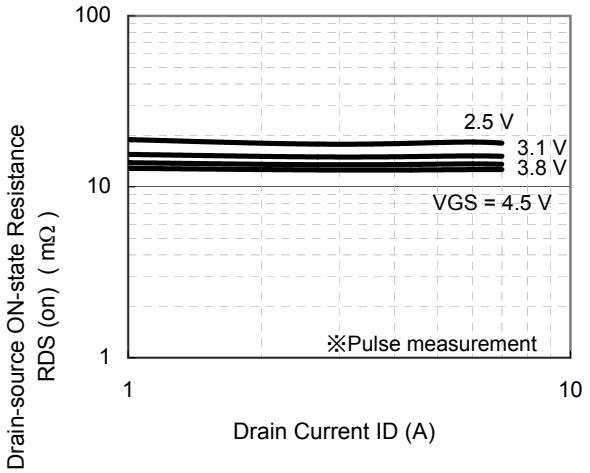
Technical Data (reference)

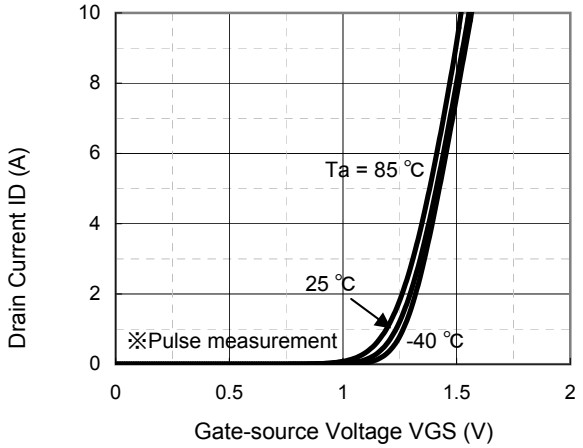
ID - VDS



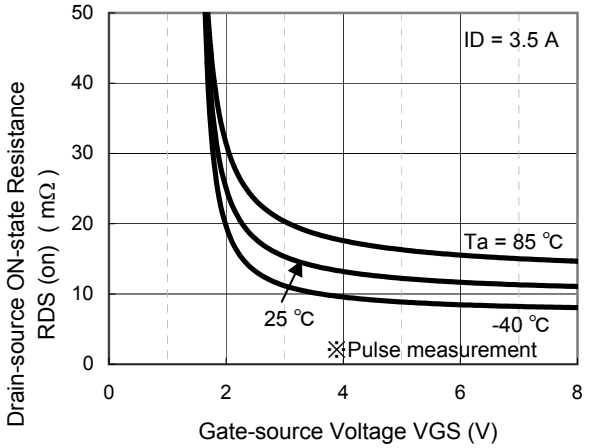
RDS(on) - ID



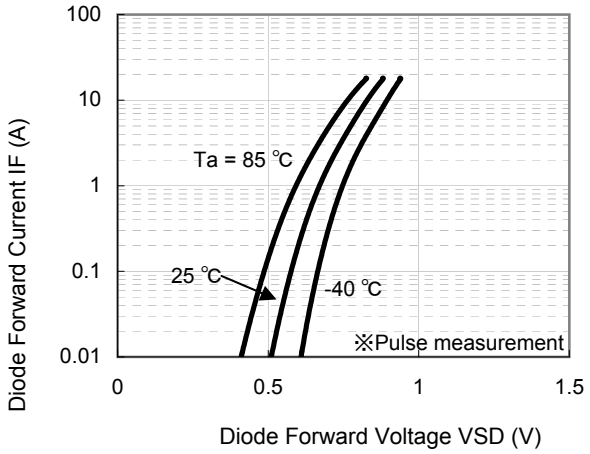
ID - VGS



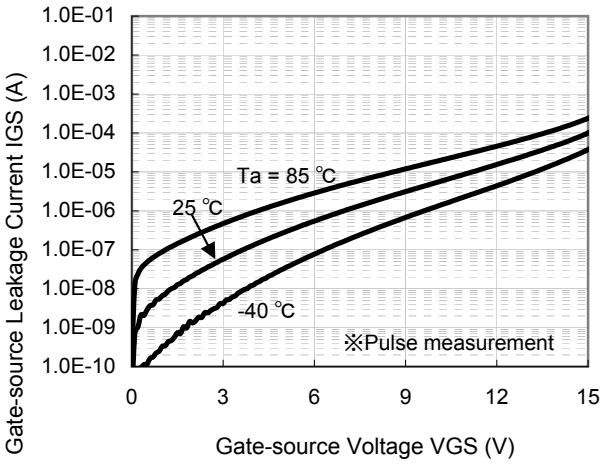
RDS(on) - VGS



IF - VF



IGS - VGS



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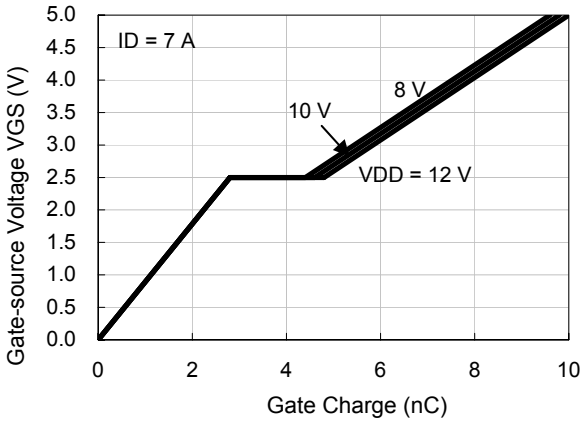
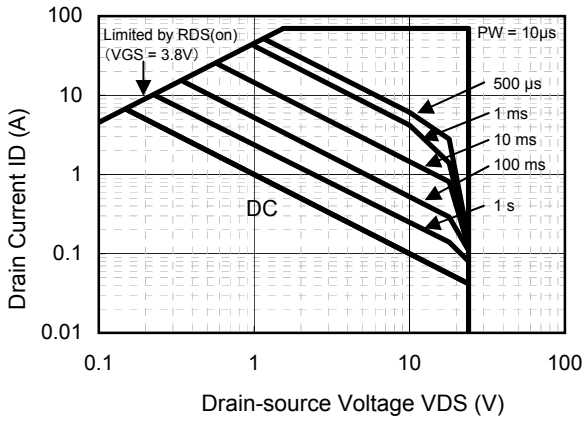
Technical Data (reference)

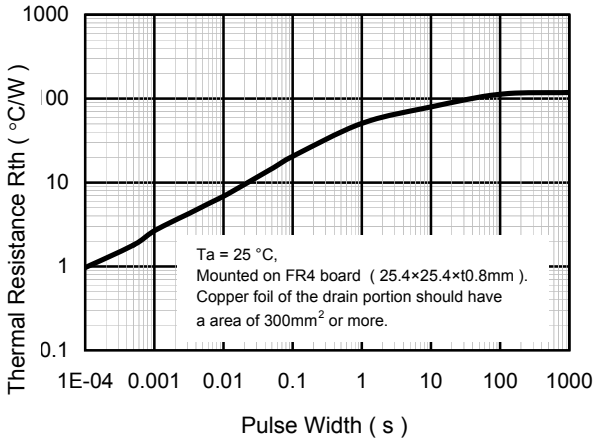
Dynamic Input/Output Characteristics



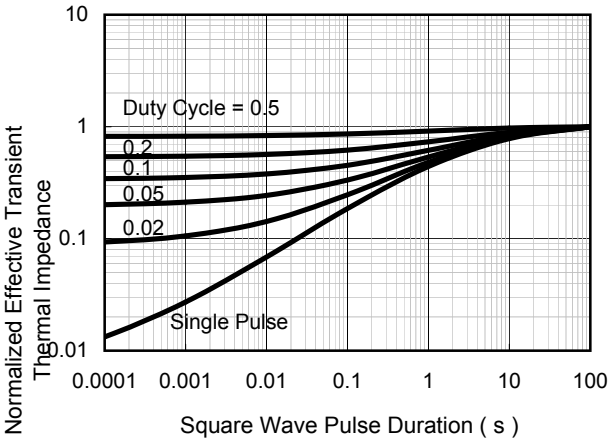
Safe Operating Area



Rth - tsw



Thermal Response



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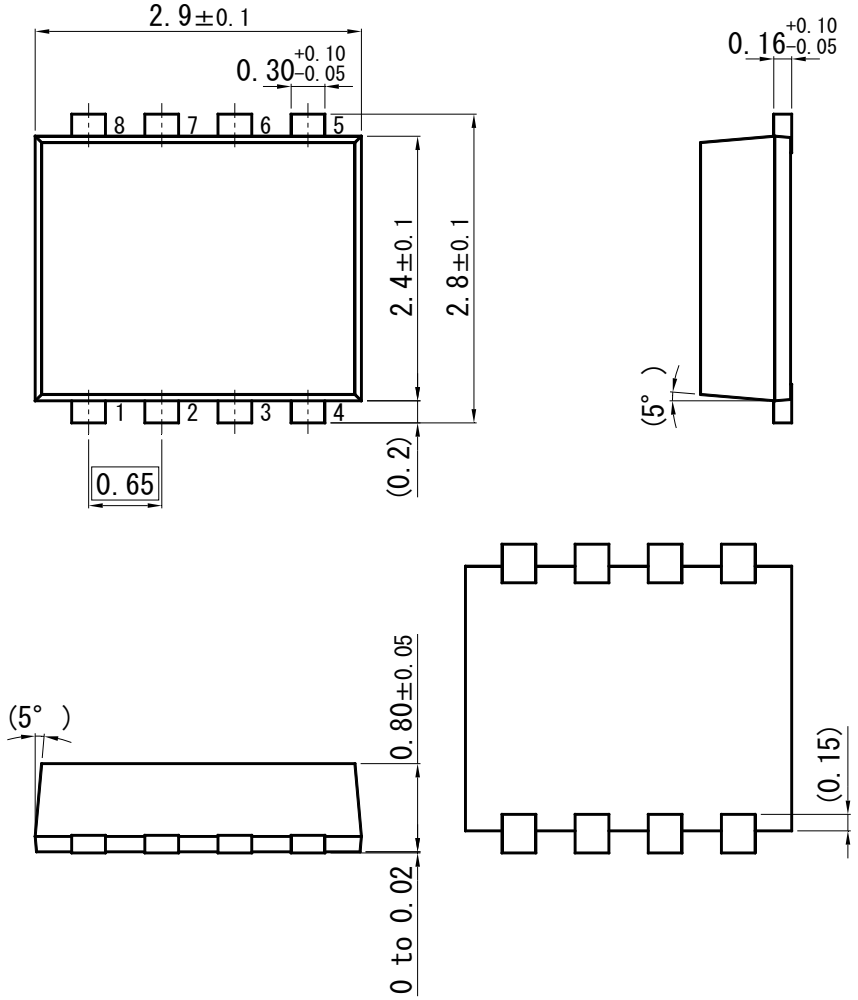
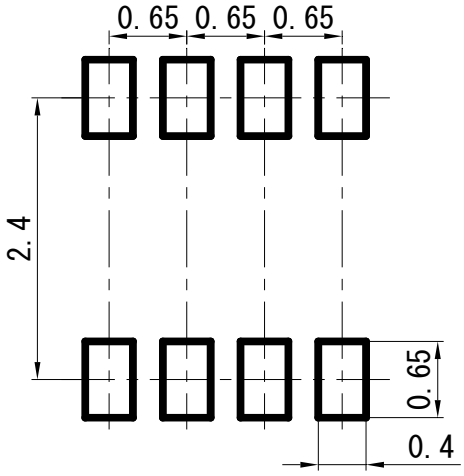
WMini8-F1

Unit: mm



■Land Pattern (Reference) (Unit: mm)



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