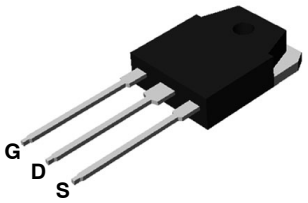
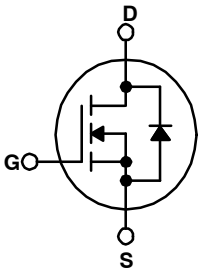
MOSFET – N-Channel, SUPERFET®

600 V, 20 A, 190 mΩ

FCA20N60



TO−3P−3L
CASE 340BZ



Description

SUPERFET MOSFET is **onsemi**'s first generation of high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on− resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switch− ing performance, dv/dt rate and higher avalanche energy. Con− sequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.

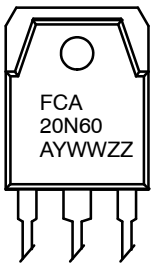
Features

- 650 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 150 mΩ
- Ultra Low Gate Charge (Typ. Qg = 75 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 165 pF)
- 100% Avalanche Tested
- This Device is Pb−Free

Applications

- Solar Inverter
- AC−DC Power Supply

MARKING DIAGRAM



FCA20N60	= Specific Device Code
A	= Assembly Location
YWW	= Date Code (Year and Week)
ZZ	= Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping†
FCA20N60	TO−3P−3L (Pb−Free)	450 Units / Tube
FCA20N60−F109	TO−3P−3L (Pb−Free)	450 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MOSFET MAXIMUM RATINGS

(T_C = 25°C unless otherwise noted.)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate−Source Voltage	±30	V
I_D	Drain Current – Continuous (T_C = 25°C) – Continuous (T_C = 100°C)	 20 12.5	A
I_{DM}	Drain Current – Pulsed (Note 1)	60	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	690	mJ
I_{AR}	Avalanche Current (Note 1)	20	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	20.8	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation – (T_C = 25°C) – Derate Above 25°C	 208 1.67	 W W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8” from Case for 5 Seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	41.7	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V, T_J = 25°C	600	–	–	V
		I_D = 250 μA, V_{GS} = 0 V, T_J = 150°C	–	650	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.6	–	V/°C
BV_{DS}	Drain−Source Avalanche Breakdown Voltage	V_{GS} = 0 V, I_D = 20 A	–	700		V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 480 V, T_C = 125°C	–	–	10	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	–	–	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 10 A	–	0.15	0.19	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 10 A	–	17	–	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	2370	3080	pF
C_{oss}	Output Capacitance		–	1280	1665	pF
C_{rss}	Reverse Transfer Capacitance		–	95	–	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1 MHz	–	65	85	pF
C_{oss}(eff.)	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	165	–	pF
Q_g	Total Gate Charge at 10 V	V_{DS} = 480 V, I_D = 20 A, V_{GS} = 10 V (Note 4)	–	75	98	nC
Q_{gs}	Gate to Source Charge		–	13.5	18	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	36	–	nC
Switching Characteristics						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 300 V, I_D = 20 A, V_{GS} = 10 V R_G = 25 Ω (Note 4)	–	62	135	ns
t_r	Turn−On Rise Time		–	140	290	ns
$t_{d(off)}$	Turn−Off Delay Time		–	230	470	ns
t_f	Turn−Off Fall Time		–	65	140	ns
Drain−Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	20	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	60	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 20 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 20 A, dI_F/dt = 100 A/μs	–	530	–	ns
Q_{rr}	Reverse Recovery Charge		–	10.5	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:
1. Repetitive Rating: Pulse width−limited by maximum junction temperature.
2. I_{AS} = 10 A V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 20 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature typical Characteristics.

TYPICAL CHARACTERISTICS

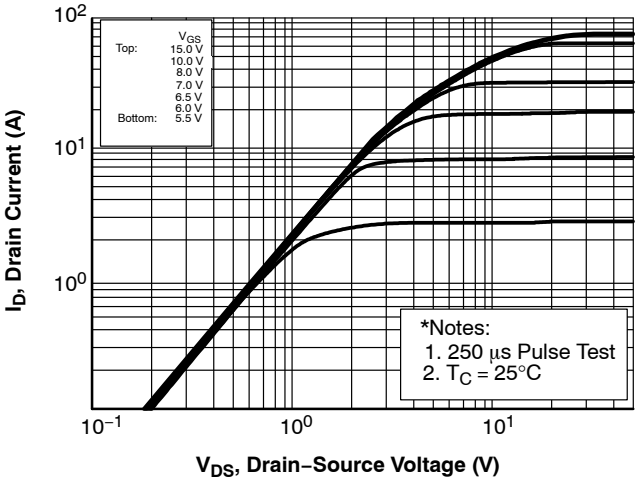


Figure 1. On−Region Characteristics

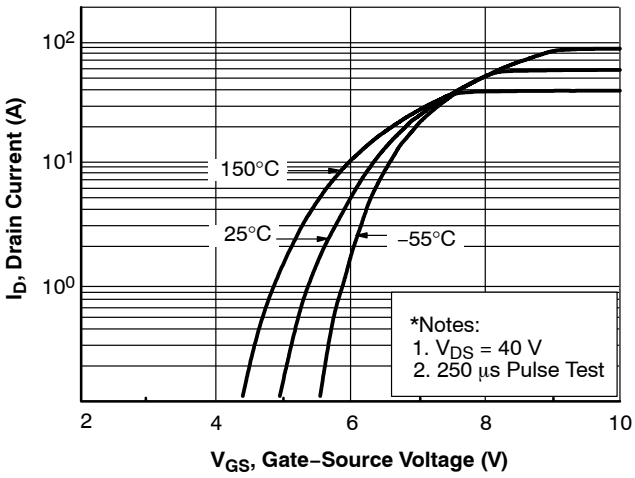


Figure 2. Transfer Characteristics

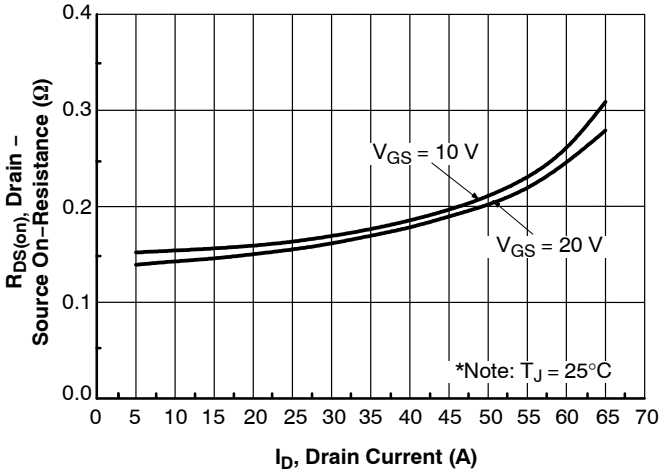


Figure 3. On−Resistance Variation vs Drain Current and Gate Voltage

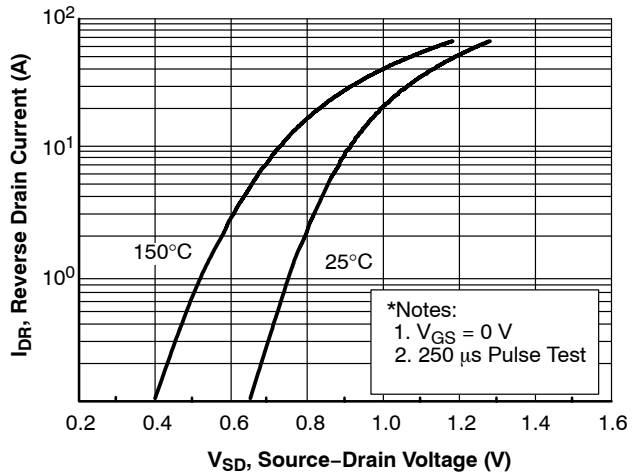


Figure 4. Body Diode Forward Voltage Variation vs Source Current and Temperature

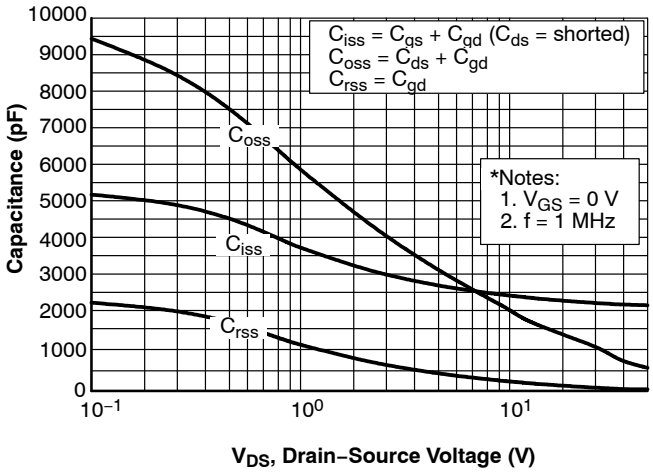


Figure 5. Capacitance Characteristics

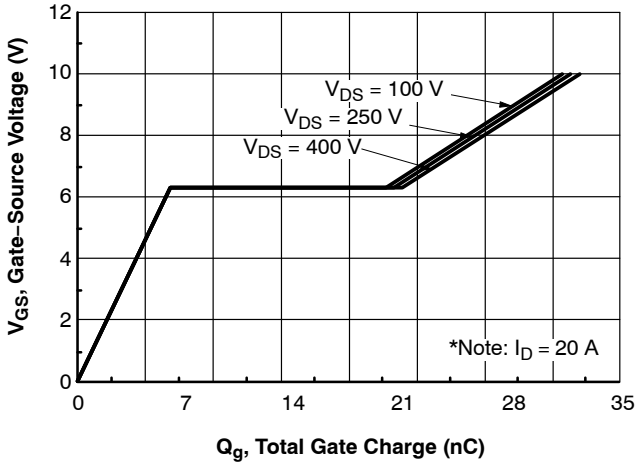


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

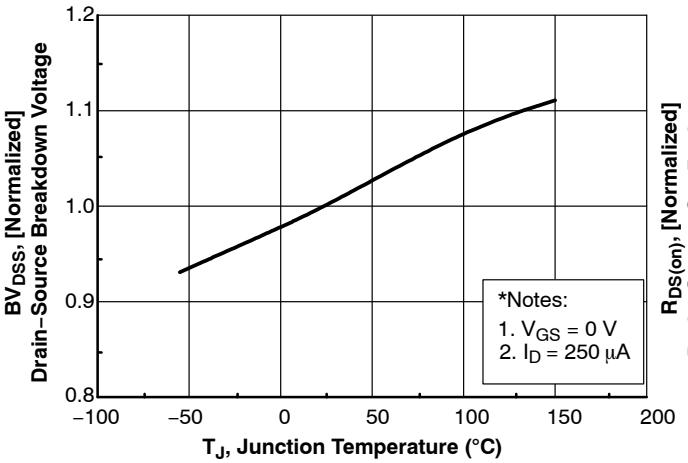


Figure 7. Breakdown Voltage Variation vs Temperature

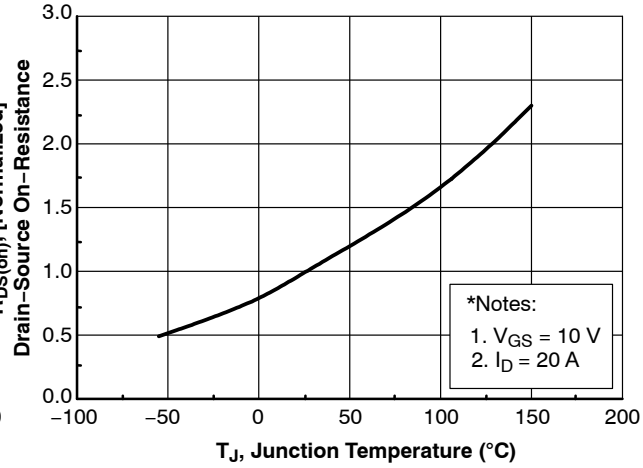


Figure 8. On−Resistance Variation vs Temperature

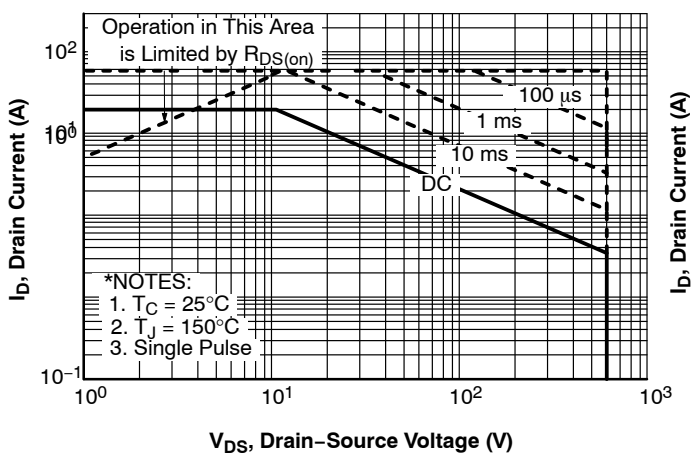


Figure 9. Maximum Safe Operating Area

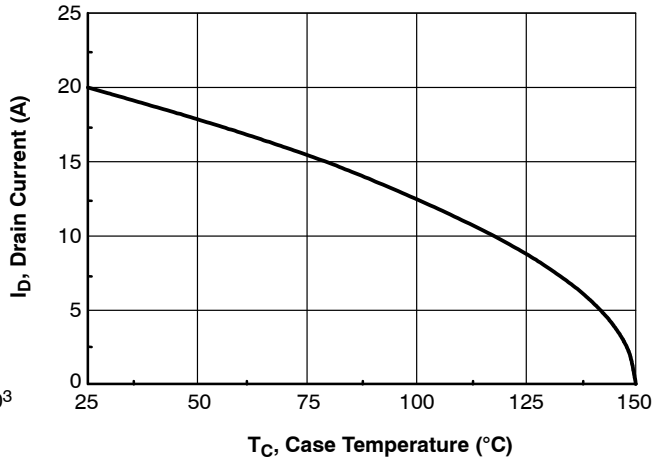


Figure 10. Maximum Drain Current vs. Case Temperature

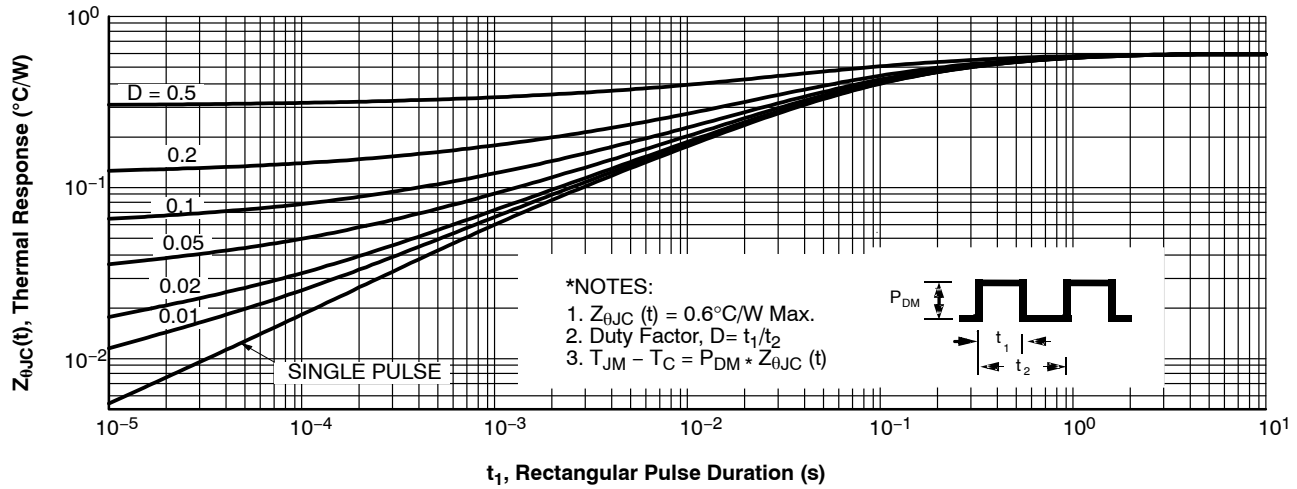


Figure 11. Transient Thermal Response Curve

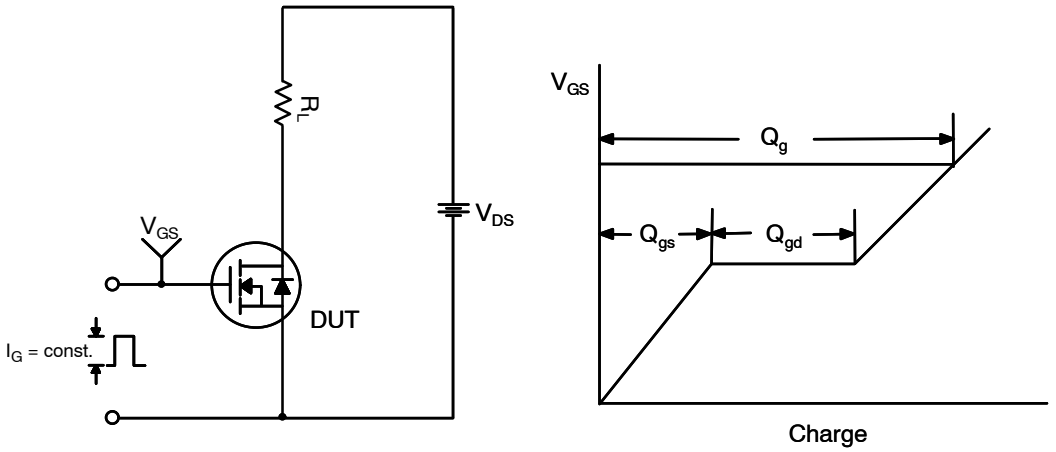


Figure 12. Gate Charge Test Circuit & Waveform

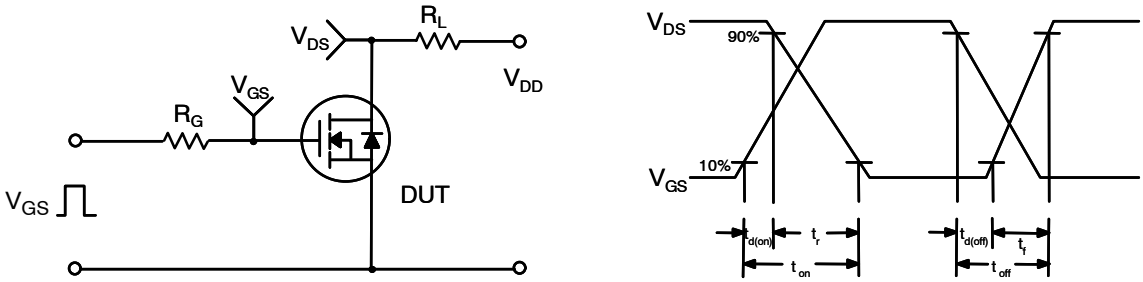


Figure 13. Resistive Switching Test Circuit & Waveforms

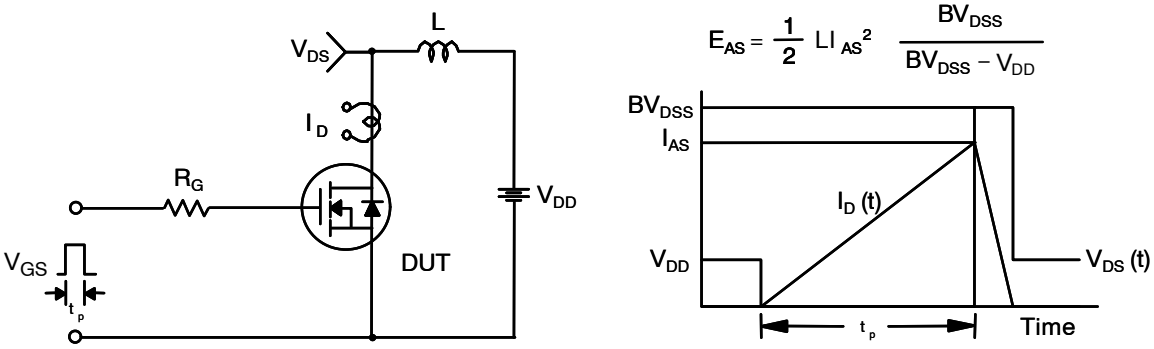


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

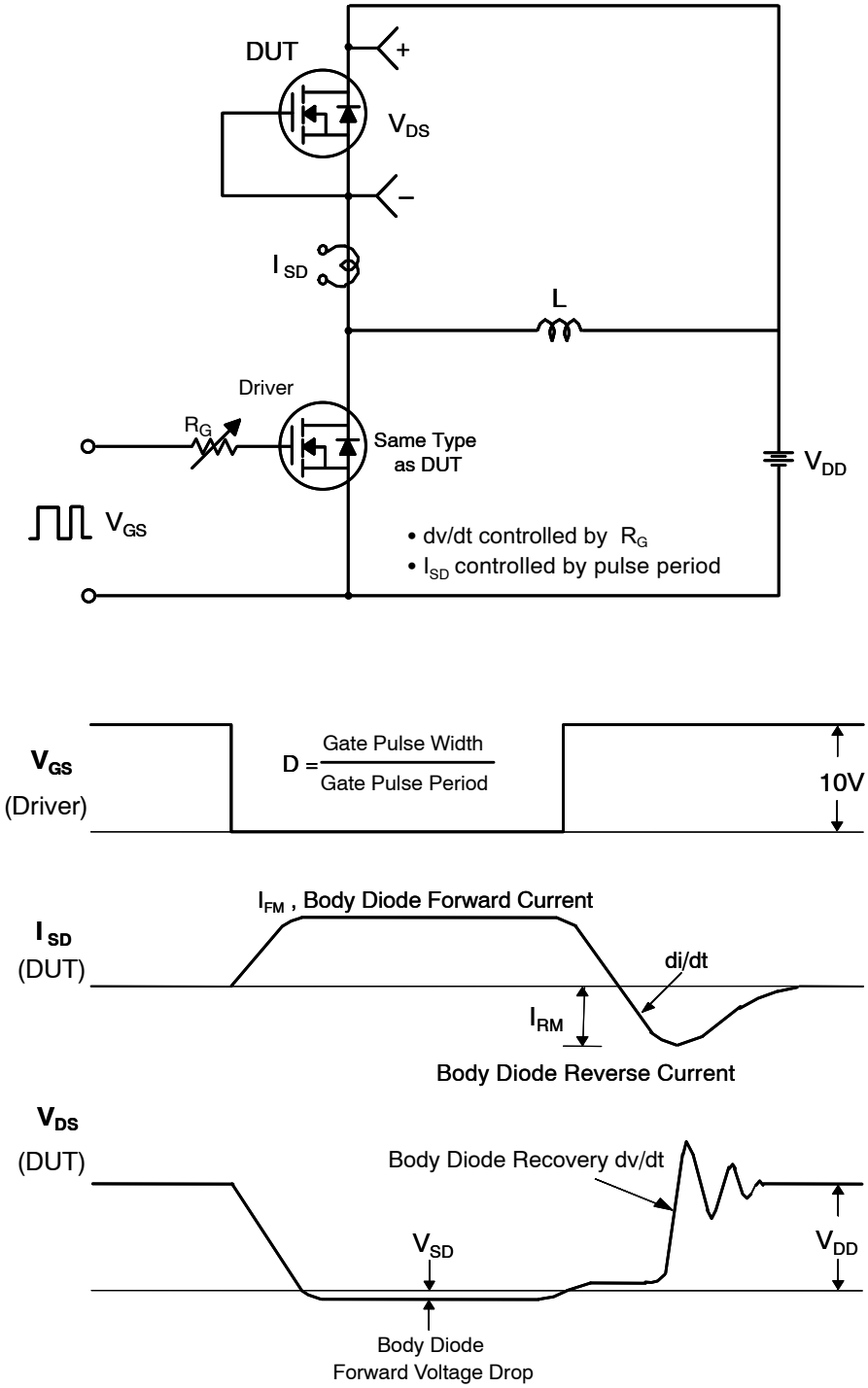


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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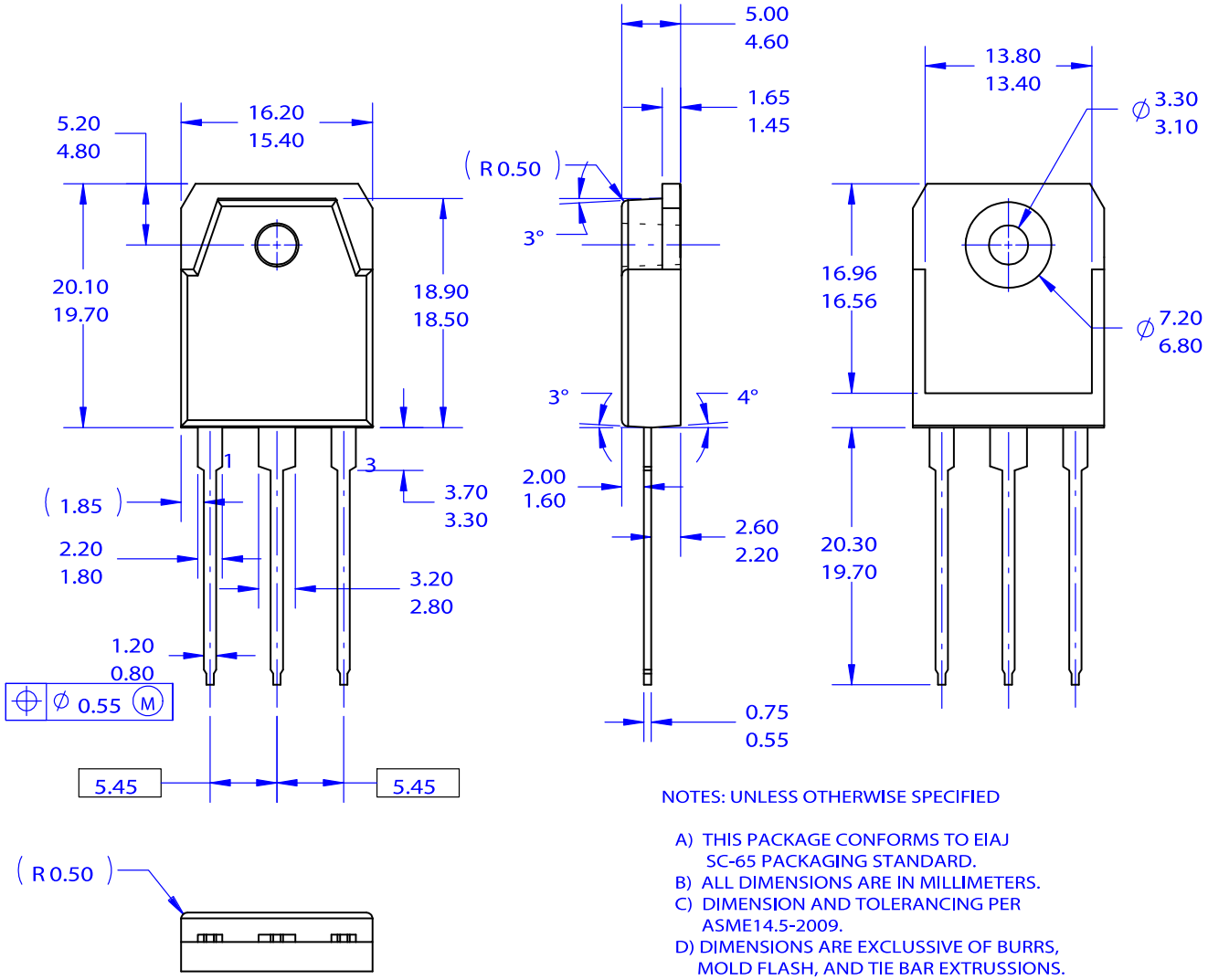
CASE 340BZ
ISSUE O

DATE 31 OCT 2016



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSION AND TOLERANCING PER ASME14.5-2009.
D) DIMENSIONS ARE EXCLUSSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSSIONS.

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