

# FCB36N60N

## N-Channel SupreMOS® MOSFET

600 V, 36 A, 90 mΩ

### Features

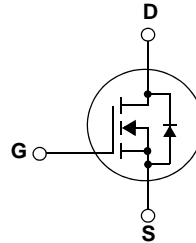
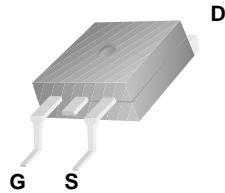
- $R_{DS(on)} = 81 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 18 \text{ A}$
- Ultra low gate charge (Typ.  $Q_g = 86 \text{ nC}$ )
- Low effective output capacitance (Typ.  $C_{oss,eff} = 361 \text{ pF}$ )
- 100% avalanche tested
- RoHS compliant

### Description

The SupreMOS® MOSFET is Fairchild Semiconductor®'s next-generation of high voltage super-junction (SJ) technology employing a deep trench filling process that differentiate it from the conventional MOSFETs. This advanced technology and precise process control provide lowest  $R_{sp}$  on-resistance, superior switching performance and ruggedness. SupreMOS MOSFET is suitable for high frequency switching power converter applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.

### Applications

- Solar Inverter
- AC-DC Power Supply



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted\*

Symbol	Parameter	FCB36N60N	Unit
$V_{DSS}$	Drain to Source Voltage	600	V
$V_{GSS}$	Gate to Source Voltage	$\pm 30$	V
$I_D$	Drain Current	-Continuous ( $T_C = 25^\circ\text{C}$ )	36
		-Continuous ( $T_C = 100^\circ\text{C}$ )	22.7
$I_{DM}$	Drain Current	- Pulsed (Note 1)	108
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	1800
$I_{AR}$	Avalanche Current		12
$E_{AR}$	Repetitive Avalanche Energy		3.12
dv/dt	MOSFET dv/dt Ruggedness		100
	Peak Diode Recovery dv/dt	(Note 3)	20
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	312
		- Derate above $25^\circ\text{C}$	2.6
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

\*Drain current limited by maximum junction temperature

### Thermal Characteristics

Symbol	Parameter	FCB36N60N	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.4	$^\circ\text{C/W}$
$R_{\theta JA}^*$	Thermal Resistance, Junction to Ambient *	40	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

\*When mounted on the minimum pad size recommended (PCB Mount)

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCB36N60N	FCB36N60N	D <sup>2</sup> -PAK	330mm	24mm	800

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}, T_C = 25^\circ\text{C}$	600	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{ mA}, \text{Referenced to } 25^\circ\text{C}$	-	0.7	-	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}$	-	-	10	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	-	100	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 18\text{ A}$	-	81	90	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 18\text{ A}$	-	41	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$	-	3595	4785	pF
$C_{oss}$	Output Capacitance		-	149	200	pF
$C_{rss}$	Reverse Transfer Capacitance		-	4	6	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	80	-	pF
$C_{oss\text{eff}}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 380\text{ V}, V_{GS} = 0\text{ V}$	-	361	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 18\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4)	-	86	112	nC
$Q_{gs}$	Gate to Source Gate Charge		-	15.4	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	26.4	-	nC
ESR	Equivalent Series Resistance (G-S)	Drain Open	-	1	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 18\text{ A}$ $R_G = 4.7\ \Omega$ (Note 4)	-	23	56	ns
$t_r$	Turn-On Rise Time		-	22	54	ns
$t_{d(off)}$	Turn-Off Delay Time		-	94	198	ns
$t_f$	Turn-Off Fall Time		-	4	18	ns

### Drain-Source Diode Characteristics

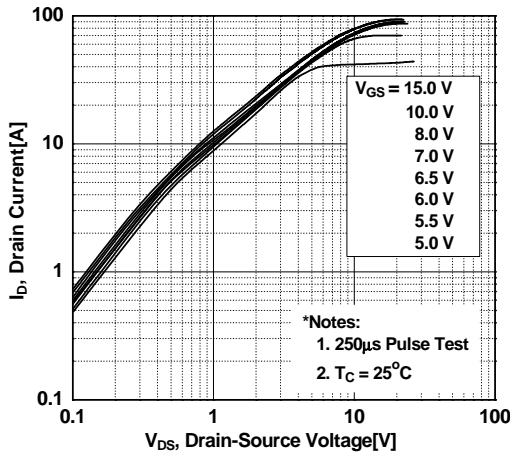
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	36	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	108	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 18\text{ A}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 18\text{ A}$	-	574	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F/dt = 100\text{ A}/\mu\text{s}$	-	10	-	$\mu\text{C}$

#### Notes:

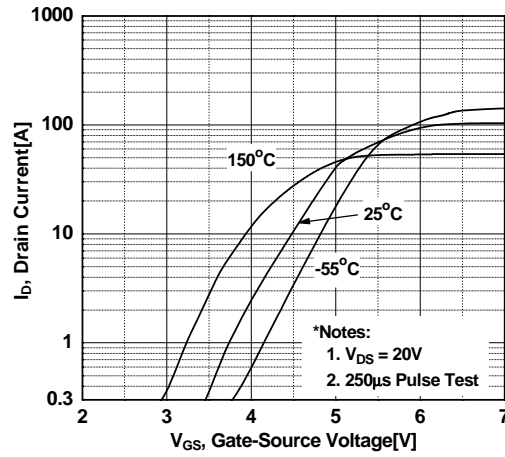
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $I_{AS} = 12\text{ A}, R_G = 25\ \Omega, \text{Starting } T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 36\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} = 380\text{ V}, \text{Starting } T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

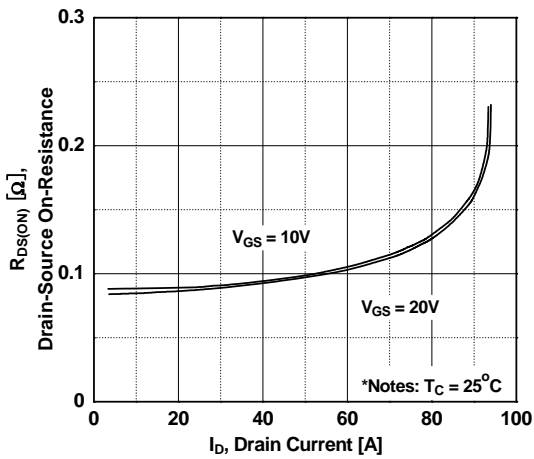
**Figure 1. On-Region Characteristics**



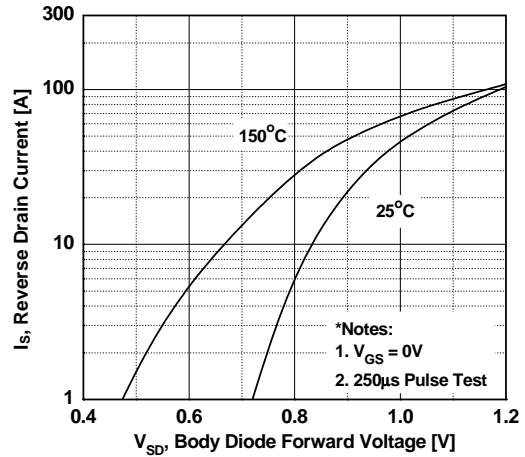
**Figure 2. Transfer Characteristics**



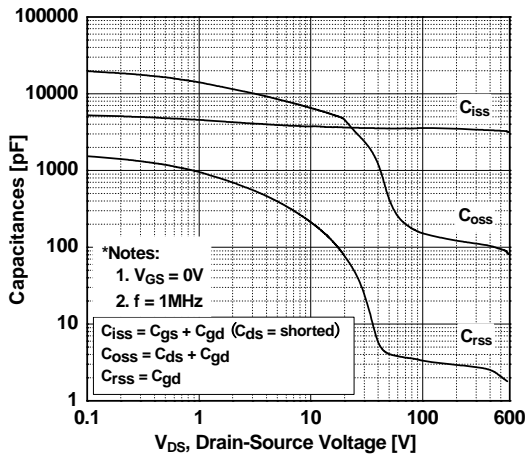
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



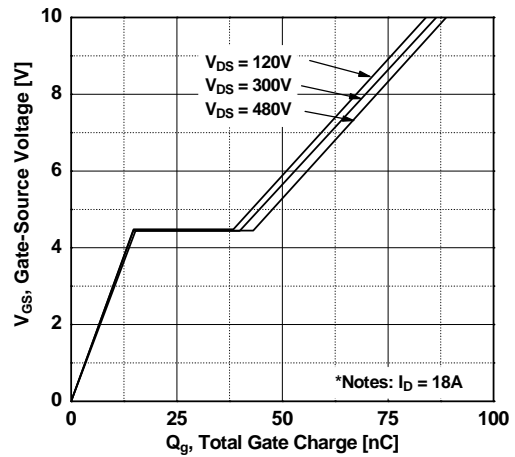
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

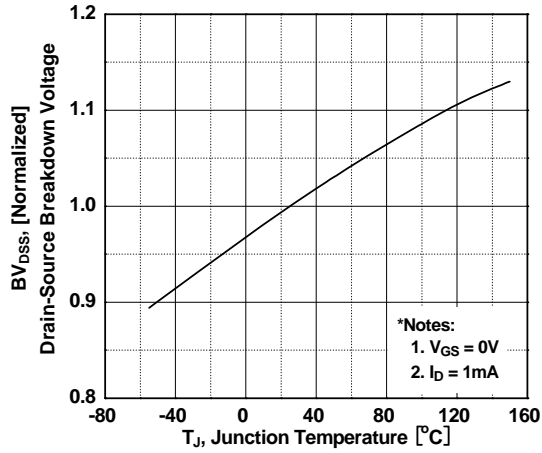


**Figure 6. Gate Charge Characteristics**

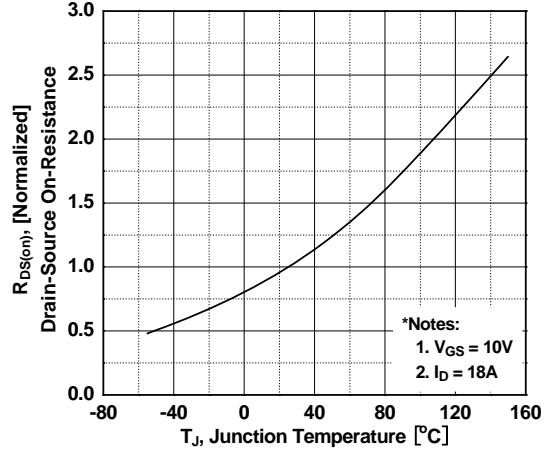


**Typical Performance Characteristics** (Continued)

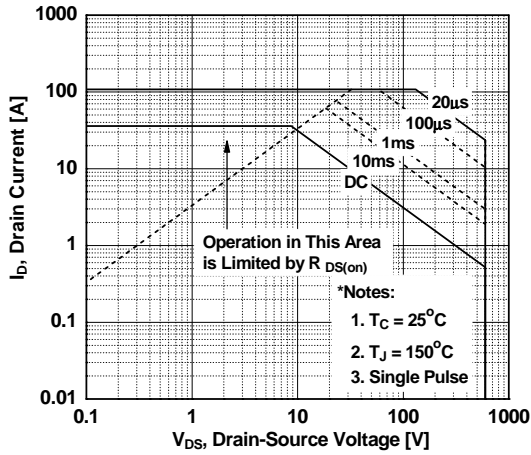
**Figure 7. Breakdown Voltage Variation vs. Temperature**



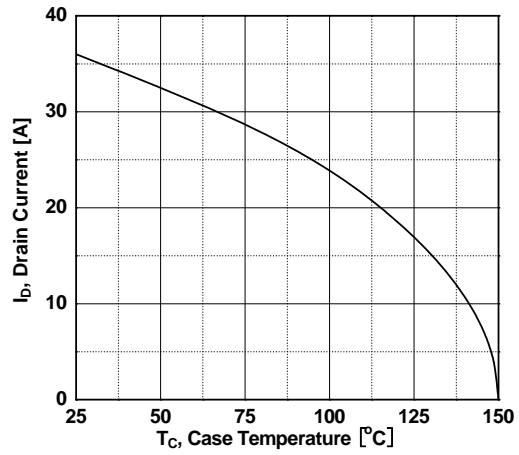
**Figure 8. On-Resistance Variation vs. Temperature**



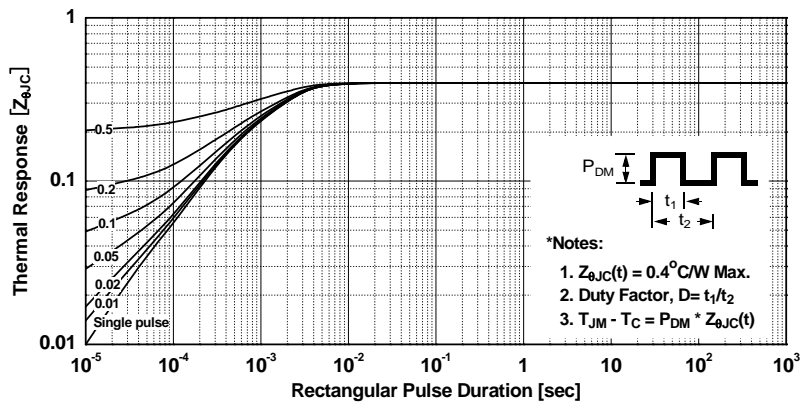
**Figure 9. Maximum Safe Operating Area**



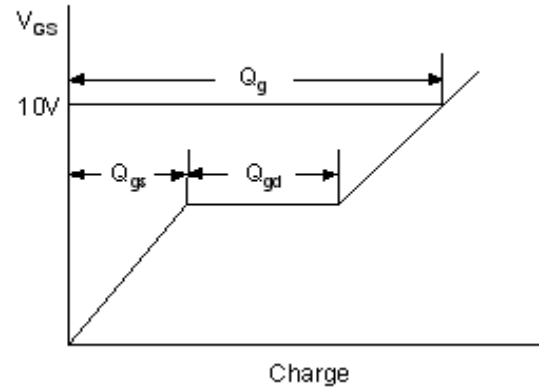
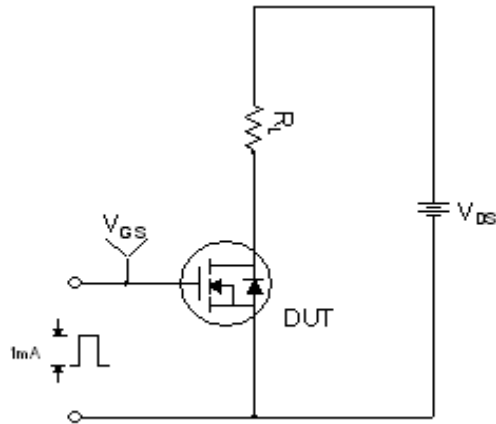
**Figure 10. Maximum Drain Current vs. Case Temperature**



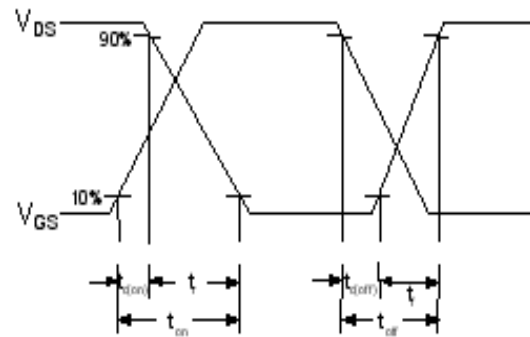
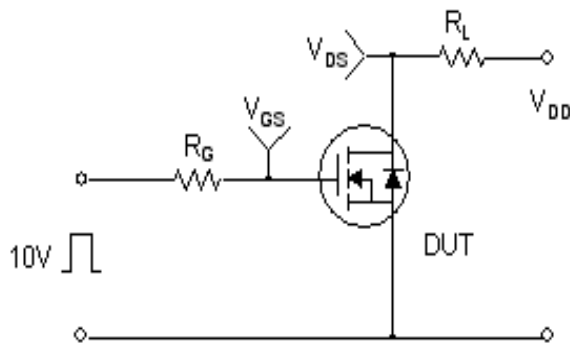
**Figure 11. Transient Thermal Response Curve**



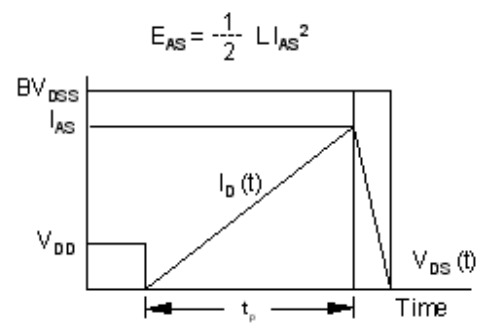
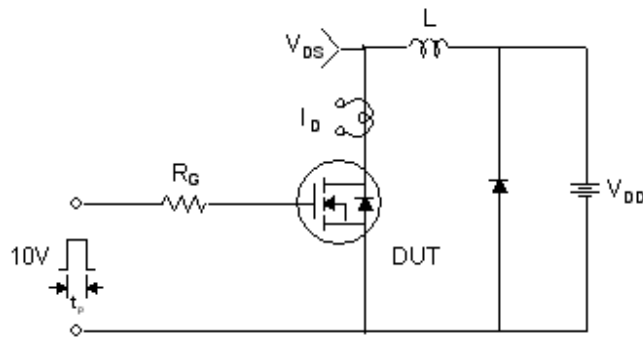
Gate Charge Test Circuit & Waveform



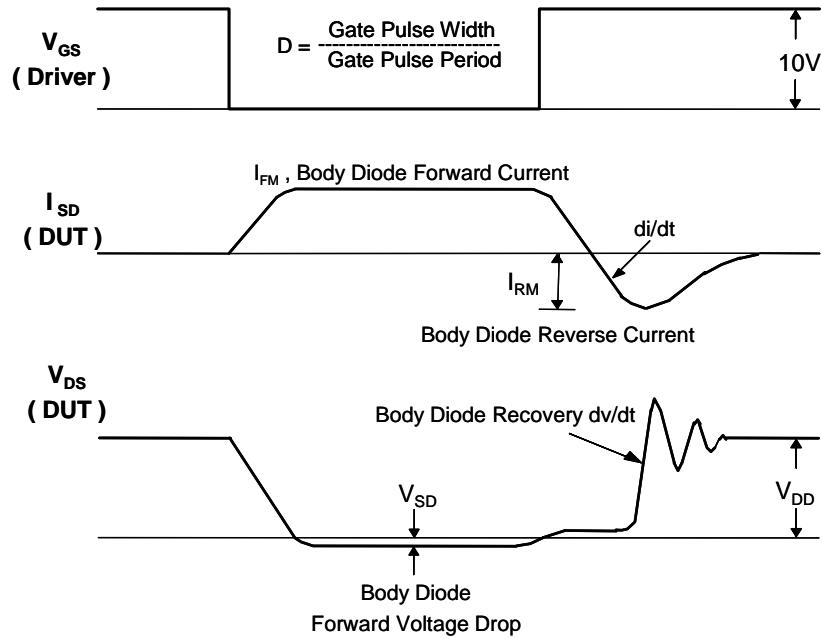
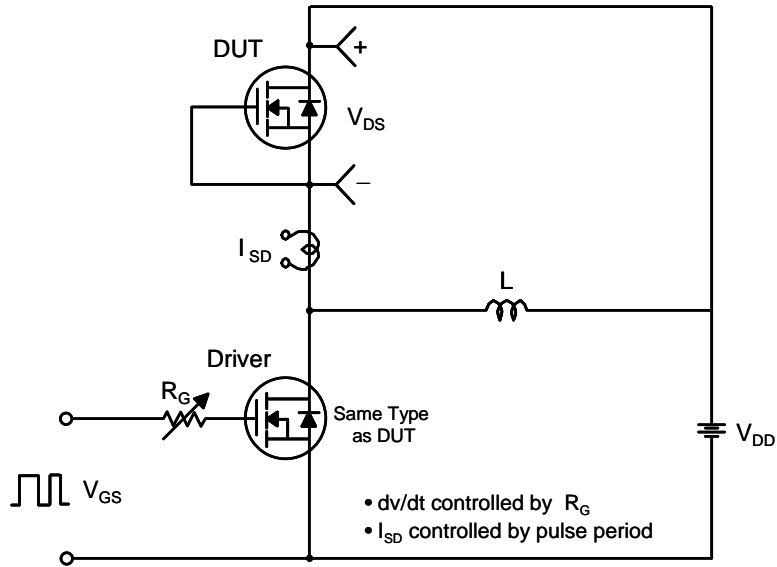
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

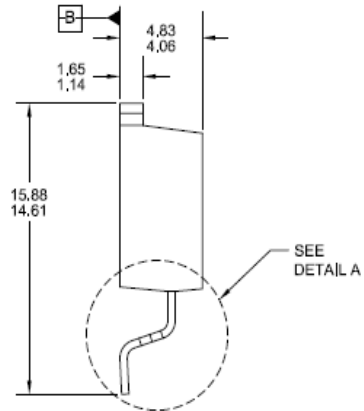
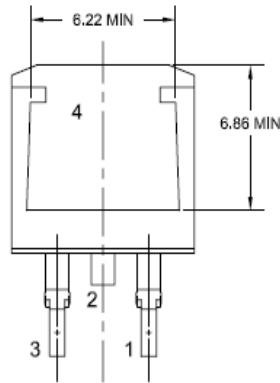
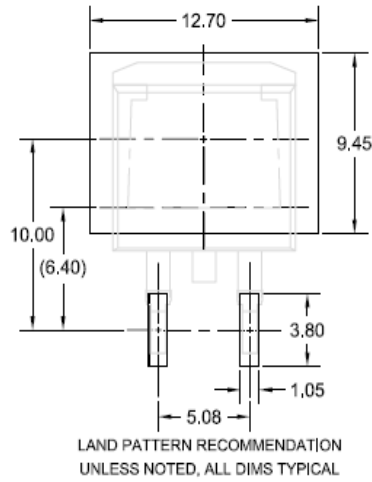
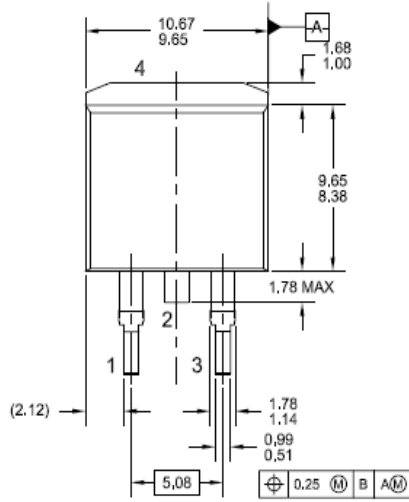


Peak Diode Recovery dv/dt Test Circuit & Waveforms

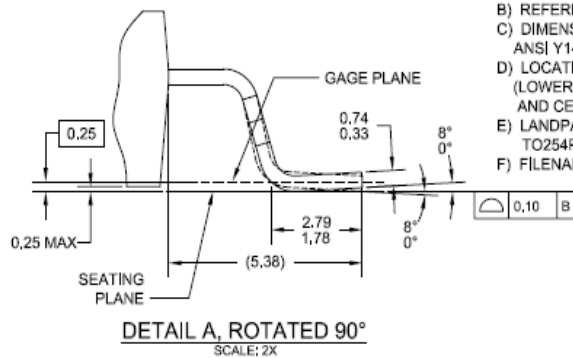


Mechanical Dimensions

D<sup>2</sup>PAK





- NOTES: UNLESS OTHERWISE SPECIFIED  
 A) ALL DIMENSIONS ARE IN MILLIMETERS.  
 B) REFERENCE JEDEC, TO-263, VARIATION AB.  
 C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1994.  
 D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).  
 E) LANDPATTERN RECOMMENDATION PER IPC TO254P1524X482-3N  
 F) FILENAME: TO263A02REV6





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