FAIRCHILD SEMICONDUCTOR®

November 2013

FCD600N60Z

N-Channel SuperFET® II MOSFET

600 V, 7.4 A, 600 mΩ

Features

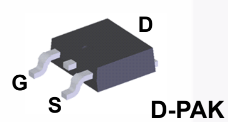
- 650 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 510 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 20 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 74 pF)
- 100% Avalanche Tested
- ESD Improved Capacity
- RoHS Compliant

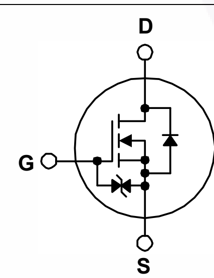
Applications

- LCD / LED / PDP TV and Monitor Lighting
- Solar Inverter
- AC-DC Power Supply

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FCD600N60Z	Unit
V_{DSS}	Drain to Source Voltage		600	V
V_{GSS}	Gate to Source Voltage	- DC	±20	V
		- AC (f > 1 Hz)	±30	V
I_D	Drain Current	- Continuous (T_C = 25°C)	7.4	A
		- Continuous (T_C = 100°C)	4.7	
I_{DM}	Drain Current	- Pulsed (Note 1)	22.2	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		135	mJ
I_{AR}	Avalanche Current (Note 1)		1.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		0.89	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25°C)	89	W
		- Derate Above 25°C	0.71	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FCD600N60Z	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	100	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD600N60Z	FCD600N60Z	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 mA, T_J = 25°C	600	-	-	V
		V_{GS} = 0 V, I_D = 10 mA, T_J = 150°C	650	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C	-	0.67	-	V/°C
BV_{DS}	Drain to Source Avalanche Breakdown Voltage	V_{GS} = 0 V, I_D = 7.4 A	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 480 V, V_{GS} = 0 V	-	-	5	µA
		V_{DS} = 480 V, T_C = 125°C	-	-	20	
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±10	uA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA	2.5	-	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 3.7 A	-	0.51	0.6	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 3.7 A	-	6.7	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	-	840	1120	pF
C_{oss}	Output Capacitance		-	630	840	pF
C_{rss}	Reverse Transfer Capacitance		-	30	45	pF
C_{oss}	Output Capacitance	V_{DS} = 380 V, V_{GS} = 0 V, f = 1 MHz	-	16.5	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	74	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 380 V, I_D = 3.7 A, V_{GS} = 10 V (Note 4)	-	20	26	nC
Q_{gs}	Gate to Source Gate Charge		-	3.4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	7.5	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	2.89	-	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 380 V, I_D = 3.7 A, V_{GS} = 10 V, R_G = 4.7 Ω (Note 4)	-	13	36	ns
t_r	Turn-On Rise Time		-	7	24	ns
$t_{d(off)}$	Turn-Off Delay Time		-	39	88	ns
t_f	Turn-Off Fall Time		-	9	28	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	7.4	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	22.2	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 3.7 A	-	-	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 3.7 A, dI_F/dt = 100 A/µs	-	200	-	ns
Q_{rr}	Reverse Recovery Charge		-	2.3	-	µC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 1.5 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \leq$ 3.7 A, di/dt $\leq$ 200 A/µs, $V_{DD} \leq BV_{DSS}$, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

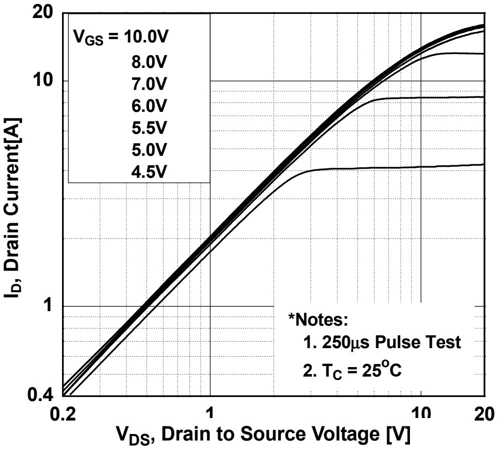


Figure 2. Transfer Characteristics

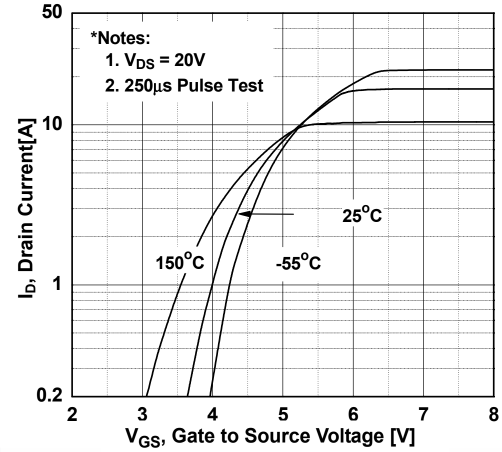


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

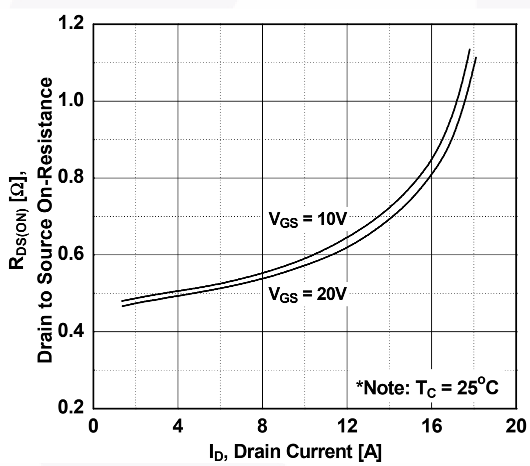


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

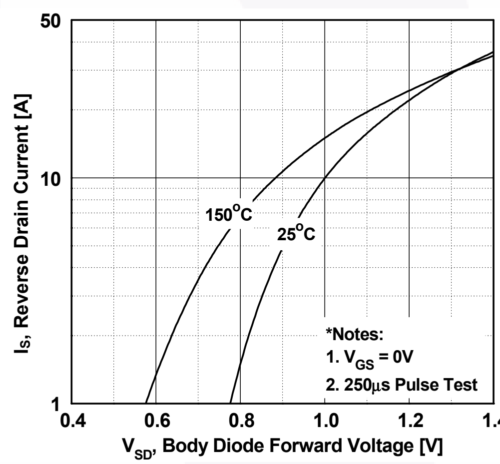


Figure 5. Capacitance Characteristics

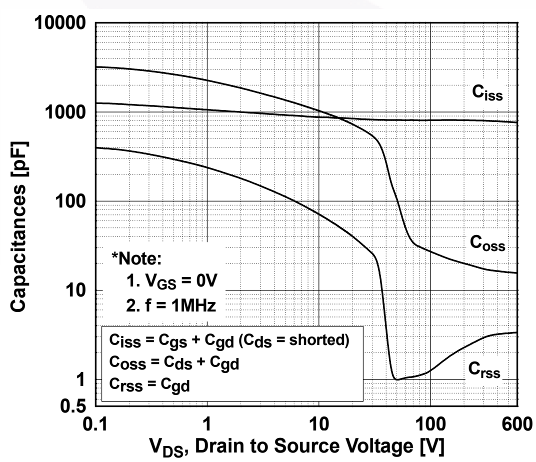
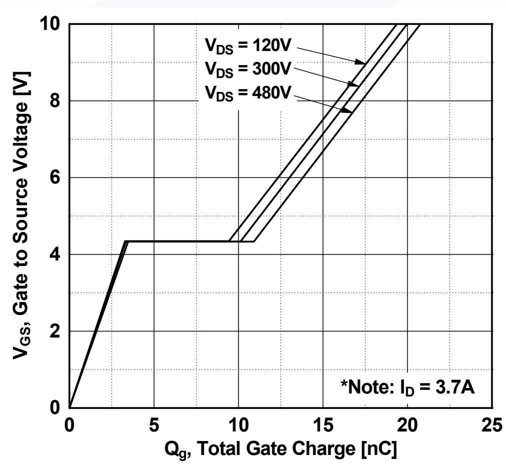


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

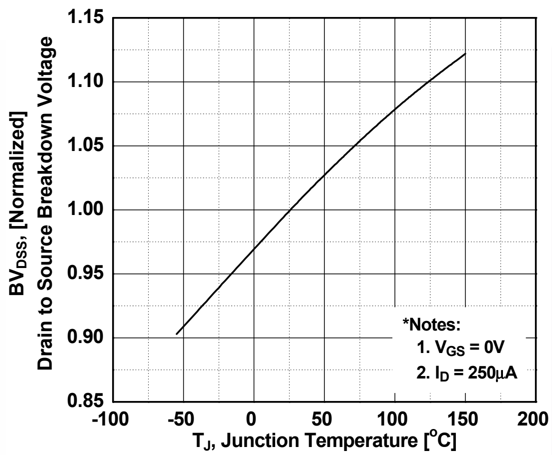


Figure 8. On-Resistance Variation vs. Temperature

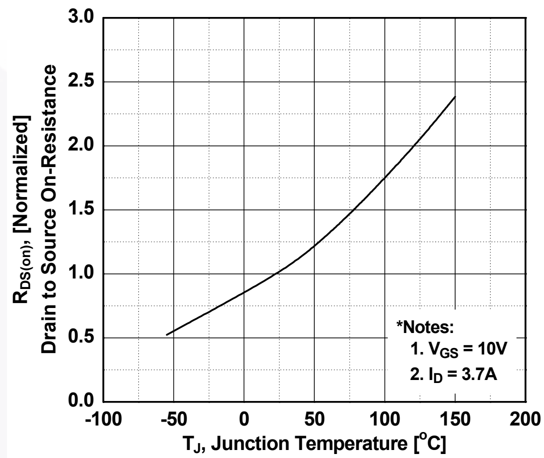


Figure 9. Maximum Safe Operating Area

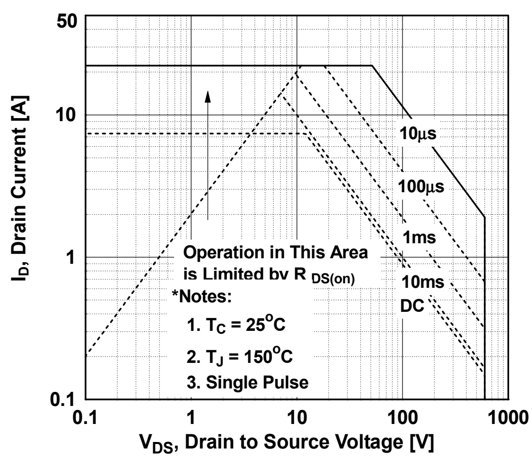


Figure 10. Maximum Drain Current vs. Case Temperature

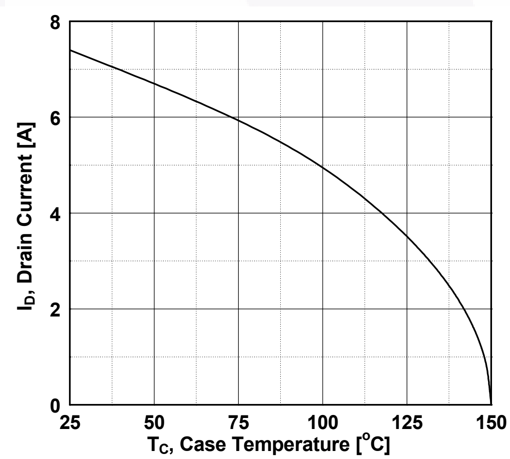
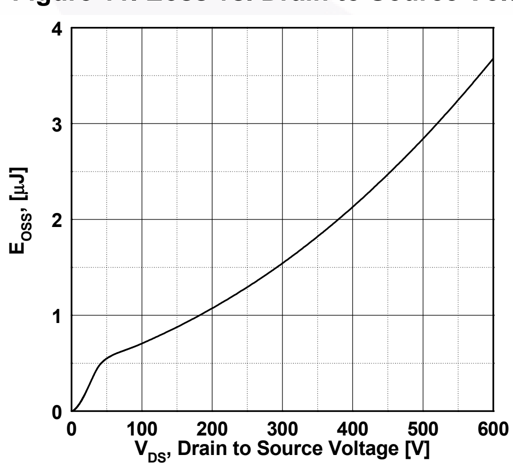
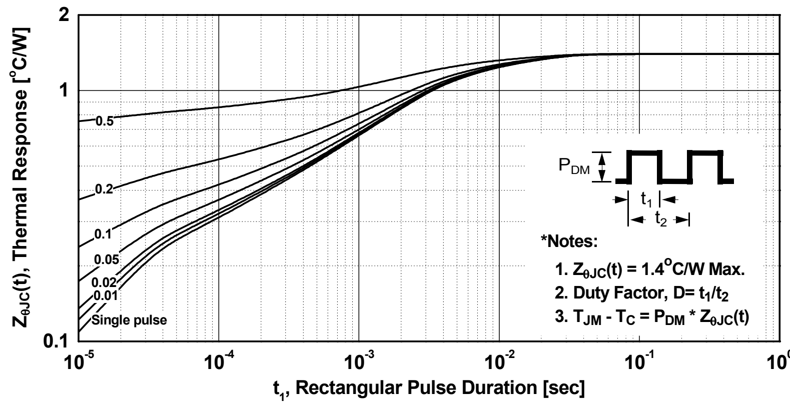


Figure 11. Eoss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



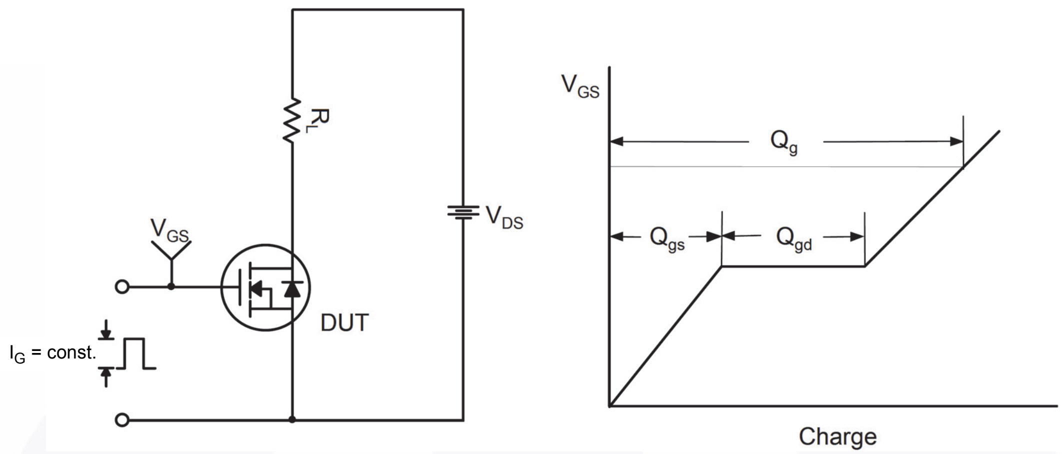


Figure 13. Gate Charge Test Circuit & Waveform

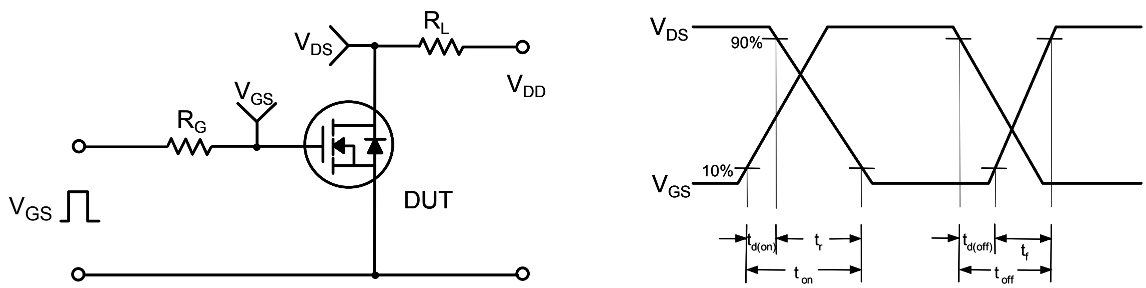


Figure 14. Resistive Switching Test Circuit & Waveforms

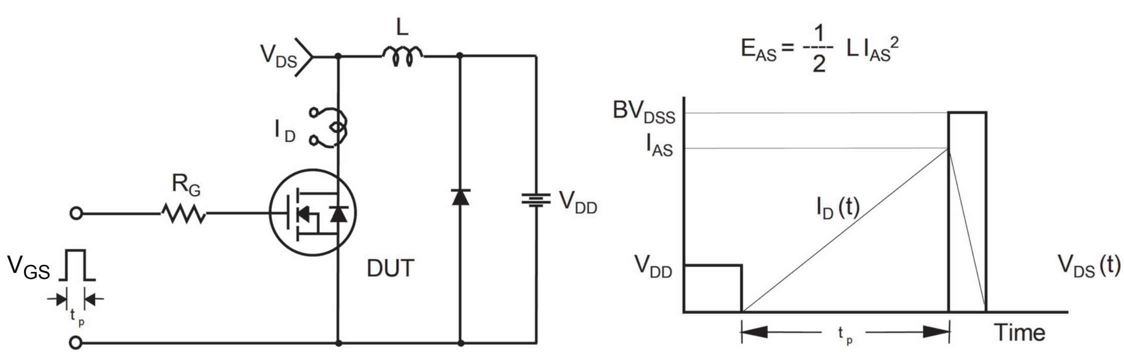


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

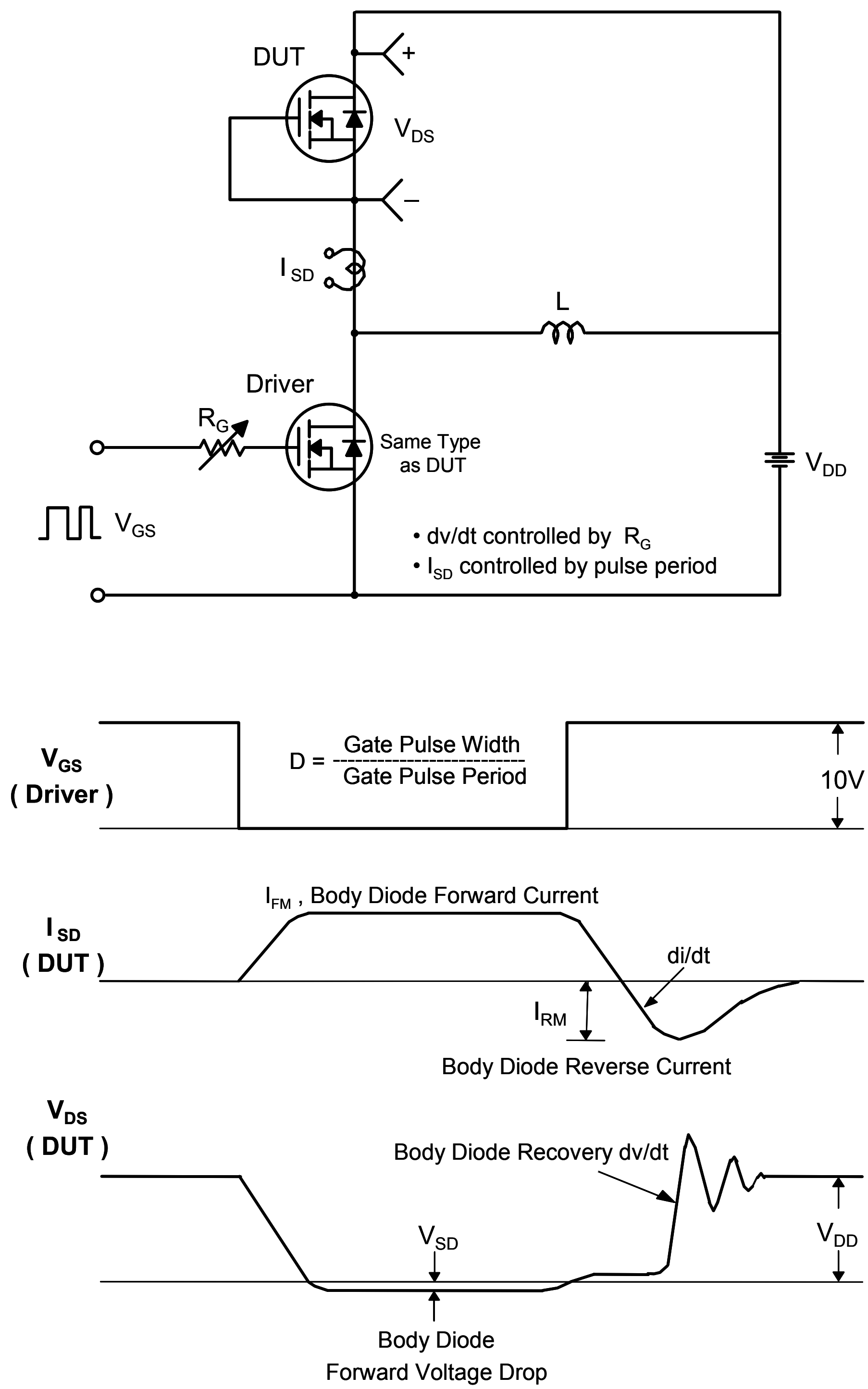


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

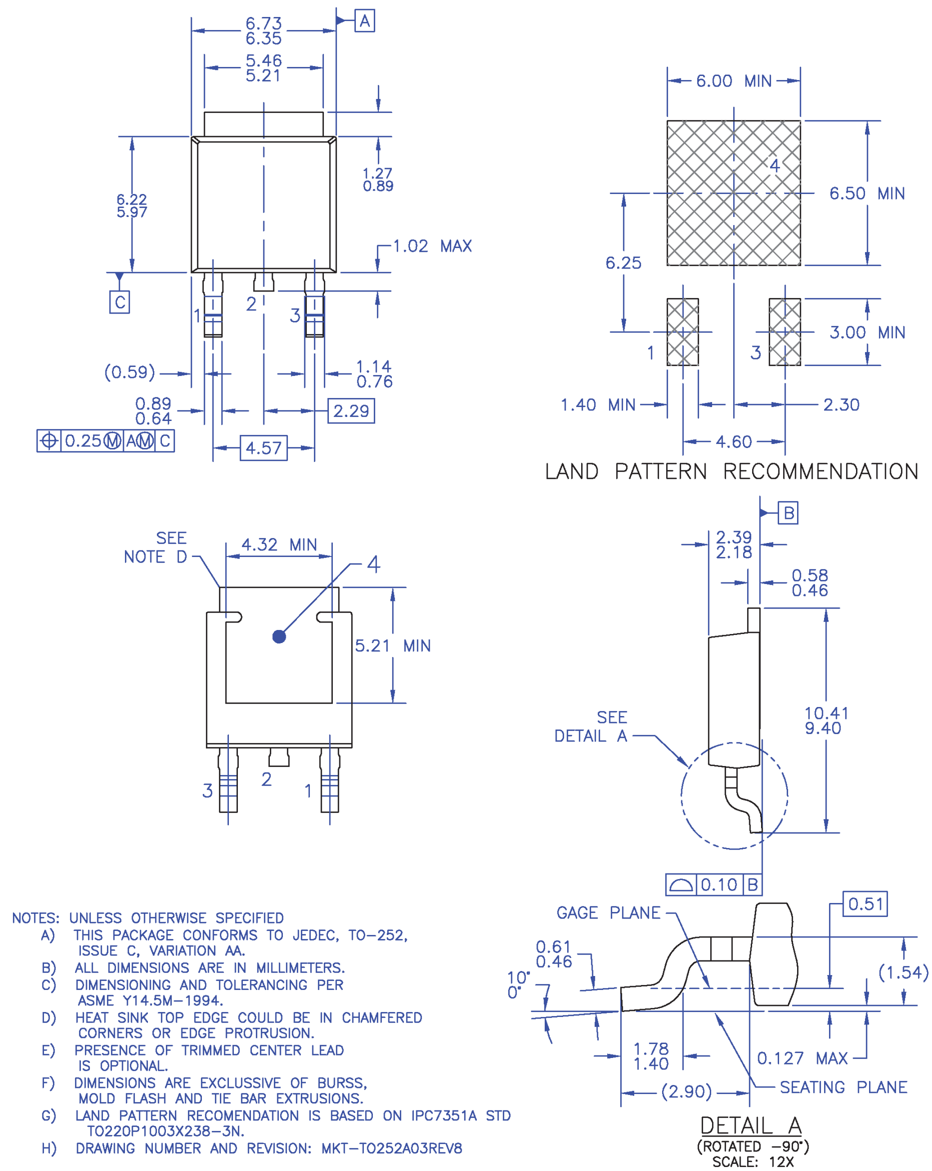


Figure 17. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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