

December 2014

FCH072N60F

N-Channel SuperFET® II FRFET® MOSFET

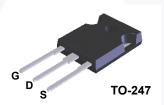
600 V, 52 A, 72 mΩ

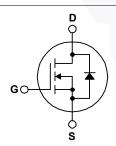
Features

- 650 V @ T_J = 150°C
- Typ. $R_{DS(on)} = 65 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. Q_q = 165 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 441 pF)
- · 100% Avalanche Tested
- · RoHS Compliant

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		Unit
V _{DSS}	Drain to Source Voltage		600	V
V	Cata ta Cauraa Valtaga	- DC	±20	V
V _{GSS} Gate to Source Voltage	Gate to Source voltage	- AC (f > 1 Hz)	±30	V
	Drain Current	- Continuous (T _C = 25°C)	52	А
I _D	Drain Current	- Continuous (T _C = 100°C)	33	A
I _{DM}	Drain Current	- Pulsed (Note 1)	156	Α
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		1128	mJ
I _{AR}	Avalanche Current (Note 1)		9.5	Α
E _{AR}	Repetitive Avalanche Energy (Note 1)		4.8	mJ
dv/dt	MOSFET dv/dt		100	V/ns
uv/ul	Peak Diode Recovery dv/dt	(Note 3)	50	V/IIS
n	Dawar Dissination	$(T_C = 25^{\circ}C)$	481	W
P _D	Power Dissipation	- Derate Above 25°C	3.85	W/°C
T _J , T _{STG}	Operating and Storage Temp	perature Range	-55 to +150	°C
TL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds 300			οС

Thermal Characteristics

Symbol	Parameter FCH072N60F		Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.26	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	pient, Max. 40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH072N60F	FCH072N60F	TO-247	Tube	N/A	N/A	30 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS} Drain to Source Breakdo	Drain to Source Breakdown Voltage	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}, T_C = 25^{\circ}\text{C}$	600	-	-	V
	Diain to Source Breakdown voltage	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}, T_C = 150^{\circ}\text{C}$	650	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	0.67	-	V/°C
ı	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	-	-	10	^
I _{DSS}	Zero Gate voltage Drain Current	$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	163	-	μА
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$		-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	3	-	5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 26 A	-	65	72	mΩ
9 _{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 26 \text{ A}$	-	42		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 400 V V 0 V	-	6510	8660	pF
C _{oss}	Output Capacitance	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz		205	275	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 WH 12	- \	1.5	2.5	pF
C _{oss}	Output Capacitance	$V_{DS} = 380 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	- \	110	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	441	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	$V_{DS} = 380 \text{ V}, I_D = 26 \text{ A},$	-	165	215	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	36	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	66	-	nC
ESR	Equivalent Series Resistance(G-S)	f = 1 MHz	-	0.78	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	43	96	ns
t _r		$V_{DD} = 380 \text{ V}, I_D = 26 \text{ A},$	-	38	86	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_{G} = 4.7 Ω	-	140	290	ns
t _f	Turn-Off Fall Time	(Note 4)	-	25	60	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current			-	52	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	156	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 26 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 26 A,	-	175	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	1.29	// -	μС

Notes:

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. I_{AS} = 9.5 A, R_{G} = 25 Ω , starting T_{J} = 25°C.
- 3. $I_{SD} \le 26$ A, di/dt ≤ 200 A/ μ s, $V_{DD} \le 380$ V, starting T_J = 25°C.
- ${\bf 4.} \ {\bf Essentially \ independent \ of \ operating \ temperature \ typical \ characteristics.}$

Typical Performance Characteristics

Figure 1. On-Region Characteristics

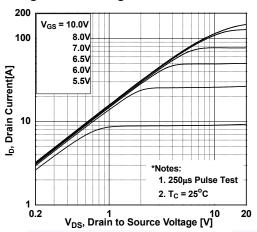


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

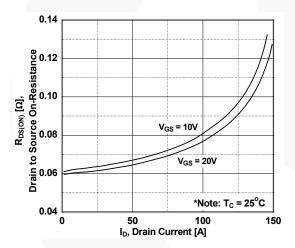


Figure 5. Capacitance Characteristics

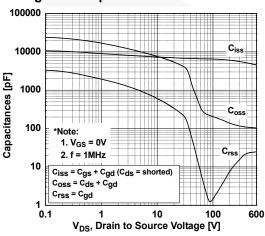


Figure 2. Transfer Characteristics

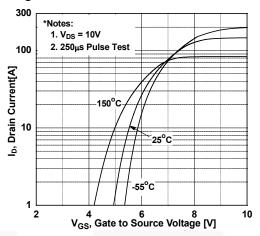


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

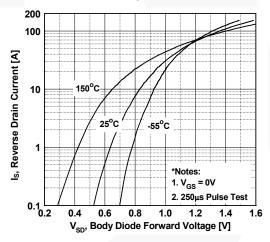
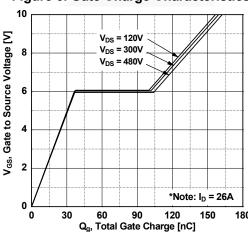


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

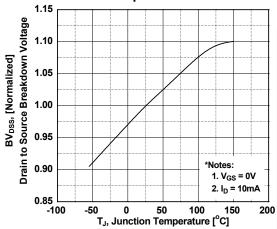


Figure 9. Maximum Safe Operating Area

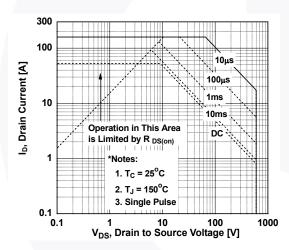


Figure 11. Eoss vs. Drain to Source Voltage

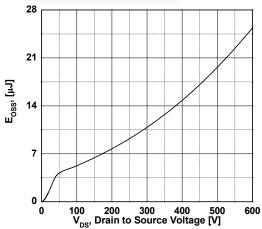


Figure 8. On-Resistance Variation vs. Temperature

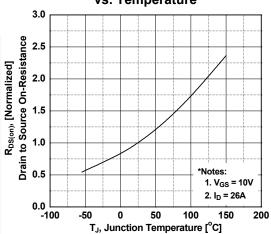
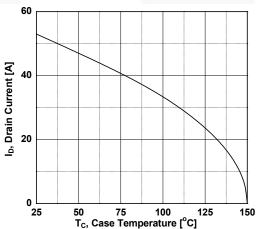
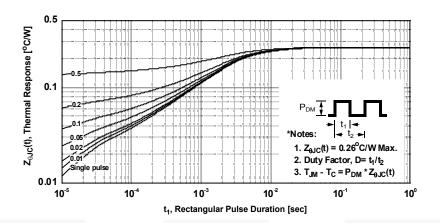


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



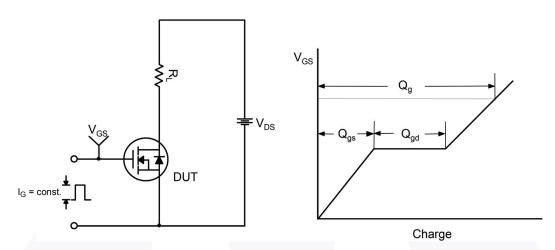


Figure 13. Gate Charge Test Circuit & Waveform

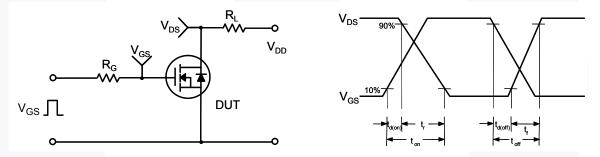


Figure 14. Resistive Switching Test Circuit & Waveforms

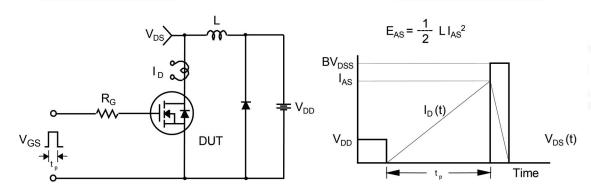


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

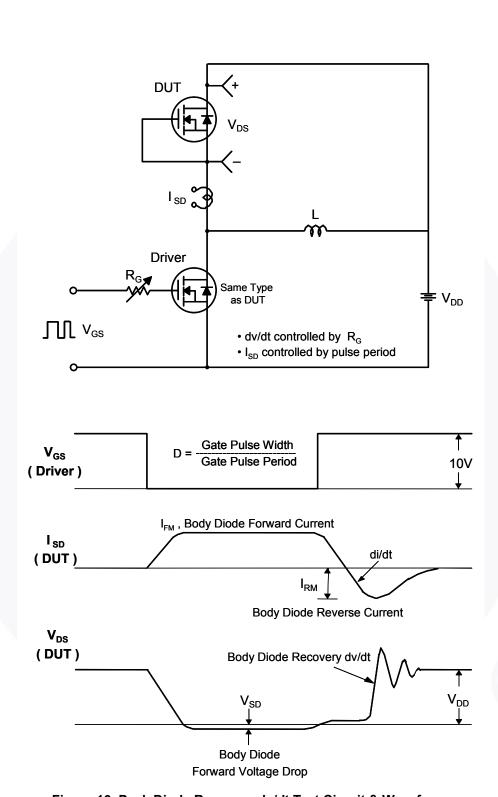
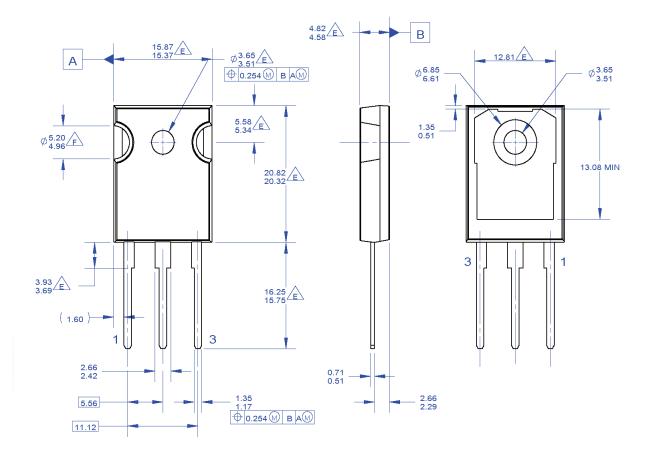


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE REFERENCE: JEDEC TO-247,
- ISSUE E, VARIATION AB, DATED JUNE, 2004.
 B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
- FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 1994

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F NOTCH MAY BE SQUARE

G. DRAWING FILENAME: MKT-TO247A03_REV03

Figure 17. TO-247, Molded, 3-Lead, Jedec Variation AB

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