

FCP380N60 / FCPF380N60

N-Channel SuperFET® II MOSFET

600 V, 10.2 A, 380 mΩ

Features

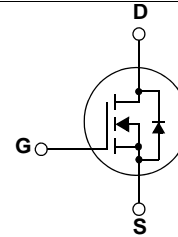
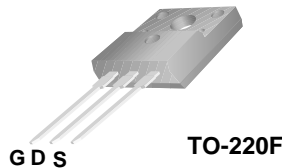
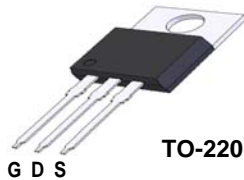
- 650 V @ $T_J = 150^\circ\text{C}$
- Max. $R_{DS(on)} = 380\text{ m}\Omega$
- Ultra low gate charge (typ. $Q_g = 30\text{ nC}$)
- Low effective output capacitance (typ. $C_{oss-eff} = 95\text{ pF}$)
- 100% avalanche tested

Applications

- LCD / LED / PDP TV Lighting
- Solar Inverter
- AC-DC Power Supply

Description

SuperFET®II MOSFET is Fairchild Semiconductor®'s first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFETII MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency.



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FCP380N60	FCPF380N60	Unit	
V_{DSS}	Drain to Source Voltage	600		V	
V_{GSS}	Gate to Source Voltage	-DC	± 20	V	
		-AC (f > 1 HZ)	± 30		
I_D	Drain Current	-Continuous ($T_C = 25^\circ\text{C}$)	10.2	10.2*	A
		-Continuous ($T_C = 100^\circ\text{C}$)	6.4	6.4*	
I_{DM}	Drain Current	- Pulsed (Note 1)	30.6	30.6*	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	211.6	mJ	
I_{AR}	Avalanche Current	(Note 1)	2.3	A	
E_{AR}	Repetitive Avalanche Energy	(Note 1)	1.06	mJ	
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	20	V/ns	
	MOSFET dv/dt		100		
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	106	31	W
		- Derate above 25°C	0.85	0.25	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$	
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$	

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FCP380N60	FCPF380N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.18	4	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case to Heat Sink (Typical)	0.5	0.5	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCP380N60	FCP380N60	TO-220	-	-	50
FCPF380N60	FCPF380N60	TO-220F	-	-	50

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 150^\circ\text{C}$	650	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C	-	0.6	-	$\text{V}/^\circ\text{C}$
BV_{DS}	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ A}$	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.5	-	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$	-	0.33	0.38	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 5\text{ A}$	-	11	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$	-	1250	1665	pF
C_{oss}	Output Capacitance		-	905	1205	pF
C_{rss}	Reverse Transfer Capacitance		-	45	60	pF
C_{oss}	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	23	-	pF
$C_{oss\text{ eff.}}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	95	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 5\text{ A}$ $V_{GS} = 10\text{ V}$	-	30	40	nC
Q_{gs}	Gate to Source Gate Charge		-	5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	10	-
ESR	Equivalent Series Resistance	Drain Open	-	1	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 5\text{ A}$ $V_{GS} = 10\text{ V}, R = 4.7\text{ }\Omega$	-	14	38	ns
t_r	Turn-On Rise Time		-	7	24	ns
$t_{d(off)}$	Turn-Off Delay Time		-	45	100	ns
t_f	Turn-Off Fall Time		(Note 4)	-	6	22

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	10.2	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	30.6	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 5\text{ A}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 5\text{ A}$	-	240	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt = 100\text{ A}/\mu\text{s}$	-	2.7	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS} = 2.3\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 5.1\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

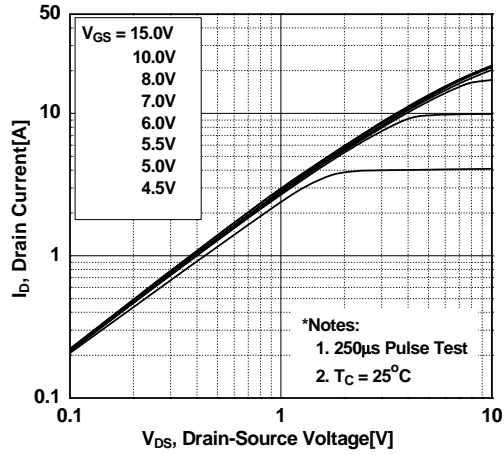


Figure 2. Transfer Characteristics

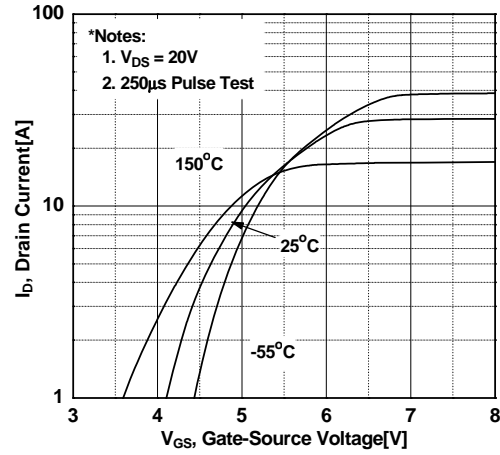


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

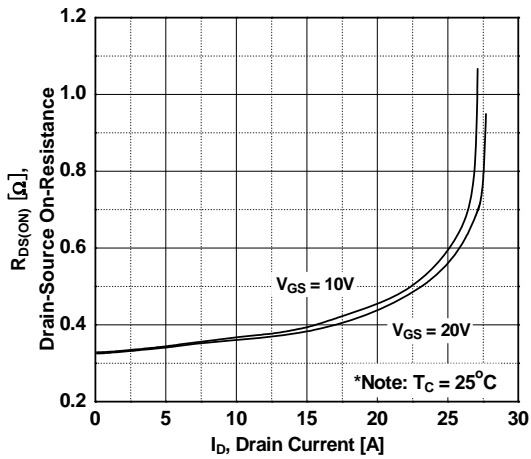


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

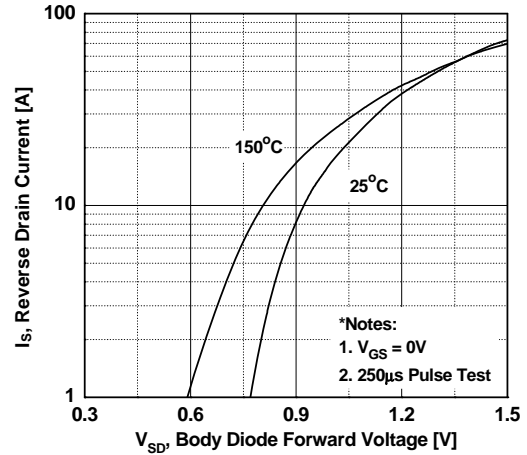


Figure 5. Capacitance Characteristics

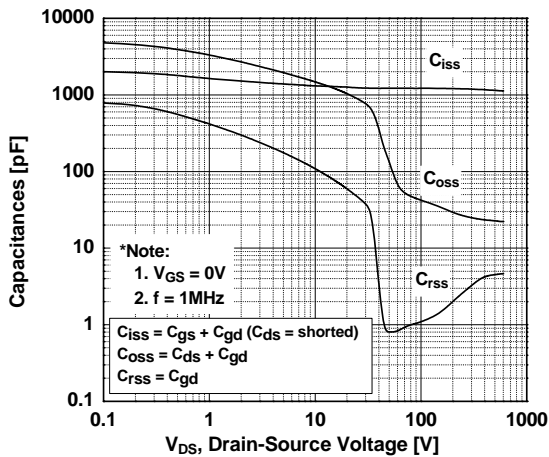
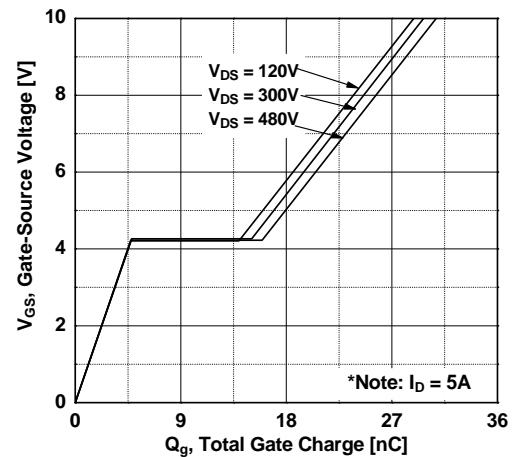


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

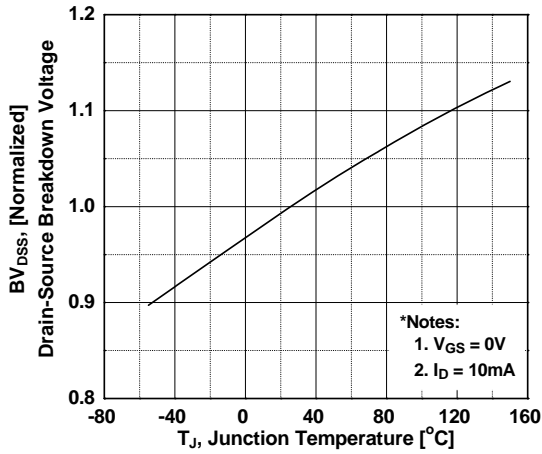


Figure 8. On-Resistance Variation vs. Temperature

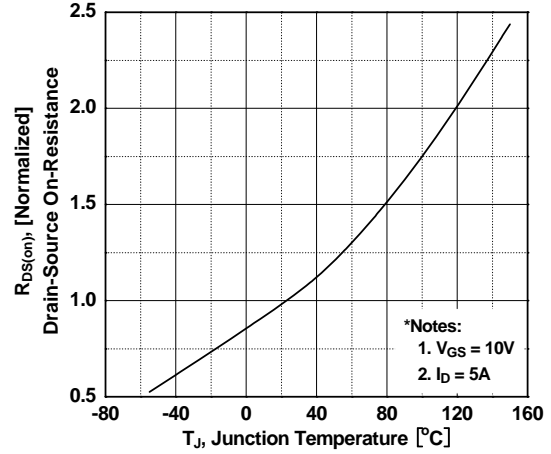


Figure 9. Maximum Safe Operating Area vs. Case Temperature - FCP380N60

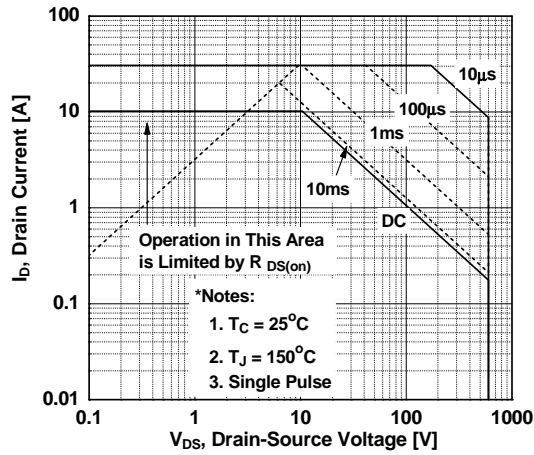


Figure 10. Maximum Safe Operating Area vs. Case Temperature - FCPF380N60

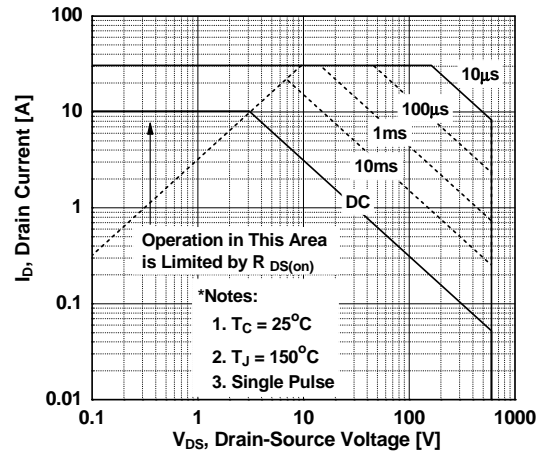


Figure 11. Maximum Drain Current

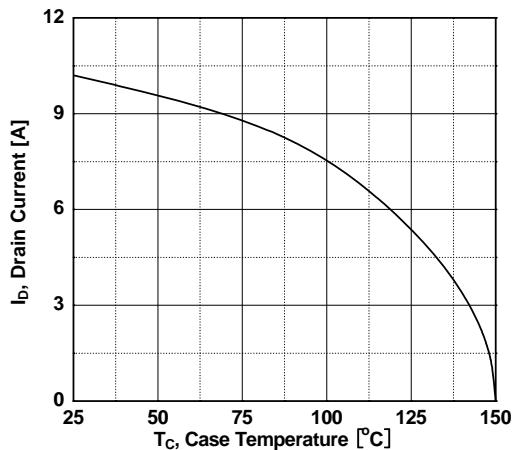
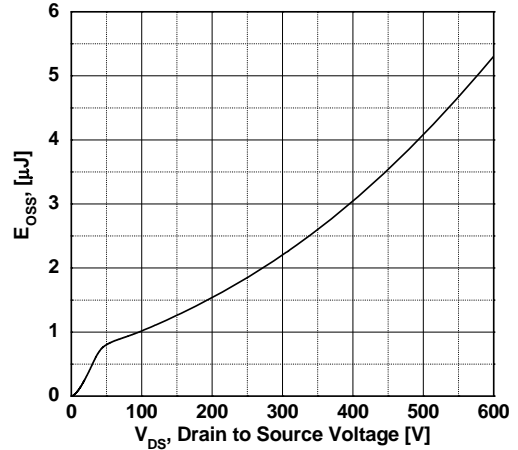


Figure 12. E_{oss} vs. Drain to Source Voltage Switching Capability



Typical Performance Characteristics (Continued)

Figure 13. Transient Thermal Response Curve - FCP380N60

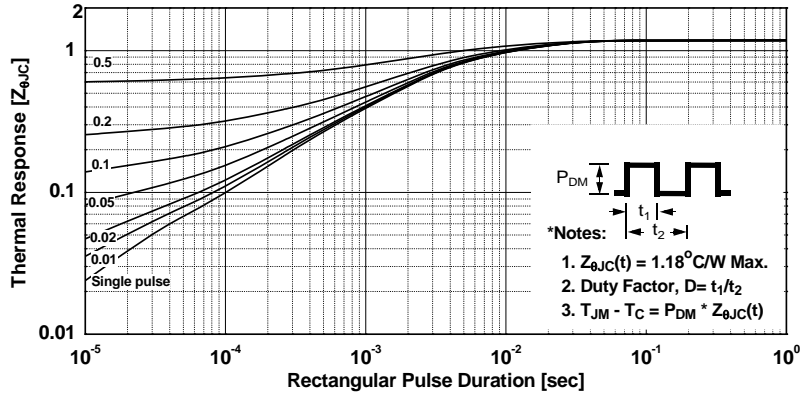
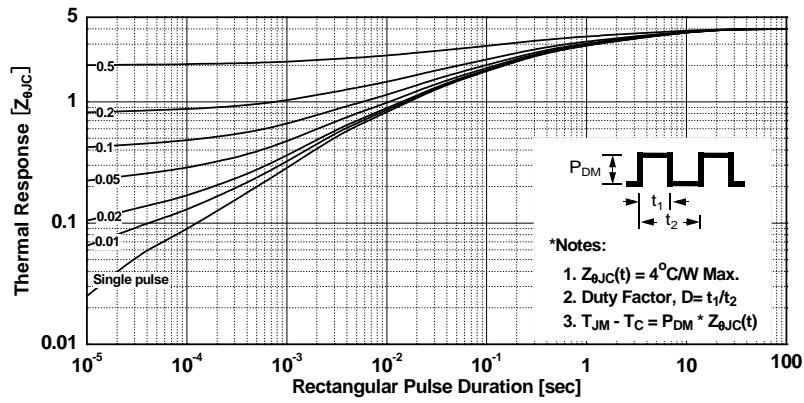
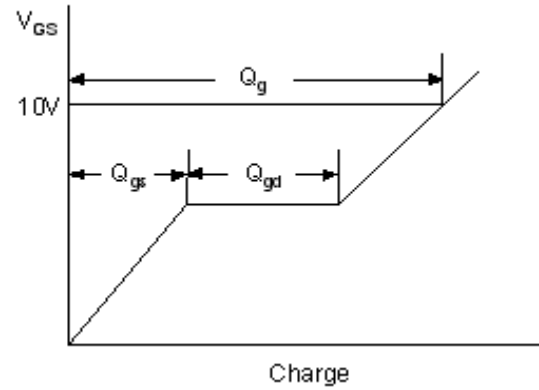
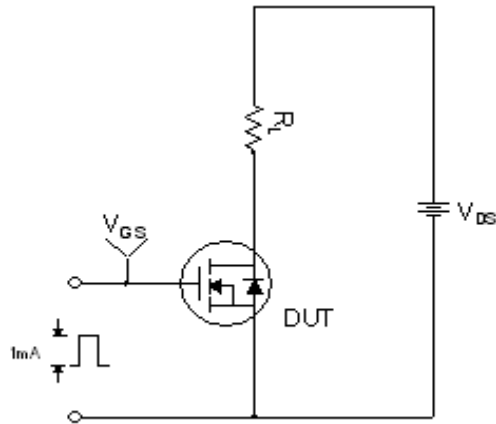


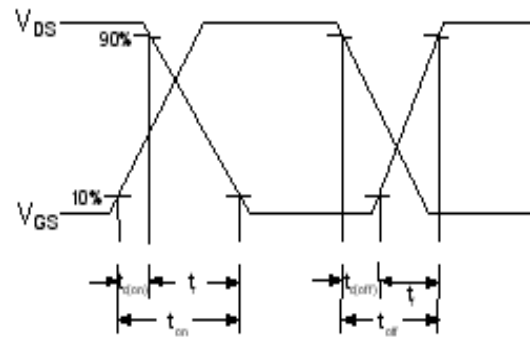
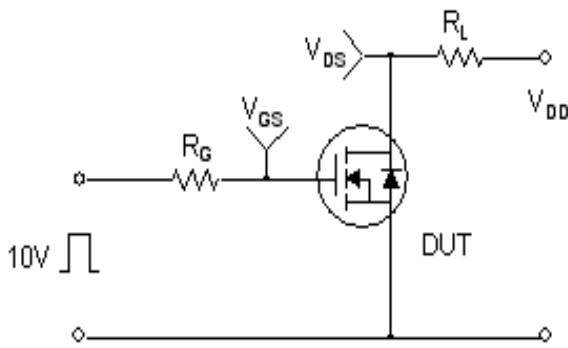
Figure 14. Transient Thermal Response Curve - FCPF380N60



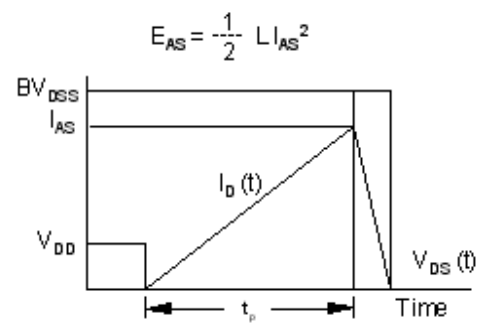
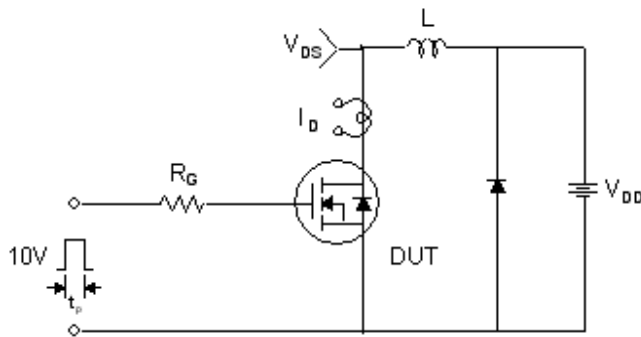
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

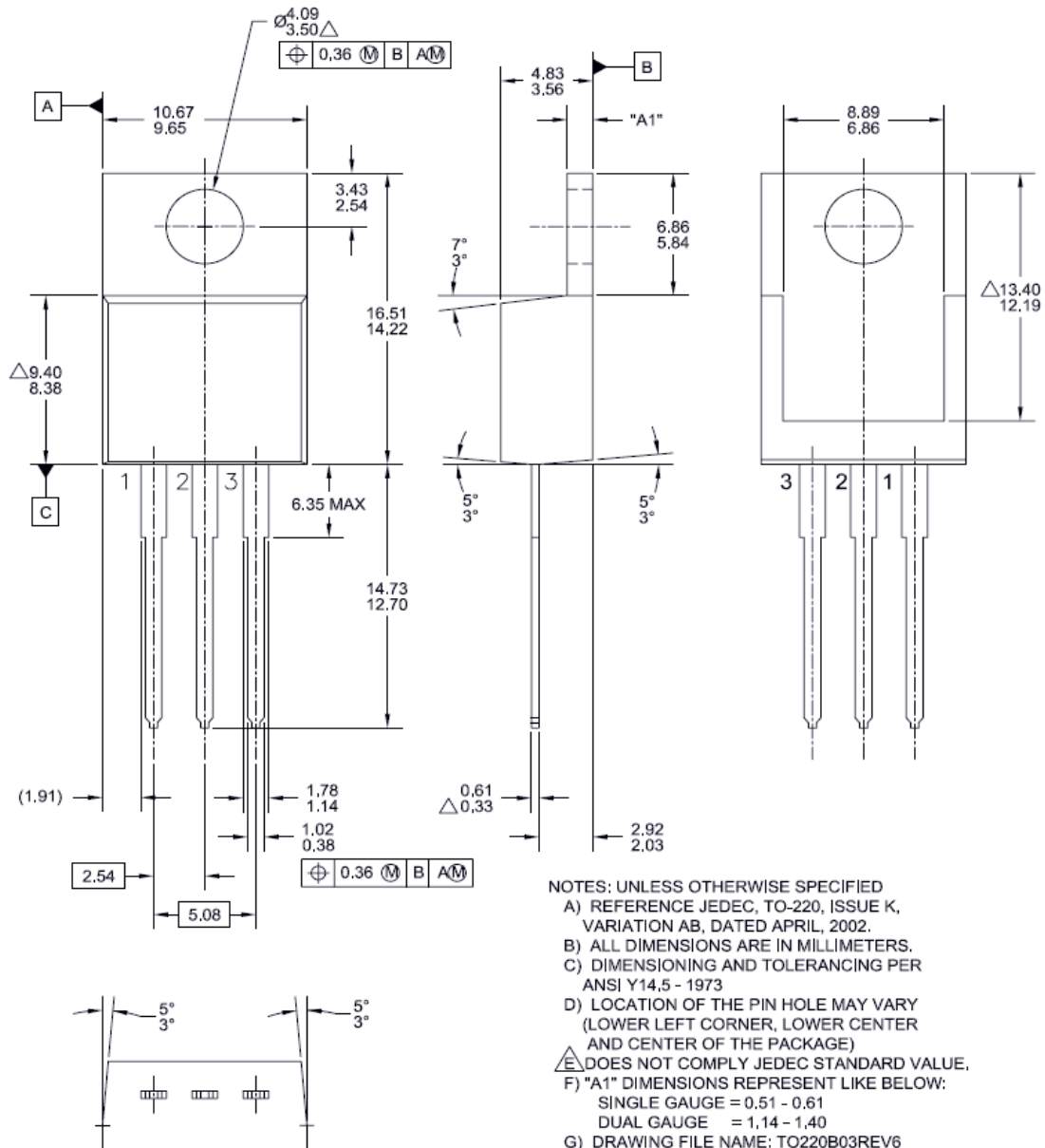


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

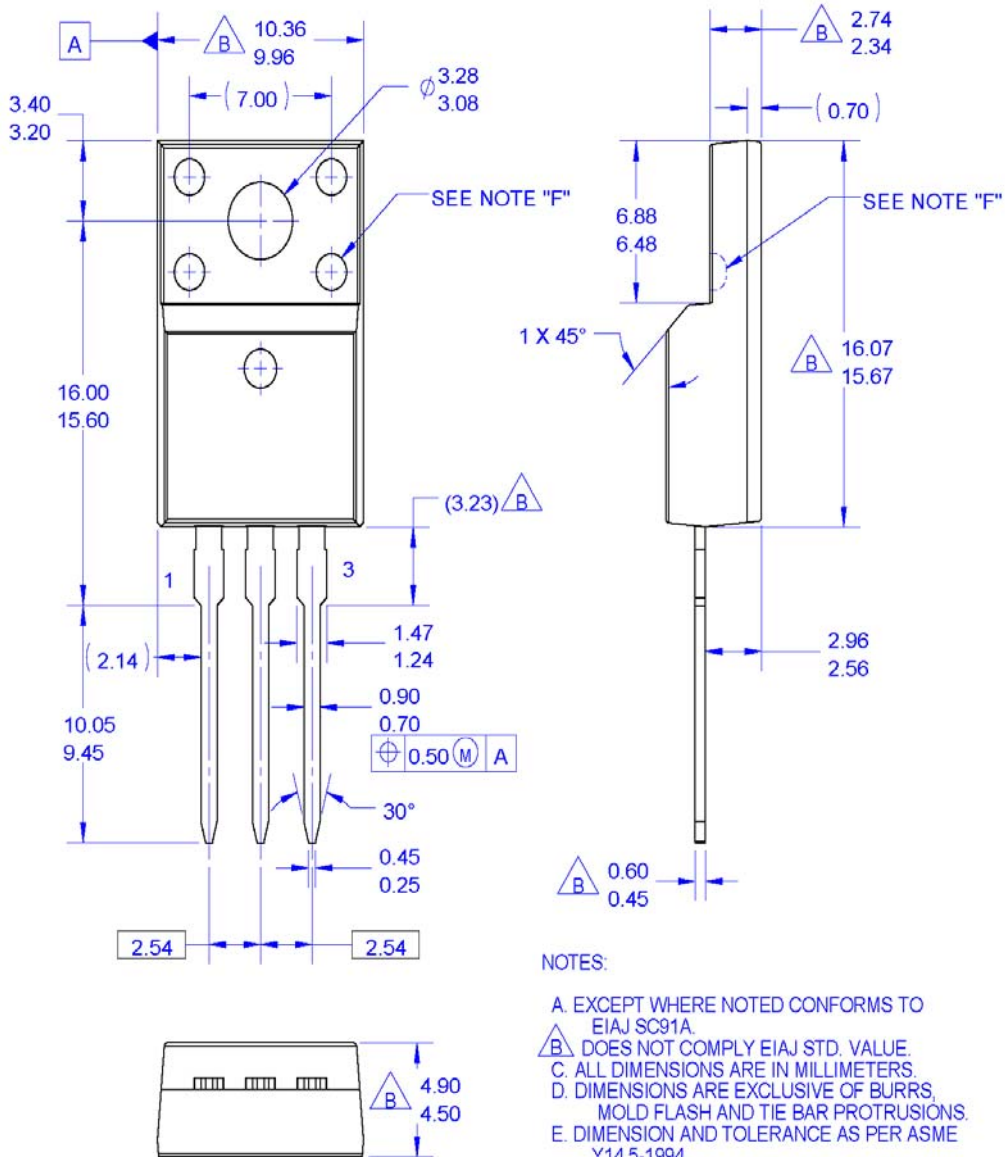
TO-220



Dimensions in Millimeters

Package Dimensions

TO-220F (Retractable)



NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3


*** Front/Back Side Isolation Voltage : AC 2500V**

Dimensions in Millimeters



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- | | | | |
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| AccuPower™ | F-PFST™ | PowerXS™ | SYSTEM GENERAL®* |
| AX-CAP®* | FRFET® | Programmable Active Droop™ | TinyBoost™ |
| BitSiC™ | Global Power Resource SM | QFET® | TinyBuck™ |
| Build it Now™ | Green Bridge™ | QS™ | TinyCalc™ |
| CorePLUS™ | Green FPS™ | Quiet Series™ | TinyLogic® |
| CorePOWER™ | Green FPS™ e-Series™ | RapidConfigure™ | TINYOPTO™ |
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- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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